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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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HD74SSTV16857B

1:1 14-bit SSTL_2 Registered Buffer

REJ03D0023-0100Z
(Previous ADE-205-712 (Z))
Rev.1.00
Jun.03.2003

Description

The HD74SSTV16857B is a 14-bit registered buffer designed for 2.3 V to 2.7 V V_{CC} operation and LVCMOS reset ($\overline{\text{RESET}}$) input / SSTL_2 data (D) inputs and CLK input.

Data flow from D to Q is controlled by differential clock pins (CLK, $\overline{\text{CLK}}$) and the $\overline{\text{RESET}}$. Data is triggered on the positive edge of the positive clock (CLK), and the negative clock ($\overline{\text{CLK}}$) must be used to maintain noise margins. When $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are low.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

Features

- Supports LVCMOS reset ($\overline{\text{RESET}}$) input / SSTL_2 data (D) inputs and CLK input
- Differential SSTL_2 (Stub series terminated logic) CLK signal
- Flow through architecture optimizes PCB layout
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74SSTV16857BTEL	TSSOP-48 pin	TTP-48DBV	T	EL (1,000 pcs / Reel)
HD74SSTV16857BNEL	TVSOP-48 pin	TTP-48DEV	N	EL (1,000 pcs / Reel)

Note: Please consult the sales office for the above package availability.

Function Table

Inputs				Output Q
RESET	CLK	CLK	D	
L	X	X	X	L
H	↓	↑	H	H
H	↓	↑	L	L
H	L or H	H or L	X	Q ₀ ⁻¹

H : High level

L : Low level

X : Immaterial

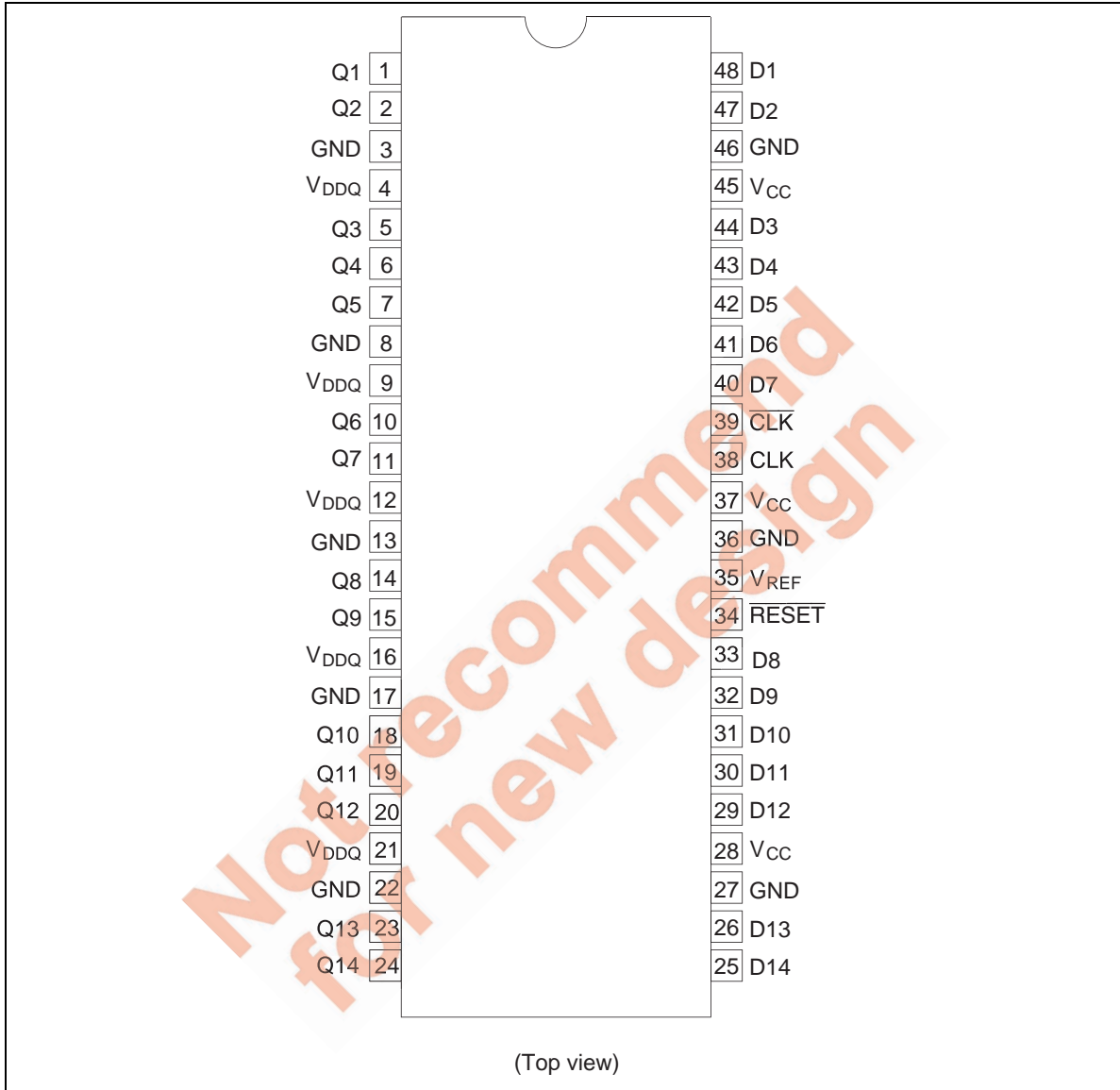
↑ : Low to high transition

↓ : High to low transition

Note: 1. Output level before the indicated steady state input conditions were established.

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Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC} or V_{DDQ}	-0.5 to 3.6	V	
Input voltage ^{*1}	V_I	-0.5 to $V_{DDQ}+0.5$	V	
Output voltage ^{*1, 2}	V_O	-0.5 to $V_{DDQ}+0.5$	V	
Input clamp current	I_{IK}	±50	mA	$V_I < 0$ or $V_I > V_{CC}$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{DDQ}$
Continuous output current	I_O	±50	mA	$V_O = 0$ to V_{DDQ}
V_{CC} , V_{DDQ} or GND current / pin	I_{CC} , I_{DDQ} or I_{GND}	±100	mA	
Package thermal impedance	θ_{JA}	115	°C / W	TSSOP
Storage temperature	T_{stg}	-65 to +150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This current will flow only when the output is in the high state and $V_O > V_{DDQ}$.

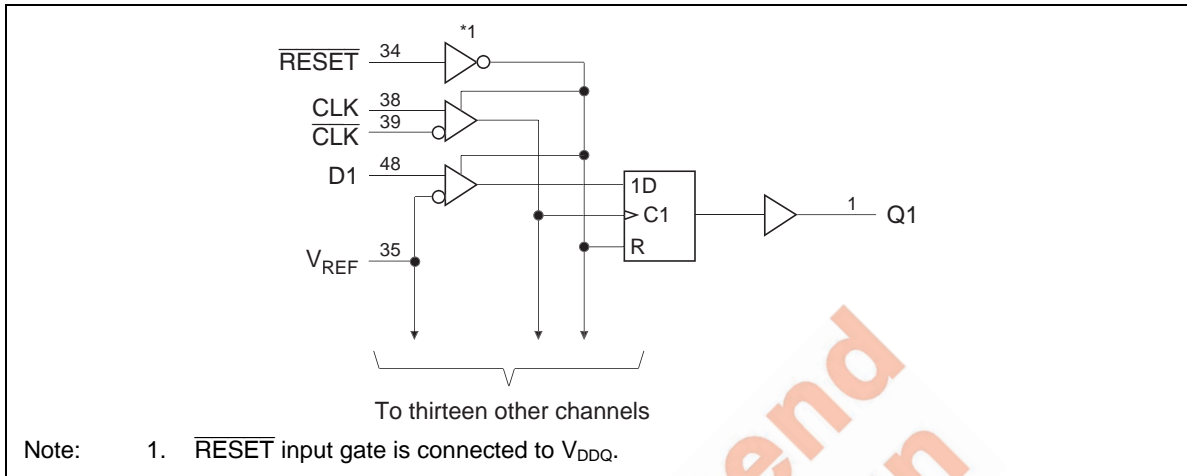
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Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	V_{CC}	V_{DDQ}	2.5	2.7	V	
Output supply voltage	V_{DDQ}	2.3	2.5	2.7	V	
Reference voltage	V_{REF}	1.15	1.25	1.35	V	$V_{REF} = 0.5 \times V_{DDQ}$
Termination voltage	V_{TT}	$V_{REF} - 40 \text{ mV}$	V_{REF}	$V_{REF} + 40 \text{ mV}$	V	
Input voltage	V_I	0	—	V_{CC}	V	
AC high level input voltage	V_{IH}	$V_{REF} + 310 \text{ mV}$	—	—	V	D
AC low level input voltage	V_{IL}	—	—	$V_{REF} - 310 \text{ mV}$	V	D
DC high level input voltage	V_{IH}	$V_{REF} + 150 \text{ mV}$	—	—	V	D
DC low level input voltage	V_{IL}	—	—	$V_{REF} - 150 \text{ mV}$	V	D
High level input voltage	V_{IH}	1.7	—	$V_{DDQ} + 0.3$	V	$\overline{\text{RESET}}$
Low level input voltage	V_{IL}	-0.3	—	0.7	V	$\overline{\text{RESET}}$
Differential input voltage	(Common mode range) V_{CMR}	0.97	—	1.53	V	CLK, $\overline{\text{CLK}}$
	(Minimum peak to peak input) V_{PP}	360	—	—	mV	CLK, $\overline{\text{CLK}}$
High level output current	I_{OH}	—	—	-20	mA	
Low level output current	I_{OL}	—	—	20	mA	
Operating temperature	T_a	0	—	70	°C	

Note: The $\overline{\text{RESET}}$ input of the device must be held at V_{DDQ} or GND to ensure proper device operation. The differential inputs must not be floating, unless $\overline{\text{RESET}}$ is low.

Logic Diagram



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Electrical Characteristics

Item	Symbol	V _{CC} (V)	Min	Typ	Max	Unit	Test Conditions
Input diode voltage	V _{IK}	2.3	—	—	-1.2	V	I _{IN} = -18 mA
Output voltage	V _{OH}	2.3 to 2.7	V _{CC} -0.2	—	—	V	I _{OH} = -100 μA
		2.3	1.95	—	V _{DDQ}	I _{OH} = -16 mA	
	V _{OL}	2.3 to 2.7	—	—	0.2	I _{OL} = 100 μA	
		2.3	0	—	0.35	I _{OL} = 16 mA	
Input current (All inputs)	I _{IN}	2.7	—	—	±5	μA	V _{IN} = 2.7 V or 0
Quiescent supply current	I _{CC} ^{*2}	2.7	—	25	45	mA	V _{IN} = V _{IH(AC)} or V _{IL(AC)} , I _O = 0
Standby current	I _{CC(stdy)}	2.7	—	—	10	μA	RESET = GND
Dynamic operating clock only	I _{CCD} ^{*2}	2.7	—	38	45	μA/	RESET = V _{CC} , clock V _I = V _{IH(AC)} or V _{IL(AC)} , MHz CLK and CLK switching 50% duty cycle
Dynamic operating per each data input	I _{CCD} ^{*2}	2.7	—	11	15	μA/	RESET = V _{CC} , clock V _I = V _{IH(AC)} or V _{IL(AC)} , MHz CLK and CLK switching 50% / duty cycle. One data input data switching at half clock input frequency, 50% duty cycle.
Output high ^{*3}	r _{OH}	2.3 to 2.7	7	—	20 ^{*4}	Ω	I _{OH} = -20 mA
Output low ^{*3}	r _{OL}	2.3 to 2.7	7	—	20 ^{*4}	Ω	I _{OL} = 20 mA
r _{OH} - r _{OL} each separate bit ^{*3}	r _{O(Δ)}	2.5	—	—	4	Ω	I _O = 20 mA, Ta = 25°C
Input capacitance	Data inputs	C _{IN}	2.5 ^{*1}	—	3.5	pF	V _I = V _{REF} ±310 mV
	CLK and CLK			—	3.5		V _{CMR} = 1.25 V, V _{PP} = 360 mV
	RESET			—	3.0		V _I = V _{CC} or GND

- Notes: 1. All typical values are at V_{CC} = 2.5 V, Ta = 25°C.
 2. Total I_{CC} (max) = I_{CC} + {I_{CCD} (clock)×f(clock)} + {I_{CCD} (Data)×1/2f(clock)×14}
 3. This is effective in the case that it did terminate by resistance.
 4. See figure. 1, 2.

Switching Characteristics

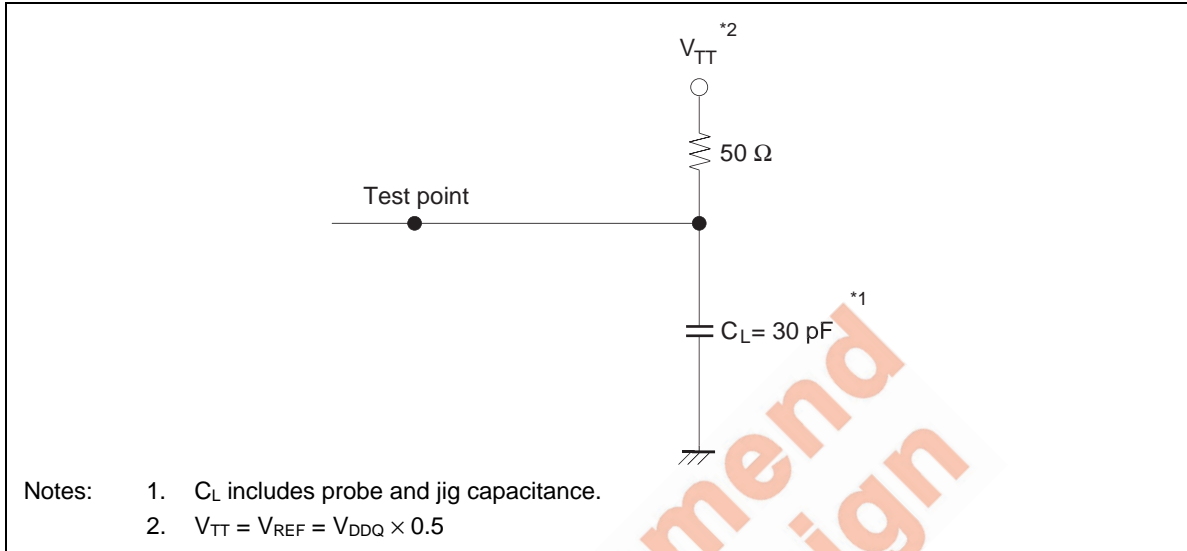
Item	Symbol	$V_{CC} = 2.5 \pm 0.2 \text{ V}$		Unit	Test Condition	
		Min	Max			
Clock frequency ^{*1}	f_{clock}	—	200	MHz		
Setup time	Fast slew rate ^{*4, 6}	t_{su}	0.75	—	ns	Data before CLK \uparrow , $\overline{\text{CLK}}\downarrow$
	Slow slew rate ^{*5, 6}		0.9	—		
Hold time	Fast slew rate ^{*4, 6}	t_{h}	0.75	—	ns	Data after CLK \uparrow , $\overline{\text{CLK}}\downarrow$
	Slow slew rate ^{*5, 6}		0.9	—		
Differential inputs active time	t_{act}	22	—	ns	Data inputs must be low after RESET high.	
Differential inputs inactive time	t_{inact}	22	—	ns	Data and clock inputs must be held at valid levels (not floating) after RESET low.	
Pulse width	t_{w}	2.5	—	ns	CLK, $\overline{\text{CLK}}$ "H" or "L"	
Output slew ^{*3}	t_{SL}	1	4	volt/ns		

($C_L = 30 \text{ pF}$, $R_L = 50 \text{ }\Omega$, $V_{\text{REF}} = V_{\text{TT}} = V_{\text{DDQ}} \times 0.5$)

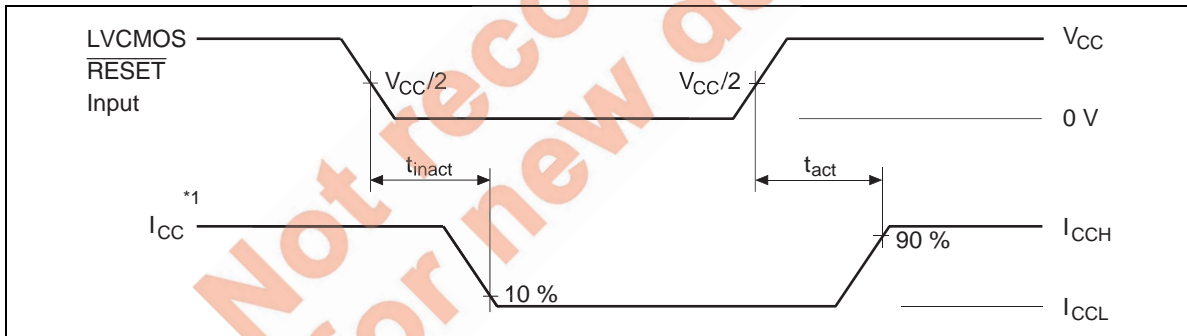
Item	Symbol	$V_{CC} = 2.5 \pm 0.2 \text{ V}$			Unit	FROM (Input)	TO (Output)
		Min	Typ	Max			
Maximum clock frequency	f_{max}	200	—	—	MHz		
Propagation delay time ^{*2}	$t_{\text{PLH}}, t_{\text{PHL}}$	1.1	—	2.8	ns	CLK, $\overline{\text{CLK}}$	Q
	t_{PHL}	—	—	5.0			$\overline{\text{RESET}}$

- Notes:
1. Although the clock is differential, all timing is relative to CLK going high and $\overline{\text{CLK}}$ going low.
 2. This timing relationship is specified into test load (see waveforms – 3, 4) with all of the outputs switching.
 3. Assumes into an equivalent, distributed load to the address net structure defined in the application information provided in this specification.
 4. For data signal input slew rate $\geq 1 \text{ V/ns}$.
 5. For data signal input slew rate $\geq 0.5 \text{ V/ns}$ and $< 1 \text{ V/ns}$.
 6. CLK, $\overline{\text{CLK}}$ signals input slew rates are $\geq 1 \text{ V/ns}$.

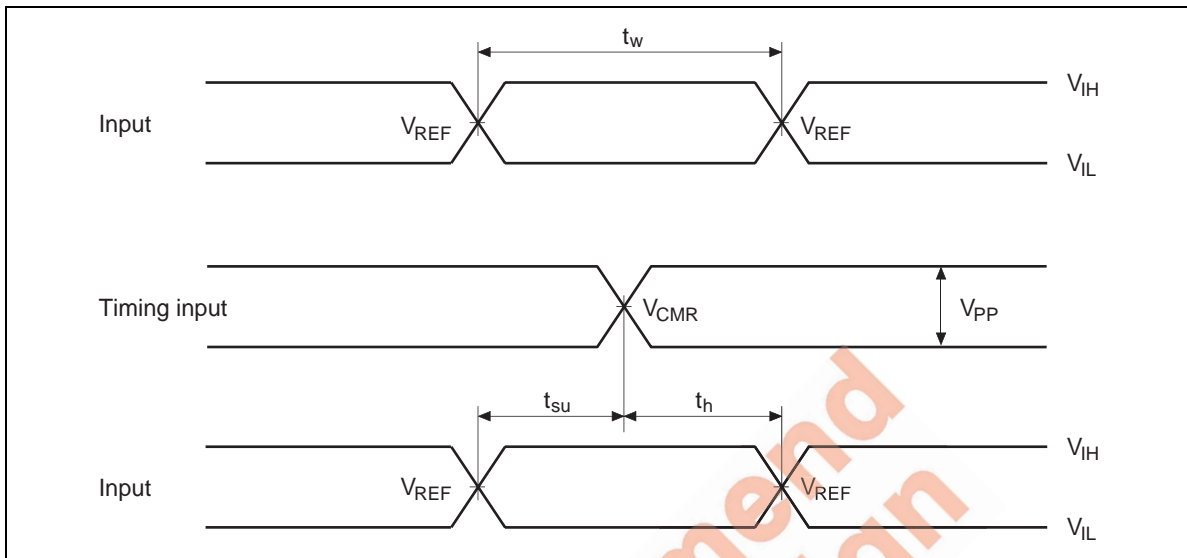
Test Circuit



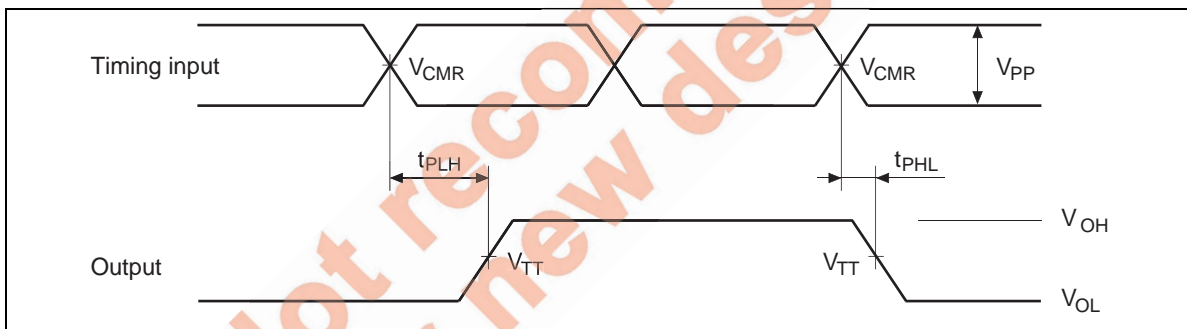
Waveforms - 1



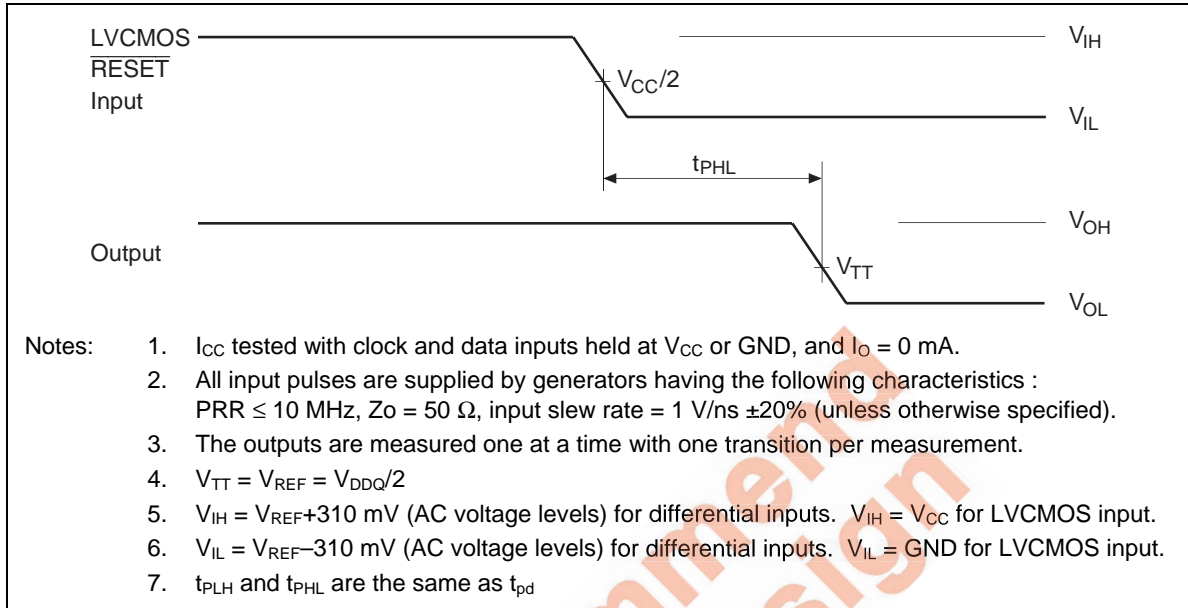
Waveforms – 2



Waveforms – 3



Waveforms – 4



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Application Data

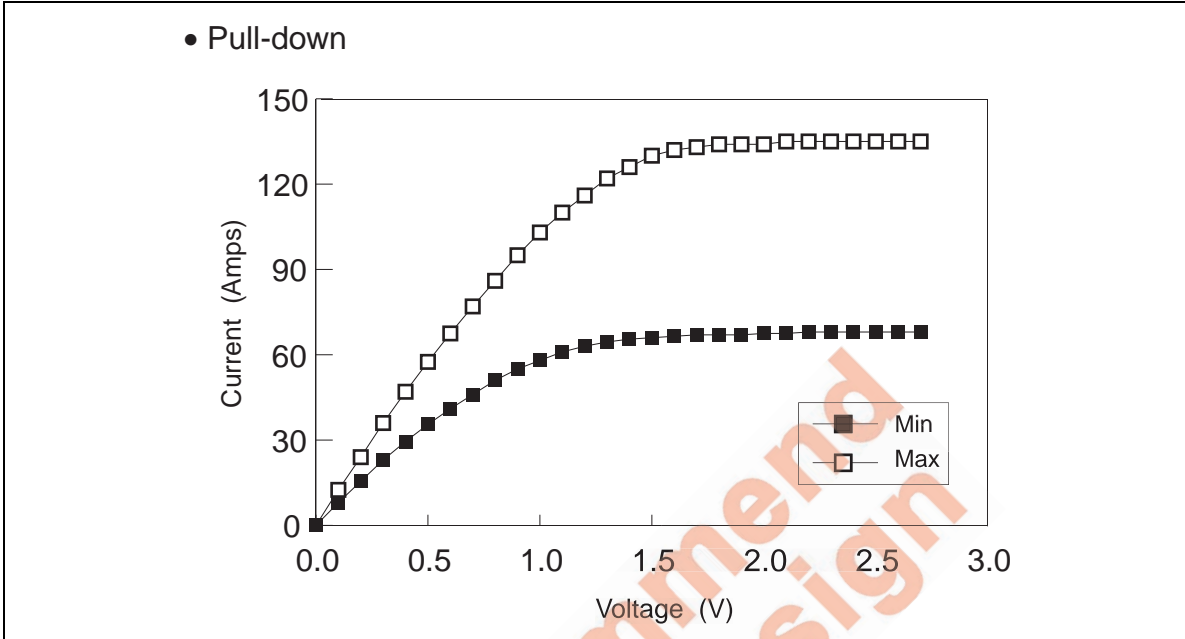


Figure. 1

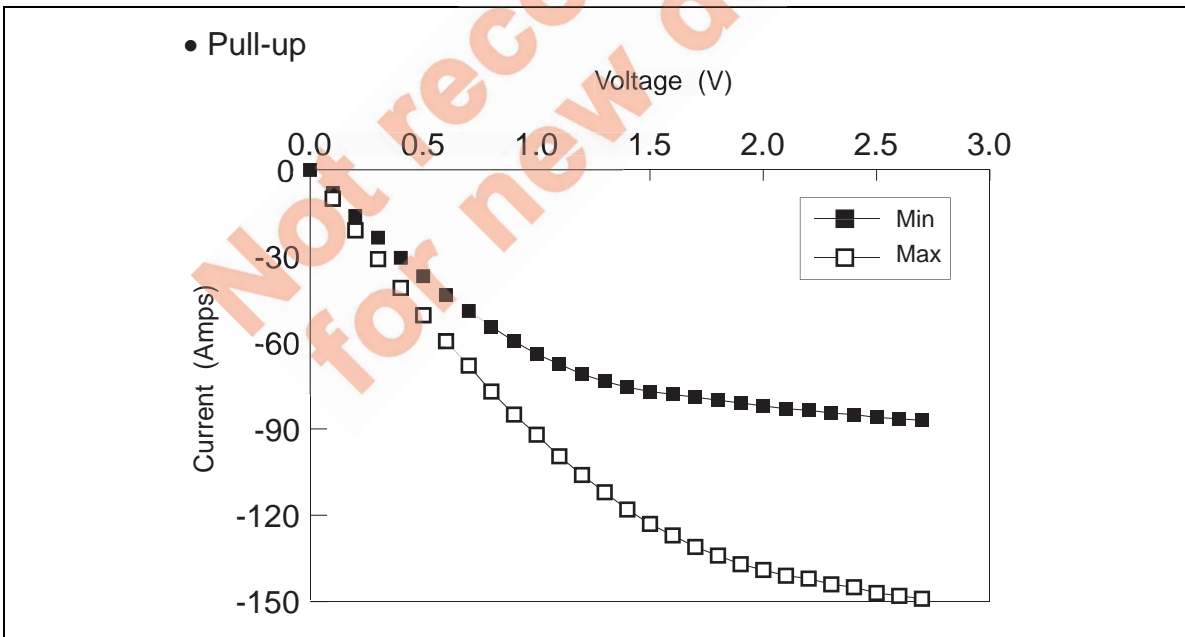
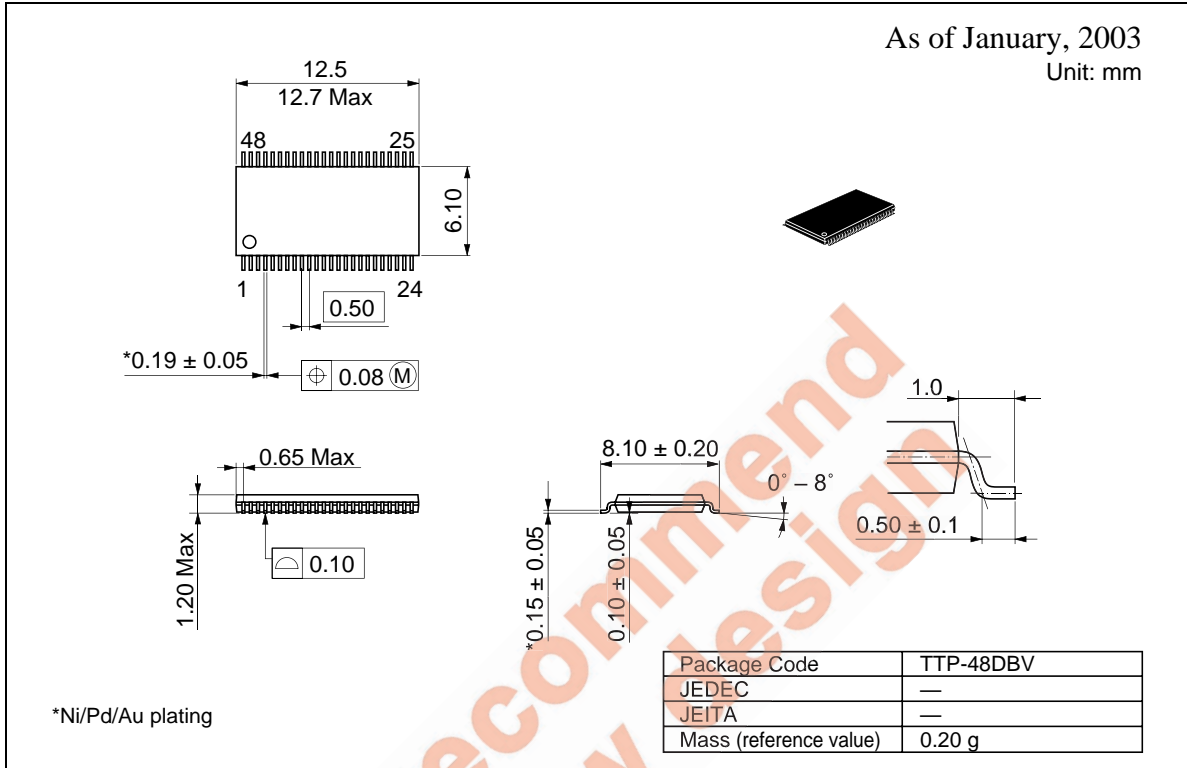


Figure. 2

Curve Data

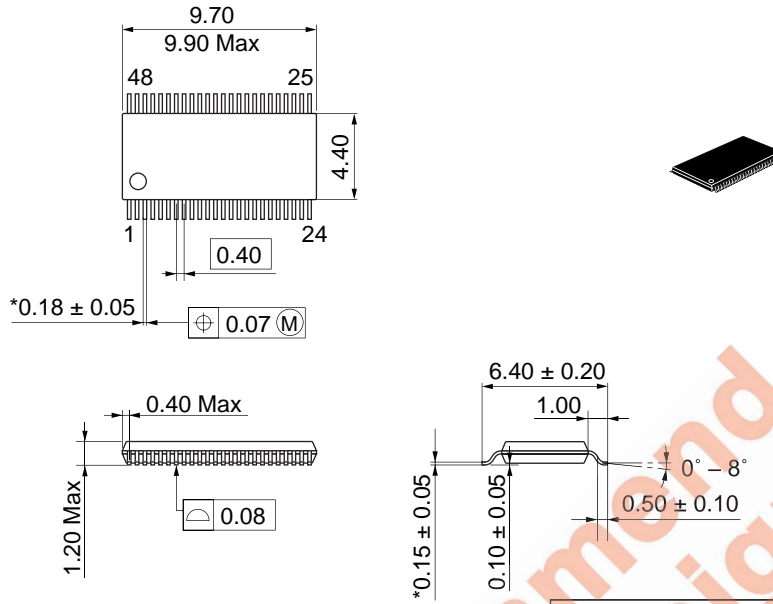
Voltage (V)	Pull-down		Pull-up	
	I (mA)	I (mA)	I (mA)	I (mA)
	Min	Max	Min	Max
0	0	0	0	0
0.1	8	12.5	-8	-10
0.2	15.5	24	-16	-21
0.3	23	36	-23.5	-31
0.4	29.5	47	-30.5	-41
0.5	35.5	57.5	-37	-50.5
0.6	41	67.5	-43.5	-59.5
0.7	46	77	-49	-68
0.8	51	86	-54.5	-77
0.9	55	95	-59.5	-85
1	58	103	-64	-92
1.1	61	110	-67.5	-99.5
1.2	63	116	-71	-106
1.3	64.5	122	-73.5	-112
1.4	65.5	126	-75.5	-118
1.5	66	130	-77	-123
1.6	66.5	132	-78	-127
1.7	67	133	-79	-131
1.8	67	134	-80	-134
1.9	67	134	-81	-137
2	67.5	134	-82	-139
2.1	67.5	135	-83	-141
2.2	68	135	-83.5	-142
2.3	68	135	-84.5	-144
2.4	68	135	-85	-145
2.5	68	135	-86	-147
2.6	68	135	-86.5	-148
2.7	68	135	-87	-149

Package Dimensions



As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-48DEV
JEDEC	—
JEITA	—
Mass (reference value)	0.12 g

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Keep safety first in your circuit designs!

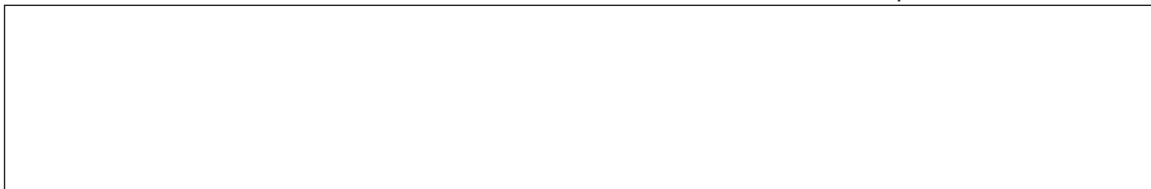
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