OKI SEMICONDUCTOR

Dear customers,

About the change in the name such as "Oki Electric Industry Co. Ltd." and "OKI" in documents to OKI Semiconductor Co., Ltd.

The semiconductor business of Oki Electric Industry Co., Ltd. was succeeded to OKI Semiconductor Co., Ltd. on October 1, 2008. Therefore, please accept that although the terms and marks of "Oki Electric Industry Co., Ltd.", “Oki Electric”, and "OKI" remain in the documents, they all have been changed to "OKI Semiconductor Co., Ltd.". It is a change of the company name, the company trademark, and the logo, etc. , and NOT a content change in documents.

October 1, 2008
OKI Semiconductor Co., Ltd.

OKI SEMICONDUCTOR CO., LTD.

550-1 Higashiasakawa-cho, Hachioji-shi, Tokyo 193-8550, Japan
http://www.okisemi.com/en/

OKI Semiconductor

This version: Aug. 1998
Previous version: Nov. 1996

MSM7705-01/02/03

4ch Single Rail CODEC

GENERAL DESCRIPTION

The MSM7705-01/02/03 are four-channel CODEC CMOS ICs for voice signals ranging from 300 to 3400 Hz. These devices contain filters for A/D and D/A conversion.
Designed especially for a single-power supply and low-power applications, these devices contain four-channel A/D and D/A converters in a single chip and achieve a reduced footprint and a reduced number of external components.
The MSM7705-01/02/03 are best suited for digital telephone terminals, digital PABXs, and push-button phones.

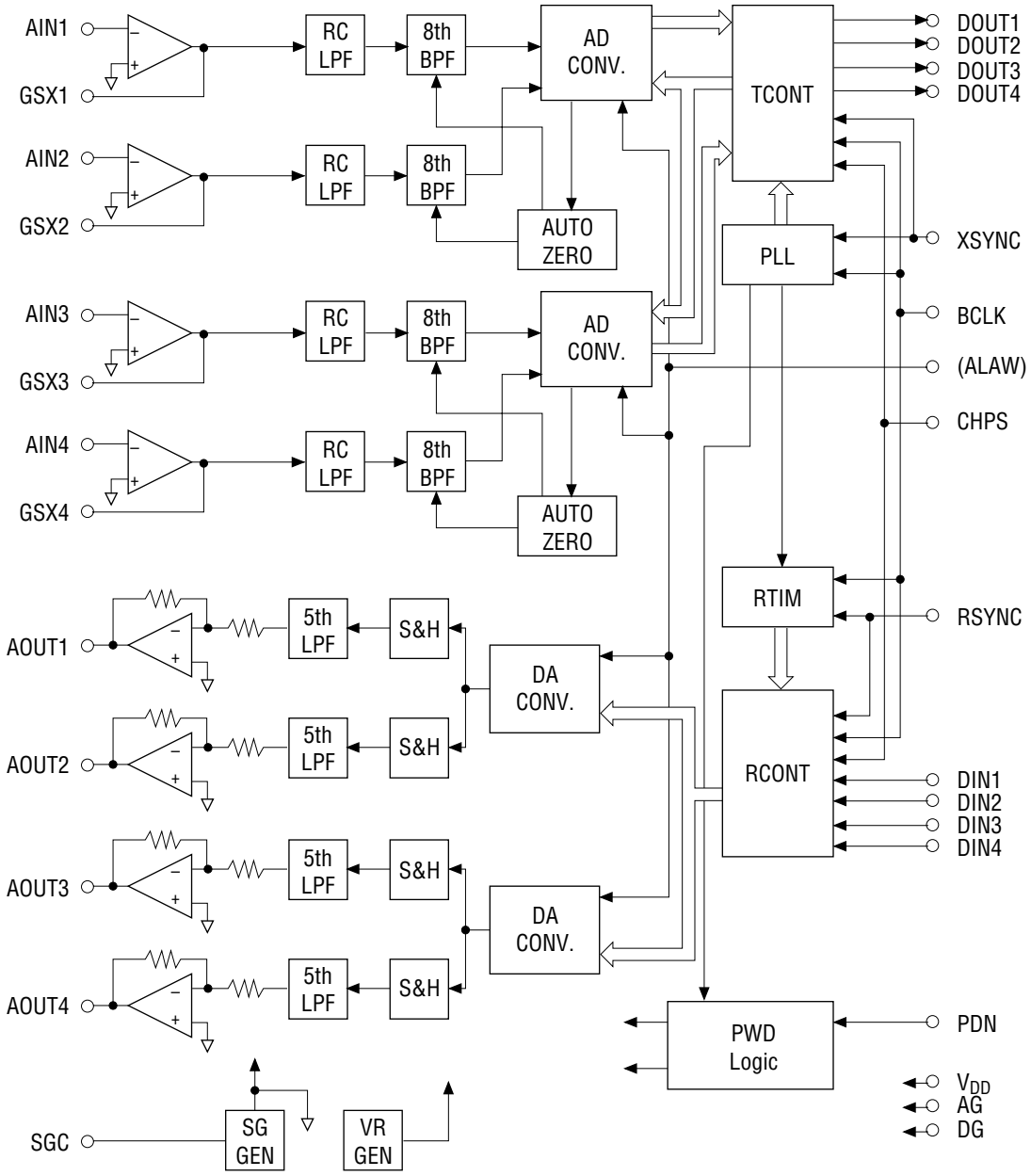
FEATURES

- Single power supply: +5 V
- Power consumption

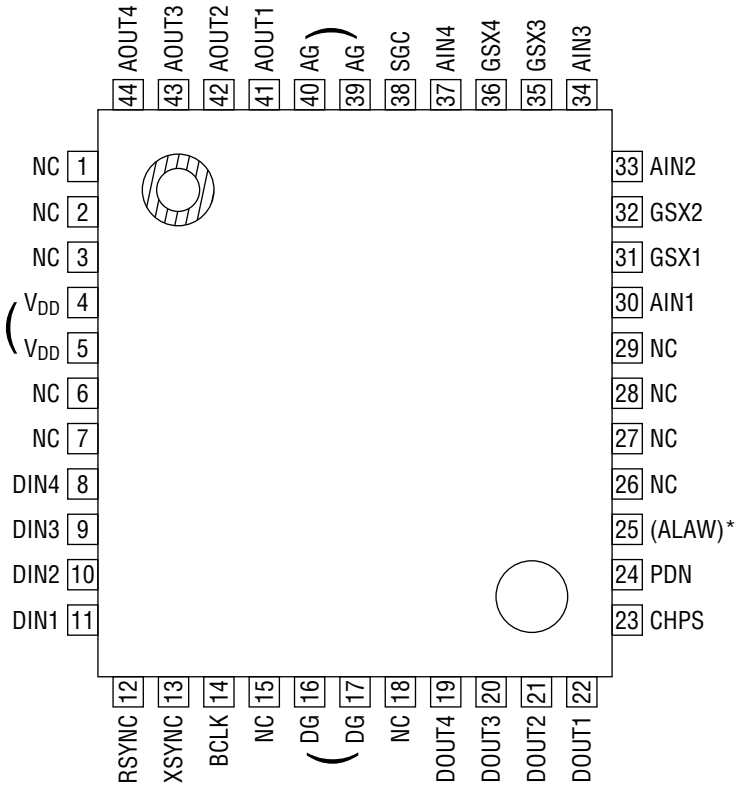
Operating mode:	70 mW Typ.	140 mW Max.
Power-saving mode:	14 mW Typ.	32 mW Max.
Power-down mode:	0.05 mW Typ.	0.3 mW Max.

- Conforms to ITU-T Companding law
  - MSM7705-01: μ/A-law pin-selectable
  - MSM7705-02: μ-law
  - MSM7705-03: A-law
- Built-in PLL eliminates a master clock
- The PCM interface can be switched between 4 channel serial/parallel
- Transmission clock: 64/128/256/512/1024/2048 kHz
  96/192/384/768/1536/1544 kHz
  (During 4 channel serial mode, the 64, 96, 128, and 192 kHz clocks are disabled)
- Transmit gain adjustable for each channel
- Built-in reference voltage supply
- Analog output can directly drive a 600 Ω line transformer
- Package:
  44-pin plastic QFP (QFP44-P-910-0.80-2K) (Product name : MSM7705-01GS-2K)
  (Product name : MSM7705-02GS-2K)
  (Product name : MSM7705-03GS-2K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC : No connect pin

44-Pin Plastic QFP

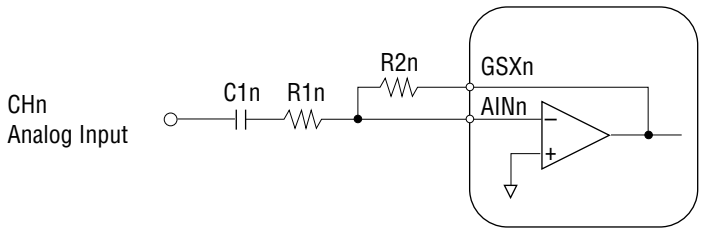
V_{DD}, DG, and AG have two pins each. Each of these pairs are internally connected with each other.

* The ALAW pin is only supported by MSM7705-01GS-2K.

PIN AND FUNCTIONAL DESCRIPTIONS

AIN1, AIN2, AIN3, AIN4, GSX1, GSX2, GSX3, GSX4

AIN1, AIN2, AIN3, and AIN4 are the transmit analog inputs for channels 1, 2, 3 and 4 respectively.
GSX1, GSX2, GSX3, and GSX4 are the transmit level adjustments for channels 1, 2, 3 and 4 respectively.
AIN1, AIN2, AIN3, and AIN4 are connected to the inverting inputs for the op-amps. GSX1, GSX2, GSX3, and GSX4 are connected to the outputs for the op-amps. They are used to adjust levels as shown below, and are connected to the outputs of the op-amps.
During power saving mode and power down mode, the GSX1, GSX2, GSX3, and GSX4 outputs are at 0 V.
When these pins are not used, connect AIN1 to GSX1, AIN2 to GSX2, AIN3 to GSX3, and AIN4 to GSX4.



CHn Gain
Gain = R2n/R1n ≤ 10
R1n: Variable
R2n > 20 kΩ
C1n > 1/(2 × 3.14 × 30 × R1n) (F)

AOUT1, AOUT2, AOUT3, AOUT4

AOUT1, AOUT2, AOUT3, and AOUT4 are the receive filter outputs for channels 1, 2, 3, and 4 respectively.
When the digital signal of +3 dBm0 is input to DIN1, DIN2, DIN3, and DIN4, the output signal has an amplitude of 3.4 V_{PP} above and below the signal ground voltage (SG : 1/2 V_{DD}). The output can drive a load of 600 Ω or more.
During power saving or power down mode, these outputs are at the voltage level of SG with a high impedance.

DIN1, DIN2, DIN3

PCM signal inputs for channels 1, 2, and 3 when the parallel mode is selected.
D/A conversion is performed by the serial PCM signals to these pins, the RSYNC signals synchronous with the serial PCM signals, and the BCLK signal. Then the analog signals are output from AOUT1, AOUT2, and AOUT3 pins, respectively.
The data rate of the PCM signal is equal to the frequency of the BCLK signal.
The PCM signal is shifted at the falling edge of the BCLK signal and latched into the internal register when shifted by eight bits.
The start of the PCM data (MSD) is identified at the rising edge of RSYNC.
When the serial mode is selected, this pin is not used and should be connected to GND (0 V).

DIN4

PCM signal input for channel 4 when the parallel mode is selected.
D/A conversion is performed by the serial PCM signal to this pin, the RSYNC signal synchronous with the serial PCM signal, and the BCLK signal. Then the analog signal is output from AOUT4 pin.
The data rate of the PCM signal is equal to the frequency of the BCLK signal.
The PCM signal is shifted at the falling edge of the BCLK signal and latched into the internal register when shifted by eight bits.
The start of the PCM data (MSD) is identified at the rising edge of RSYNC.
When the serial mode is selected, this pin is used for the 4ch multiplexed PCM signal input.

BCLK

Shift clock signal input for DIN1, DIN2, DIN3, DIN4, DOUT1, DOUT2, DOUT3, and DOUT4. The frequency is equal to the data rate. Setting this signal to logic "1" or "0" drives both transmit and receive circuits to the power saving state.

RSYNC

Receive synchronizing signal input.
Eight bits of PCM data required are selected from a series of PCM signal to the DIN1, DIN2, DIN3, and DIN4 pins by the receive synchronizing signal.
All timing signals in the receive section are synchronized by this synchronizing signal. This signal must be synchronized in phase with the BCLK (generated from the same clock source as BCLK). The frequency should be 8 kHz ±50 ppm to guarantee the AC characteristics which are mainly the frequency characteristics of the receive section.
However, this device operates in the range of 6 kHz to 10 kHz unless the frequency characteristics of the system used are strictly specified, but the electrical characteristics specified in the data sheet are not guaranteed.

XSYNC

Transmit synchronizing signal input.
PCM output signal from the DOUT1, DOUT2, DOUT3, and DOUT4 pins is output in synchronization with this transmit synchronizing signal. This synchronizing signal triggers the PLL and synchronizes all timing signals of the transmit section.
This synchronizing signal must be synchronized in phase with BCLK.
The frequency should be 8 kHz ±50 ppm to guarantee the AC characteristics which are mainly the frequency characteristics of the transmit section.
However, this device can be operated in the range of 6 kHz to 10 kHz unless the frequency characteristics of the system used are strictly specified, but the electrical characteristics are not guaranteed.
Setting this signal to logic "1" or "0" drives both transmit and receive circuits to power saving state.

DOUT1

PCM signal output of channel 1 when the parallel mode is selected.
The PCM output signal is output from MSD in a sequential order, synchronizing with the rising edge of the BCLK signal.
MSD may be output at the rising edge of the XSYNC signal, based on the timing between BCLK and XSYNC.
This pin is in a high impedance state except during 8-bit PCM output. It is also in a high impedance state during power-saving state or power-down state.
When the serial mode is selected, this pin is configured to be the output of serial multiplexed 4ch PCM signal.
A pull-up resistor must be connected to this pin because it is an open drain output.
This device is compatible with the ITU-T recommendation on coding law and output coding format.
The MSM7705-03 (A-law) outputs the character signal, inverting the even bits.

Input/Output Level	PCMIN/PCMOUT	
	MSM7705-02 (μ-law)	MSM7705-03 (A-law)
	MSD	MSD
+Full scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
+0	1 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1
–0	0 1 1 1 1 1 1 1	0 1 0 1 0 1 0 1
–Full scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

DOUT2, DOUT3, DOUT4

PCM signal outputs for channels 2, 3, and 4 when parallel mode is selected.
The PCM output signal is output from MSD in a sequential order, synchronizing with the rising edge of the BCLK signal.
MSD may be output at the rising edge of the XSYNC signal, based on the timing between BCLK and XSYNC.
This pin is in a high impedance state except during 8-bit PCM output. It is also in a high impedance state during power-saving state or power-down state.
When the serial mode is selected, this pin is unconnected.
A pull-up resistor must be connected to each of these pins because it is an open drain output.
This device is compatible with the ITU-T recommendation on coding law and output coding format.
The MSM7705-03 (A-law) outputs the character signal inverting the even bits.

CHPS

Control signal input for the mode selection of PCM input and output.
When this signal is at a logic "1" level, the PCM input and output are in parallel mode. The PCM data of CH1, CH2, CH3, and CH4 is input to DIN1, DIN2, DIN3, and DIN4 outputs from DOUT1, DOUT2, DOUT3, and DOUT4 with the same timing.
When this signal is at logic "0" level, the PCM input and output are in serial mode. The PCM data of CH1 to CH4 is input from DIN4 and output from DOUT1 as time division multiplexed data.

PDN

Power down control signal.
When PDN is at a logic "0" level, both transmit and receive circuits are in power down state.

V_{DD}

Power supply for +5 V.
A power supply for an analog circuit in the system to which the device is applied should be used.
A bypass capacitor of 0.1 µF to 1 µF with excellent high-frequency characteristics and a capacitor of 10 µF to 20 µF should be connected between this pin and the AG pin if needed.

AG

Analog signal ground.

DG

Ground for digital signal circuits.
This ground is separate from the analog signal ground. The DG pin must be connected to the AG pin on the printed circuit board to make a common analog ground.

SGC

Used to generate the signal ground voltage level by connecting a bypass capacitor.
Connect a 0.1 µF capacitor with excellent high frequency characteristics between the AG pin and the SGC pin.

ALAW

Control signal input of the companding law selection.
Only the MSM7705-01GS-2K has this pin. The CODEC will operate in the µ-law when this pin is at a logic "0" level and will operate in the A-law when this pin is at a logic "1" level. The CODEC operates in the µ-law if the pin is left open, since this pin is internally pulled down.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	0 to 7.0	V
Analog Input Voltage	V_{AIN}	—	–0.3 to V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	Voltage must be fixed		4.75	5.0	5.25	V
Operating Temperature	Ta	—		–30	+25	+85	°C
Analog Input Voltage	V_{AIN}	Gain = 1		—	—	3.4	V_{PP}
High Level Input Voltage	V_{IH}	XSYNC, RSYNC, BCLK, DIN1, DIN2, DIN3, DIN4, PDN, CHPS, ALAW		2.2	—	V_{DD}	V
Low Level Input Voltage	V_{IL}			0	—	0.8	V
Clock Frequency	F_C	BCLK = (When in 4ch serial mode, 64, 96, 128, 192 kHz are not used)		64, 128, 256, 512, 1024, 2048, 96, 192, 384, 768, 1536, 1544			kHz
Sync Pulse Frequency	F_S	XSYNC, RSYNC		6.0	8.0	10.0	kHz
Clock Duty Ratio	D_C	BCLK		40	50	60	%
Digital Input Rise Time	t_{Ir}	XSYNC, RSYNC, BCLK, DIN1, DIN2, DIN3, DIN4, PDN, CHPS		—	—	50	ns
Digital Input Fall Time	t_{If}			—	—	50	ns
Transmit Sync Pulse Setting Time	t_{XS}	BCLK→XSYNC, See Fig. 1		100	—	—	ns
	t_{SX}	XSYNC→BCLK, See Fig. 1		100	—	—	ns
Receive Sync Pulse Setting Time	t_{RS}	BCLK→RSYNC, See Fig. 1		100	—	—	ns
	t_{SR}	RSYNC→BCLK, See Fig. 1		100	—	—	ns
Sync Pulse Width	t_{WS}	XSYNC, RSYNC		1 BCLK	—	100	µs
DIN Setup Time	t_{DS}	DIN1, DIN2, DIN3, DIN4		100	—	—	ns
DIN Hold Time	t_{DH}	DIN1, DIN2, DIN3, DIN4		100	—	—	ns
Digital Output Load	R_{DL}	DOUT1, DOUT2,	Pull-up resistor	0.5	—	—	kΩ
	C_{DL}	DOUT3, DOUT4	—	—	—	100	pF
Analog Input Allowable DC Offset	V_{off}	Transmit gain stage, Gain = 1		V_{DD}/2 –100	—	V_{DD}/2 +100	mV
		Transmit gain stage, Gain = 10		V_{DD}/2 –10	—	V_{DD}/2 +10	mV
Allowable Jitter Width	—	XSYNC, RSYNC		—	—	500	ns

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

(V_{DD} = +5 V ±5%, Ta = –30°C to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	Operating mode, No signal	—	14.0	28.0	mA
	I_{DD2}	Power-save mode, PDN = 1, XSYNC or BCLK OFF	—	2.6	6.0	mA
	I_{DD3}	Power-down mode, PDN = 0 BCLK OFF	—	0.01	0.05	mA
High Level Input Voltage	V_{IH}	—	2.2	—	V_{DD}	V
Low Level Input Voltage	V_{IL}	—	0.0	—	0.8	V
High Level Input Leakage Current	I_{IH}	—	—	—	2.0	µA
Low Level Input Leakage Current	I_{IL}	—	—	—	0.5	µA
Digital Output Low Voltage	V_{OL}	Pull-up resistor > 500 Ω	0.0	0.2	0.4	V
Digital Output Leakage Current	I_O	—	—	—	10	µA
Input Capacitance	C_{IN}	—	—	5	—	pF

Transmit Analog Interface Characteristics

(V_{DD} = +5 V ± 5%, Ta = –30°C to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Input Resistance	R_{INX}	AIN1, AIN2, AIN3, AIN4		10	—	—	MΩ
Output Load Resistance	R_{LGX}	GSX1, GSX2, GSX3, GSX4 with respect to SG		20	—	—	kΩ
Output Load Capacitance	C_{LGX}			—	—	30	pF
Output Amplitude	V_{OGX}			–1.7	—	+1.7	V
Offset Voltage	V_{OSGX}		Gain = 1	–20	—	+20	mV

Receive Analog Interface Characteristics

(V_{DD} = +5 V ±5%, Ta = –30°C to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Output Load Resistance	R_{LAO}	AOUT1	Each output; with respect to SG	0.6	—	—	kΩ
Output Load Capacitance	C_{LAO}	AOUT2	—	—	—	50	pF
Output Amplitude	V_{OAO}	AOUT3 AOUT4	R_L = 0.6 kΩ; with respect to SG	–1.7	—	+1.7	V
Offset Voltage	V_{OSAO}		—	–100	—	+100	mV

AC Characteristics

(V_{DD} = +5 V ±5%, Ta = –30°C to +85°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Transmit Frequency Response	Loss T1	60	0		20	26	—	dB
	Loss T2	300			–0.15	+0.07	+0.20	
	Loss T3	1020			Reference			
	Loss T4	2020			–0.15	–0.04	+0.20	
	Loss T5	3000			–0.15	+0.03	+0.20	
	Loss T6	3400			0	0.40	0.80	
Receive Frequency Response	Loss R1	300	0		–0.15	–0.03	+0.20	dB
	Loss R2	1020			Reference			
	Loss R3	2020			–0.15	+0.04	+0.20	
	Loss R4	3000			–0.15	+0.11	+0.20	
	Loss R5	3400			0.0	0.47	0.80	
Transmit Signal to Distortion Ratio	SD T1	1020	3	*1	35	43	—	dB
	SD T2		0		35	41	—	
	SD T3		–30		35	38	—	
	SD T4		–40		29	31.5	—	
	SD T5		–45		24	27	—	
Receive Signal to Distortion Ratio	SD R1	1020	3	*1	36	43	—	dB
	SD R2		0		36	41	—	
	SD R3		–30		36	40	—	
	SD R4		–40		30	33.5	—	
	SD R5		–45		25	30	—	
Transmit Gain Tracking	GT T1	1020	3		–0.3	+0.02	+0.3	dB
	GT T2		–10		Reference			
	GT T3		–40		–0.3	+0.04	+0.3	
	GT T4		–50		–0.5	+0.15	+0.5	
	GT T5		–55		–1.2	+0.40	+1.2	
Receive Gain Tracking	GT R1	1020	3		–0.3	0.0	+0.3	dB
	GT R2		–10		Reference			
	GT R3		–40		–0.3	+0.04	+0.3	
	GT R4		–50		–0.5	+0.16	+0.5	
	GT R5		–55		–1.2	+0.37	+1.2	

*1 Psophometric filter is used

AC Characteristics (Continued)

(V_{DD} = +5 V ±5%, Ta = –30°C to +85°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Idle Channel Noise	Nidle T	—	—	AIN = SG *1 *2	—	–73.5	–70	dBm0p
					—	–71.5	–68	
	Nidle R	—	—	*1 *3	—	–78	–75	
Absolute Level (Initial Difference)	AV T	1020	0	V_{DD} = 5.0 V Ta = 25°C	0.821	0.850	0.880	Vrms
	AV R				0.821	0.850	0.880	
Absolute Level (Deviation of Temperature and Power)	AV Tt			V_{DD} = 5 V ±5% Ta = –30 to +85°C	–0.2	—	+0.2	dB
	AV Rt				–0.2	—	+0.2	dB
Absolute Delay	t_D	1020	0	A to A BCLK = 64 kHz	—	—	0.60	ms
Transmit Group Delay	t_{GD} T1	500	0	*4	—	0.19	0.75	ms
	t_{GD} T2	600			—	0.11	0.35	
	t_{GD} T3	1000			—	0.02	0.125	
	t_{GD} T4	2600			—	0.05	0.125	
	t_{GD} T5	2800			—	0.07	0.75	
Receive Group Delay	t_{GD} R1	500	0	*4	—	0.00	0.75	ms
	t_{GD} R2	600			—	0.00	0.35	
	t_{GD} R3	1000			—	0.00	0.125	
	t_{GD} R4	2600			—	0.09	0.125	
	t_{GD} R5	2800			—	0.12	0.75	
Crosstalk Attenuation	CR T	1020	0	TRANS → RECV	75	80	—	dB
	CR R			RECV → TRANS	70	76	—	
	CR CH			CH to CH	75	80	—	

*1 Psophometric filter is used
*2 Upper columns are specified for the μ-law, lower for the A-law
*3 Input "0" code to PCMIN
*4 Minimum value of the group delay distortion

AC Characteristics (Continued)

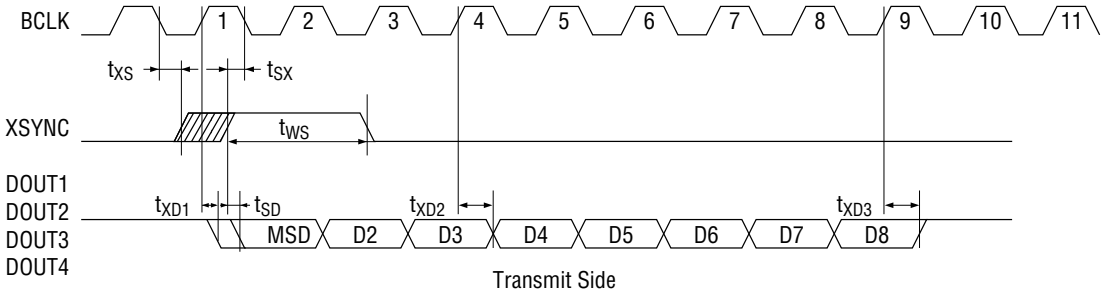
(V_{DD} = +5 V ±5%, Ta = –30°C to +85°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Discrimination	DIS	4.6 kHz to 72 kHz	0	0 to 4000 Hz	30	32	—	dB
Out-of-band Spurious	S	300 to 3400	0	4.6 kHz to 100 kHz	—	–37.5	–35	dBm0
Intermodulation Distortion	IMD	fa = 470 fd = 320	–4	2fa – fd	—	–52	–35	dBm0
Power Supply Noise Rejection Ratio	PSR T	0 to 50 kHz	50 mV_{PP}	*5	—	30	—	dB
	PSR R							
Digital Output Delay Time	t_{SD}	C_L = 100 pF + 1 LSTTL			20	—	200	ns
	t_{XD1}				20	—	200	
	t_{XD2}				20	—	200	
	t_{XD3}				20	—	200	

*5 Measurement performed under idle channel noise

TIMING DIAGRAM

Transmit Timing



Receive Timing

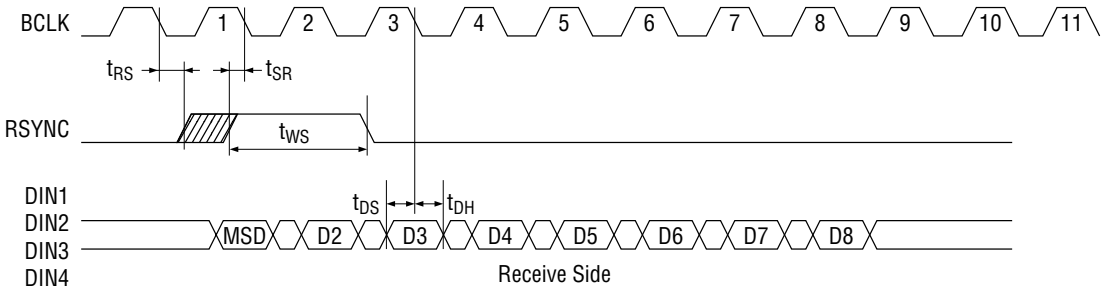


Figure 1 Timing Diagram in the Parallel Mode (CHPS = 1)

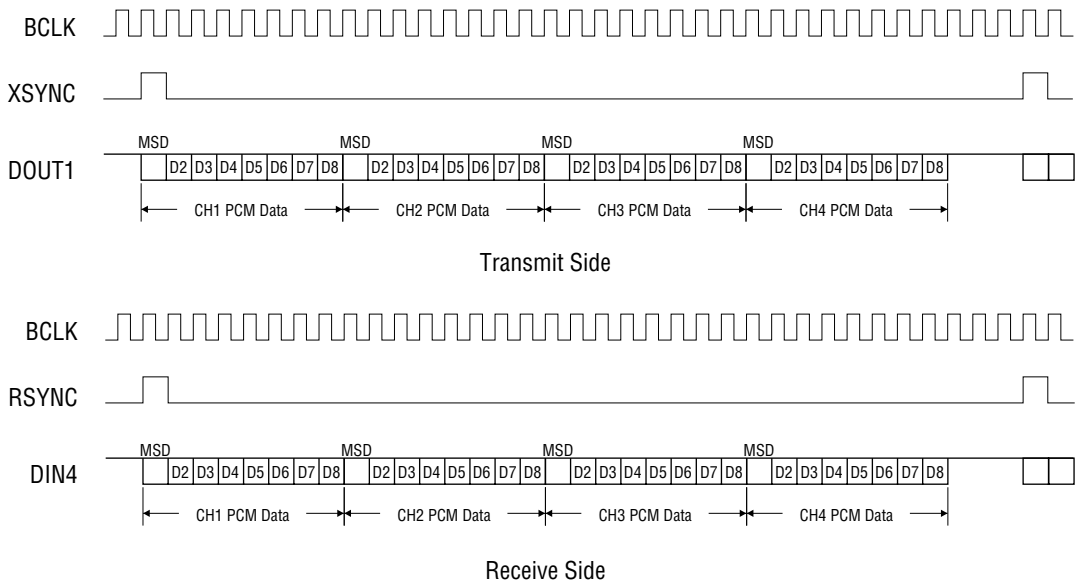
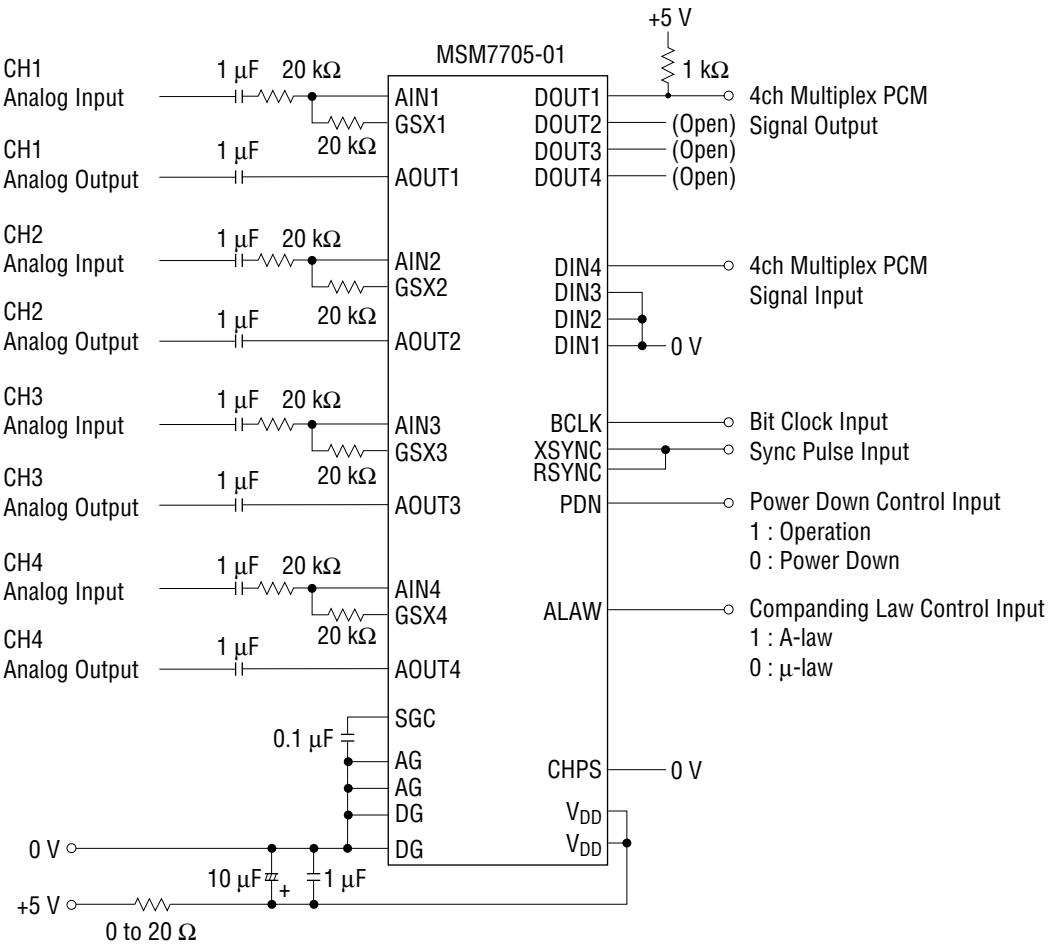


Figure 2 Timing Diagram in the Serial Mode (CHPS = 0)

APPLICATION CIRCUIT

Example of Basic Connection (PCM Serial Mode Operation)



APPLICATION INFORMATION

DOUT Pull-up Resistor

A value of the pull-up resistor for the DOUT pin should be determined depending on frequencies of BCLK and load capacitance.
If a smaller value is used, there may be some degradation in noise performance, resulting in an increase in supply current.

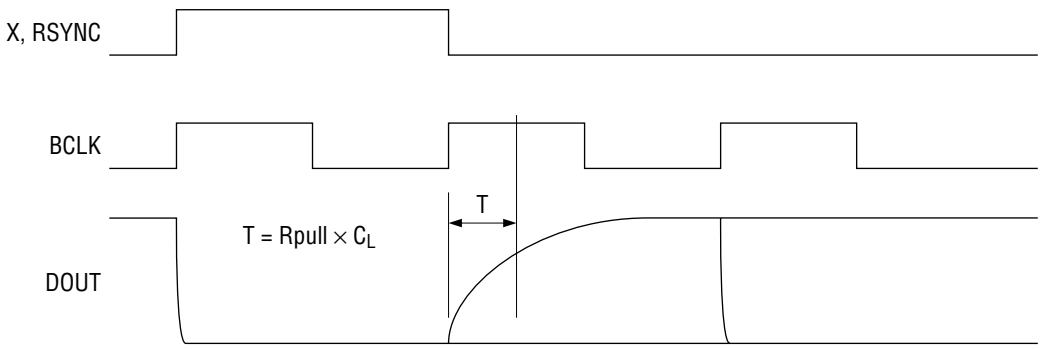
Equation to give pull-up resistor

$$Rpull = \frac{\frac{1}{4 \times f_{BCLK}} - 50\ ns}{C_L} \ (\Omega)$$

where
f_{BCLK} = Frequency of BCLK
C_L = Load capacitance of the PCMOUT pin (approximately 20 pF for a CMOS or TTL load)
50 ns = Internal delay of the MSM7705

Condition for Calculation

If data is turned back from DOUT to DIN under the condition the SYNC signal and BCLK signal rise simultaneously, the data can normally be transferred.



Calculation Example for Typical Values

BCLK (kHz)	Rpull (kΩ)			
	C_L = 10 pF	C_L = 20 pF	C_L = 50 pF	C_L = 100 pF
64	385.6	192.8	77.1	38.6
128	190.3	95.2	38.1	19.0
256	92.7	46.3	18.5	9.3
512	43.8	21.9	8.8	4.4
1024	19.4	9.7	3.9	1.9
1544	11.2	5.6	2.2	1.1
2048	7.2	3.6	1.4	0.7

Choice of Actual Resistor Value

If the calculated value is more than or equal to 100 kΩ, 100 kΩ should be employed. +10% of the calculated value is within a tolerance, thus, for example, the value of 10 kΩ can be used for the calculated value of 9.3 kΩ in the above examples.

Channel Crosstalk

The MSM7705 contains the 4-channel CODEC. The circuit and trace design and pin layout are made to minimize crosstalk between channels inside the LSI device provided the following should be taken into consideration.

Transmit side

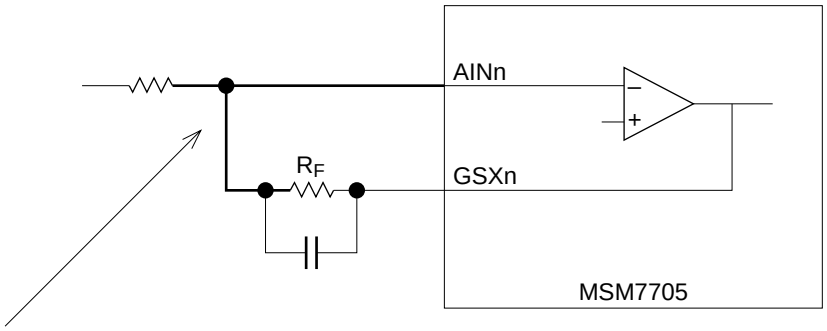
The GSX1 – AIN2, AIN3, and AIN4 traces should not be kept closer.
The GSX2 – AIN1, AIN3, and AIN4 traces should not be kept closer.
The GSX3 – AIN1, AIN2, and AIN4 traces should not be kept closer.
The GSX4 – AIN1, AIN2, and AIN3 traces should not be kept closer.

AIN1, AIN2, AIN3, and AIN4, which are op-amp inverting input pins, have higher resistance, therefore proximity of these lines to signal lines of other channels may cause crosstalk.

Receive side

The channel outputs AOUT1, AOUT2, AOUT3, and AOUT4 of the receive side are amplifier outputs with lower resistance, thus crosstalk due to PCB traces is smaller. Nevertheless, the PCB traces should not be run closer together and in parallel wherever possible.

How to Avoid Transmit Side Amplifier Oscillation Due to PCB Layout



The trace length (illustrated by the bold line in the above drawing) should be kept as short as possible in order to avoid oscillation.
The length of less than 2 cm or 3 cm is permissible, though it depends on PCB layout.
It is recommended to connect a capacitor of 20 pF to 50 pF across the feedback resistor R_F, if the oscillation occurs.

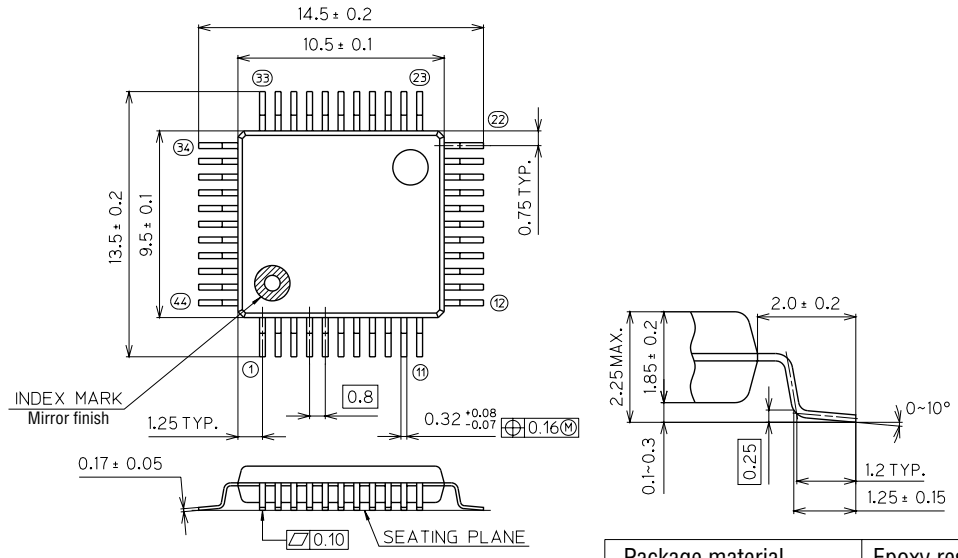
NOTES ON USED

- To ensure proper electrical characteristics, use bypass capacitors with excellent high frequency characteristics for the power supply and keep them as close as possible to the device pins.
- Connect the AG pin and the DG pin as close as possible. Connect to the system ground with low impedance.
- Mount the device directly on the board when mounted on PCBs. Do not use IC sockets. If the use of IC socket is unavoidable, use the short lead type socket.
- When mounted on a frame, use electro-magnetic shielding, if any electro-magnetic wave sources such as power supply transformers surround the device.
- Keep the voltage on the V_{DD} pin not lower than –0.3 V even instantaneously to avoid latch-up that may otherwise occur when power is turned on.
- Use a low noise (particularly, low level type of high frequency spike noise or pulse noise) power supply to avoid erroneous operation and the degradation of the characteristics of these devices.

PACKAGE DIMENSIONS

(Unit : mm)

QFP44-P-910-0.80-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.41 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).