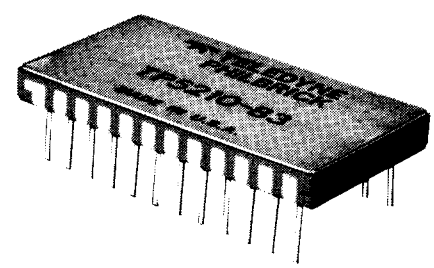
Military Standard 12 Bit High Speed A/D Converters

TP5210 Series

5210 Series 12 bit A/D converters are the military/aerospace industry's most widely accepted 12 bit A/D's. This acceptance is cornerstoned by the 5210's outstanding reliability history, by its true 12 bit performance from −55°C to +125°C, and by its ability to maintain specified accuracy over temperature without trimming potentiometers. 5210 Series devices are now designed into over 50 military/aerospace programs. All part numbers in the series are multisourced, and the 5210 Series are the first A/D's considered for QPL listing (MIL-M-38510/120 is rapidly approaching completion).

5210 Series A/D's are successive approximation type devices. The Teledyne Philbrick design replaces the traditional discrete transistor switching array and its associate thin-film resistor network with a monolithic DAC for a much lower chip count and improved reliability. A proprietary comparator preamplifier greatly reduces comparator oscillations resulting in much cleaner, more repeatable digital output transitions. The preamp allows the DAC to settle into a virtual ground, and the resulting speed improvements allow the typical TP5210 to maintain accuracy and linearity with conversion times to 7μsec. A new 1mA TC zener diode reference has not only lowered power consumption (560mW typical), its low drift allows the TP5210 to maintain much tighter accuracy drifts. In most cases, an internal-reference TP5210 can easily replace an external-reference device from another manufacturer and save the cost of the reference. Though the TP5210 is indeed a superior second source, its guaranteed performance specifications are similar to those of other 5210 Series devices. Our innovative design, however, makes it easy for us to screen for faster or more accurate devices, and we would like the opportunity to quote your tightened requirements.

The TP5210 Series is completely pin and function compatible with MN5210 Series and MN5200 Series devices. Its small, 24 pin, hermetically sealed DIP package; its low power consumption; and its fully guaranteed, factory trimmed, adjustment free operation make it an excellent choice for military/aerospace data acquisition applications. For full −55°C to +125°C operation and MIL-STD-883 high reliability screening (Method 5008), add "-83" to selected part number.



FEATURES

- 7μsec Typical Conversion Time
- ± ½LSB Linearity Guaranteed Over Temperature
- No Missing Codes Guaranteed Over Temperature
- Low 560mW Power Consumption
- Hermetically Sealed 24 Pin DIP
- −55°C to +125°C Fully Specified Operation
- Optional MIL-STD-883 Screening

APPLICATIONS

- High Reliability Data Acquisition Systems
- High Ambient Temperature Instrumentation
- Airborne Instrumentation Requiring No Recalibration

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ABSOLUTE MAXIMUM RATINGS

+15V Supply (+V_{CC}, Pin 15)	−0.5 to +18 Volts
−15V Supply (−V_{CC}, Pin 13)	+0.5 to −18 Volts
+5V Supply (+V_{dd}, Pin 2)	−0.5 to +7 Volts
Analog Input (Pin 14)	±15 Volts
Digital Inputs (Pins 1, 24)	−0.5 to +5.5 Volts
Digital Outputs	+V_{dd}
Reference Input (TP5213, 14, 15, 17)	0 to −15 Volts
Operating Temperature Range	−55°C to +125°C
Specified Temperature Range	
TP521X	0°C to +70°C
TP521X-83 (Note 1)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V and +5V, for Ext. Ref. Models V_{Ref} = −10.000V, unless otherwise specified).

ANALOG INPUTS	MODEL NUMBER (Internal Ref.)	MODEL NUMBER (External Ref.)
Input Range (Input Impedance)		
0 to −10V (5kΩ)	TP5210	TP5213
−5V to +5V (5kΩ)	TP5211	TP5214
−10V to +10V (10kΩ)	TP5212	TP5215
0 to +10V (5kΩ)	TP5216	TP5217

TRANSFER CHARACTERISTICS (Note 2)	TYP.	MAX.	TYP.	MAX.	UNITS
Linearity Error: +25°C	±¼	±½	±¼	±½	LSB
0°C to +70°C (TP521X)	±¼	±½	±¼	±½	LSB
−55°C to +125°C (TP521X-83)		±½		±½	LSB
Differential Linearity Error	±½		±½		LSB
No Missing Codes	Guaranteed Over Temperature				
Full Scale Absolute Accuracy (Note 3):					
+25°C	±0.025	±0.05	±0.025	±0.05	%FSR
0°C to +70°C (TP521X)	±0.1	±0.4	±0.05	±0.1	%FSR
−55°C to +125°C (TP521X-83)	±0.2	±0.4	±0.05	±0.1	%FSR
Zero Error (Note 4): +25°C	±0.01	±0.025	±0.01	±0.025	%FSR
0 to +70°C (TP521X)	±0.015	±0.05	±0.015	±0.05	%FSR
−55°C to +125°C (TP521X-83)	±0.025	±0.05	±0.025	±0.05	%FSR
Gain Error (Note 5)	±0.025		±0.025		%
Gain Drift	±10		±3		ppm/°C
Conversion Time (Note 6)	7	13	7	13	μsec

DIGITAL INPUTS (ALL UNITS)	MIN.	TYP.	MAX.	UNITS
Logic Levels: Logic "1"	2.0		+5.5	Volts
Logic "0"	0		+0.7	Volts
Clock Input (Note 7): Pulse Width High	125			nsec
Pulse Width Low	175			nsec
Loading High (V_{in} = 2.4V)		2	20	μA
Loading Low (V_{in} = 0.3V)		−0.25	−0.4	mA
Frequency (Note 6)		1.7	1	MHz
Start Convert Input: Loading High (V_{in} = 2.4V)		4	40	μA
Loading Low (V_{in} = 0.3V)		−0.25	−0.4	mA
Setup Time Start Low to Clock (Note 8)	25			nsec

DIGITAL OUTPUTS (ALL UNITS)	MIN.	TYP.	MAX.	UNITS
Logic Coding (Note 9): Unipolar Ranges	Complementary Straight Binary			
Bipolar Ranges	Complementary Offset Binary			
Logic Levels: Logic "1"	2.4	3.6		Volts
Logic "0"		0.15	0.3	Volts
Output Drive Capability, All Outputs (Note 10): Logic "1"	8			TTL Loads
Logic "0"	2			TTL Loads

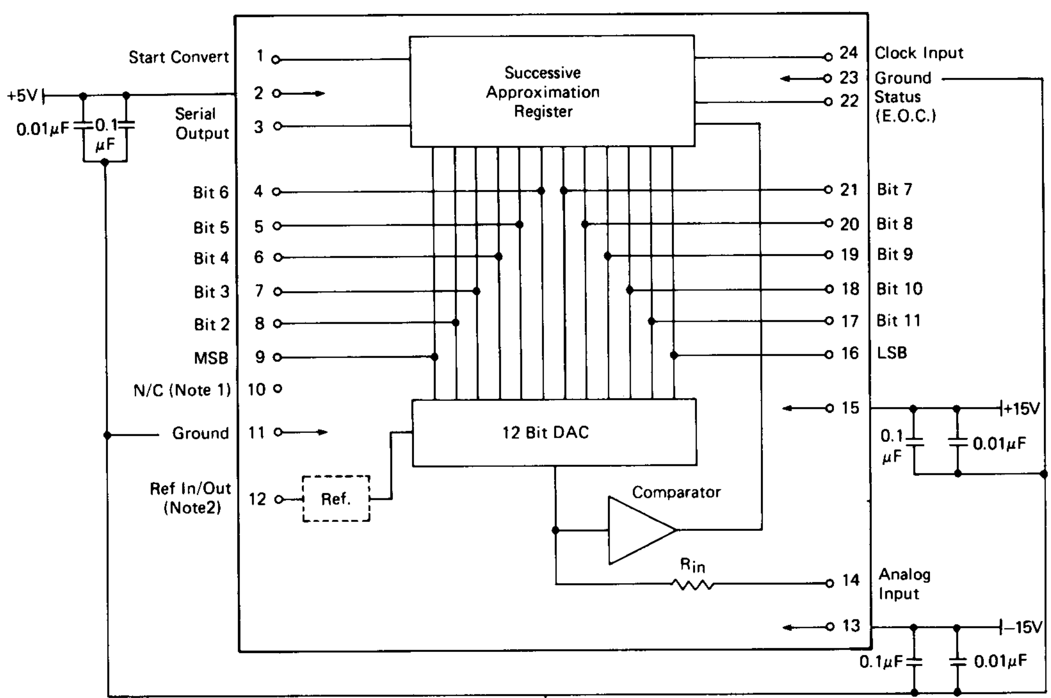
REFERENCE INPUT/OUTPUT	MIN.	TYP.	MAX.	UNITS
Internal Reference: Voltage		−6.3		Volts
Accuracy		±2		%
Tempco of Drift		±5		ppm/°C
Max. External Current			100	μA
External Reference: Voltage		−10.000		Volts
Loading		200		μA

POWER SUPPLIES (ALL UNITS)	MIN.	TYP.	MAX.	UNITS
Power Supply Range: ± 15V Supplies			± 10	%
+ 5V Supply			± 5	%
Power Supply Rejection: + 15V Supply		± 0.002	± 0.005	%FSR/%Vs
− 15V Supply		± 0.001	± 0.003	%FSR/%Vs
Current Drain: + 15V Supply		7	13	mA
− 15V Supply		− 19	− 29	mA
+ 5V Supply		34	57	mA
− 10V Reference (TP5213/14/15/17)		200		μA
Power Consumption		560	915	mW

SPECIFICATION NOTES:

1. "-83" versions of TP5210 Series devices are fully specified and guaranteed for − 55°C to + 125°C operation and are screened to the high reliability requirements of MIL-STD-883, Method 5008.
2. For a 12 bit converter, 1LSB = 0.024%FSR. FSR stands for Full Scale Range and is equal to the peak to peak voltage of the selected input range. For the ± 10V input range, FSR is 20 volts, and 1LSB is equal to 4.88mV. For the 0 to + 10V, 0 to − 10V, and ± 5V ranges, FSR is 10 volts, and 1LSB is equal to 2.44mV.
3. For TP5210/13 Full Scale Accuracy refers to the deviation between the ideal and the actual input voltage at which the all "1's" to 111...110 output transition occurs. For TP5216/17, it refers to the accuracy of the all "0's" to 000...001 transition. For TP5211/12/13/14, it refers to the accuracy of both the all "0's" to 000...001 and all "1's" to 111...110 transitions. See Digital Output Coding for an explanation of output transitions.
4. Zero error refers to the accuracies of the actual input voltages for the following output transitions: TP5210/13—all "0's" to 000...001. TP5216/17—all "1's" to 111...110. TP5211/12/13/14—100...000 to 011...111.
5. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from all "1's" to 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0001 to all "0's".
6. Conversion time is defined as the width of the converter's status (E.O.C.) pulse (see Timing Diagram). Teledyne Philbrick guarantees TP5210 Series converters will meet all specs with clock frequencies up to 1MHz. A 1MHz clock gives a status pulse that is 12μsec wide. The 13μsec spec reflects the fact that unless careful timing precautions are taken, it will usually take 13 clock periods to update digital output data. Units will typically maintain specified linearity and accuracy with clock frequencies to 1.7MHz (7μsec conversion time).
7. The clock may be asymmetrical with minimum positive or negative pulse widths.
8. In order to reset the converter, start convert must be brought low at least 25nsec prior to a low to high clock transition. See Timing Diagram.
9. Serial and parallel output data have the same coding. Serial data is in Non-Return to Zero (NRZ) format. See Output Coding and Timing Diagram.
10. One TTL load is defined as sinking 40μA with a logic "1" applied and sourcing 1.6mA with a logic "0" applied.

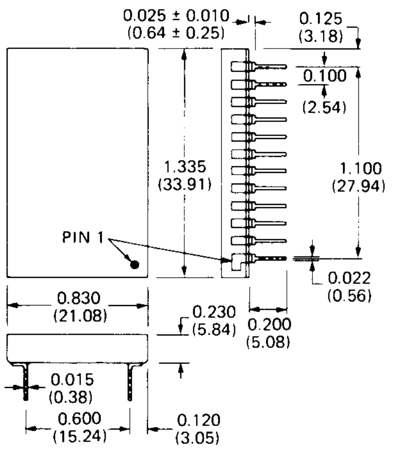
Functional Block Diagram



Note 1: Pin 10 is a N/C for TP5210 Series A/D's. Other 5210's may require a 2.2μF capacitor between this pin and + 15V. If this capacitor is already installed in your system, it will not affect the TP5210.

Note 2: TP5210/11/12/16 have an internal − 6.3V reference that is also brought out to this pin. TP5213/14/15/17 require an external − 10V reference applied to this pin.

Package Dimensions 24 Pin DIP



Dimensions in inches (millimeters)

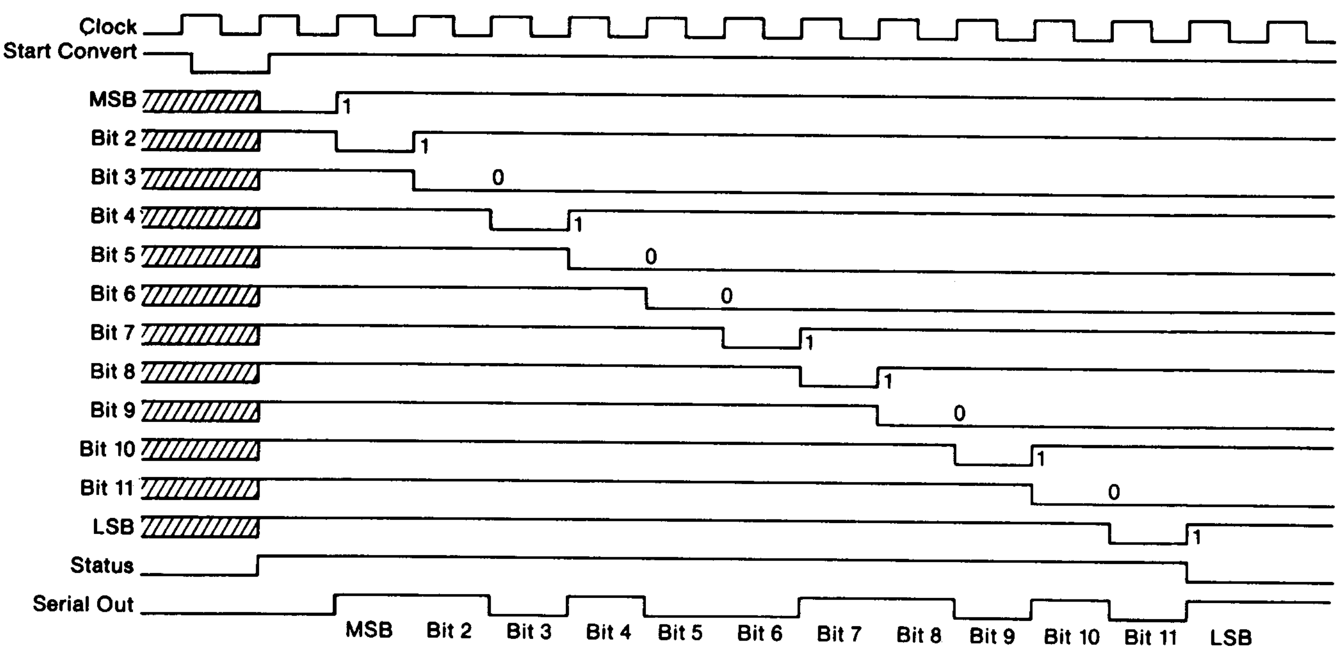
Pin Designations

Pin 1	Start Convert	Pin 24	Clock Input
Pin 2	+5V Supply	Pin 23	Ground
Pin 3	Serial Output	Pin 22	Status (E.O.C.)
Pin 4	Bit 6	Pin 21	Bit 7
Pin 5	Bit 5	Pin 20	Bit 8
Pin 6	Bit 4	Pin 19	Bit 9
Pin 7	Bit 3	Pin 18	Bit 10
Pin 8	Bit 2	Pin 17	Bit 11
Pin 9	Bit 1(MSB)	Pin 16	Bit 12 (LSB)
Pin 10	N/C	Pin 15	+15V Supply
Pin 11	Ground	Pin 14	Analog Input
Pin 12	Ref. Out (−6.3V) Ref. In (−10.0V)	Pin 13	−15V Supply

Applications Information

Timing Diagram

The converter is reset (MSB = "0", all other bits = "1", status = "1") by holding the start convert low during a low to high clock transition. The start convert must be low for a minimum of 25nsec prior to the clock transition. The delay between the resetting clock edge and status actually rising to a "1" is 120nsec maximim. Holding the start low will hold the converter in the reset state. Actual conversion will begin on the next rising clock edge (after the start has returned high) with the MSB being set to its final value. Subsequent bits will be set to their final values on subsequent rising clock edges. Status drops to a "0" as the LSB is set to its final value. Conversion time is defined as the width of the status pulse. Both serial and parallel data bits become valid on the same rising clock edges. Serial data is still valid on subsequent falling clock edges, and these edges can be used to clock serial data into receiving registers. Parallel output data will be valid 30nsec (maximum) after the status (E.O.C.) output has returned low. Parallel output data will remain valid and the status output will remain low until another conversion is initiated. The start convert may be brought low at any time during a conversion to reset and begin converting again. When the converter is initially "powered up", it may come on at any point in the conversion cycle.



Grounding and Bypassing

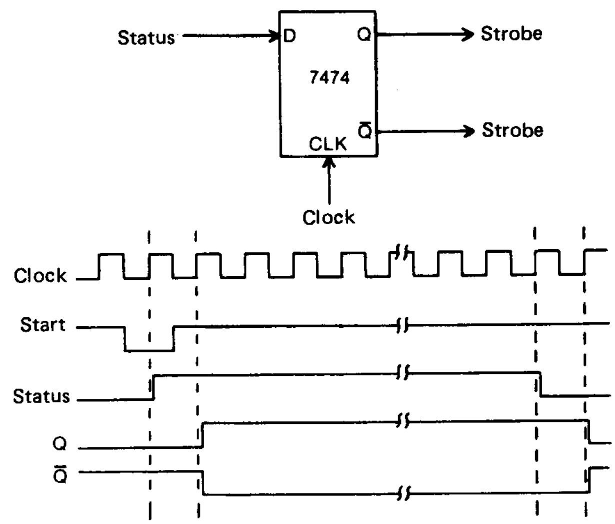
With proper grounding and bypassing, TP5210 Series A/D Converters will meet all their published performance specifications without the need for additional external components. The unit's two ground pins (pins 11 and 23) are not connected to each other internally. They should be tied together as close to the package as possible and both connected to system analog ground. It is preferable to have a large analog ground plane beneath the TP5210 and have pins 11 and 23 soldered directly to it. Potential differences between pins 11 and 23 and the ground of the analog signal source will result in TP5210 accuracy and linearity errors. If runs to pins 11 and 23 have to be made separately, an 0.01μF ceramic capacitor should be connected between pins 11 and 23 as close to the unit as possible, and conductor runs should be as wide as possible.

Power supply connections should be short and direct, and all supplies should be bypassed to the same ground the converter is tied to. Bypass capacitors should be located as close to the converter as possible and should consist of one large value capacitor (0.1μF tantalum or larger) in parallel with an 0.01μF ceramic capacitor.

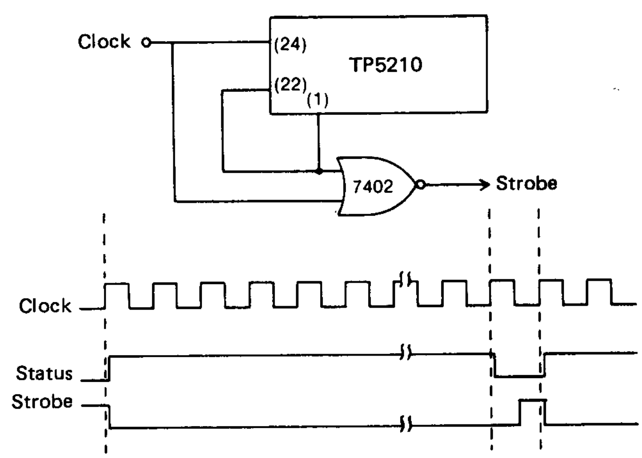
To minimize lead resistance and inductance, the A/D's signal source should be located as close to the A/D as possible and connected to the same ground (preferably "further away" from the system unipoint ground than the A/D). See the section entitled "Using the TP5210 with S/H Amplifiers" for tips on choosing signal sources for fast successive approximation type A/D converters. Unlike other 5210 type A/D's, the TP5210 does not require a 2.2μF capacitor from pin 10 to +15V to achieve specified performance. The presence of such a capacitor will not affect TP5210 performance, however, and a TP5210 Series A/D can be plugged into a socket originally designed for a 5210 or 5200 device from another manufacturer with no changes.

Status Output

The status or end of conversion (E.O.C.) output will be set to a logic "1" when the converter is reset; will remain high during conversion; and will drop to a logic "0" when conversion is complete. Due to propagation delays, the least significant bit (LSB) of a given conversion may not be valid until a maximum of 30nsec after status has returned low. Therefore, an adequate delay must be provided if status is to be used to strobe latches to hold output data. Simple gate delays can be employed or the status can be made the input of a D flip flop whose clock input is the same as the converter clock (see sketch). In this situation, the Q output will change one clock period after status changes.



If continuously converting, the status (E.O.C.) output can be NORed with the converter clock, as shown below, to produce a positive strobe pulse ½ period wide, ½ period after the status output has gone low. The rising edge of this pulse can be used to latch data after each conversion.

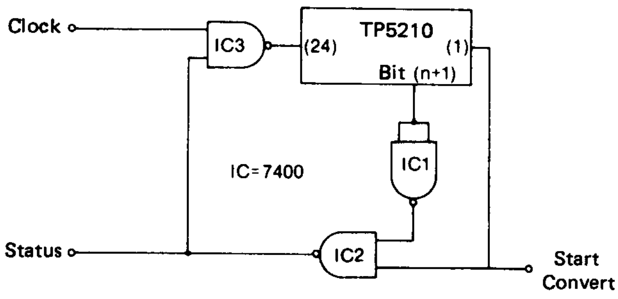


Continuous Converting

The TP5210 converters can be made to continuously convert by tying the status output (pin 22) to the start convert input (pin 1). In this configuration, status (start convert) will go low at the end of a conversion (see Timing Diagram) and the next rising clock edge will reset the converter bringing status (start convert) high again. The MSB will be set on the next rising clock edge. The result is that the status will go low for approximately one clock period following each conversion. Please read the section describing the status output. See below for continuous conversions while short cycling.

Short Cycling

For applications requiring less than 12 bits resolution, TP5210 Series A/D's can be truncated or short cycled to the desired number of bits with a proportionate decrease in conversion time. The following circuit may be used to truncate at n bits.

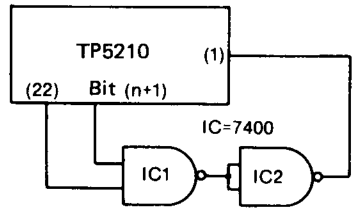


Short Cycling Single Conversion

Assuming a conversion is already in progress, bit (n + 1) will go low as bit n is being set (see Timing Diagram). Since the start convert signal is high at this time, status (the output of IC2) will go low gating off the clock at IC3 ending the conversion. To begin a new conversion, start convert is brought low driving status high and gating on the clock. The first rising clock edge the converter sees with start convert low will reset the converter bringing bit (n + 1) high again. Now status will remain high as start convert is brought back high allowing the conversion to continue. Therefore, in this configuration, status and start convert function normally, i.e., the same as status and start convert for a converter not being short cycled.

Short Cycling and Continuous Converting

A previous section described how continuous converting for 12 bits could be accomplished by simply tying the status output back to the start convert input. To continuosly convert at n bits, one simply has to tie the bit (n + 1) output back to the start convert input. The bit (n + 1) output acts like a status when one short cycles at n bits. It goes high when the converter is reset, remains a "1" during the conversion, and drops to a "0" as bit n is being set. Since it is possible for the converter to come on in any state at power-on, a lock-up condition may occur if bit (n + 1) comes on as a "1" and the conversion process comes on at bit (n + 2). This situation can be avoided by making the start convert input the AND function of bit (n + 1) and the status output.

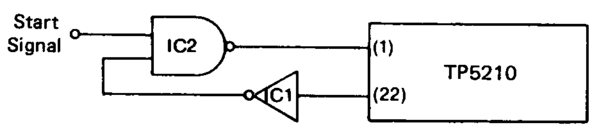


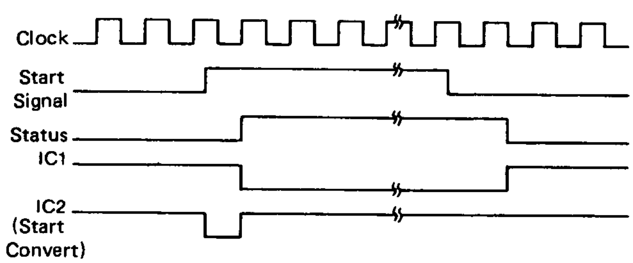
Short Cycling Continuous Converting

If one is already using the circuit described in the section labeled Short Cycling, one can short cycle and continuously convert by making the start convert input the AND function of status (IC2) and status (pin 7) outputs.

Triggering with a Positive Edge

If it is inconvenient to generate a negative going start convert pulse of the proper width, TP5210 Series A/D's can be made to start converting on a positive going edge by employing the circuit shown below. Assuming the previous conversion is done and the start signal is low, the status output will be low, the output of IC1 will be high, and the output of IC2 will be high. A rising edge as a start signal will drive the output of IC2 low. The converter will reset on the next rising clock edge. Resetting brings the status high; IC1 goes low; the start signal is still high so the output of IC2 goes high allowing the conversion to continue immediately. The start signal has only to be brought back down before the conversion is completed.



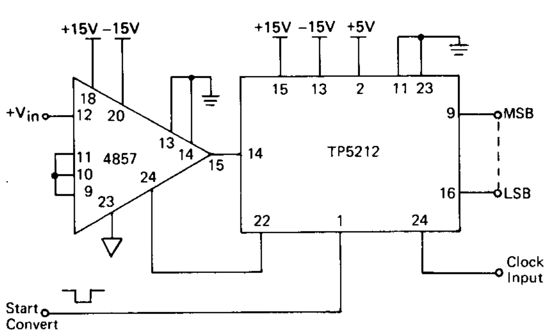


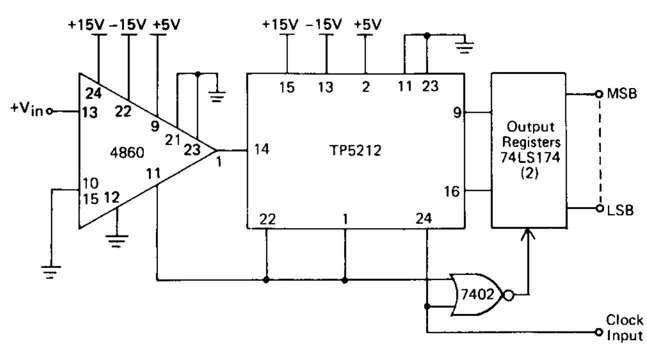
Using a Sample-Hold Amplifier with TP5210 Series A/D's

Sample-hold (S/H) and track-hold (T/H) amplifiers can be used with the TP5210 Series A/D's in a number of different configurations. There are three major considerations when using S/H's with SA type A/D converters. First, the S/H's output impedance should be very low compared to the A/D's input impedance (normally 1 to 10kΩ) at frequencies up to 5 times the A/D's clock frequency. Second, the S/H output should be able to fully recover from current transients in less than 1 A/D clock period. These requirements are due to the fact that as the A/D's internal DAC settles just prior to each output bit being determined, the S/H output may be required to sink and source high frequency current components, and changes in its output voltage will cause system accuracy errors. The third consideration is the S/H spec called sample-to-hold settling time (transient settling time). As you switch a S/H from the sample to the hold mode, an output transient usually occurs, and one must be sure this transient has settled before the A/D makes its final decision on the MSB.

If the TP5210 is used in a single conversion mode with an external start pulse, the S/H can be driven directly (or inverted) from the A/D's status output. The status output changes state when the converter receives a convert command, and this change can drive the S/H from the track to the hold mode. The change in state of the status output at the end of conversion can put the S/H back in to the track mode. The diagram below illustrates a TP5210 mated with a Teledyne Philbrick 4857 (1μsec max acquistion time, 500nsec max sample-to-hold settling time) in this manner. Since the 4857's MSB output is not set to its final value until one clock period (approximately 1μsec) after a conversion begins, the 4857's sample-to-hold transient will be completely settled, and no extra precautions are necessary.

If the TP5210 is used in a continuous convert mode, its status output goes low for approximately 1 clock period following each conversion. If this is enough time for a given S/H to acquire a new signal to 0.01%, the S/H can again be controlled by the A/D's status output. The diagram below shows such a scheme using a TP5212 and a Teledyne Philbrick 4860 (200nsec max acquisition time, 100nsec max sample-to-hold settling time). At the end of each conversion, the status 1→0 change will put the 4860 back into the signal acquisition (tracking) mode. One half clock period (500nsec) later, the output of the NOR gate goes high and this rising edge can be used to strobe digital output data into a receiving register. 500nsec after that event, the converter begins another conversion, and the status 0→1 change drives the 4860 in the hold mode. The output of the NOR gate can be used as a data valid sense point. When it is a "0", data in the receiving register is valid. When it is a "1", data is changing. See the 4857, 4860, 4189 and the TPADC85/87 data sheets for additional tips on mating S/H's and A/D's.

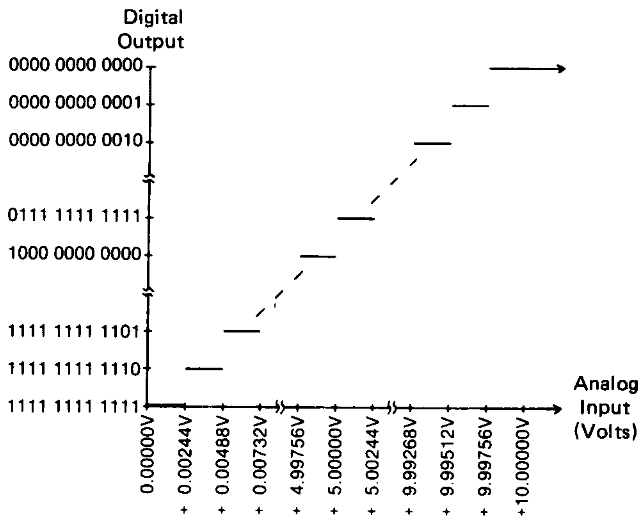




Digital Output Coding

Because of the inherent uncertainty associated with quantizing an analog signal, the only points along an ADC's input/output transfer function that accurately describe the function are the transition voltages—the analog input voltages at which the digital output changes from one code to the next. The sketch to the right shows the ideal input/output transfer function for the TP5216 and TP5217 (0 to + 10V input ranges). The table below lists five of the most important transition voltages for each of the TP5210 Series' four input ranges. 1111 1111 111* indicates a unit's digital output ideally changes from 1111 1111 1111 to 1111 1111 1110 (or vice versa) at the input voltage listed for the input range selected. **** **** **** signifies the center of an input/output range where the digital output changes from 1000 0000 0000 to 0111 1111 1111. CSB = Complementary Straight Binary. COB = Complementary Offset Binary.

Ideal Transfer Function 0 to +10V Range



Analog Input (DC Volts)					Digital Output Transition
Part Number	**TP5210/5213**	**TP5211/5214**	**TP5212/5215**	**TP5216/5217**	
Input Range	0 to − 10V	± 5V	± 10V	0 to + 10V	
Logic Coding	CSB	COB	COB	CSB	
LSB Size	2.44mV	2.44mV	4.88mV	2.44mV	MSB LSB
Transition Voltage	0.0000V	+ 5.0000V	+ 10.0000V	+ 10.0000V	0000 0000 0000
	− 0.0024V	+ 4.9976V	+ 9.9951V	+ 9.9976V	0000 0000 000*
	− 4.9976V	+ 0.0024V	+ 0.0049V	+ 5.0024V	0111 1111 111*
	− 5.0000V	0.0000V	0.0000V	+ 5.0000V	**** **** ****
	− 5.0024V	− 0.0024V	− 0.0049V	+ 4.9976V	1000 0000 000*
	− 9.9976V	− 4.9976V	− 9.9951V	+ 0.0024V	1111 1111 111*
	− 10.0000V	− 5.0000V	− 10.0000V	0.0000V	1111 1111 1111

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