MP8790

2 MSPS, CMOS 12-Bit Analog-to-Digital Converter with Parallel and Serial Logic Interface Port

EXAR

FEATURES

- **12-Bit ADC with DNL = ±1 LSB, INL = ±2 LSB**
- **SNR > 60 dB**
- **Sampling Frequency ≤ 2 MHz**
- **Internal Track and Hold: Input –3 dB Frequency = 10 MHz**
- **Single 5 V Supply**
- **Rail-to-Rail Input Range**
- **V_{REF} Range: 1.5 V to V_{DD}**
- **CMOS Low Power: 200 mW (typ)**
- **15 Equally Spaced Ladder Taps for Non-Linear Transfer Function**
- **Three-State Outputs**
- **Binary and Two's Complement Digital Output Mode**
- **Serial and Parallel Port**
- **Overflow and Underflow Outputs**
- **Precision Aperture Output**
- **Latch-Up Free**
- **28 Pin Package: MP8791 & MP8792**

APPLICATIONS

- **Instrumentation**
- **DAS**
- **Radar**
- **Medical Imaging**
- **Ultrasound**
- **Broadcast and Studio Video**
- **Magnetic Resonance Signal Acquisition**
- **Digital Oscilloscopes**
- **Spectrum Analysis**
- **Digital Radio**

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GENERAL DESCRIPTION

The MP8790 is a 12-bit 2-step high speed Analog-to-Digital Converter with DNL = ±1 LSB and INL = ±2 LSB. The MP8790 contains an internal track and hold which allows for analog input signals as fast as 2 MHz and can convert signals at a 2 MSPS rate.

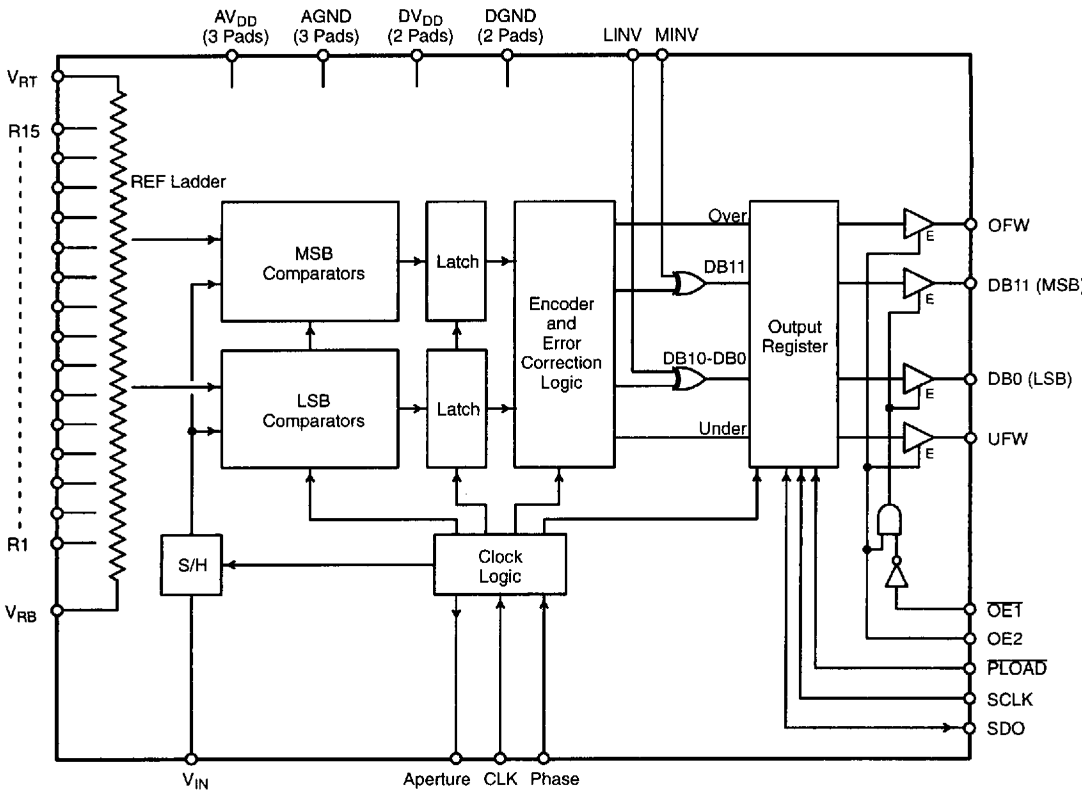
The MP8790 operates with a single supply ranging from +3 V to +5 V while consuming less than 200 mW of power (typical). Separate pins for reference ladder terminals and power supplies allow flexibility for various A_{IN}, ΔV_{REF}, and power supply ranges.

Data is presented at the parallel output port every clock cycle after a 2.5 cycle pipeline delay. The digital output port is also equipped with a 3-state function, as well as a serial data port. LINV and MINV enable binary and 2's complement data formatting. The 15 ladder tap pins (R1-R15) can accommodate transfer function adjustment, linearity, and speed enhancement.

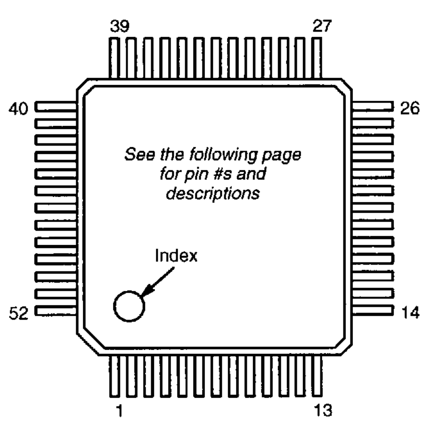
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PQFP	–40 to +85°C	MP8790AE	±1	2 1/2

SIMPLIFIED BLOCK DIAGRAM



PIN CONFIGURATIONS



52 Pin PQFP
QN52 (10 mm X 10 mm)
Contact Factory for Package Drawing

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	R10	Ref. Resistor Ladder Tap (10/16 V_{REF})
2	R12	Ref. Resistor Ladder Tap (12/16 V_{REF})
3	R11	Ref. Resistor Ladder Tap (11/16 V_{REF})
4	R3	Ref. Resistor Ladder Tap (3/16 V_{REF})
5	R13	Ref. Resistor Ladder Tap (13/16 V_{REF})
6	R4	Ref. Resistor Ladder Tap (4/16 V_{REF})
7	R1	Ref. Resistor Ladder Tap (1/16 V_{REF})
8	R15	Ref. Resistor Ladder Tap (15/16 V_{REF})
9	R2	Ref. Resistor Ladder Tap (2/16 V_{REF})
10	R6	Ref. Resistor Ladder Tap (6/16 V_{REF})
11	V_{RB}	Negative Reference
12	V_{RT}	Positive Reference
13	R14	Ref. Resistor Ladder Tap (14/16 V_{REF})
14	AV_{DD}	Analog Positive Supply
15	AV_{DD}	Analog Positive Supply
16	AGND	Analog Ground
17	AGND	Analog Ground
18	MINV	Invert MSB (Active High)
19	LINV	Invert LSB (Active High)
20	UFW	Underflow Bit
21	DB0	Data Output Bit 0 (LSB)
22	DB1	Data Output Bit 1
23	DB2	Data Output Bit 2
24	DB3	Data Output Bit 3
25	DB4	Data Output Bit 4
26	DB5	Data Output Bit 5

PIN NO.	NAME	DESCRIPTION
27	SDO	Serial Data Out
28	DV_{DD}	Digital Positive Supply
29	DV_{DD}	Digital Positive Supply
30	DGND	Digital Ground
31	DGND	Digital Ground
32	PHASE	Phase Clock Polarity Control
33	SCK	Serial CLK
34	Aperture	Aperture Delay Sync
35	OFW	Overflow
36	OE2	Output Enable (Active High)
37	$\overline{OE}$	Output Enable (Active Low)
38	CLK	Clock
39	$\overline{PLOAD}$	Serial Shift Register Data Load
40	DB6	Data Output Bit 6
41	DB7	Data Output Bit 7
42	DB8	Data Output Bit 8
43	DB9	Data Output Bit 9
44	DB10	Data Output Bit 10
45	DB11	Data Output Bit 11
46	R7	Ref. Resistor Ladder Tap (7/16 V_{REF})
47	R9	Ref. Resistor Ladder Tap (9/16 V_{REF})
48	R5	Ref. Resistor Ladder Tap (5/16 V_{REF})
49	AGND	Analog Ground
50	V_{IN}	Analog Input
51	AV_{DD}	Analog Positive Supply
52	R8	Ref. Resistor Ladder Tap (8/16 V_{REF})

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 5$ V, FS = 2 MHz (50% Duty Cycle), $V_{REF(+)} = 5.0$ V, $V_{REF(-)}$ = AGND, TA = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution			12		Bits	
Sampling Rate	FS		2		MHz	
ACCURACY[1]						
Differential Non-Linearity	DNL			±1	LSB	
Integral Non-Linearity	INL			±3	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+20		LSB	
Full Scale Error	EFS		–20		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	$V_{REF(+)}$	1.5		AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			V	
Differential Ref. Voltage[3]	V_{REF}	1.5		AV_{DD}	V	
Ladder Resistance	R_L		550		Ω	
ANALOG INPUT[2]						
Input Bandwidth (–3 dB)[4]	BW		10		MHz	
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V p-p	
Input Capacitance Sample[5]	C_{IN}		50		pF	
Input Capacitance Convert[5]			8		pF	
Aperture Delay from Clock	t_{AP}		20		ns	
Aperture Delay from Aperture Signal	t_{AP}		0		ns	Aperture pin load 5 pF. Measured at 50% point.
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}		2.4		V	
Logical "0" Voltage	V_{IL}		0.8		V	
Leakage Currents [6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK, $\overline{OE1}$, OE2, MINV, LINV			10		µA	
Input Capacitance			5		pF	
Clock Timing						
Clock Period	t_S	200	500		ns	Functional
Rise & Fall Time[7]	t_R, t_F		15		ns	Functional
"High" Time	t_{PWH}	100	220		ns	Functional
"Low" Time	t_{PWL}	100	220		ns	
Duty Cycle			50		%	
Serial Register Timing						
Shift Clock Period	t_{SC}		50		ns	
Shift Clock to Data Delay	t_{SD}		20		ns	
Minimum Pulse Width $\overline{PLOAD}$	t_S		50		ns	
Clock↑ to $\overline{PLOAD}$↓ For Valid D11	t_{CP}		0		ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}		DV_{DD}-0.5		V	I_{LOAD} = 4 mA
Logical "1" Source Current	I_{OH}		4		mA	$V_{OH} = DV_{DD}$-0.5
Logical "0" Voltage	V_{OL}		0.5		V	I_{LOAD} = 4 mA
Logical "0" Sink Current	I_{OL}		4		mA	V_{OL} = 0.5 V
Tristate Leakage	I_{OZ}		1		µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay	t_{DL}		30		ns	
Data Enable Delay	t_{DEN}		20		ns	
Data Tristate Delay	t_{DHZ}		20		ns	
POWER SUPPLIES[8]						
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}		5		V	
Current (AV_{DD} + DV_{DD})	I_{DD}		40	45	mA	
AC PARAMETERS[2]						
Signal Noise Ratio (N+D)	SINAD		66		dB	

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/4096) is the DNL error. The INL error is the maximum distance (in LSB's) from the best fit line to any transition voltage. Accuracy is a function of the sampling rate (FS).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 –3 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.

5 Switched capacitor analog input requires driver with low output resistance.

6 All inputs have diodes to DV_{DD} and DGND. Input(s) $\overline{OE}$ and MINV have internal pull down(s). Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.

7 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.

8 AGND & DGND pins are connected through the silicon substrate.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND .... 7 V
$V_{REF(+)}$ & $V_{REF(-)}$ .... V_{DD} +0.5 to GND –0.5 V
V_{IN} .... V_{DD} +0.5 to GND –0.5 V
All Inputs .... V_{DD} +0.5 to GND –0.5 V
All Outputs .... V_{DD} +0.5 to GND –0.5 V

Storage Temperature .... –65 to +150°C
Lead Temperature (Soldering 10 seconds) .... +300°C
Package Power Dissipation Rating @ 75°C
PQFP 900mW
Derates above 75°C .... 12mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

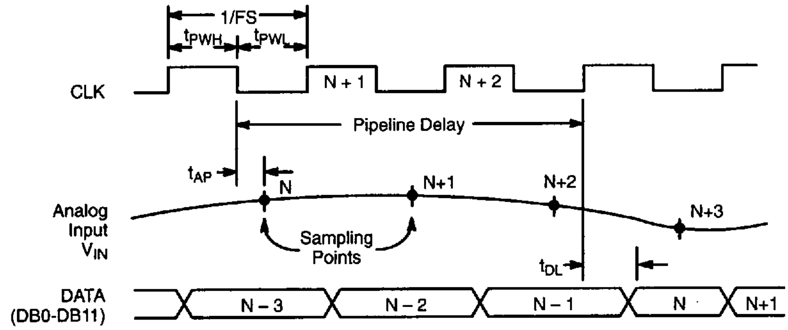


Figure 1. MP8790 Timing Diagram

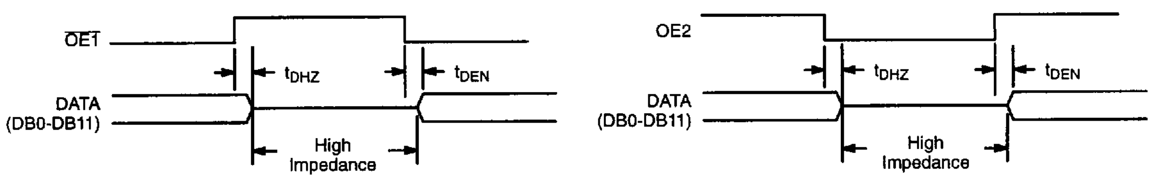
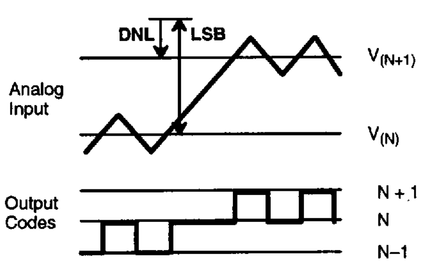


Figure 2. 3-State Timing Diagram



Code Width (N) = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{RT} - V_{RB}$] / 1024

$DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - LSB$

Figure 3. DNL Measurement

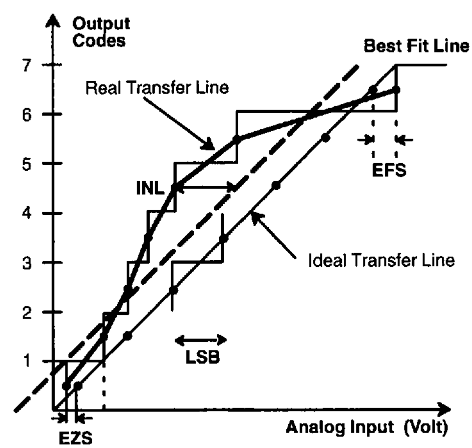


Figure 4. INL Error Calculation

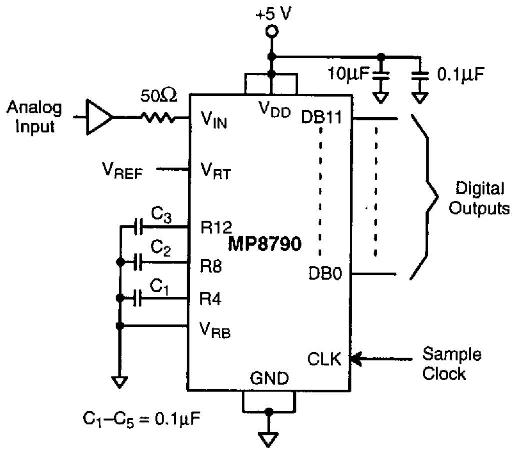


Figure 5. Typical Circuit Connections

$\overline{OE1}$	OE2	DBO-DB9	OFW & UFW
0	1	enabled	enabled
1	1	3-state	enabled
X	0	3-state	3-state

PHASE Clock Polarity Control (input)

This signal controls the phase relationship between the signal applied at the CLK pin and the internal clock signals. When PHASE is high, V_{IN} is sampled at the high to low CLK transition and the digital data changes after a low to high CLK transition. When PHASE is low, V_{IN} is sampled at the low to high CLK transition and the digital data changes after a high to low CLK transition. See timing diagram *Figure 6.* PHASE has an internal pull up device.

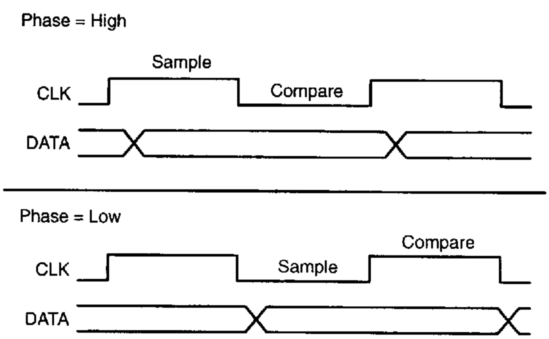


Figure 6. Clock Phase Relationship

OFW & UFW: Overflow & Underflow (Outputs)

These signals indicate when the Analog Input (V_{IN}) goes outside the V_{RB} to V_{RT} range. Both pins are normally at low logic levels. When $V_{IN} > V_{RT}$, OFW will go high and the data bits (DB0 – DB11) will show full scale (i.e. all 1's if MINV & LINV are low). When $V_{IN} < V_{RB}$, UFW will go high and the data bits will show negative full scale (i.e. all 0's if MINV & LINV are low).

$\overline{OE1}$ & OE2: Output Enable (inputs)

These signals control the 3-state drivers on the digital outputs DB0 – DB11, OFW and UFW. During normal operation, $\overline{OE1}$ should be held low and OE2 should be held high so that all outputs are enabled (NOTE: internal resistors will pull $\overline{OE1}$ and OE2 to these levels if they are not connected). When $\overline{OE1}$ is driven high, DB0 – DB11 goes into high impedances mode. When OE2 is driven low, DB0 – DB11, OFW and UFW all go into high impedance mode. These controls operate asynchronous to the clock and they only control the output drivers. The internal output register will get updated if the clock is running while the outputs are in 3-state mode. If possible, $\overline{OE1}$ should be in 3-state during Clock = 1 (PHASE = 1) to reduce digital noise coupling into A_{IN} during the sample time. Aperture provides a convenient control for this purpose since it guarantees that the A_{IN} sample period is complete when the outputs are enabled.

SDO: Serial Data output

After the internal shift register is updated using the $\overline{PLOAD}$ signal, the SDO pin outputs the A/D result starting with the MSB (which appears just after the $\overline{PLOAD}$ strobe). Each bit is output on the rising edge of SCLK.

SCLK: Serial Data Port Clock

The SCLK controls the output of the serial port through SDO. SDO is updated on every rising edge of SCLK. The $\overline{PLOAD}$ signal will override the SCLK signal.

$\overline{PLOAD}$:

Serial data port shift register load: When $\overline{PLOAD}$ is low (i.e. level triggered not edge triggered) the current parallel data will be loaded into the shift register. $\overline{PLOAD}$ overrides SCLK. When $\overline{PLOAD}$ is high, the data can be shifted out through the SDO pin with SCLK.

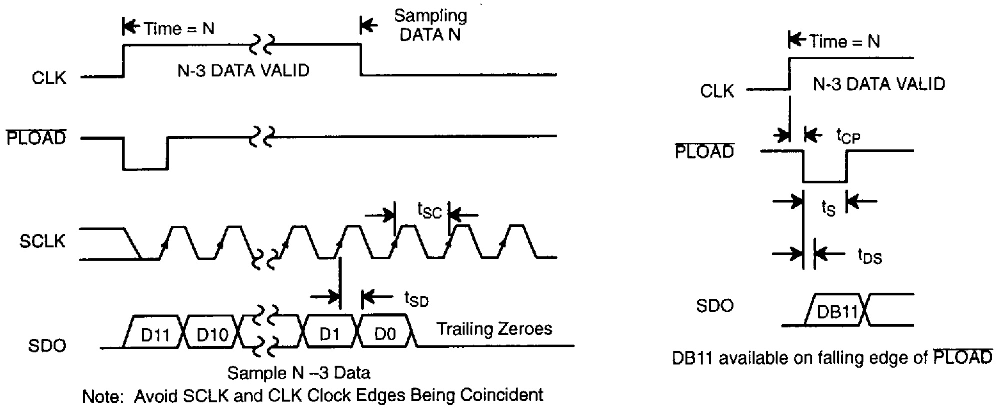


Figure 7. Serial Port Timing Chart PHASE = 1

APERTURE: Aperture Delay Sync (output)

This signal is high when the internal sample/hold function is sampling V_{IN}, and goes low when it is in the hold mode (when the ADC is comparing the stored input value to the reference ladder). The value of V_{IN} at the high to low transition of APERTURE is the value that will be digitized. A system can monitor this signal and adjust the CLK to accurately synchronize the sampling point to an external event. The Aperture pin may also be used to control the $\overline{OE1}$ (outputs between 3-state and active mode). This will reduce the errors introduced by digital output coupling during the A_{IN} sample time.

	MINV LINV	0 0	0 1	1 0	1 1
V_{IN}	V_{RT}	111 . . . 11 111 . . . 10	100 . . . 00 100 . . . 01	011 . . . 11 011 . . . 10	000 . . . 00 000 . . . 01
	⋮	⋮	⋮	⋮	⋮
	mid scale	100 . . . 01 100 . . . 00	111 . . . 10 111 . . . 11	000 . . . 01 000 . . . 00	011 . . . 10 011 . . . 11
		011 . . . 11	000 . . . 00	111 . . . 11	100 . . . 00
	⋮	⋮	⋮	⋮	⋮
	V_{RB}	000 . . . 01 000 . . . 00	011 . . . 10 011 . . . 11	100 . . . 01 100 . . . 00	111 . . . 10 111 . . . 11
		binary	inverted 2's complement	2's complement	inverted binary

Table 1. Output Data Format Truth Table

MINV & LINV: Digital Output Format (inputs)

These signals control the format of the digital output data bits DB0 – DB11. Normally both pins are held low so the data is in straight binary format (all 0's when $V_{IN}=V_{RB}$; all 1's when $V_{IN}=V_{RT}$). If MINV is pulled high, then the MSB (DB11) will be inverted. If LINV is pulled high, then the LSBs (DB0 – DB10) will be inverted. The OFW and UFW bits are not affected by these signals.

MINV & LINV are meant to be static digital signals. If they are to change during operation, they should only change when the CLK is low (assuming PHASE is high, if PHASE is low then these signals should only change when CLK is high). Changing MINV and/or LINV on the wrong phase of the CLK will not hurt anything, but the effects on the digital outputs will not be seen until the output latch of the output register is enabled. MINV and LINV have internal pull down devices. Please see the simplified logic circuit *Figure 8.*

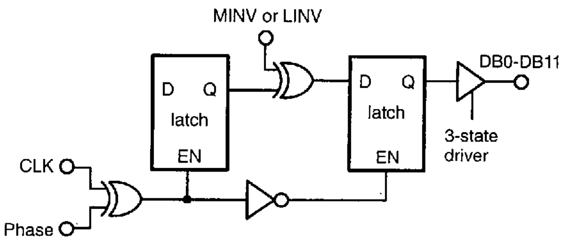


Figure 8. MINV, LINV Simplified Logic Circuit

V_{IN} Analog Input

This part has a switched capacitor type input circuit. This means that the input impedance changes with the phase of the input clock. V_{IN} is sampled at the high to low clock transition. The diagram *Figure 9.* shows an equivalent input circuit.

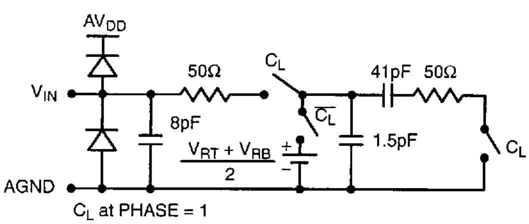


Figure 9. Equivalent Input Circuit

R1 thru R15: Reference Ladder Taps

These taps connect to every sixteenth point along the reference ladder; R1 is 1/16th up from V_{RB}, R7 is 15/16ths up from V_{RB} (or 1/16th down from V_{RT}). Normally these pins should have 0.1 microfarad capacitors to V_{SS}, this helps reduce the INL errors by stabilizing the reference ladder voltages. These taps can also be used to alter the transfer curve of the ADC. A 16 segment, piecewise linear, custom transfer curve can be designed by connecting voltage sources to these pins. The internal interconnect resistance from the pin to the ladder is less than 3Ω for the even numbered taps, (i.e. R2,R4,R6, etc.) and is approximately 10Ω for the odd numbered taps.

Alternating the transfer curve may be desirable to make the probability of codes for a certain range of V_{IN} be enhanced or minimized.

Sometimes this is referred to as probability density function shaping, or histogram shaping.

For Log shapes, the MP8790 is ideal since it provides 16 segments.

0.8 V maximum per tap is recommended for applications above 85°C. Up to 1.6 V is allowed for applications under 85°C.

APPLICATION NOTES

V_{IN} signals should not exceed AV_{DD} +0.5V or go below AGND –0.5V. All pins have internal protection diodes that will protect them from short transients (<100µs) outside the supply range.

AGND & DGND pins are connected internally through the P– substrate. DC voltage differences between AGND and DGND pins will cause undesirable internal substrate currents.

The power supply (V_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to AGND, placed as close to the chip as possible.

The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

At least three of the reference tap pins (R4, R8, R12) should be decoupled with 0.1µF to 1µF capacitors. This will help stabilize the internal reference voltages thus reducing any INL errors.

The reference tap pins (R1-R16) can be used to create piecewise-linear transfer functions. By forcing custom voltages on these pins, a 16 segment transfer function can be made. See *Figure 10. and Figure 11.*

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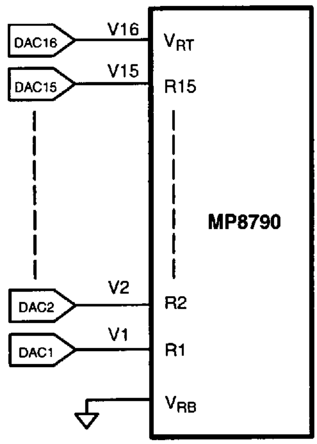
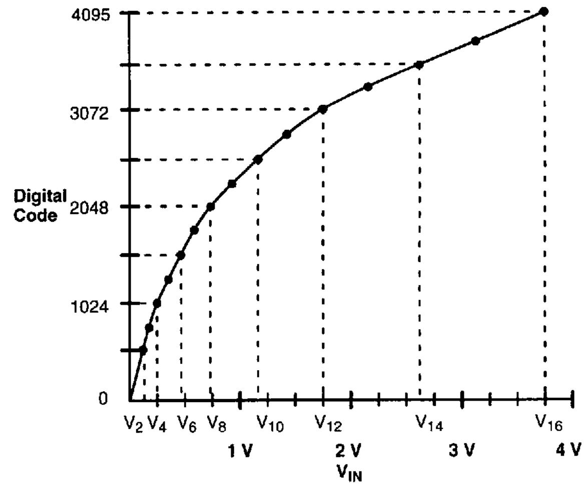


DAC MP7642

Only the Ladder detail shown.

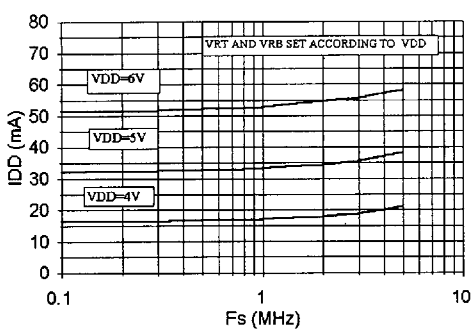
Figure 10. A/D with Programmed Ladder Control for Creating a Piecewise Linear Transfer Function



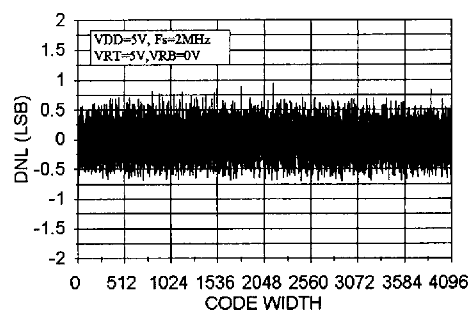
Even Voltages Shown

Figure 11. Example of a Piecewise Linear Transfer Function

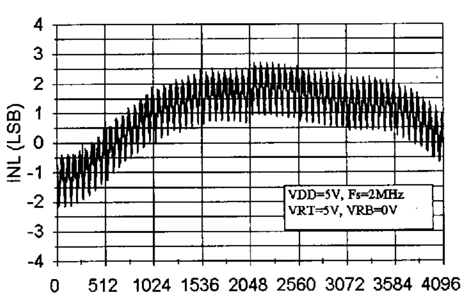
PERFORMANCE CHARACTERISTICS



Graph 1. I_{DD} vs. F_S



Graph 2. DNL Error Plot



Graph 3. INL Error Plot