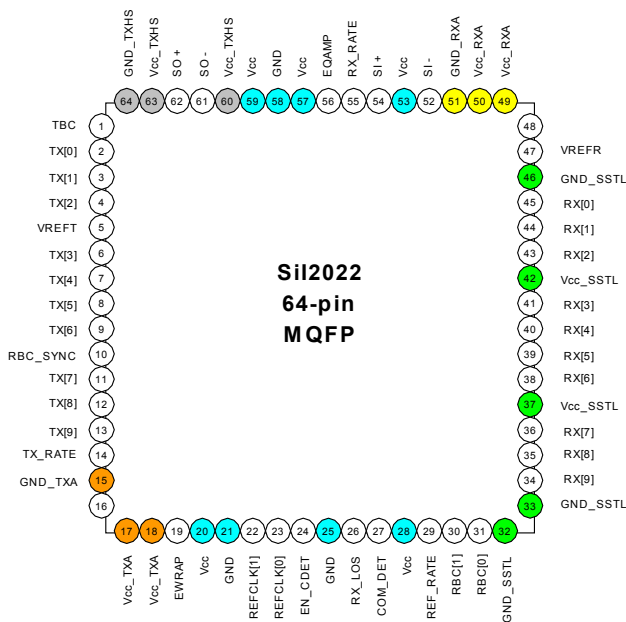


General Description

Silicon Image’s Sil2022 is a serializer/deserializer (SerDes) capable of transmitting and receiving data at 1.0625 and 2.125 gigabits-per-second (Gbps) targeting Fibre Channel applications. Designed for power, performance and price, the Sil2022 SerDes makes use of a robust, low-power, low-cost, low-jitter, CMOS design that comes in compact 64-pin, 14 mm MQFP package. The Sil2022 supports selectable transmit and receive data rates for automatic speed negotiation and a narrow 10-bit SSTL_2 compatible interface for parallel data input/output. The innovative PLL design enables high data reliability and ease-of-design while eliminating the need for external PLL capacitors.

The Sil2022 leverages much of the circuit innovation at the physical layer of Silicon Image’s proprietary reduced overhead Multi-layer Serial Link (MSL™) architecture, which was pioneered and proven with our market-leading PanelLink® products. Silicon Image has shipped over 25 million units of PanelLink products for host systems and displays in the PC and the CE markets, notable for their noisy operating conditions. The MSL technology is a multi-layered approach to providing cost-effective, multi-gigabit semiconductor solutions on a single chip for high-bandwidth applications.

Figure 1. Sil2022 Pin Diagram



Features

General

- Fibre Channel-compliant
- Multi-rate: 1.0625 Gbps and 2.125 Gbps

Low Power

- Single 3.3V supply for core circuits and high-speed I/O
- Power dissipation at 2.125 Gbps: 446 mW (typical)

Cost Effective

- Standard CMOS technology
- Compact 64-pin, 14 x 14mm MQFP package

Narrow parallel I/O Interface

- 10-bit interface with DDR for 2.125 Gbps mode
- SSTL_2 and High-Speed Parallel Interface (HSPI)-compliant
- Separate transmit byte clock (TBC) for latching parallel input data

Highly Reliable Serial Interface

- Separately selectable Tx and Rx data rates
- Low-jitter PLL : 3.5 ps (random jitter), 32 ps (deterministic jitter)
- Pre-emphasis control
- On-chip termination resistor

Proven Technology

- MSL™-based technology proven with PanelLink® ICs for the PC and the CE markets (2-5 Gbps, over 25M units shipped)
- Robust design for “noisy” environments

Functional Block Diagram

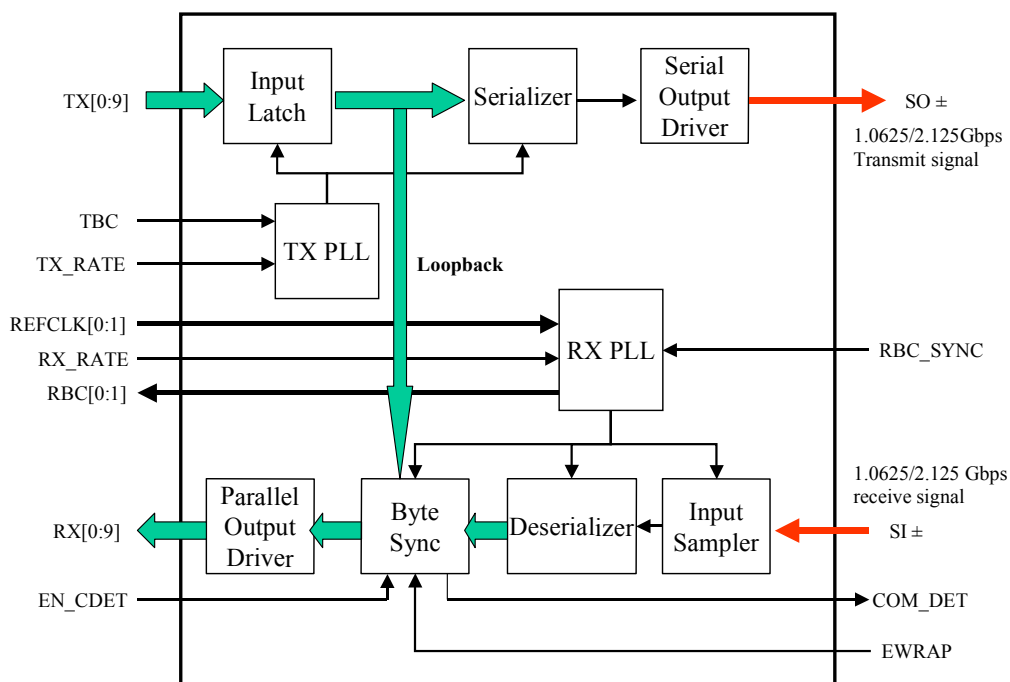


Figure 2. Functional Block Diagram

SiI2022 Block Diagram

The SiI2022 (Figure 2) is designed to transmit and receive 10-bit wide parallel data over high-speed serial communication lines. The parallel data applied to the transmitter is expected to be encoded per the 8B/10B encoding scheme with special reserved characters for link management purposes. The SiI2022 incorporates the following:

- SSTL_2 Parallel I/O
- High Speed Phase Locked Loops
- Parallel to Serial Converter
- High Speed Serial Clock and Data Recovery Circuitry
- Comma Character Recognition per Fibre Channel Specifications
- Byte Alignment Circuitry
- Serial to Parallel Converter

INPUT LATCH

The transmitter accepts 10-bit wide single ended SSTL_2 parallel data at inputs TX[0:9]. The SSTL_2 TBC clock provided by the sender of the transmit data is used as the transmit byte clock. The TX[0:9] and TBC signals must be properly aligned as shown in Figure 3. If TX_RATE = 1, TX[0:9] data are latched between both edges of TBC. If TX_RATE = 0, TX[0:9] data are latched on the falling edge of TBC. The TX[0:9] and TBC inputs are unterminated SSTL_2 inputs.

TX PLL/CLOCK GENERATOR

The Transmitter Phase Locked Loop and Clock Generator block is responsible for generating all internal clocks needed by the transmitter section to perform its functions. These clocks are based on the supplied transmit byte clock (TBC). Incoming data must be synchronous with TBC.

SERIALIZER

The SERIALIZER accepts 10-bit wide parallel data from the INPUT LATCH. Using internally generated high-speed clocks, this parallel data is multiplexed into a 2.125 Gbps serial data stream. The data bits are transmitted sequentially from TX[0] to TX[9]. The leftmost bit of K28.5+ is on TX[0].

SERIAL OUTPUT DRIVER

The SERIAL OUTPUT DRIVER block drives the serial data to the serial output line. In normal operation, the serialized TX[0:9] data is placed at SO±. In parallel loopback (EWRAP=1) mode, the SO± pins are held static at logic 1. In addition, the SERIAL OUTPUT DRIVER block allows the user to control the amount of pre-emphasis used on the SO± pins. If pre-emphasis is used, 0 to 1 and 1 to 0 transitions on SO± have greater amplitude than 0 to 0 and 1 to 1 transitions. This increased amplitude is used to offset the effects of skin loss and dispersion on long PCB transmission lines. Pre-emphasis is controlled by the EQAMP pin.

RX PLL/CLOCK RECOVERY

The Receiver Phase Locked Loop and Clock Recovery block is responsible for frequency and phase locking onto the incoming serial data stream and recovering the bit and byte clocks. An automatic locking feature allows the Rx PLL to lock onto the input data stream without external PLL training controls. It does this by continually frequency locking onto the 106.25 MHz reference clock, and then phase locking onto the selected input data stream. An internal circuitry monitors the frequency of RX PLL and invokes the phase detection as the frequency is locked.

INPUT SAMPLER

The INPUT SAMPLER is responsible for converting the serial input signal into a retimed bit stream. To accomplish this, it uses the high-speed serial clock generated from the RX PLL/CLOCK RECOVERY block. This serial bit stream is sent to the DESERIALIZER block.

DESERIALIZER

The DESERIALIZER block is responsible for converting the serial data from INPUT SAMPLER to parallel data.

BYTE SYNC

The BYTE SYNC block is responsible for recognizing the first seven bits of the K28.5+ positive disparity comma character (0011111xxx). When recognized, the BYTE SYNC block works with the RX PLL/CLOCK RECOVERY block to select the proper parallel data edge out of the bit stream so that the next comma character starts at RX[0]. When a comma character is detected and realignment of the receive byte clock RBC[0:1] is necessary, these clocks are stretched (never slivered) to the next correct alignment position. RBC[0:1] will be aligned by the start of the next ordered set (four-byte group) after K28.5+ is detected. The start of the next ordered set will be aligned with the rising edge of RBC[1], independent of the RX_RATE pin setting. Per the Fibre Channel encoding scheme, comma characters must not be transmitted in consecutive bytes so that the receive byte clocks may maintain their proper recovered frequencies.

PARALLEL OUTPUT DRIVER

The PARALLEL OUTPUT DRIVERS present the 10-bit parallel recovered data (RX[0:9]) properly aligned to the receive byte clock (RBC[0:1]) as shown in Figures 5. These output drivers provide single ended SSTL_2 compatible signals.

Electrical Specifications

Absolute Maximum Conditions

Symbol	Description	Min	Typ	Max	Units
V_{CC}	Supply Voltage 3.3V	-0.5		4.0	V
V_I	Input Voltage	-0.3		$V_{CC} + 0.3$	V
T_J	Junction Temperature (with power applied)			125	°C
T_{STG}	Storage Temperature	-65		150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)		33		°C/W

Notes: Permanent device damage may occur if absolute maximum conditions are exceeded.

Functional operation should be restricted to the conditions described under Normal Operating Conditions below.

Normal Operating Conditions

Symbol	Description	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3.15	3.3	3.45	V
T_A	Ambient Temperature (with power applied)	0	25	70	°C

DC Digital I/O Specifications

Under normal operating conditions unless otherwise specified.

$V_{DDQ} = 2.30V$ to $2.70V$. V_{DDQ} is the FC-1/MAC device I/O supply voltage.

Symbol	Parameter	Min	Typ	Max	Units
VREFT	Input reference voltage	1.15	1.25	1.35	V
V_{IH}	High level input Voltage	$VREFT + 0.35$		$V_{DDQ} + 0.30$	V
V_{IL}	Low level input Voltage	-0.30		$VREFT - 0.35V$	V
V_{IHPECL}	High level LVPECL input Voltage for REFCLK[0:1]	2.10		2.60	V
V_{ILPECL}	Low level LVPECL input Voltage for REFCLK[0:1]	1.30		1.80	V
$V_{IHLVTTL}$	High level LVTTTL input Voltage for REFCLK[0:1]	2.0			V
$V_{ILLVTTL}$	Low level LVTTTL input Voltage for REFCLK[0:1]			0.80	V
VREFR	Output reference voltage	1.15	1.25	1.35	V
V_{OH}	High level output voltage	$VREFR + 0.38$		V_{DDQ}	V
V_{OL}	Low level output voltage	GND		$VREFR - 0.43$	V

DC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{SOUT75}	SO+/SO- differential peak-to-peak voltage swing.	Terminated by 75 Ohms	1100	1400	2000	mV
V _{SOUT50}	SO+/SO- differential peak-to-peak voltage swing.	Terminated by 50 Ohms.	800	1050	2000	mV
V _{IN}	SI+/SI- differential peak-to-peak input sensitivity		200		2000	mV
V _{DIH}	SI+/SI- differential Input common-mode voltage ^[3]			1.65		V
V _{DOH}	SO+/SO-differential Output common-mode voltage ^[3]			2.78		V
P _{CC}	Power dissipation	C _{LOAD} =5pF 2.125 Gbps rate TX+/- = 50ohms terminated		446 ^[1]	680 ^[2]	mW

[1] Sending/Receiving Random Pattern

[2] Sending/Receiving Worst Case (maximum transitions) Pattern

[3] Self biased

REFCLK[0:1], TBC Parameters

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
T _{REF_FREQ}	Nominal Frequency		106.25		MHz
T _{REF_J}	REFCLK[0:1] frequency tolerance	-200		200	ppm
T _{REF_DUTY}	REFCLK[0:1] duty cycle	40%		60%	

Transmit Function AC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
T _{TXS}	TX[0:9] setup time to the falling edge of TBC (TX_RATE=0)	1400			ps
T _{TXH}	TX[0:9] hold time from the falling edge of TBC (TX_RATE=0)	1400			ps
T _{TCT}	TX[0:9], TBC transition time (TX_RATE=1)			1880	ps
T _{TCV}	TX[0:9], TBC valid/stable time (TX_RATE=1)	2820			ps
T _{RISE}	SO+/SO- rise time into 50 Ohms. Measured from 20% and 80% of full swing.		160		ps
T _{FALL}	SO+/SO- fall time into 50 Ohms. Measured from 20% and 80% of full swing.		160		ps
T _{TXLAT}	Latency from TX[0:9] parallel input to SO+/SO- serial output		0.4+10		ns..bit

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Symbol	Parameter	Min	Typ	Max	Units
T _{TRJ}	SO+/SO- output random RMS jitter ^{[4][5]}		3.5		ps
T _{TDJ}	SO+/SO- output deterministic jitter		32		ps

[4] Random jitter was measured according to "Fibre Channel Specification X3.230-1994 FC-PH, Annex A, Section A.4.4 (oscilloscope method)".

[5] Deterministic jitter was measured according to "Fibre Channel Specification X3.230-1994 FC-PH, Annex A, Section A.4.3"

Receiver Function AC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
T _{AXS}	Mode A , RX[0:9] setup time to the rising edge of RBC[0:1]	2.7			ns
T _{AXH}	Mode A , RX[0:9] hold time to the rising edge of RBC[0:1]	1.5			ns
T _{ARR}	Mode A , RBC[1] to RBC[0] rising edge skew	8.9		9.9	ns
T _{BXS}	Mode B , RX[0:9] setup time to the rising edge of RBC[0] , or falling edge of RBC[1]	1.7			ns
T _{BXH}	Mode B , RX[0:9] hold time to the rising edge of RBC[0] , or falling edge of RBC[1]	1.7			ns
T _{CXS}	Mode C , RX[0:9] setup time to the rising edge of RBC[0:1]	1.4			ns
T _{CXH}	Mode C , RX[0:9] hold time to the rising edge of RBC[0:1]	1.4			ns
T _{CRR}	Mode C , RBC[1] to RBC[0] rising edge skew	4.5		4.9	ns
T _{DCT}	Mode D , RX[0:9] transition time			1.7	ns
T _{DCV}	Mode D , RX[0:9] valid/stable time	3			ns
T _{RRISE} , T _{RFALL}	Parallel output rise/fall. Measured from 20% and 80% of full swing.			1.5	ns
T _{RDUTY}	Duty cycle of RBC[0:1]. Measured from 20% and 80% of full swing.	40%		60%	

Conditions:

1. RBC[1] /RBC[0] and RX[0:9] are loaded by 5pF to ground for these measurements.

Receiver Timing Characteristics

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
F _{lock}	PLL Locking time			200	μs
B _{sync}	Bit sync time		200	2500	bits
T _{RXLAT}	Latency from SI+/SI- serial input to RX[0:9] parallel output		2.4+29		ns..bit

AC Timing

Transmit Timing

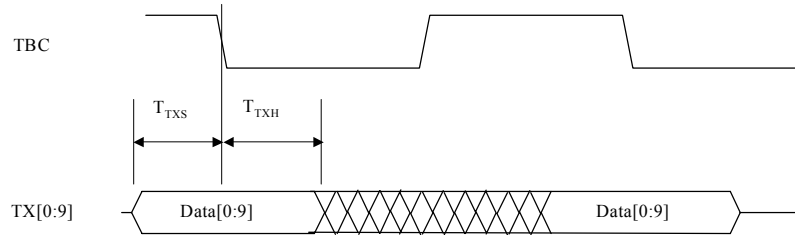


Figure 3. Input Timing for TX_RATE = 0 (1.0625 Gbps mode)

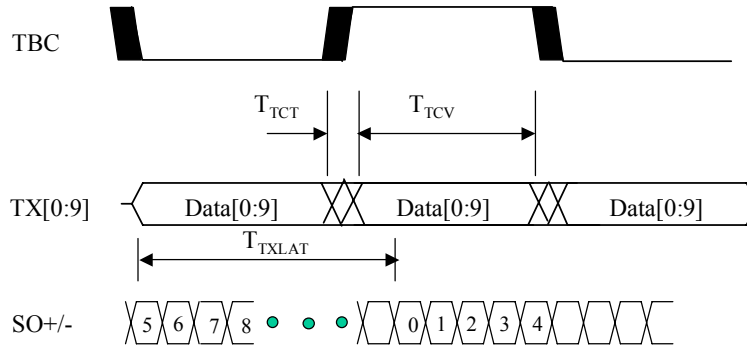


Figure 4. Input Timing for TX_RATE = 1 (2.125 Gbps mode)

Receive Timing

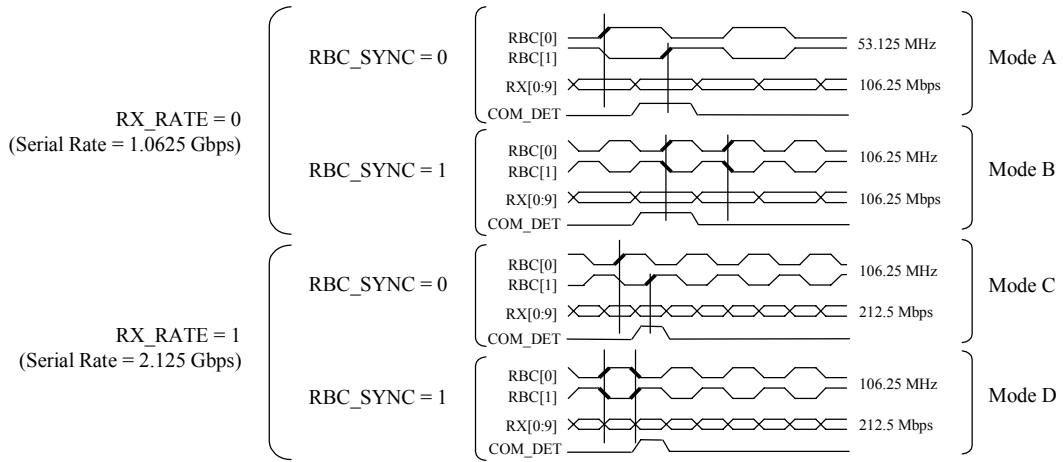


Figure 5. Parallel Output Modes

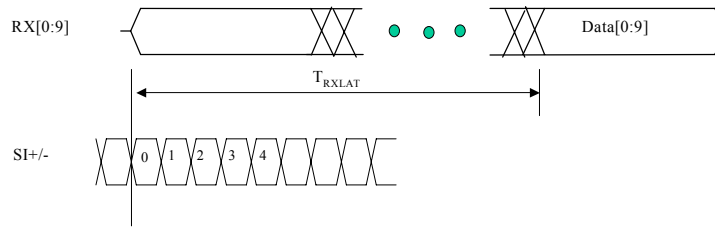


Figure 6. RX Latency

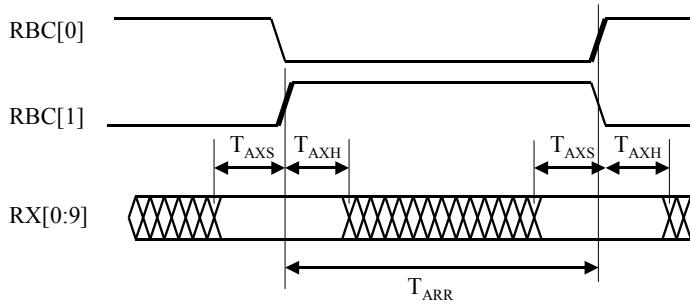


Figure 7. Mode A Timing Diagram (RX_RATE=0, RBC_SYNC=0)

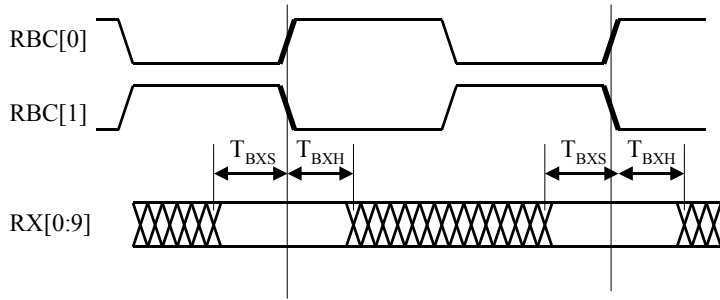


Figure 8. Mode B Timing Diagram (RX_RATE=0, RBC_SYNC=1)

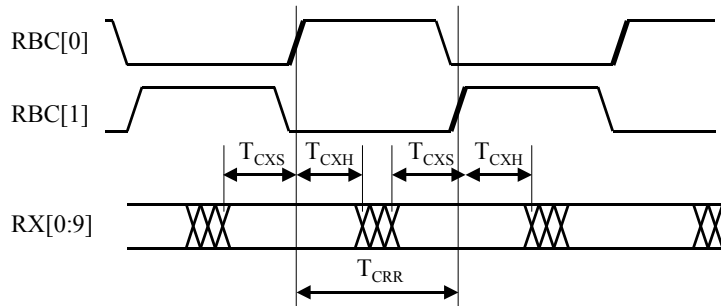


Figure 9. Mode C Timing Diagram (RX_RATE=1, RBC_SYNC=0)

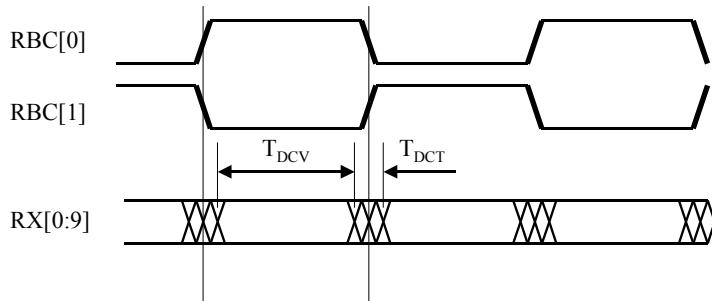
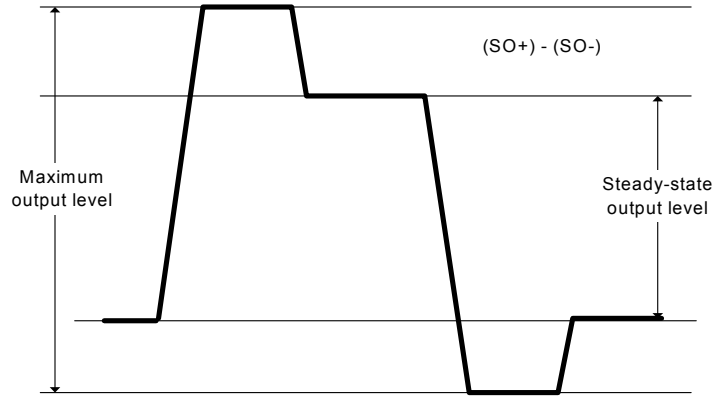


Figure 10. Mode D Timing Diagram (RX_RATE=1, RBC_SYNC=1)



SO+/- terminated by 50 ohms, $V_{cc} = 3.3V$, $T_A = 25\text{ }^\circ\text{C}$
 The maximum output level (EQAMP pin = 3.3V) = V_{sout50} in the DC specifications.

Figure 11. Waveform for Pre-emphasis Values

Pins Descriptions

Functional Pins

Pin Name	Pin #	Type	Description
TX[0], TX[1], TX[2], TX[3], TX[4], TX[5], TX[6], TX[7], TX[8], TX[9]	2, 3, 4, 6, 7, 8, 9, 11, 12, 13	In – SSTL_2	TX[0:9] : Input pins for the 10-bit encoded data character that is to be transmitted serially over the SO± differential outputs. The first serial bit transmitted will be TX[0].
RX[0], RX[1], RX[2], RX[3], RX[4], RX[5], RX[6], RX[7], RX[8], RX[9]	45, 44, 43, 41, 40, 39, 38, 36, 35, 34	Out – SSTL_2	RX[0:9] : 10-bit received data.
SO+ SO-	62 61	Out Out	SO±: Serialized, high speed. When parallel loop-back is disabled (EWRAP=0) these pins are active. When EWRAP=1, these pins are driven to logic 1.
SI+ SI-	54 52	In In	SI± : Serialized, high speed, differential inputs. Serial data is accepted when EWRAP is low.
REFCLK[1], REFCLK[0]	22 23	In-PECL or In-LVTTL In-LVTTL	REFCLK[0:1] are differential reference clock inputs. This clock source is used by both receive sections of the device. When REF_RATE=1, these pins are used to input a 53.125 MHz clock signal. When REF_RATE=0, these pins input a 106.25 MHz clock signal. These pins can be driven by a differential PECL clock source, or by a LVTTL single-ended clock on REFCLK[1] with REFCLK[0] connecting to GND via 0.1µF capacitor.
TBC	1	In – SSTL_2	Transmit byte clock. This clock is used to capture the parallel input data (TX[0:9]). When TX_RATE = 0, the falling edge of TBC is used to capture the parallel data. When TX_RATE=1, data is captured between both the rising and falling edges of TBC resulting in a doubling of the data rate.
RBC[1] RBC[0]	30 31	Out – SSTL_2	Recovered clock output. These clock outputs are used by external devices to capture the RX[0:9] parallel data. The two clocks are 180 degrees out of phase with each other. The relationship between these clocks and the parallel data depends on the settings of RX_RATE, RBC_SYNC.
REF_RATE	29	In – SSTL_2	Sets the rate of the input reference clock. REF_RATE=0, the reference clock frequency is 106.25 MHz. REF_RATE=1 the reference clock frequency is 53.125 MHz.
RX_RATE	55	In – SSTL_2	Receiver rate. The setting of this signal determines the rate at which the receiver operates. RX_RATE=0, the incoming serial stream is sampled at 1.0625 Gbps and the parallel data is driven out with the rising edge of RBC[1]. RX_RATE=1, the incoming serial stream is sampled at 2.125 Gbps and the parallel data is driven out with the rising edge of RBC[1] and RBC[0].
TX_RATE	14	In – SSTL_2	Transmitter rate. The setting of this signal determines the rate at which the transmitter operates. TX_RATE=0, the incoming parallel data stream is sampled on the falling edge of TBC. The data is then serialized and transmitted at a rate of 1.0625 Gbps. TX_RATE=1, the incoming serial stream is sampled between BOTH edges of TBC. The data is then serialized and transmitted at a rate of 2.125 Gbps.

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Pin Name	Pin #	Type	Description
RBC_SYNC	10	In – SSTL_2	When RX_RATE = 0, Setting RBC_SYNC determines the frequency of RBC, RBC=53.125 MHz for RBC_SYNC = 0, and RBC= 106.25 MHz for RBC_SYNC= 1. When RX_RATE = 1, setting RBC_SYNC = 1 the receiver parallel output data and clocks transition simultaneously and, setting RBC_SYNC = 0 clocks transition between the data transitions.
EQAMP	56	In- External Circuit Node	Equalization control. This pin is used to input a voltage reference that sets the amount of equalization on the SO± outputs. For maximum equalization connect this pin to ground. To disable the equalization connect this pin to V _{cc} .
EWRAP	19	In – SSTL_2	Enable parallel loop-back mode. When loop-back is enabled, parallel input data is looped to the parallel output data, the serializer/deserializer circuits are bypassed. EWRAP=0 loop-back mode is disabled. EWRAP=1, loop-back mode is enabled.
EN_CDET	24	In –SSTL_2	Enable comma detection (activated with high).
COM_DET	27	Out – SSTL_2	Comma detection signal. This signal is driven high when a comma character of positive disparity (001111xxx) is detected on the high-speed serial input lines.
RX_LOS	26	Out – SSTL_2	Indicates whether there is any valid signal on SI± pins. If RX+/- > 200mVp-p, RX_LOS = 0 If RX+/- < 200mVp-p and RX+/- > 75mV, RX_LOS = undefined If RX+/- < 75mVp-p, RX_LOS = 1, RX[0:9] = B'111111111'
VREFT	5	In - Analog	Voltage reference input, set by external voltage divider to 1.25V for SSTL_2 input. If this pin is floated, 1.25V is generated internally.
VREFR	47	Out - Analog	Voltage reference output, externally outputs the voltage reference corresponding to 1.25V for SSTL_2 output.

Power & Ground Pins

Pin Name	Pin #	Type	Description
Vcc	20, 28, 53, 57, 59	Power	Power supply for digital logic circuits (3.3V).
Vcc_TXA	17, 18	Power	Power supply for transmit PLL (3.3V). For the best performance, this supply should be as noise free as possible.
Vcc_RXA	49, 50	Power	Power supply for receive PLL (3.3V). For the best performance, this supply should be as noise free as possible.
Vcc_TXHS	60, 63	Power	High Speed Transmitter Supply. For the best performance, Noise on this line should be minimized.
Vcc_SSTL	37, 42	Power	Power supply for I/O pads.
GND	21, 25, 58	Ground	Ground for digital logic circuits.
GND_TXA	15	Ground	For the best performance, this ground should be as noise free as possible.
GND_RXA	51	Ground	For the best performance, this ground should be as noise free as possible.
GND_TXHS	64	Ground	High Speed Transmitter Ground. For the best performance, Noise on this line should be minimized.
GND_SSTL	32, 33, 46	Ground	Ground for I/O pads.

Sil2022 Pin Diagram

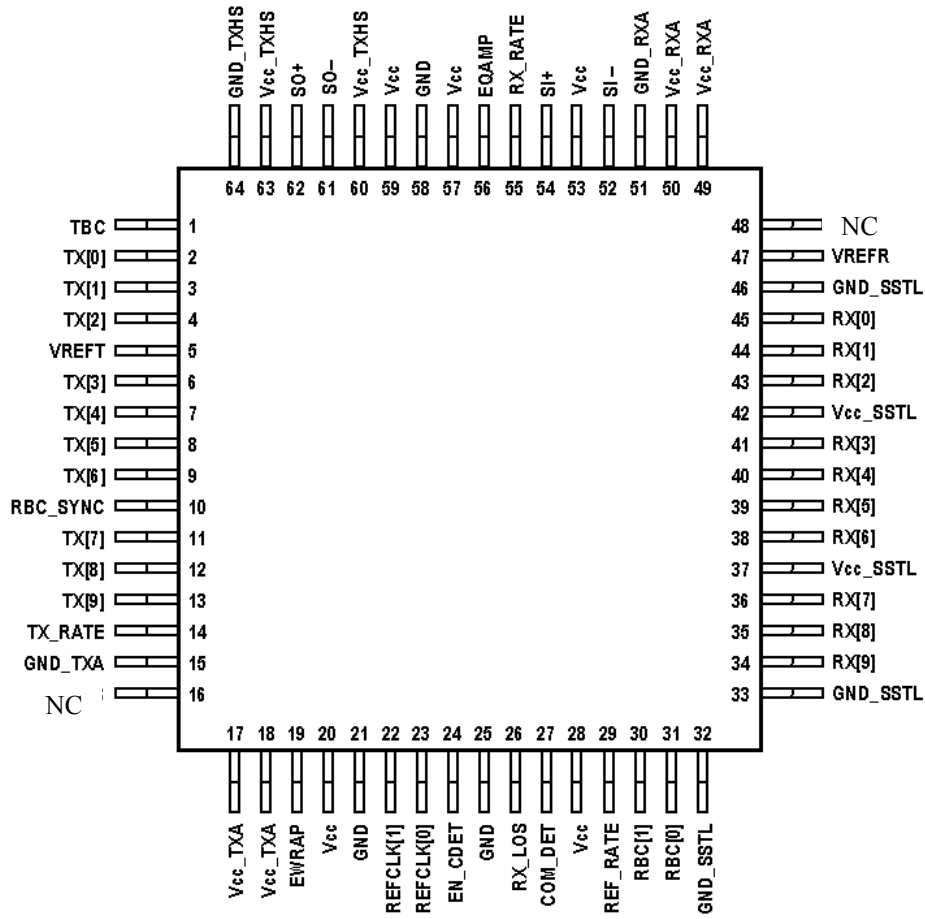
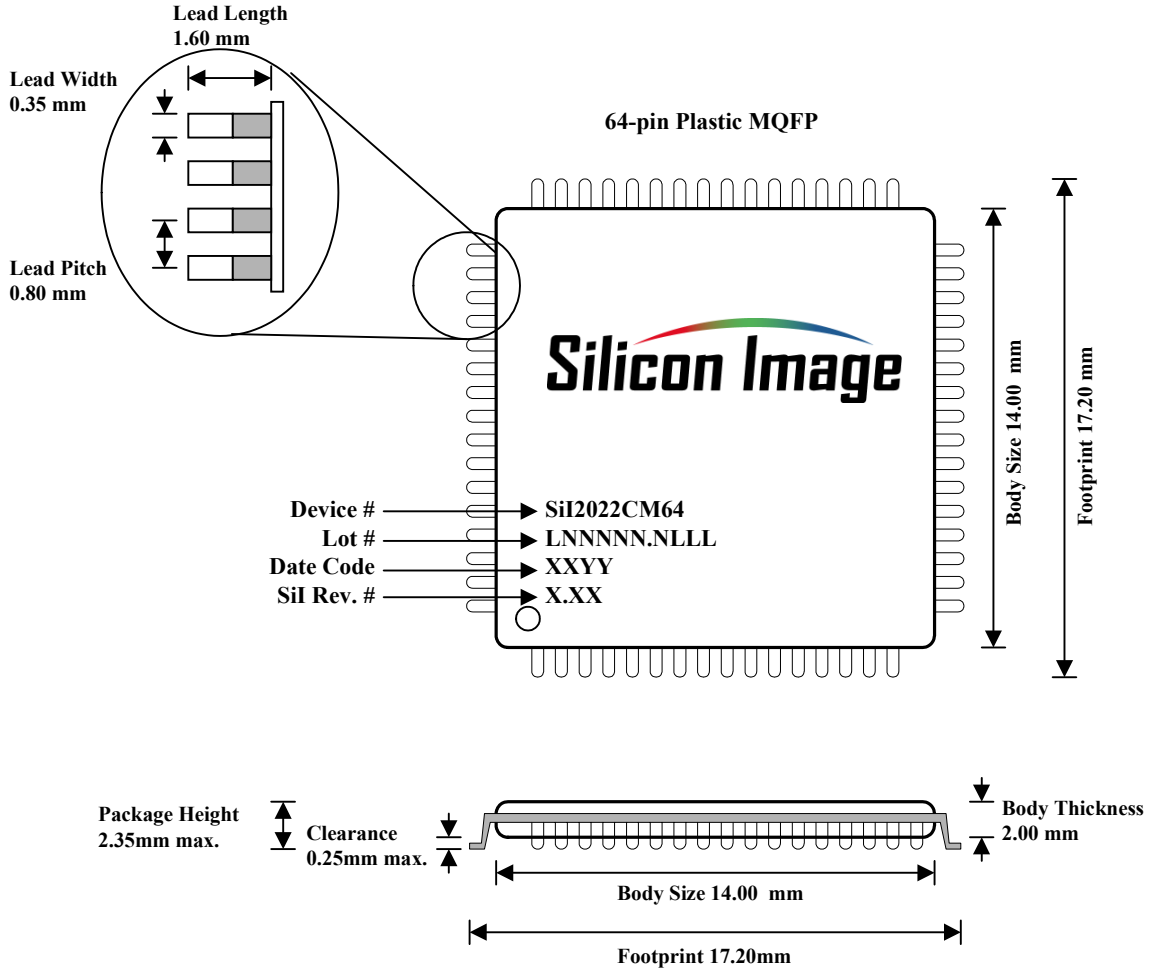


Figure 12. Sil2022 Pin Diagram (Top view)

Package Dimensions

64-pin MQPF Package Dimensions



JEDEC code MS-022 BB

Figure 13. SiI2022CM64 Package Diagram

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Part Ordering Number:

SiI2022CM64 (64 pin MQFP)

Revision History:

<u>Revision</u>	<u>Comment</u>	<u>Date</u>
1.0	Preliminary Data Sheet	04/18/2002

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