Configuration EPROM
for FLEX 8000 Devices

March 1995, ver. 3 Data Sheet

Features

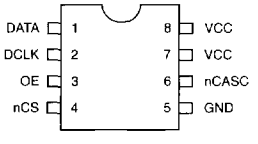
- Serial EPROM family designed to configure FLEX 8000 devices
- Simple 4-wire interface to FLEX 8000 devices for ease of use
- Low current during configuration (15 mA) and near-zero standby current (100 µA)
- Software design support with Altera's MAX+PLUS II development system for 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations
- Programming support with Altera's Master Programming Unit (MPU) and programming hardware from other manufacturers, including Data I/O
- Available in compact, one-time programmable (OTP) ceramic and plastic packages (see Figure 1):
  - 8-pin CerDIP
  - 8-pin PDIP
  - 20-pin PLCC
  - 32-pin TQFP

Functional Description

In SRAM-based devices, configuration data must be reloaded each time the system initializes, or whenever new configuration data is desired. Altera's serial Configuration EPROMs store configuration data for SRAM-based Altera FLEX 8000 devices.

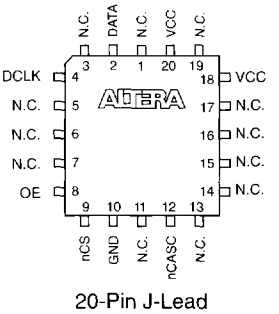
Figure 1. Configuration EPROM Package Pin-Out Diagrams

Package outlines not drawn to scale.



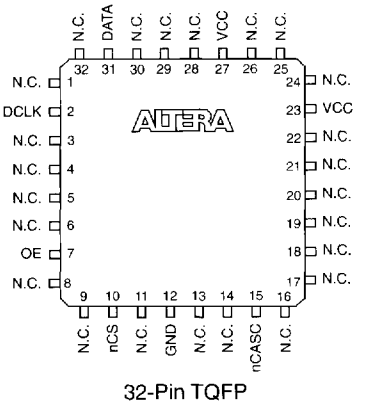
8-Pin DIP

EPC1064
EPC1064V
EPC1213



20-Pin J-Lead

EPC1064
EPC1064V
EPC1213



32-Pin TQFP

EPC1064
EPC1064V

The EPC1064 and EPC1064V are 65,536 × 1 bit devices, and the EPC1213 is a 212,992 × 1 bit device. Table 1 shows the Configuration EPROM that is appropriate for each FLEX 8000 device.

Table 1. Typical Applications for Altera Configuration EPROMs

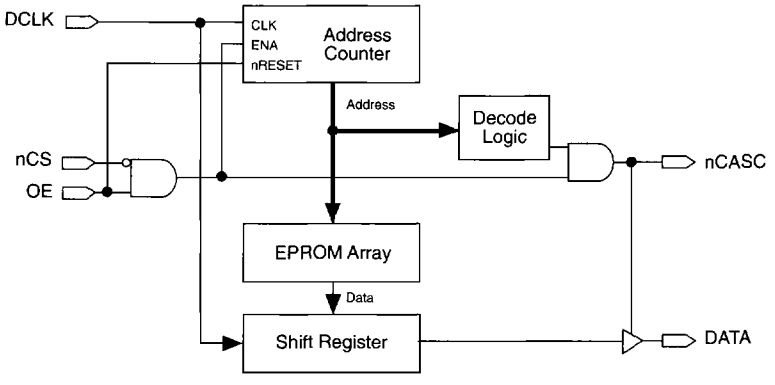
FLEX 8000 Device	Configuration EPROM
EPF8282, EPF8282A	EPC1064
EPF8282V, EPF8282AV	EPC1064V
EPF8452, EPF8452A	EPC1064
EPF8636A	EPC1213
EPF8820, EPF8820A	EPC1213
EPF81188, EPF81188A	EPC1213
EPF81500, EPF81500A	EPC1213, *Note (1)*

Note:
(1) The EPF81500 and EPF81500A require two EPC1213 devices for configuration.

Figure 2 shows a block diagram of the Configuration EPROM. Configuration data is stored in the EPROM array and clocked out serially by the DCLK input. The Output Enable (OE), Chip-Select (nCS), and Clock (DCLK) pins supply the control signals for the address counter and the output tri-state buffer. The device presents the configuration data as a serial bitstream on the DATA pin. This data is routed into the FLEX 8000 device via the DATA0 input pin. The nCASC pin provides handshaking between multiple Configuration EPROMs, so that a set of devices can be linked together to serially configure a large FLEX 8000 device or multiple FLEX 8000 devices.

Go to the *FLEX 8000 Programmable Logic Device Family Data Sheet* in this data book for more information on FLEX 8000 device architecture. Go to *Application Note 33 (Configuring FLEX 8000 Devices)* and *Application Note 38 (Configuring Multiple FLEX 8000 Devices)* in the ***FLEX 8000 Handbook*** for more information on FLEX 8000 device configuration.

Figure 2. Configuration EPROM Functional Block Diagram



The control signals for Configuration EPROMs (DCLK, nCS, and OE) interface directly to the FLEX 8000 device control signals. A FLEX 8000 device can control the entire configuration process and retrieve the configuration data from the Configuration EPROM without an external intelligent controller. The FLEX 8000 device can be set to configure automatically at system power-up by connecting nCONFIG to VCC.

The OE and nCS pins work together to control the tri-state buffer on the DATA output pin, and to enable the address counter in the Configuration EPROM. When OE is driven low, the device resets the address counter and tri-states the DATA pin. When the OE pin is driven high again, the device is controlled by the nCS pin. If nCS is held high after the OE reset pulse, the counter is disabled, and the DATA output pin is tri-stated. When nCS is driven low, the counter is enabled and the DATA output pin is enabled. The nCS pin can then be held either high or low to control the output and counter. When OE is driven low again, the address counter is reset and the DATA output pin is tri-stated regardless of the state of nCS.

When the Configuration EPROM has driven out all of its data and nCASC is driven low, it will tri-state the DATA pin to avoid contention with other Configuration EPROMs. Upon power-up, the address counter is automatically reset. Table 2 describes the pin functions of Altera Configuration EPROMs.

Table 2. Configuration EPROM Pin Functions

Pin Name	Pin Number			Pin Type	Description
	8-Pin PDIP	20-Pin PLCC	32-Pin TQFP		
DATA	1	2	31	Output	Serial data output.
DCLK	2	4	2	Input	Clock input. Rising edges on DCLK increment the internal address counter and cause the next bit of data to be presented on DATA. The counter is incremented only if the OE input is held high and the nCS input is held low.
OE	3	8	7	Input	Output Enable (active high) and Reset (active low). A low logic level resets the address counter. A high logic level enables DATA and permits the address counter to count.
nCS	4	9	10	Input	Chip-select input (active low). A low input allows DCLK to increment the address counter and enables DATA.
nCASC	6	12	15	Output	Cascade-select output (active low). This output goes low when the address counter has reached its maximum value. nCASC is usually connected to the nCS input of the next Configuration EPROM in a daisy-chain, so the next DCLK clocks data out of the next Configuration EPROM.
GND	5	10	12	Ground	A 0.2-µF decoupling capacitor must be placed between the VCC and GND pins.
VCC	7, 8	18, 20	23, 27	Power	Power pin.

Device Configuration

The active serial (AS) and multi-device sequential active serial (MD-SAS) configuration schemes use a Configuration EPROM (e.g., EPC1213) as a data source for a FLEX 8000 device.

For complete information on configuring FLEX 8000 devices, go to the *FLEX 8000 Programmable Logic Device Family Data Sheet* in this data book and *Application Note 33 (Configuring FLEX 8000 Devices)*, and *Application Note 38 (Configuring Multiple FLEX 8000 Devices)* in the ***FLEX 8000 Handbook***.

MAX+PLUS II Support

The MAX+PLUS II development system provides programming support for Altera Configuration EPROMs. The MAX+PLUS II software automatically generates a Programmer Object File (**.pof**) for every Configuration EPROM in a project. In a multi-device project, MAX+PLUS II can combine the programming files for multiple FLEX 8000 devices into one or more Configuration EPROMs. MAX+PLUS II selects the appropriate Configuration EPROM to most efficiently store the data for each FLEX 8000 device.

The POF includes a preamble, cyclic redundancy check (CRC), and synchronization data that allow it to be used in a serial bitstream. The POF is programmed into the Configuration EPROM with MAX+PLUS II and a Configuration EPROM programming adapter. A number of other programming hardware manufacturers, including Data I/O, support programming of Configuration EPROMs. See *Altera Programming Hardware* and *Programming Hardware Manufacturers* in this data book.

Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND, *Note (2)*	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			20	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			100	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage for 5.0-V device		4.75	5.25	V
	Supply voltage for 3.3-V device		3.0	3.6	V
V_I	Input voltage	With respect to GND, *Note (2)*	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			20	ns
t_F	Input fall time			20	ns

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	5.0-V device high-level TTL output voltage	I_{OH} = –4 mA DC	2.4		V
	3.3-V device high-level TTL output voltage	I_{OH} = –0.1 mA DC	V_{CC} – 0.2		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC		0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10	10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–10	10	µA

Supply Current

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby)			100		µA
I_{CC1}	V_{CC} supply current (during configuration)	DCLK = 6 MHz		10		mA

Capacitance *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Timing Parameters

			EPC1064V		EPC1064 EPC1213		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Unit
t_{OEZX}	OE high to DATA output enabled			75		50	ns
t_{CSZX}	nCS low to DATA output enabled			75		50	ns
t_{CSXZ}	nCS high to DATA output disabled			75		50	ns
t_{CSS}	nCS low setup time to first DCLK rising edge		150		100		ns
t_{CSH}	nCS low hold time after DCLK rising edge		0		0		ns
t_{DSU}	Data setup time before rising edge on DCLK, *Note (6)*		75		50		ns
t_{DH}	Data hold time after rising edge on DCLK, *Note (6)*		0		0		ns
t_{CO}	DCLK to DATA out delay, *Note (7)*			100		75	ns
t_{CK}	Clock period		240		160		ns
f_{CK}	Clock frequency			4		6	MHz
t_{CL}	DCLK low time		120		80		ns
t_{CH}	DCLK high time		120		80		ns
t_{XZ}	OE low or nCS high to DATA output disabled			75		50	ns
t_{OEW}	OE pulse width to guarantee counter reset		150		100		ns
t_{CASC}	Last DCLK + 1 to nCASC low delay			90		60	ns
t_{CKXZ}	Last DCLK + 1 to DATA tri-state delay			75		50	ns
t_{CEOUT}	nCS high to nCASC high delay			150		100	ns

Notes to tables:

(1) See *Operating Requirements for Altera Devices* in this data book.

(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.

(3) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.

(4) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5.0 V ± 10%, T_A = –55° C to 125° C for military use.

(5) Capacitance is sample-tested only.

(6) This parameter applies to the FLEX 8000 device.

(7) Eight Clock cycles are required after the t_{CSS} setup time has been met to clock out the first eight bits. These bits are all high and are used to synchronize the configuration process. The ninth Clock cycle presents the first configuration data bit.