PHAST®-12E Device

Programmable, High-Performance ATM/PPP/TDM SONET/SDH Terminator for Level 12 with Enhanced Features

TXC-06212

DATA SHEET

FEATURES

- Supports simultaneous termination of ATM, POS, and TDM (Time Division Multiplexed, e.g., VT1.5, VC-4 etc.) traffic
- Integrated clock recovery and synthesis for four 155.52 Mbit/s signals or one 622 Mbit/s signal
- STS-12/STS-12c/STM-4/STM-4c, or quad STS-3c/STM-1 framing and performance monitoring
- Complete Transport/Section Overhead processing and generation per Bellcore and ITU-T standards
- Complete Path Overhead processing and generation for one STS-12/STS-12c/STM-4/STM-4c signal or for four STS-3c/STM-1 signals for ATM/PPP
- VC-4 cross connect for STS-12, STM-4, and 4xSTS-3c/STM-1 operation
- Loop timing mode selectable from one of the four recovered clocks or from a separate reference clock input
- APS for ATM/PPP payloads using the UTOPIA port(s)
- Cell or frame delineation function for four STS-3c/STM-1 or one STS-12/STS-12c/STM-4/STM-4c signal
- "PPP" support per RFC1662 and RFC2615 for all inputs
- UTOPIA L2 (cell) 8/16-bit interface at 25 MHz/50 MHz
- UTOPIA L2P (frame) 16-bit interface at 50 MHz
- Quad byte-parallel Telecom Bus at 19.44 Mbyte/s
- Access to Line or Section DCC via a port
- Ring port for UPSR support
- Selectable Intel/Motorola-compatible microprocessor interface
- Boundary scan capability (IEEE 1149.1)
- +3.3 V ±5% I/O and +2.5 V ±5% CORE power supplies
- 2.2 W (four 155 Mbit/s interfaces), 1.5 W (one interface at 622 Mbit/s)
- 675-lead enhanced plastic ball grid array package
- Device Software Driver available

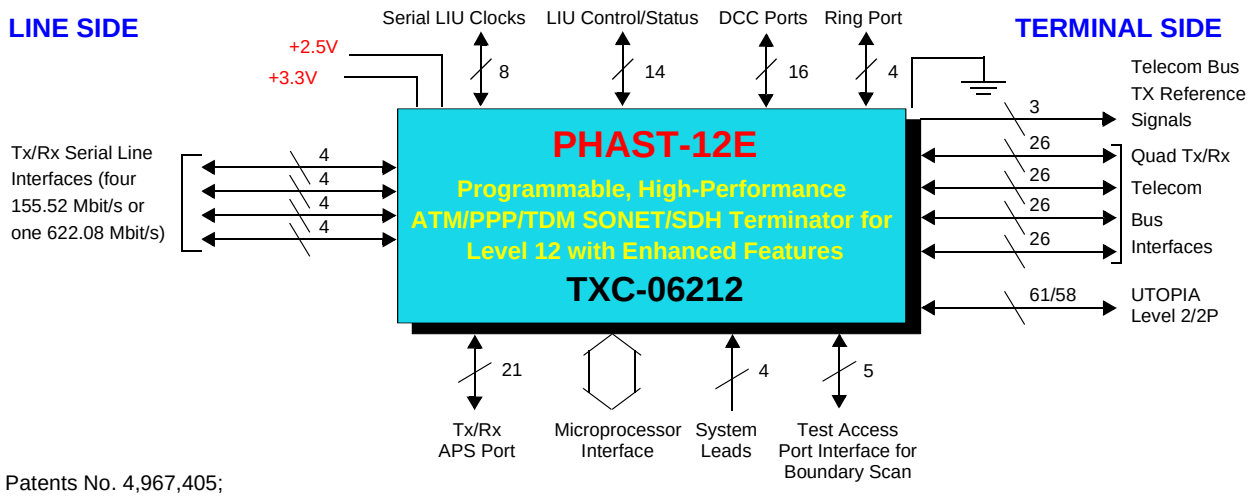
DESCRIPTION

The PHAST®-12E is a highly integrated SONET/SDH terminator device designed for ATM cell, frame, higher order multiplexing, and transmission applications. A single PHAST-12E device can terminate four individual STS-3c or STM-1 lines or a single STS-12/12c or STM-4/4c line. Each SONET/SDH terminator has an associated line interface block that performs clock synthesis and clock recovery for four 155.52 Mbit/s signals or single 622.08 Mbit/s serial operation.

The PHAST-12E can terminate ATM payloads from any of the above signals into a 16-bit or 8-bit UTOPIA Level 2 PHY interface. PPP payloads are terminated into a 16-bit wide UTOPIA Level 2P interface. STM (VT/TU) payloads can be terminated into four 8-bit wide Telecom Bus interfaces. The PHAST-12E facilitates multiservice applications by providing simultaneous termination of ATM, Packet over SONET/SDH (POS), and TDM traffic that are contained in separate SPEs/VCs. When terminating concatenated payloads, the four Telecom Bus interfaces act in concert as a single 32-bit wide Telecom Bus interface. Single-device APS switching or 1:N APS between multiple PHAST-12E devices is also provided for ATM and PPP payloads.

APPLICATIONS

- Multiservice applications
- SONET/SDH add/drop or higher order terminal multiplexers
- Transport of ATM/PPP or VT/TU payloads over SONET/SDH
- Transmission of E1/DS1, E3/DS3 or E4 over SONET/SDH
- ATM and packet switches



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* Please note that TranSwitch provides documentation for all of its products. Current editions of many documents are available from the Products page of the TranSwitch Web site at www.transwitch.com. Customers who are using a TranSwitch Product, or planning to do so, should register with the TranSwitch Marketing Department to receive relevant updated and supplemental documentation as it is issued. They should also contact the Applications Engineering Department to ensure that they are provided with the latest available information about the product, especially before undertaking development of new designs incorporating the product.

LIST OF FIGURES

LIST OF TABLES

These tables provide detailed information on the registers and bits in the PHAST-12E Memory Map, and they are grouped according to the subsection headings for the memory map in the Table of Contents above. 'Table 4, " on page 168 lists the PHAST-12E "chiplets" and the address ranges they use in memory. For each memory map subsection, the first table lists the associated registers and subsequent tables describe the bits situated in all of these registers, with one or more registers described in each table.

APPLICABLE STANDARDS DOCUMENTATION

Standards documents applicable to the functions of the PHAST®-12E are listed in the table below. The addresses and other contact information for the organizations that publish or distribute them are provided at the rear of this document. References to these documents are made in the text by showing the document number in brackets, e.g., [G.707].

Document No.	Description
G.707	ITU-T, Network Node Interface for the Synchronous Digital Hierarchy, (03/96)
G.783	ITU-T, Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks, (04/97)
G.803	ITU-T, Architectures of Transport Networks Based on the Synchronous Digital Hierarchy (SDH), (06/97)
GR-1400	Bellcore, GR-1400-CORE, SONET Dual-Fed Unidirectional Path Switched Ring (UPSR) Equipment Generic Criteria, Issue 1, (March 1994)
GR-253	Bellcore, GR-253-CORE, Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria, Issue 2, (12/95), Revision 2 (01/99)
GR-496	Bellcore, GR-496-CORE, SONET Add-Drop Multiplexer (SONET ADM) Generic Criteria, Issue 1, (December 1998)
GR-499	Bellcore, GR-499-CORE, Transport Systems Generic Requirements (TSGR): Common Requirements, Issue 2, (December 1998)
I.361	ITU-T, Integrated Services Digital Network (ISDN) - Overall Network Aspects and Functions, (11/95)
I.432.1	ITU-T, B-ISDN User-Network Interface - Physical Layer Specification, (08/96)
IEEE 1149.1	IEEE Standard Access Port and Boundary Scan Architecture (1990, supplement a 1993, and supplement b 1994)
RFC1662	IETF, PPP in HDLC-like Framing, (07/94)
RFC2615	IETF, PPP Over SONET/SDH, (06/99)
T1.105-1995	ANSI, Synchronous Optical Network (SONET) - Basic Description including Multiplex Structure, Rates, and Formats, (1995)
T1.231-1997	ANSI, Digital Hierarchy - Layer 1 In-Service Digital Transmission Performance Monitoring, (1997)
UL2v1	ATM Forum, UTOPIA Level 2, Version 1.0, (06/95)

SCOPE

This document provides a detailed description of the features, characteristics and operation of the TranSwitch PHAST-12E (Programmable High performance ATM/PPP/TDM SONET/SDH Terminator for Level 12 with Enhanced Features) device. The primary applications of the PHAST-12E are transport of ATM/PPP payloads over SONET/SDH, higher-order muxes, add/drop muxes, and multiservice applications.

Throughout this document, SONET and SDH terminologies are used interchangeably when describing portions of the payload or overhead of a SONET/SDH frame. SDH terminology provides more “granularity” for describing parts of a frame and hence is used more often. e.g., An STS-3c-SPE can be referred to as a VC-4 in this document, an STS-3c-SPE plus its pointer is referred to as an AU-4, etc.

Also, depending on the context of the discussion, the # is used as an index, where # = 1-4. e.g., LOSSSIG# = LOSSSIG1, LOSSSIG2, LOSSSIG3, and LOSSSIG4.

OVERVIEW

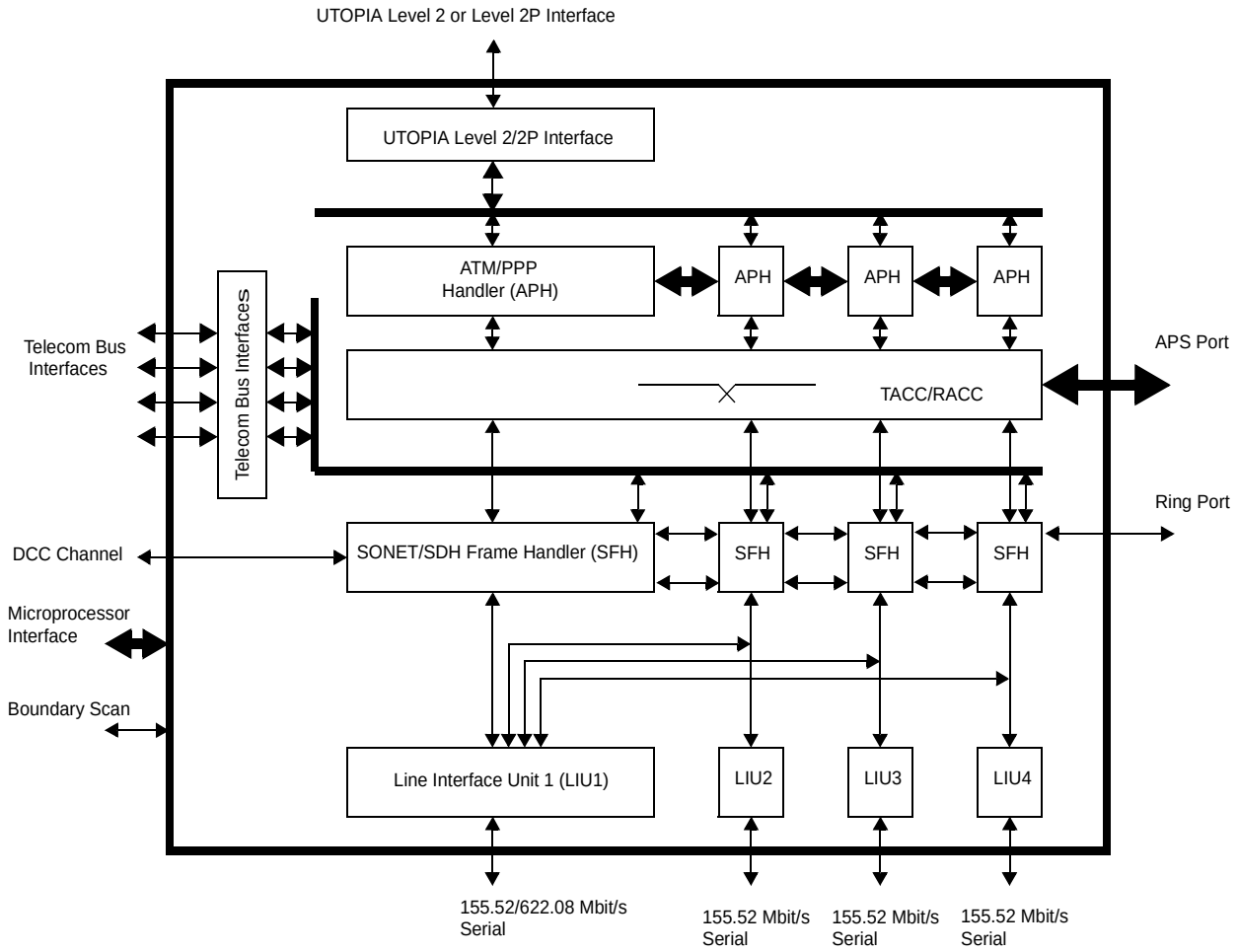


Figure 1. PHAST-12E TXC-06212 High Level Block Diagram

The PHAST-12E is a highly integrated SONET/SDH terminator device designed for transmission, cell, and frame applications. It contains four independent SONET/SDH terminators, which can either terminate ATM/PPP payloads into a UTOPIA Level 2 PHY or Level 2P interface, or it can interface the SONET/SDH frames to up to four Telecom Bus interfaces. It is a 2.5 volt and 3.3 volt device with mainly 3.3 volt inputs and outputs for its non-Line Interface signals. The inputs and outputs are not 5 Volt tolerant. Several other interfaces are provided to facilitate DCC channel connection to an external HDLC controller, APS and ring operation. The PHAST-12E is being provided in a 675-lead enhanced plastic ball grid array package.

The PHAST-12E is composed of a number of circuits that perform fairly specific functions. These circuits are termed chiplets. Related chiplets are grouped together to form more complex/multi-functional circuits called blocks. The various blocks are grouped together to form a circuit that performs the termination of a SONET/SDH stream. These circuits are called macros. The PHAST-12E has four such macros and hence can terminate up to four SONET/SDH streams operating at 155.52 Mbit/s. Additionally, the four macros can operate together in whole and in part to support termination of channelized and unchannelized 622.08 Mbit/s SONET/SDH streams.

The Telecom Bus interfaces and the UTOPIA Level 2/2P interface can be used simultaneously to support multiservice applications where TDM, ATM, and PPP data need to be terminated by the same device, at the same time.

e.g., The PHAST-12E can be configured for STS-12 mode and terminate 4 individual STS-3c-SPEs. Two of the STS-3c-SPEs can be terminated into the Telecom Bus interface while the other two STS-3c-SPEs can be terminated into the UTOPIA Level 2/2P Multi PHY interface. When the PHY that contains ATM cells is selected, the UTOPIA Level 2/2P interface behaves like a UTOPIA Level 2 interface. When the PHY that contains PPP frames is selected, the UTOPIA Level 2/2P interface behaves like a UTOPIA Level 2P interface.

A single PHAST-12E device can terminate four individual STS-3c or STM-1 lines, or a single STS-12/12c line, or STM-4/4c line. Each SONET/SDH terminator has an associated line interface block that performs clock synthesis and clock recovery for four 155.52 Mbit/s serial signals. The first line interface block can also perform clock synthesis and clock recovery for a single 622.08 Mbit/s serial signal. Table 1 below summarizes these features.

Table 1. Signals Terminated by the PHAST-12E

Signal	Number of Signals that can be terminated	Payload Granularity	Number of Payloads that can be Simultaneously Processed	Cross Connect Type available	Available Payload Handling
STS-3c	4	STS-3c payload	All 4	STS-3c-SPE	Each STS-3c-SPE payload can contain either ATM, PPP, or TDM
STM-1	4	C-4	All 4	VC-4	Each C-4 can contain either ATM, PPP, or TDM
STS-12	1	STS-3c payload	All 4	STS-3c-SPE	Each STS-3c-SPE payload can contain either ATM, PPP, or TDM
STS-12c	1	STS-12c payload	1	Not Available	The STS-12c-SPE payload can contain either ATM, PPP, or TDM
STM-4	1	C-4	All 4	VC-4	Each C-4 can contain either ATM, PPP, or TDM
STM-4c	1	C-4-4c	1	Not Available	The C-4-4c can contain either ATM, PPP, or TDM

The PHAST-12E can terminate ATM payloads from any of the above signals into either a single 16-bit or 8-bit UTOPIA Level 2 PHY interface. PPP payloads are terminated into a 16-bit wide UTOPIA Level 2P interface. TDM payloads can be terminated into up to four 8-bit wide Telecom Bus interfaces. When terminating concatenated payloads (STS-12c-SPE/VC-4-4c), the four Telecom Bus Interfaces act in concert as a single 32-bit wide Telecom Bus interface. Single-device APS switching or 1:N APS between multiple PHAST-12E devices is also provided for ATM and PPP payloads.

LINE INTERFACES AND SONET/SDH FRAME HANDLERS

Each SONET/SDH terminator has a Line Interface Unit (LIU) block associated with it that performs clock synthesis and clock recovery for 155.52 Mbit/s serial operation. The first Line Interface Unit block can also perform clock synthesis and clock recovery for 622.08 Mbit/s serial operation. The line interfaces support a timing loopback function, where a TX LIU has the capability to select one of the RX recovered clocks and use that clock as its TX reference clock.

The Line Interfaces are connected to corresponding SONET/SDH Frame Handler (SFH) blocks. These blocks provide the Regenerator Section Overhead (RSOH) and Multiplex Section Overhead (MSOH) functions, i.e., TOH functions, as well as the Path Overhead (POH) functions. All receive and transmit RSOH, MSOH, and POH bytes are stored in the on-chip RAM from where they can be observed/transmitted and also accessed via the microprocessor interface. The four SONET/SDH Frame Handler blocks can operate independently for STM-1/STS-3c applications or can operate together for STM-4/STS-12[1] or STM-4c/STS-12c applications. Four individual interfaces are provided for each DCC channel (regenerator or multiplex section) for connection to an external HDLC controller. In the case of STS-12/12c or STM-4/4c modes, only the first DCC port is used. The DCC bytes can optionally be inserted via the microprocessor interface. A Ring Port is provided that is used to communicate Line FEBE and RDI, K1 and K2 bytes plus associated alarms (and, when ATM or PPP processing is performed, K3 byte and associated indications as well as path FEBE and RDI information) between PHAST-12E devices. The SONET/SDH Frame Handlers can interface to either the external Telecom Bus Interfaces or the ATM/PPP Handler (APH) blocks.

TELECOM BUS INTERFACES

The PHAST-12E has four individual and independent Telecom Bus Interfaces which provide an alternative interface to the UTOPIA Level 2/2P style interface. The Telecom Bus Interface is a byte-wide interface with control signals for identification of the VC-4/VC-4c and TOH time slots as well as the location of the J0 and J1 bytes. There is one Telecom Bus Interface associated with each SONET/SDH Frame Handler. As is the case with the SONET/SDH Frame Handlers, the four Telecom Bus Interfaces can operate in concert with each other as one 32-bit wide Telecom Bus Interface when STM-4c/STS-12c frames are being processed. The PHAST-12E is not restricted to ATM or "PPP in HDLC-like Framing" payloads due to the general nature of the Telecom Bus Interface. However, when the Telecom Bus Interface is used, the PHAST-12E does not provide POH processing. Transmit Retiming is programmable on a per Telecom Bus basis and is performed at the VC-4 level. Transmit Retiming is the process of retiming the transmit Telecom Bus data, which may have a different frequency and phase from that of the SONET/SDH Frames being transmitted. Pointer recalculation and adjustments are used to accommodate the phase and frequency differences. Receive retiming is not available. For cases where transmit retiming is not used, a reference clock and frame signal are provided by the PHAST-12E to be used by external devices that are supplying data to the transmit Telecom Bus Interfaces. Failure inputs and outputs are provided for each Telecom Bus Interface. In the receive direction these leads signal to a downstream device that conditions for generating all 1s AIS have been detected by the PHAST-12E. In the transmit direction these leads signal to the PHAST-12E to generate Path AIS in the transmit direction.

1. Already for STM-4/STS-12 operation, the OFPs (Overhead Frame Processors) in the SFH blocks have to jointly calculate the B1 and perform frame scrambling over the entire frame. STM-4c/STS-12c, in addition, requires joint B3 calculation, etc.

ATM/PPP HANDLER BLOCKS

There are four individual ATM/PPP Handler (APH) blocks. These process the ATM/PPP data and interface to the Transmit APS Cross Connect (TACC) and Receive APS Cross Connect (RACC) blocks. When processing ATM Cells or PPP data, each ATM/PPP block provides a four-cell deep FIFO for clock separation in each direction. Cell rate decoupling is also performed where idle or unassigned cells can be generated. The header and payload bytes of the idle or unassigned cells in the transmit direction can be programmed via the microprocessor interface. A $1+X^{43}$ polynomial payload scrambler/descrambler function can be enabled via a global control bit for PPP operation.

When the ATM/PPP Handler blocks are processing PPP data they perform octet stuffing of flag characters (7E Hex) and control escape characters (7D Hex) in the transmit direction, and in the receive direction all control escape characters are destuffed. These blocks can optionally perform 16- or 32-bit Frame Check Sequence (FCS) generation/calculations on a per chiplet basis as selected via control bits. Frame delimiting and interframe flag fill are provided in the transmit direction. An optional $1+X^{43}$ polynomial scrambler/descrambler function can be enabled via a global control bit. Also a Transparent Mode of operation is possible, for applications where the "PPP in HDLC-like Framing" processing is performed external to the PHAST-12E. Registers for programming maximum and minimum allowable received frame lengths are provided. Received frames that equal or exceed the maximum programmed frame length are always discarded. Received frames that are below the minimum programmed frame length may optionally be discarded.

The ATM/PPP Handlers can work individually or in concert with each other depending upon the type of payload being processed. If individual SPEs/VCs are being processed, such as in the case of STM-4/STS-12 or four individual STM-1/STS-3c streams then the ATM/PPP blocks work individually. If an STM-4c/STS-12c is being processed, then all four ATM/PPP blocks work in parallel as one ATM/PPP Handler.

APS FUNCTIONS

APS functions are facilitated via an APS interface and the TACC/RACC blocks. These blocks consist of two 5 x 5 cross connects and two bidirectional APS interfaces, one for transmit and one for receive. The 5 x 5 cross connects handle the data from the four receive/transmit channels plus the receive/transmit APS interfaces. If a single PHAST-12E is used, 1:1, 1:2, and 1:3 APS are supported. If more than one PHAST-12E is used, such as in a multiple STM-1/STS-3c situation, a 1:N (N = 1 - 14) protection scheme can be achieved, provided that the two bidirectional APS interfaces are used. The APS function is not available when the Telecom Bus Interface is used, or when concatenated payloads such as AU-4-4c are being processed.

UTOPIA/PACKET INTERFACE

The UTOPIA Level 2/2P block interfaces to the four ATM/PPP Handler blocks. ATM cells and "PPP in HDLC-like Framing" are handled by this block. For ATM cells the UTOPIA Level 2/2P block can provide either an 8-bit or 16-bit transmit/receive UTOPIA Level 2 PHY interface. Only cell level handshaking is provided. For UTOPIA Level 2 MPHY operation, 5-bit address registers allow addresses to be assigned to the individual ATM/PPP Handler blocks. For PPP operation, the UTOPIA Level 2/2P interface is used with some additional handshaking signals to provide a 16-bit MPHY interface, called UTOPIA Level 2P, for passing PPP data in the form of programmable-size chunks. Chunk sizes can be programmed to be either 16, 32, 48, or 64 bytes in length. Indications for aborted frames and FCS errors are also provided. As is the case for ATM operation, 5-bit address registers allow addresses to be assigned to the individual ATM/PPP Handler blocks. The UTOPIA Level 2 and Level 2P interfaces can be operated at frequencies up to 50 MHz when a 16-bit wide data path is used. When an 8-bit data path is used (UTOPIA Level 2 only), the UTOPIA Level 2 interface can be operated at frequencies up to 25 MHz.

LOOPBACKS

Three loopbacks are supported in the transmit direction and two are supported in the receive direction for testing purposes. In the transmit direction either ATM cells or PPP chunks can be looped back before or after they are processed. Also, the serial TX line signal can be looped back to the RX serial line. In the RX direction, the received VC-4/VC-4-4c or C-4/C-4-4c can be looped back or the entire received SONET/SDH frame can be looped back. For more detailed information on the PHAST-12E's loopback capabilities please see "Loopbacks" on page 165.

MICROPROCESSOR INTERFACE

The PHAST-12E provides a microprocessor interface that can be selected to be compatible with the Motorola 68360 microprocessor bus type interface (QUICC bus type), or the Intel style bus. The interface can be selected to be either synchronous or asynchronous. The synchronous interface can be run with a maximum clock frequency of 33.3 MHz, while the asynchronous interface can be run with a 50 MHz clock. Polling or interrupt support, and latching of critical events, are provided to accelerate interrupt processing and reduce the burden on the microprocessor. Alarm masks are provided to enable or disable interrupts. Overflow and programmable threshold interrupts are provided on certain counters. An integrated watchdog timer is provided with a programmable period to force microprocessor accesses to terminate when a timeout occurs. Access to the various configuration registers, counters, and the control and status registers is provided via this microprocessor interface.

BOUNDARY SCAN INTERFACE

The Boundary Scan Interface uses a five-lead TAP (Test Access Port) that conforms to the IEEE 1149.1-1994 standard. This TAP provides external boundary scan to read and write the PHAST-12E input and output leads from the TAP for circuit board and component testing.

CONCLUSION

There are many features included in the PHAST-12E device that make it well suited for higher-order multiplex and multiservice applications. The integrated APS Cross Connect Circuit reduces external part counts. A wide variety of signals can be terminated, such as 4xSTS-3c, 1xSTS-12(w/4xSTS-3c-SPE), 1xSTS-12c, 1xSTM-1, 1xSTM-4, and 1xSTM-4c, thus reducing the need to use and learn multiple devices to support a variety of applications. Telecom Bus and UTOPIA Level 2/2P interfaces add a high degree of flexibility for connecting to ATM and/or PPP terminating/switching equipment and/or other path terminating equipment. On-chip clock recovery and synthesis for the serial 155 Mbit/s or 622 Mbit/s interfaces eliminates the need for additional external clock recovery circuitry. The high degree of integration of complex functional blocks into a single device makes possible reduced design and debug time and shorter time to market.

BLOCK DIAGRAM

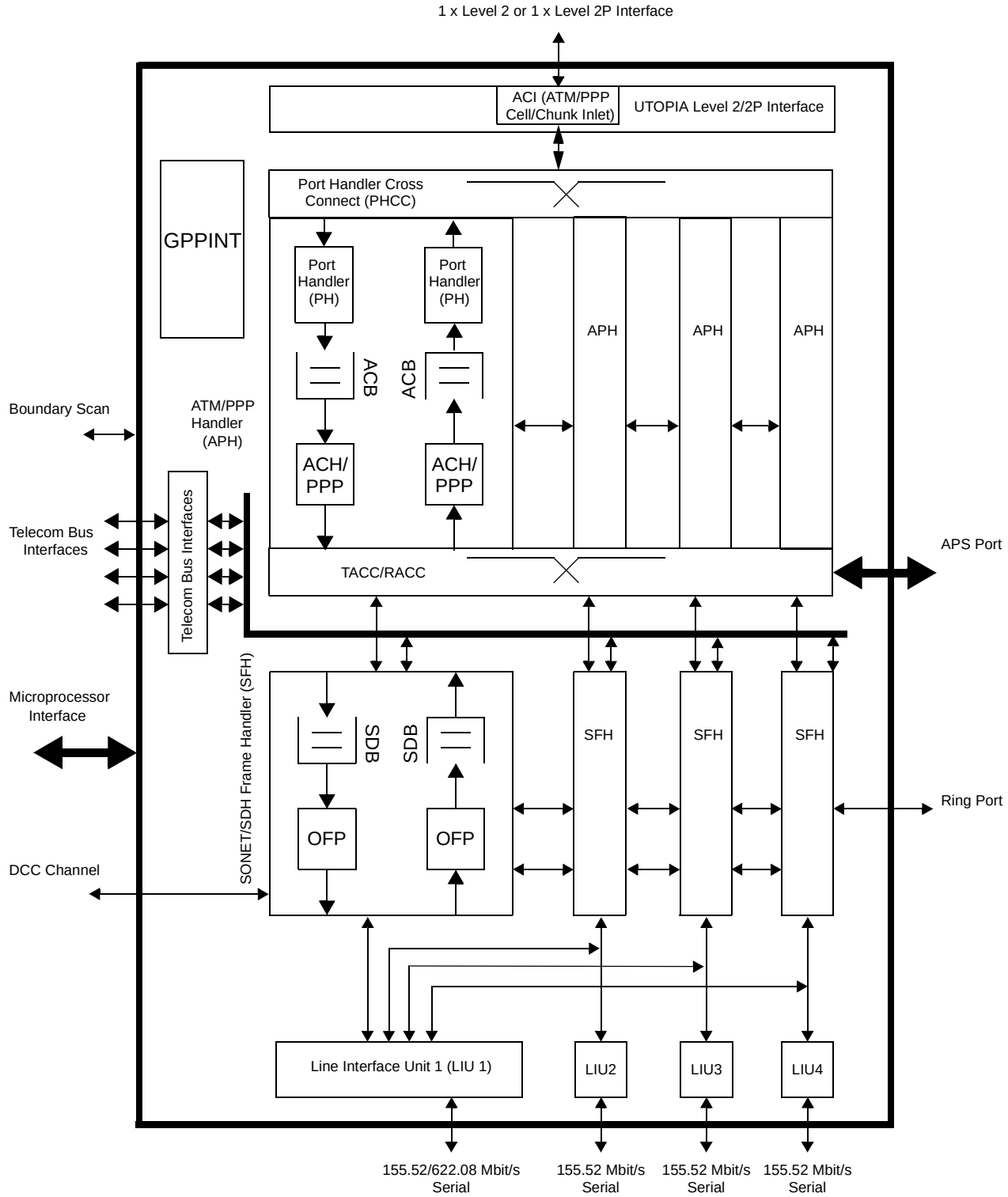


Figure 2. PHAST-12E TXC-06212 Block Diagram Showing Blocks and Chiplets

BLOCK DIAGRAM DESCRIPTION

A simplified block diagram of the PHAST-12E showing the associated chiplets is shown in Figure 2. The principal blocks that comprise the PHAST-12E are shown. These blocks, and other functional units, are listed below:

- Four Line Interface Unit (LIU) blocks, each of which contains a SIM (Serial Interface Module) sub-block (sub-blocks are also called “chiplets”). The LIUs also contain a sub-block called a PIM (Parallel Interface Module), however this sub-block is very small and it’s controls have been placed into the GPPINT (General Purpose Processing Interface) section of the memory map.
- Four SONET/SDH Frame Handler (SFH) blocks, each of which consists of the SDB (SONET/SDH Data Buffer) and transmit/receive OFP (Overhead Frame Processor) chiplets.
- Four ATM/PPP Handler (APH) blocks, each of which consists of the following chiplets: ACB (ATM Cell / PPP Chunk Buffer) and ACH/PPP (ATM Cell Handler / PPP Handler) which performs HDLC-like encapsulation, PPP over SONET/SDH and ATM cell processing, Port Handler (PH), which provide control/monitoring of the ACBs, and a Port Handler Cross Connect (PHCC) which provides RX to TX VC-4 loopbacks with the ability to perform time slot interchange of VC-4s.
- Transmit/Receive APS Cross Connect (TACC/RACC) block, which is a part of the APH, and APS port.
- UTOPIA Interface block, which contains the ACI (ATM/PPP Cell/Chunk Inlet) sub-block. The ACI sub-block is used to control the addresses of the PHYs during multi PHY mode operation, UTOPIA bus parity generation and checking, and counting of ATM cells / PPP chunks that pass through the UTOPIA Level 2/2P interface.
- Transmit/receive Telecom Bus Interface block.
- Transmit/receive DCC Port (included in SFH block).
- Microprocessor Interface.
- Transmit/receive Ring Port (included in SFH block).
- Boundary Scan Port.

The PHAST-12E can extract ATM/PPP traffic from up to four individual STM-1/STS-3c streams, or a single STM-4/4c or STS-12/12c stream and supply them to its receive UTOPIA Level 2 or Level 2P interface. Conversely, the PHAST-12E can accept ATM/PPP traffic on its transmit UTOPIA Level 2 or Level 2P interface and map the ATM/PPP streams into up to four individual STM-1/STS-3c streams or a single STM-4/4c or STS-12/12c stream. Other payload types can be handled via the transmit and receive Telecom Bus Interfaces.

A high level discussion of the features of the various blocks is given below.

GENERAL DATA FLOW

TX Data Flow

This section describes the data flow through the PHAST-12E in the TX direction for the various modes of operation.

Figure 3 shows the TX data flow in 4xSTM-1/STS-3c Mode.

- TX TDM data can be accepted by the first four Telecom Bus (TB) blocks and ATM plus PPP data can be accepted by the UTOPIA Level 2/2P Interface. Each APH block can be individually configured to accept ATM or PPP data.
- The TB and APH blocks are shown as individual blocks to indicate that they operate separately of each other.
- Four separate C-4 payloads are available for transporting data. Each SFH block can process either an individual C-4 from an APH block or a VC-4/AU-4 from the Telecom Bus Interface; thus making it possible to simultaneously support ATM, PPP, and TDM streams or any combination thereof.
- The SFH blocks perform the TOH, POH (for the ATM/PPP streams only), and pointer processing functions to create four individual STM-1/STS-3c frames each of which contains an AU-4. The four SFH blocks are shown as individual blocks to indicate that they each work independently of the other SFH blocks.
- The four LIU perform the parallel to serial conversion of the data streams at 155.52 Mbit/s to create four independent STM-1/STS-3c streams.

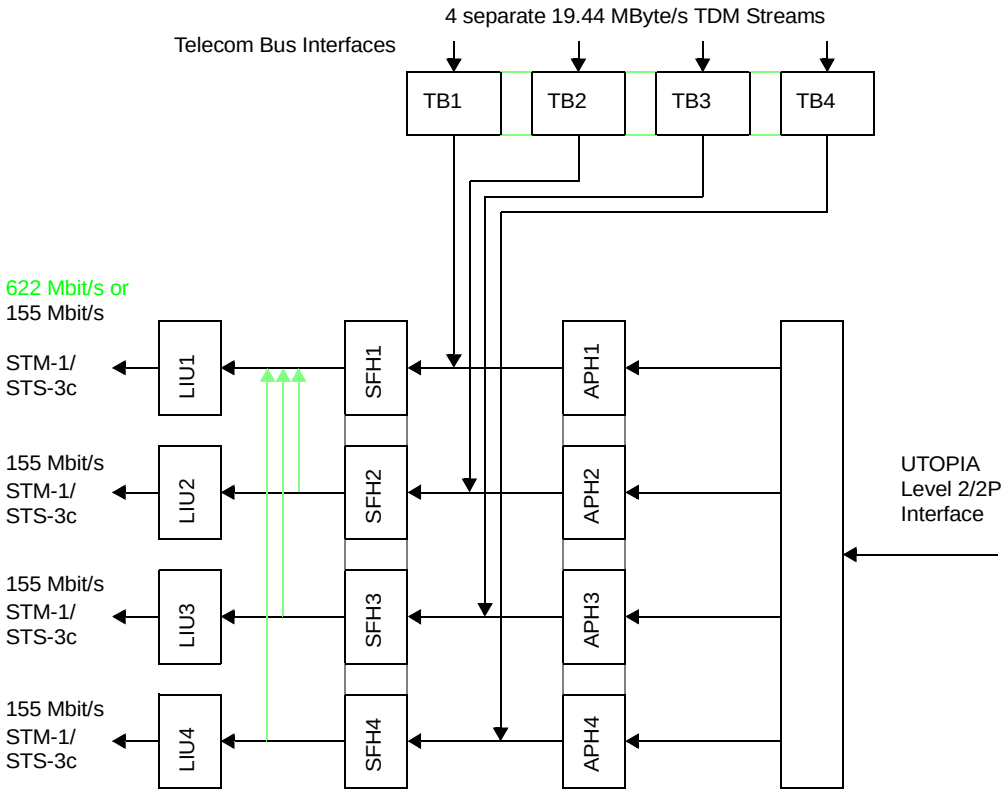


Figure 3. TX Data Flow in 4xSTM-1/STS-3c Mode

Figure 4 shows the TX data flow in 1xSTM-4/STS-12 Mode.

- TX TDM data can be accepted by the first four Telecom Bus (TB) blocks and ATM plus PPP data can be accepted by the UTOPIA Level 2/2P Interface. Each APH block can be individually configured to accept ATM or PPP data.
- The TB and APH blocks are shown as individual blocks to indicate that they operate separately of each other.
- Four separate C-4 payloads are available for transporting data. Each SFH block can process either an individual C-4 from an APH block or a VC-4/AU-4 from the Telecom Bus Interface; thus making it possible to simultaneously support ATM, PPP, and TDM streams or any combination thereof.
- The SFH blocks perform the TOH, POH (for the ATM/PPP streams only), and pointer processing functions to create an STM-4/STS-12 frame, which contains four AU-4s. The four SFH blocks are shown connected together to indicate that they work together when processing the TOH and performing the byte interleaving of the four constituent AU-4s to create a single STM-4/STS-12 frame. If it is desired to have the STS-12 stream carry twelve AU-3s instead of four AU-4s, then the Telecom Bus interfaces can be configured to accept AU-4s which actually consist of three AU-3s, by turning off the TX Retiming function of the Transmit Telecom Bus.
- The first LIU performs the parallel to serial conversion of the data stream at 622.08 Mbit/s.

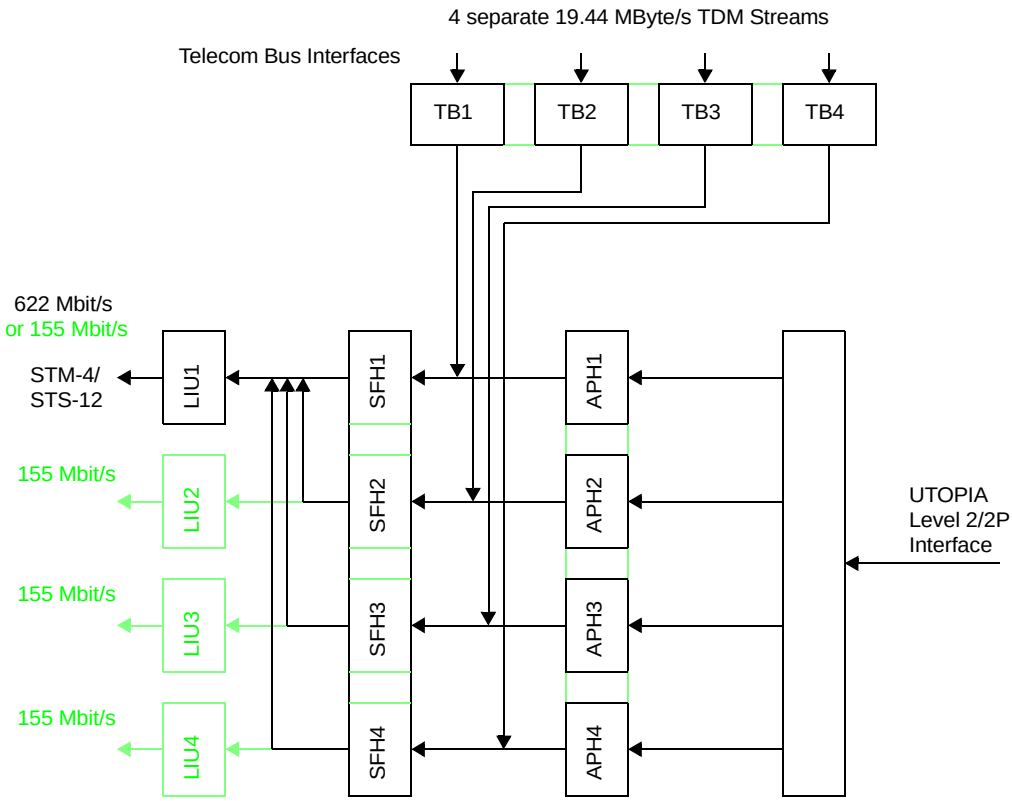


Figure 4. TX Data Flow in 1xSTM-4/STS-12 Mode

Figure 5 shows the TX data flow in 1xSTM-4c/STS-12c Mode.

- The UTOPIA Level 2/2P interface operates in Single PHY mode because only one C-4-4c is being processed. The four Telecom Bus Interfaces act together as one large Telecom Bus interface. Likewise the APH and SFH blocks act together as one large APH block and one large SFH block respectively. Either the data from the TB or the APH can be applied to the SFH block but not both.
- The SFH block can process either an individual C-4-4c from the APH block or a VC-4-4c/AU-4-4c from the Telecom Bus Interface.
- The SFH block performs the TOH, POH (for the ATM/PPP stream only), and pointer processing functions to create an STM-4c/STS-12c frame. The SFH blocks are shown connected together to indicate that they work together when processing the TOH and the AU-4-4c to create a single STM-4c/STS-12c frame.
- The first LIU performs the parallel to serial conversion of the data stream at 622.08 Mbit/s.

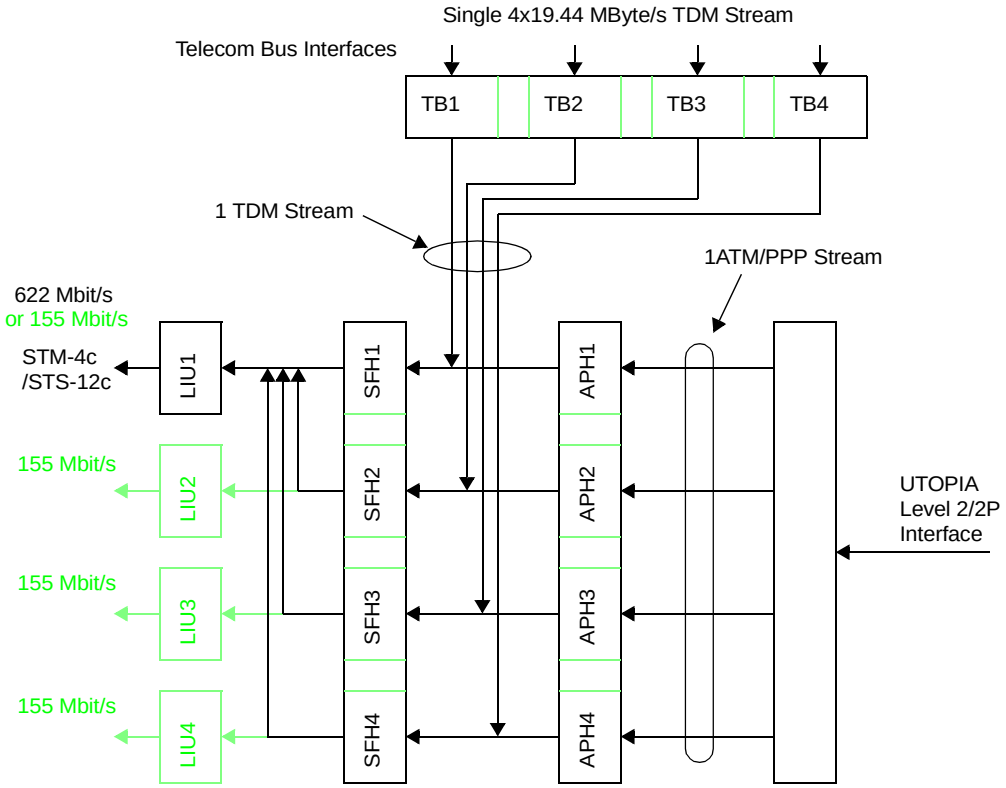


Figure 5. TX Data Flow in 1xSTM-4c/STS-12c Mode

RX Data Flow

This section describes the data flow through the PHAST-12E in the RX direction for the various modes of operation.

Figure 6 shows the RX data flow in 4xSTM-1/STS-3c Mode.

- The four individual LIUs perform clock and data recovery on the four individual STM-1/STS-3c streams. They also perform the serial to parallel conversion of the received data.
- The four individual SFH blocks perform TOH, POH (only for the VC-4s that are terminated into the APH blocks), and pointer processing functions.
- Each RX STM-1/STS-3c frame in its entirety are passed to its corresponding RX Telecom Bus. The C-4 data is passed to its APH block. Each APH block can be configured to support either ATM or PPP data. All four of the RX Telecom Busses can be running at the same time while all PHY ports of the UTOPIA Level 2/2P port can be outputting cell and chunk data from the APH blocks; thus making it possible to simultaneously support ATM, PPP, and TDM streams or any combination thereof.
- The TB and APH blocks are shown as individual blocks to indicate that they operate separately of each other.

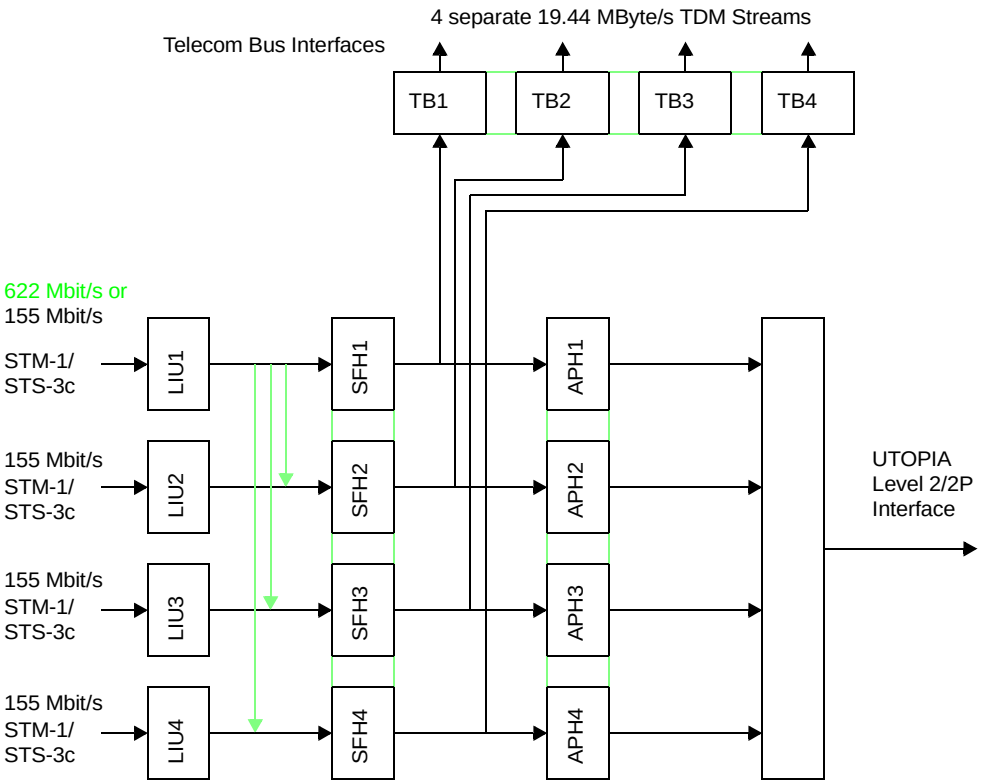


Figure 6. RX Data Flow in 4xSTM-1/STS-3c Mode

Figure 7 shows the RX data flow in 1xSTM-4/STS-12 Mode.

- LIU 1 performs clock and data recovery on the STM-4/STS-12 stream. It also performs the serial to parallel conversion of the received data.
- The four individual SFH blocks perform TOH, POH (only for the VC-4s that are terminated into the APH blocks), and pointer processing functions. The four SFH blocks are shown as one block because they work together to process the TOH and they work separately to process the four AU-4s.
- The STM-4/STS-12 frame is byte de-interleaved and passed to their corresponding TBs without modification. The C-4 data is extracted from each AU-4 and is passed to its APH block. Each APH block can be configured to support either ATM or PPP data. All four of the RX Telecom Busses can be running at the same time while all PHY ports of the UTOPIA Level 2/2P port can be outputting cell and chunk data from the APH blocks; thus making it possible to simultaneously support ATM, PPP, and TDM streams or any combination thereof.
- The TB and APH blocks are shown as individual blocks to indicate that they operate separately of each other.

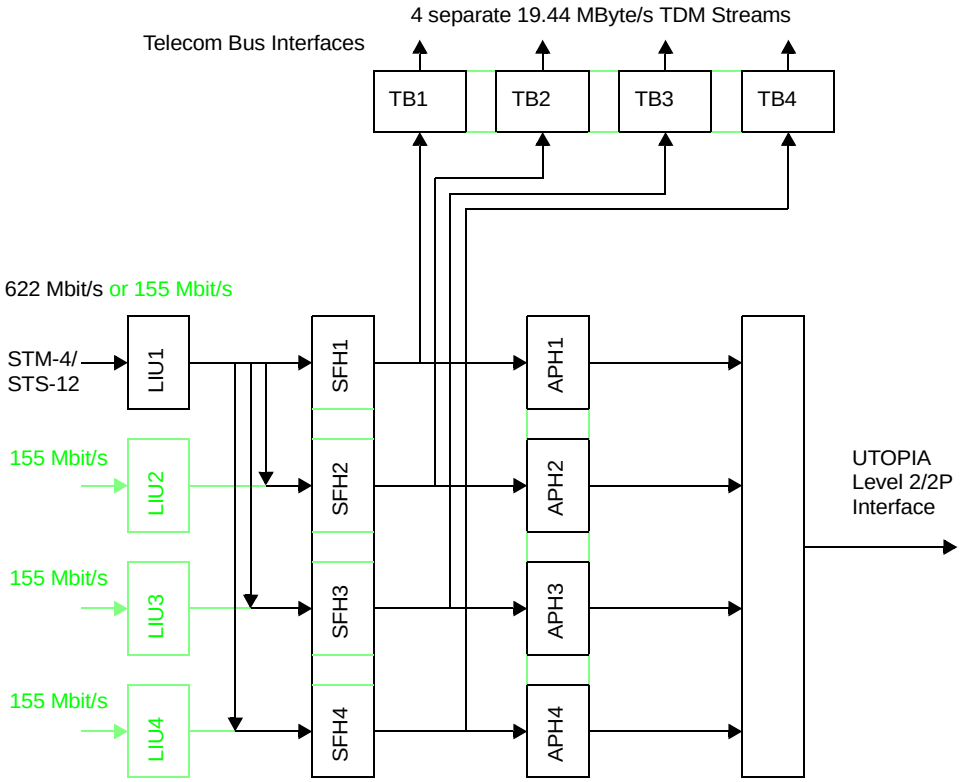


Figure 7. RX Data Flow in 1xSTM-4/STS-12 Mode

Figure 8 shows the RX data flow in 1xSTM-4c/STS-12c Mode.

- LIU 1 performs clock and data recovery on the STM-4c/STS-12c stream. It also performs the serial to parallel conversion of the received data.
- The SFH blocks, the APH blocks, and the Telecom Bus blocks are each shown as one large SFH block, APH block, and Telecom Bus block to show that they work together to process one STM-4c/STS-12c stream.
- The SFH block performs TOH, POH (only if the VC-4-4c is terminated into the APH block), and pointer processing functions.
- The STM-4c/STS-12c frame is byte de-interleaved and passed to their corresponding TBs without modification. The entire STM-4c/STS-12c frame appears at the output of the single 4x19.44MByte/s telecom bus output. The C-4-4c data, which is extracted from the AU-4-4c is passed to the APH block. The APH block can be configured to support either ATM data or PPP data. The RX Telecom Bus can be running at the same time while the UTOPIA Level 2/2P port can be outputting cell or chunk data from the APH block.
- The UTOPIA Level 2/2P interface operates in Single PHY mode because only one C-4-4c is being processed.

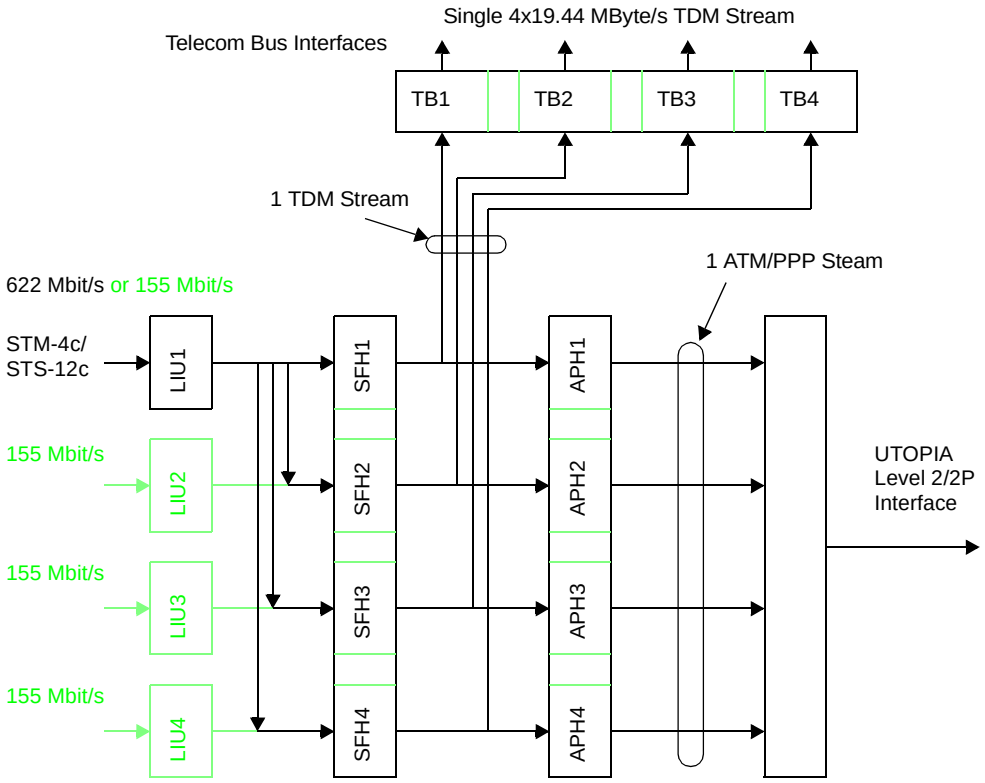


Figure 8. RX Data Flow in 1xSTM-4c/STS-12c Mode

When operating in STM-4/STM-4c/STS-12/STS-12c mode, the PHAST-12E performs a 1 to 4 demux of the data stream and can output the separated data onto the receive Telecom Buses or to the APH blocks. Since only one K2 byte is defined in an STM-4/STM-4c/STS-12/STS-12c frame, all of the Telecom Buses except the first will output “dummy” K2 bytes which may have arbitrary non-zero values. If any of the K2 bytes happens to have “111” in its three least significant bits then another device connected to the Telecom Bus, which is unable to ignore the TOH bytes, could interpret this value as a line AIS condition. Simple “glue” logic should be interposed between the PHAST-12E and any such devices on the Telecom Buses to set the “dummy” K2 bytes to 00 H. This issue does not occur if the POP-12 is used to process the POH.

LINE INTERFACES

The Line Interface section of the PHAST-12E device performs the adaptation between the external SONET/SDH signals and the internal SFH blocks.

TX Line Interfaces

The transmit line interface of the PHAST-12E consists of four Line Interface Units (LIUs). All four LIUs provide clock synthesis for 155.52 Mbit/s serial operation with the added feature that LIU 1 can also perform clock synthesis for 622.08 Mbit/s serial operation.

Clock synthesis, is provided in the transmit direction for the serial interfaces for sourcing data at the serial transmit outputs. One reference clock with selectable frequencies of 19.44 MHz, 38.88 MHz, 51.84 MHz, or 77.76 MHz is used to provide the timebase for the Transmit Clock Synthesis (TCS) circuit. Additionally a timing loopback function is provided, where one of the RX recovered clocks can be taken as the timebase for the transmit SONET/SDH streams. See “Options for Loop Timing” on page 138 for details.

RX Line Interfaces

The receive line interface of the PHAST-12E consists of four LIUs. All four LIUs provide clock recovery for 155.52 Mbit/s serial operation with the added feature that LIU 1 can also perform clock recovery for 622.08 Mbit/s serial operation.

The receive line interface of the PHAST-12E provides several options. If four individual STM-1/STS-3c streams are to be processed, the four receive paths act independently and four 155.52 Mbit/s streams can be input to the PHAST-12E. If an STM-4/STS-12 signal is to be processed, the four individual AU-4s are byte demuxed from the 622.08 Mbit/s serial stream applied to LIU 1, and are passed to their corresponding SFH blocks where they are processed. Each of the four receive paths is processing a single payload stream. When a STM-4c/STS-12c signal is to be processed, the peer blocks in the four receive paths operate together as one large block. In this case, if the Telecom Bus were being used, the four receive Telecom Bus interfaces would act as one large Telecom Bus with a 32-bit wide datapath. As mentioned above, clock recovery is provided in the receive direction for the serial interfaces.

SFH - SONET/SDH FRAME HANDLER

The SFH blocks contain the SONET/SDH Data Buffers (SDBs), which consist of 63-byte deep FIFOs in the transmit direction and 7-byte deep FIFOs in the receive direction. There is one SDB per SFH block. The purpose of the SDB is to facilitate the transfer of data between the APH or Telecom Bus and the SFH blocks, which operate off of different clock islands. Figure 57 on page 156 and Figure 58 on page 157 indicate conditions and their effects upon what gets written to the RX SDB FIFOs. The SFH blocks also contain the Overhead Frame Processor (OFP) chiplets, which process the RS, MS and Path Overhead bytes. POH processing is not performed on the SPEs/VCs that are terminated into the Telecom Bus interface.

R/TACC - RECEIVE/TRANSMIT APS CROSS CONNECT

The TX and RX APS Cross Connect blocks (TACC and RACC) consist of two separate 5 x 5 cross connects and two separate 9-bit wide bidirectional APS Interfaces. Command of the bridging is accomplished through two microprocessor-accessible control registers. Upon power-up, each APH (ATM/PPP Handler) block is bridged to its corresponding SFH. In the RX direction, when a switch is performed, the output of the SFH (typically a C-4 signal) is bridged to either, the selected APH block or the RX APS port. If desired, the C-4 data from an RX SFH block in another PHAST-12E can instead be accepted at the RX APS port and applied to an RX APH block. Additionally, a VC-4 can be passed across the RX APS interface and be received at another PHAST-12E's RX APS interface, and then passed to the PHCC to be time slot interchanged, and sent out in the transmit SONET/SDH line. In the TX direction, when a bridge is performed, the output of the APH (which is a C-4 signal) is bridged to either, the selected SFH block or the TX APS port. If desired, C-4 data from a TX APH block in another PHAST-12E can instead be accepted at the TX APS port and applied to a TX SFH block.

1:1-3 APS

In single device operation, there can be three working channels and one protection channel. If a failure occurs on one of the working channels, the TACC is configured to bridge the output of the APH block for the failing line over to the protection channel's SFH. The RACC is configured to bridge the output of the SFH of the protection channel over to the APH of the working channel. This operation is shown in Figure 9 and Figure 10 below.

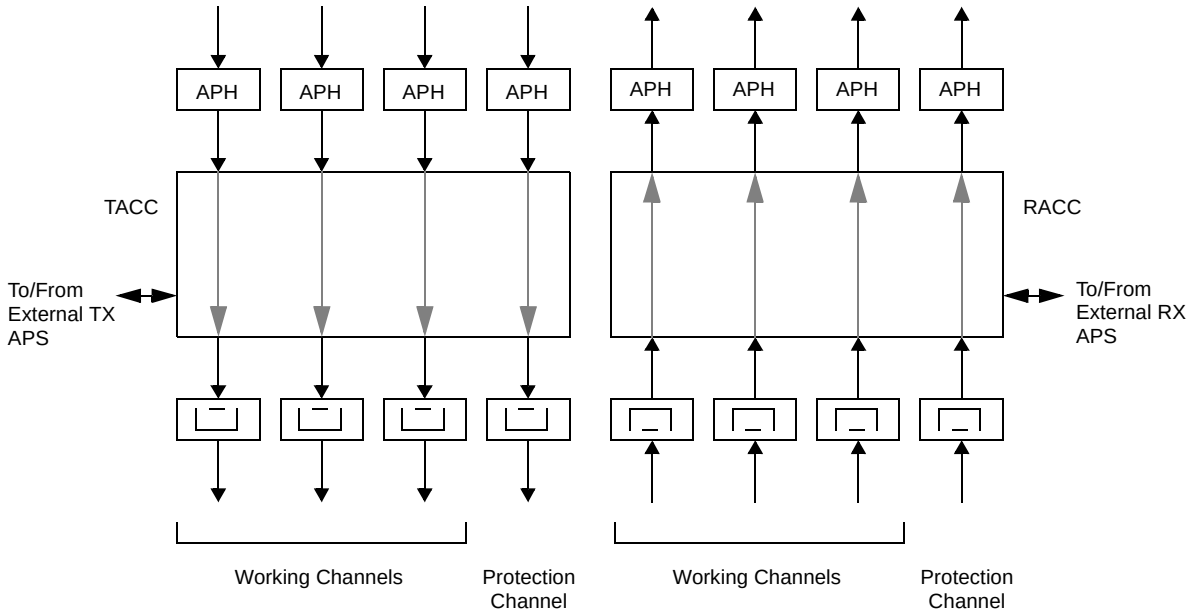


Figure 9. 1:3 Protection with one PHAST-12E Device Showing Normal Operation

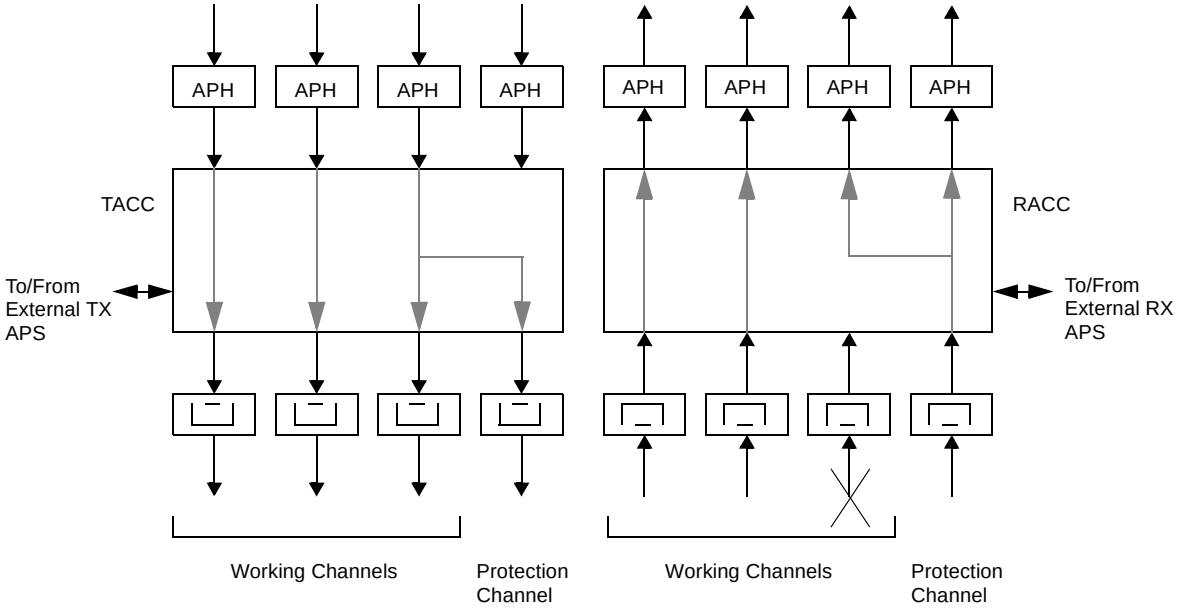


Figure 10. 1:3 Protection with one PHAST-12E Device Showing Switch and Bridge to Protection Channel

1:N APS

As shown in Figure 9 and Figure 10 above, the External Transmit and Receive APS Interfaces do not need to be used for the 1:3 protection scheme. However, if multiple PHAST-12E devices are used then the External Transmit APS Interfaces of the PHAST-12Es can be connected together and similarly the External Receive APS Interfaces of the PHAST-12Es can be connected together. In this way a 1:N protection scheme can be achieved. N can range from 1 - 14 depending on the number of PHAST-12E devices used. Figure 11 and Figure 12 below show a 1:N APS scheme when there is no failure and when there is a failure, respectively.

The APS functionality is not to be used when STM-4c or STS-12C payloads are being processed or when the Telecom Bus interface is being used. Only when ATM and PPP data in individual STM-1/STS-3c payloads are processed can the TACC and RACC be used, since the external APS port can handle data from only one C-4/STS-3c-SPE payload stream at a time. However, the TACC/RACC are still operational in STM-4 and STS-12 modes, but only one C-4/STS-3c-SPE payload can be bridged.

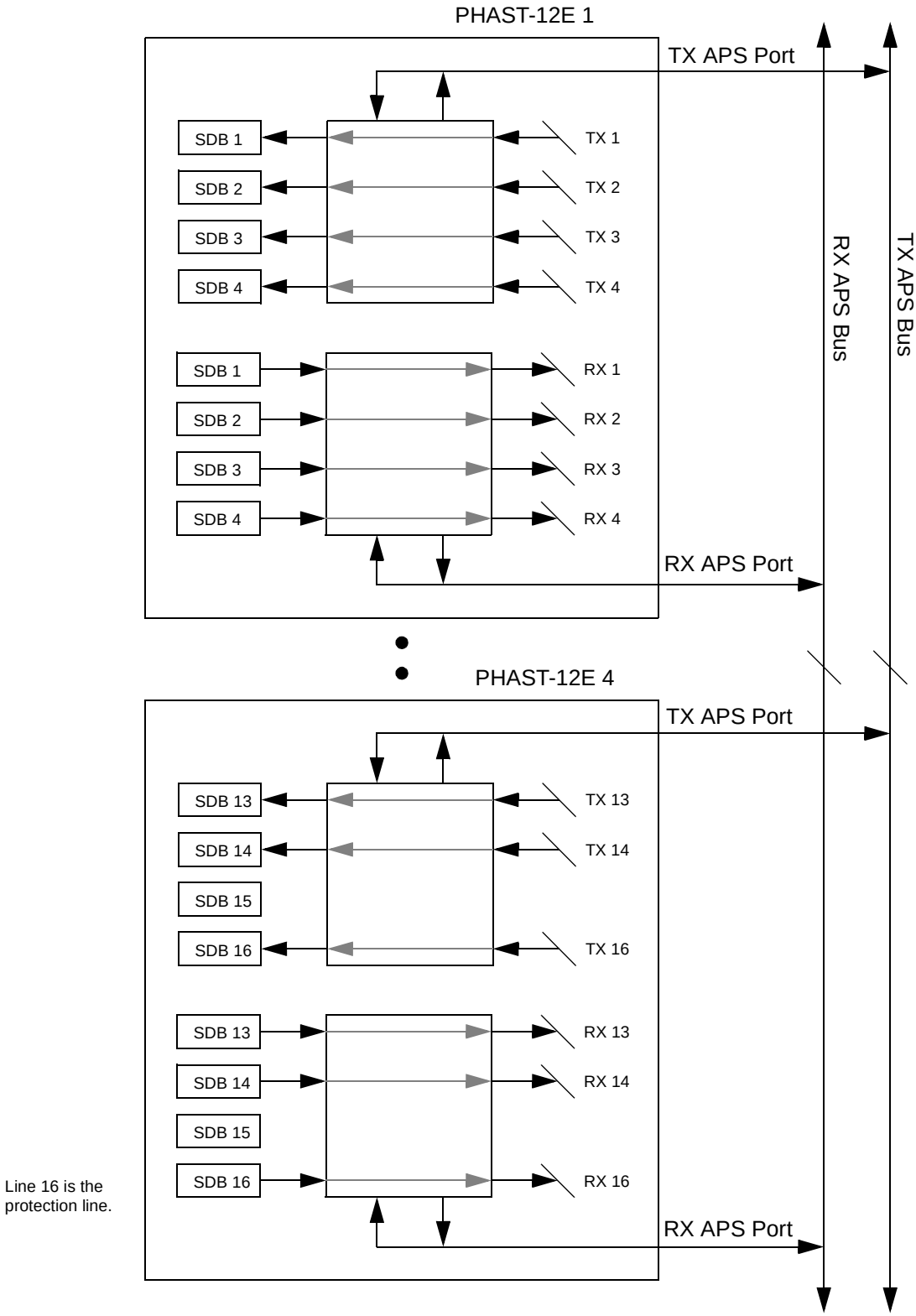


Figure 11. 1:N APS Scheme (no failure, protection line inactive)

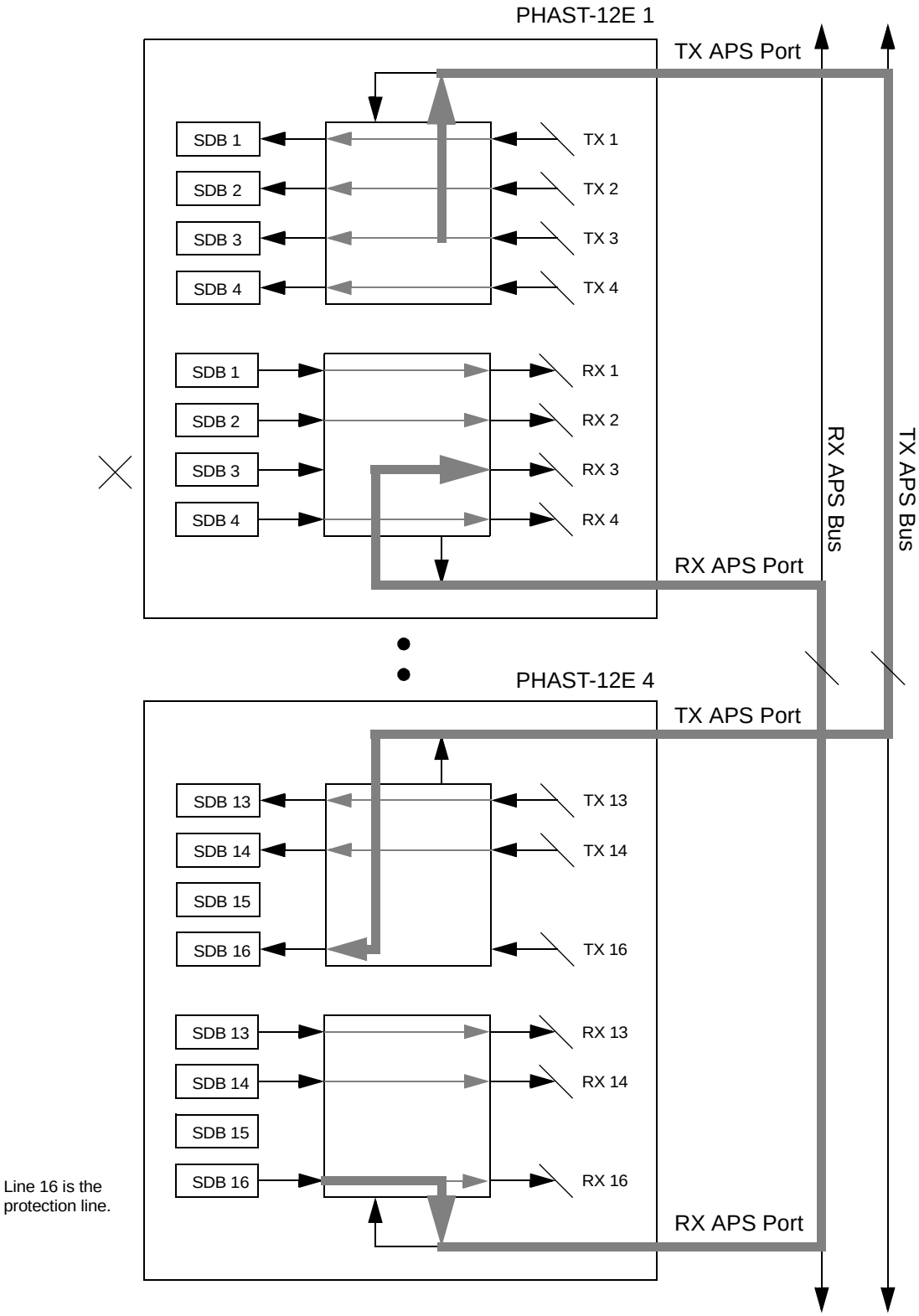


Figure 12. 1:N APS Scheme (failure, protection line active)

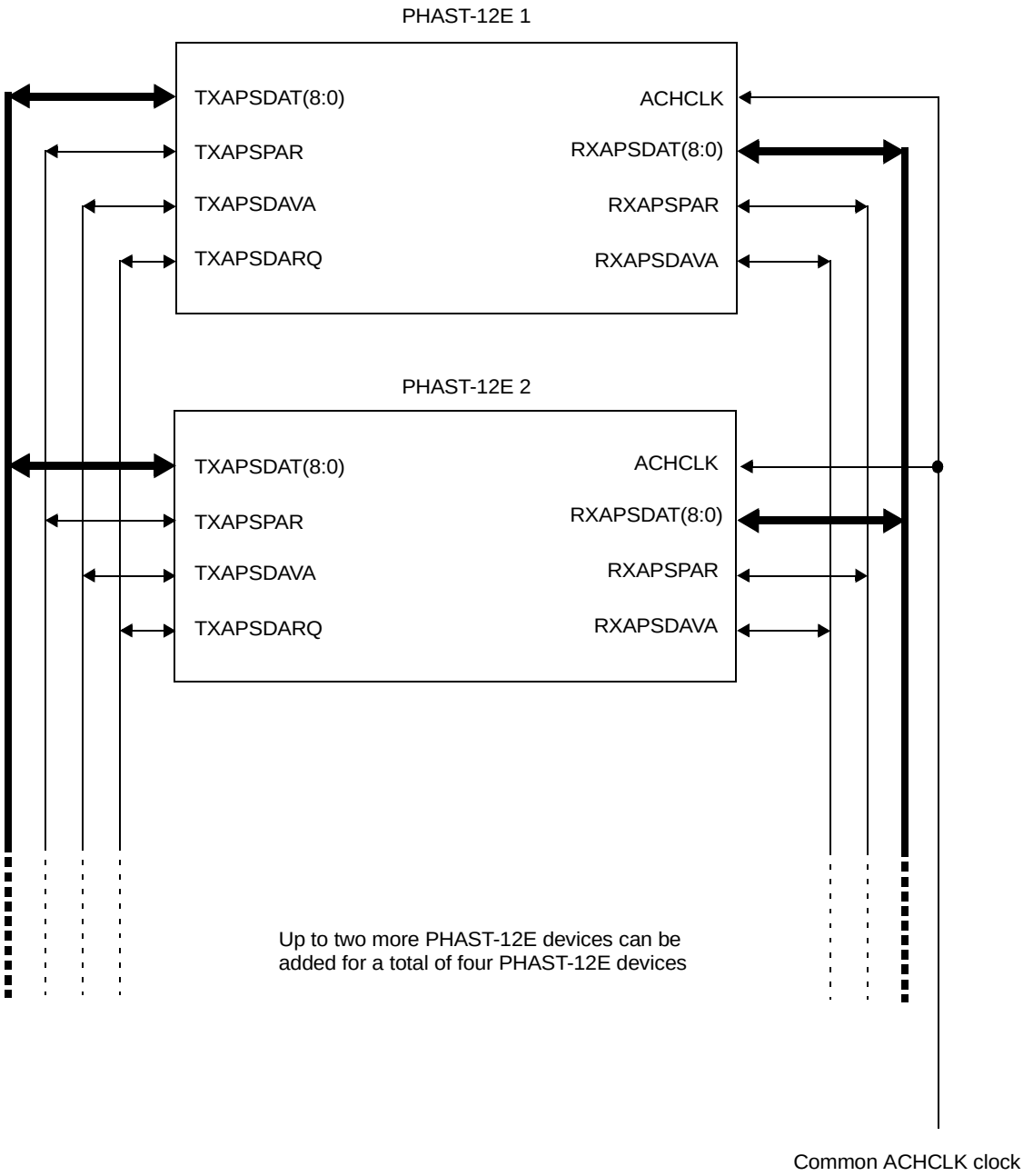


Figure 13. APS Interface Connection for Multi-device Operation

Figure 13 above shows how the APS interfaces between PHAST-12E devices should be connected. It should be noted that a common ACHCLK clock is required for all PHAST-12E devices if the APS ports are used. The skew between the ACHCLK clocks should be taken into consideration to ensure set-up and hold times are met at the interfaces that are inputs. In multi-device operation where the PHAST-12Es have different transmit reference clocks, pointer processing will need to be turned on and pointer adjustments in the transmit direction will occur. Pointer processing still needs to be enabled, even if all of the PHAST-12E devices have the same transmit reference clock.

APH - ATM/PPP HANDLER

Each of the four APH blocks contains an ACH (ATM Cell Handler) chiplet and a PPP (Point to Point Protocol) chiplet for processing ATM Cells and PPP frames. Each APH block also contains an ACB (ATM/PPP Cell/Chunk Buffer) and a PH (Port Handler) chiplet and a Port Handler Cross Connect (PHCC) which can handle VC-4s, depending on the mode of operation. The PH chiplet provides control and monitoring of the ACB FIFOs.

The APH is designed to process either up to four individual 155.52 Mbit/s ATM or PPP streams (i.e., STM-4/STS-12 or 4 x STM-1/STS-3c) or one single 622.08 Mbit/s ATM or PPP stream (i.e., STM-4c/STS-12c). It should be noted that an STM-4/STS-12 looks like four individual STM-1/STS-3c streams to the APH blocks.

When processing PPP Frame payloads the PPP chiplet performs the functions indicated in [RFC2615] and [RFC1662] for octet synchronous mapping of PPP into HDLC-like Framing for transmission over SONET/SDH. In addition to those functions, the PPP chiplet formats the PPP Frame payloads for insertion into the ATM Cell /PPP Chunk Buffer (ACB) as well as accepting PPP Frame payloads from the ACB. An optional self-synchronous scrambler/descrambler with polynomial $1+X^{43}$ is provided for scrambling the HDLC-like Frame stream. PPP Frame data which is leaving the APH in the transmit direction or entering the APH in the receive direction can be scrambled/descrambled under software control.

The ACH chiplet performs the Transmission Convergence Sublayer Functionality for ATM Cell payloads, such as HEC generation/verification, cell scrambling/descrambling, as well as HEC-based Cell Delineation.

The ACB is a four ATM cell-deep FIFO. This buffer is used to accrue/accept complete cells/chunks in ATM/PPP processing mode. This is because the PHAST-12E is a PHY layer device and only does cell/chunk level handshaking for ATM/PPP applications and therefore needs to be able to transfer entire ATM Cells or PPP Chunks at a time. When an STM-4c or STS-12c is processed, the ACB chiplets work in parallel to create one large FIFO in the transmit direction and one large FIFO in the receive direction.

NOTE: The ACB FIFO can be reset by: 1) Local reset of the corresponding ACH chiplet in STM-1 or STM-4 mode; 2) Local reset of ACH CHIPLET #1 in STM-4C mode.

PORT HANDLER CROSS CONNECT CAPABILITY

The PHAST-12E also supports cross connecting for ATM, PPP, and TDM payloads. The PHAST-12E allows individual RX ATM/PPP/TDM VC-4 (for 4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes) to be looped back and time slot interchanged to the TX direction while other ATM/PPP/TDM streams are interfaced to the UTOPIA MPHY or Telecom Bus interfaces. When a payload is cross connected through an APH block, the ATM and PPP processing is disabled and the VC-4 is passed through and cross connected. Pointer processing in the TX SFH blocks must be enabled. The CLAV/PAVO signals for the PHYs that are being cross connected are not active.

NOTE: This cross connect feature will only work for blocks that are configured for ATM mode. However, this is not a problem for cross connecting other payload types like PPP and TDM as the VC-4s that are being cross connected are simply passed through the APH blocks when being cross connected. This means that any traffic type can be cross connected. Also note that VC-4 streams that are terminated into the UTOPIA interfaces can contain ATM or PPP data.

Figure 14 below shows an example of VC-4s being cross connected. TX APH blocks 1 and 2 in Figure 14 should be configured via the PPPGP1 register to process ATM in APH block 1 and PPP in APH block 2, while TX APH blocks 3 and 4 should be configured to be ATM to allow the VC-4 cross connect function to work. In this case the traffic on TX APH blocks 3 and 4 can be anything (ATM, PPP, or TDM). RX APH blocks 1 and 3 in Figure 14 can be configured via the PPPGP1 register to be ATM on APH block 1 and PPP on APH block 3, while RX APH blocks 2 and 4 should be configured to be ATM to allow the VC-4 cross connect function to work. In this case the traffic on RX APH blocks 2 and 4 can be anything (ATM, PPP, or TDM). This cross connect capability can also be used when data is terminated into the Telecom Bus interface instead of the UTOPIA interface.

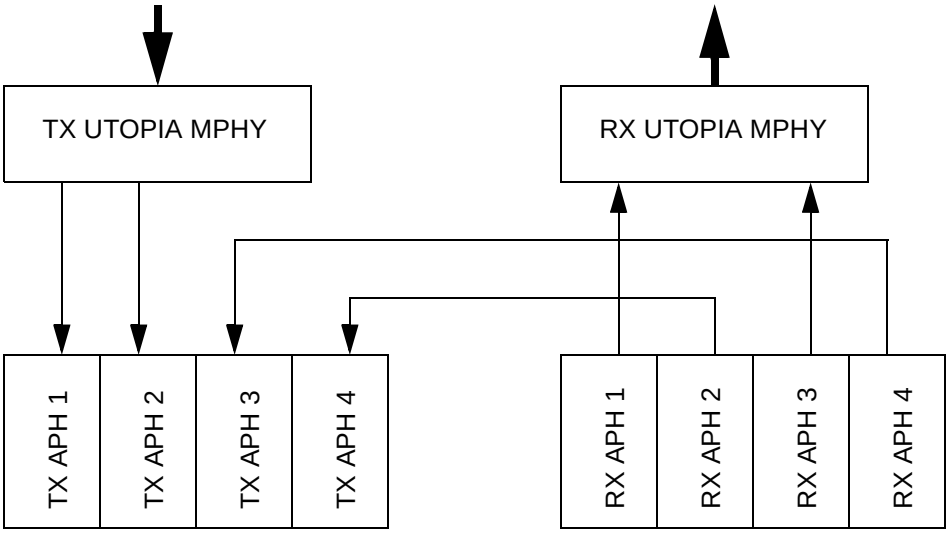


Figure 14. Example of ATM/PPP Cross Connection Feature

In order to achieve this the PPPGP1, GContTx, GContRx, PHTXGP1, PHTXGP2, PHRXGP, and OFPTXGP registers need to be set accordingly. The GContTx and GContRx registers indicate which mode the blocks work in (i.e., ATM/PPP, Telecom Bus or Cross Connect). The PHTXGP1/2 and PHRXGP registers indicate how the data is cross connected. The OFPTXGP register indicates (among other things) if pointer processing is enabled in the corresponding TX SFH block. To achieve the set-up above, the settings shown in the following table are required:

Control Bits	Setting (binary)	Comments
RxPPP(3:0),TxPPP(3:0)	00100100	RX PH chiplets 2 and 4, and TX PH chiplets 3 and 4, are set to ATM mode so that the cross connect feature can be enabled for their corresponding channels; even though those chiplets are set to ATM mode, when the cross connecting function is enabled, VC-4s are being cross connected, and thus, the traffic type (ATM, PPP, or TDM) is transparent to those chiplets.
GContTx1(1:0)	00	TX APH block 1 set to ATM/PPP Mode.
GContTx2(1:0)	00	TX APH block 2 set to ATM/PPP Mode.
GContTx3(1:0)	01	TX APH block 3 set to cross connect mode.
GContTx4(1:0)	01	TX APH block 4 set to cross connect mode.
GContRx1(1:0)	00	RX APH block 1 set to ATM/PPP Mode.
GContRx2(1:0)	01	RX APH block 2 set to cross connect mode.
GContRx3(1:0)	00	RX APH block 3 set to ATM/PPP Mode.
GContRx4(1:0)	01	RX APH block 4 set to cross connect mode.
PHT1(2:0)	001	TX APH block 1 gets its data from the TX UTOPIA Level 2/2P interface.

Control Bits	Setting (binary)	Comments
PHT2(2:0)	001	TX APH block 2 gets its data from the TX UTOPIA Level 2/2P interface.
PHT3(2:0)	111	TX APH block 3 gets its data from RX APH block 4.
PHT4(2:0)	101	TX APH block 4 gets its data from RX APH block 2.
PHR1(1:0)	01	RX APH block 1 sends its data from the RX UTOPIA Level 2/2P interface.
PHR2(1:0)	10	RX APH block 2 sends its data to the TX APH block that is requesting it.
PHR3(1:0)	01	RX APH block 3 sends its data from the RX UTOPIA Level 2/2P interface.
PHR4(1:0)	10	RX APH block 4 sends its data to the TX APH block that is requesting it.
PtrProc(3:0)	xx11	Pointer processing is turned on for TX SFH blocks 3 and 4. Pointer processing can either be enabled or disabled for TX SFH blocks 1 and 2.

Please note that if cross connects are changed “on the fly”, then the corresponding TX ACH chiplets that are involved in the change, need to have a local reset applied via their address offset xx30 H.

UTOPIA LEVEL 2/2P INTERFACE

Some additional but brief comments on the interface are provided for ATM and PPP mode operation. The “P” in UTOPIA Level 2P indicates that the PHAST-12E uses the UTOPIA interface with some added signals and modifications for transferring PPP data between the PHAST-12E and a PPP processing device, which will be called the “ATM Emulation Layer”. Each APH block is associated with a PHY port in the UTOPIA Level 2/2P interface. The UTOPIA interface can handle either ATM cells or PPP chunks at the same time. When a PHY is selected whose APH is configured to process ATM cells, UTOPIA Level 2 handshaking is performed for the cell transfer. When another PHY is selected, whose APH is configured to process PPP, UTOPIA Level 2P handshaking is performed. The UTOPIA Level 2P handshaking is described in “TX PPP Data Transfer” on page 37 and “RX PPP Data Transfer” on page 38.

ATM Mode

It should be noted that, since the PHAST-12E is a PHY layer device, no ATM switching is performed. The UTOPIA level 2 interface is compliant with [UL2v1]. When the UTOPIA level 2 interface is selected, up to four C-4s, or a single C-4-4c can be processed in a single PHAST-12E device. When 4xSTM-1/STS-3c or 1xSTM-4/STS-12 is processed, each of the four sets of transmit and receive APH blocks is considered to be a PHY. There are eight registers in the PHAST-12E (one for each transmit and receive APH block) that are used to define a unique 5-bit address to each of the PHYs. When processing an STM-4c/STS-12c stream, the UTOPIA Level 2 interface is used in single PHY mode. In this case, all of the transmit blocks operate in parallel and all of the receive blocks operate in parallel to form two large blocks, or PHYs, capable of processing the STM-4c/STS-12c payloads. Furthermore, the transmit and receive address leads of the UTOPIA Level 2 interface should be strapped low to support the single large PHY.

PPP Mode

When an APH block is configured to process PPP payloads, the UTOPIA Level 2P features are called into play when the corresponding PHY is selected. The UTOPIA Level 2P interface is a Multi-PHY (MPHY) interface with the following signals that are shared with their UTOPIA counterparts:

- TXUCLK - transmit clock input.
- TXUADDR(4:0) - 5-bit transmit MPHY address input
- TPAVO - transmit chunk available output signal. There are three other CLAV signals for multi-PHY ATM applications.
- TXSOC - transmit start of chunk input signal.
- TXUDATA(15:0) - transmit data input.
- $\overline{\text{TXENB}}$ - transmit enable input. This signal is active low.
- TXPRTY - Transmit parity input.
- RXUCLK - receive clock input.
- RXUADDR(4:0) - 5-bit receive MPHY address input
- RPAVO - receive chunk available output signal. There are three other CLAV signals for multi-PHY ATM applications.
- RXSOC - receive start of chunk input signal.
- RXUDATA(15:0) - receive data output.
- $\overline{\text{RXENB}}$ - receive enable input. This signal is active low.
- RXPRTY - receive parity output.

A number of additional signals are provided for frame delineation purposes:

- TXEOFI - transmit End of Frame input.
- TXSOFI - transmit Start of Frame input.
- TXABTO - transmit Abort output.
- TXMSI - transmit Most Significant Byte input.
- RXEOFO - receive End of Frame output.
- RXSOFO - receive Start of Frame output.
- RXABTO - receive Abort output.
- RXMSO - receive Most Significant Byte output.
- RXFCSEO - receive FCS error output (both Abort and FCS indications can optionally be provided as outputs on this lead).

Only multi-PHY handshaking is supported when processing PPP Payloads. The UTOPIA Level 2P behaves the same whether STM-1, STM-4, STM-4c, STS-3c, STS-12, or STS-12c streams are being processed. The receive and transmit APH and ACI blocks operate in parallel as one large PHY to process the STM-4c/STS-12c streams. As is the case for ATM when STM-4c/STS-12c streams are being processed, the external transmit and receive address leads should be set to low.

Operation of the UTOPIA Level 2P interface is very similar to that of multi-PHY UTOPIA. Polling and selection of PHYs are performed in exactly the same way as described in [UL2v1]. Chunks of frame data are passed across the data buses. The chunk is analogous to the ATM cell. The TXSOC and RXSOC signals are analogous to the start of cell signal. T/RPAVO is analogous to the cell available signal. TXPRTY and RXPRTY are the parity signals. Since PPP frames are of variable size they may or may not fit into a single chunk transfer. The additional signals as listed above help to facilitate frame delineation.

TX PPP Data Transfer

The format of the data on TXUDATA(15:0) depends on the setting of control bits. If a TX PPP chiplet is set to calculate and insert 16- or 32-bit FCS, TXUDATA(15:0) contains only raw frame data and intra-chunk fill when data is being transferred across the UTOPIA Level 2P interface to that chiplet. The TX PPP chiplet will calculate the FCS and append it to the frame data, insert frame delimiting flags, and stuff the control escape and flag characters between the frame delimiting flags on a frame by frame basis. These operations are described in [RFC1662]. Inter-frame flags are inserted as needed. The data can then be optionally scrambled before it is inserted into the SONET/SDH SPE (Synchronous Payload Envelope). The PHAST-12E can be programmed to have a minimum of either 1 or 2 flags in between frames. If Transparent Mode is selected, the PHAST-12E will take the TXUDATA(15:0) data and insert each entire chunk into the transmit SONET/SDH frame without modification or the data can be optionally scrambled. The TXSOFI, TXEOFI and TXMSI leads are not used when the PHAST-12E is in transparent mode and should be tied low. If a TX PPP chiplet is set to not perform any FCS processing it will just take the TXUDATA(15:0) chunk data, for that chiplet, and insert frame delimiting flags around the frames and stuff the control escape and flag characters between the frame delimiting flags per [RFC1662]. As in the other cases, the data can optionally be scrambled. When FCS processing is disabled in a TX PPP chiplet, it is expected that the TXUDATA(15:0) will contain the appropriate FCS when data is being transferred across the UTOPIA Level 2P interface to that chiplet.

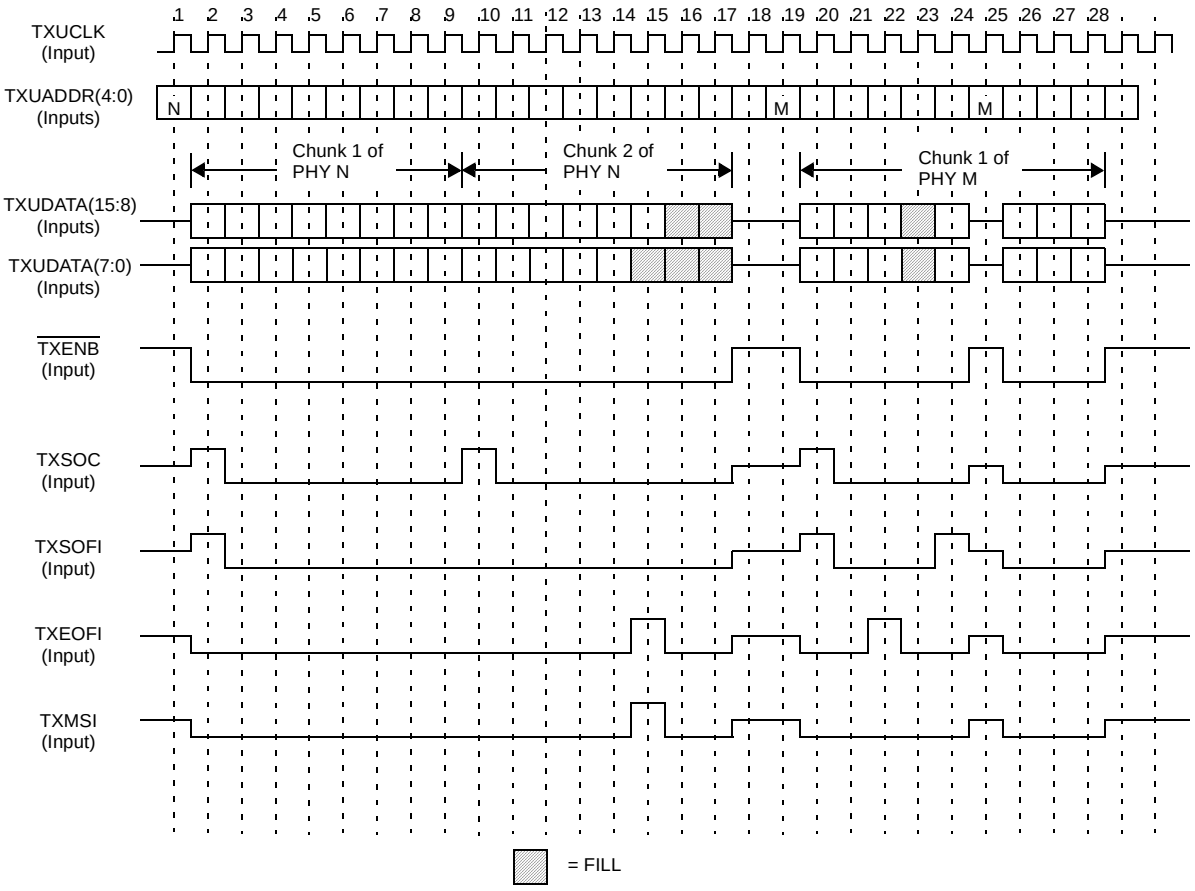


Figure 15. Transmit UTOPIA Level 2P Interface Operation for Non-Transparent mode (16-byte chunks)

Figure 15 shows the transfer of frames across the transmit UTOPIA Level 2P Interface. The TXABTO, TPAVO, and TXPRTY signals are omitted to avoid clutter. The polling and selection of PHYs is identical to that in the ATM mode of operation, which is also described in [UL2v1]. The TXUADDR(4:0), TXENB, TPAVO, TXSOC and TXPRTY signals therefore behave the same as their ATM counterparts, with the exception that TPAVO indicates that the PHAST-12E can accept at least a complete chunk of data. As stated earlier, a chunk is analogous to a cell. Chunk size is programmable to be either 16, 32, 48, or 64 bytes. Figure 15 shows the transfer of a 27-byte block of frame data using two back-to-back chunks over PHY N, then a 6-byte block of frame data over PHY M, and the first 8 bytes of another block of frame data also over PHY M. The chunk size shown is 16 bytes (with TXENB low). There are two bytes per clock period, one on TXUDATA(15:8) and one on TXUDATA(7:0). These are the most significant byte and least significant byte of a 16-bit word. PHY N is selected on clock edge 1. TXENB is used to indicate valid data and control signals at the interface. On clock edge 2, TXSOC is sampled as a '1', thus indicating the start of a chunk. Also, on clock edge 2, TXSOFI is sampled high, which indicates the start of a new block of frame data. The 27-byte block of frame data for PHY N is transferred from clock edge 2 to clock edge 15. The end of this block of frame data is indicated by the TXEOFI signal asserted high. The TXMSI signal is asserted with the TXEOFI signal to indicate that the last byte of the frame is in the Most Significant Byte position of that 16-bit word. The Least Significant Byte of that word contains fill. Since there is no more frame data to transfer across PHY N, two fill words are added to round out Chunk 2 of PHY N. Fill is data that is used to fill up empty locations in the data stream not occupied by frame data. This fill is either discarded or converted into inter-frame Flags (7E H) by the PHAST-12E. Another 16-byte block of frame data is transferred across PHY M on clock edges 20-22. The TXMSI signal is sampled low on clock edge 22, while TXEOFI is sampled high. This means that the last byte of the block of frame data is in the Least Significant Byte of that word. A word of fill is present on clock edge 23. A new block of frame data begins transfer across PHY M on clock edge 24.

There can be any number of fill words between frames in a chunk. However, a frame must always start on the Most Significant Byte of a word. Furthermore, if a block of frame data ended in a chunk which was being transferred across PHY X, and that chunk ended before another block of frame data started, then the start of the next block of frame data across PHY X must start in the first word of the next chunk transferred across PHY X.

An important note on the TXABTO lead: The TXABTO lead indicates when a transmit FIFO has underflowed during the middle of the transfer of the "HDLC-like" frame. In MPHY mode, if a transmit ACB FIFO underflow occurs in a PHY, say PHY N, while PHY M is being accessed, the TXABTO indication for PHY N will not be output until PHY N is selected. When an abort condition occurs, a 7D7E H sequence is inserted at the point in the broken frame where the FIFO underflow occurred. The rest of the frame data after the FIFO underflow occurred is ignored. If a transmit FIFO underflow occurs when a frame is not being transferred, then flag characters (7E H) are inserted into the data stream until a new frame is transmitted.

RX PPP Data Transfer

The format of the data on RXUDATA(15:0), and the control signals used, vary with the mode as selected by control bits. In transparent mode, the data in the SONET/SDH payload is extracted and optionally descrambled and output on the RXUDATA(15:0) bus. If an RX PPP chiplet is in transparent mode, only chunks are passed across the interface when the corresponding PHY is selected; FCS processing and frame delineation are not performed on the received data for that RX PPP chiplet. In that mode, the RXSOFO, RXEOFO, RXMSO, and RXFCSEO leads are not used for frame delineation purposes. However, the RXABTO, RXMSO, RXSOFO, and RXEOFO signals are used in conjunction with each other to indicate receive ACB FIFO overflow, illegal sequence detection, and for signaling recovery from reset. They also indicate when the PPP block is initially enabled. RPAVO functions normally as a chunk available / valid data and valid controls indication. If no FCS processing is selected (as opposed to transparent mode) for an RX PPP chiplet, the destuffed frame data is output on the data bus minus the frame delimiting and inter-frame flags. The control signals function normally with the exception that the RXFCSEO signal is not operational. It should be noted that, if an FCS is present in the frame, in any mode, it is also output on the data bus. If 16- or 32-bit FCS processing is selected for an RX PPP chiplet, the destuffed frame data is output on the data bus minus the frame delimiting and inter-frame flags. The FCS is not discarded and is output on the data bus. RXSOFO and RXEOFO are used to indicate the

start and end of a frame respectively. When RXMSO is asserted with RXEOFO it indicates that the end of the frame is in the Most Significant Byte of the current word.

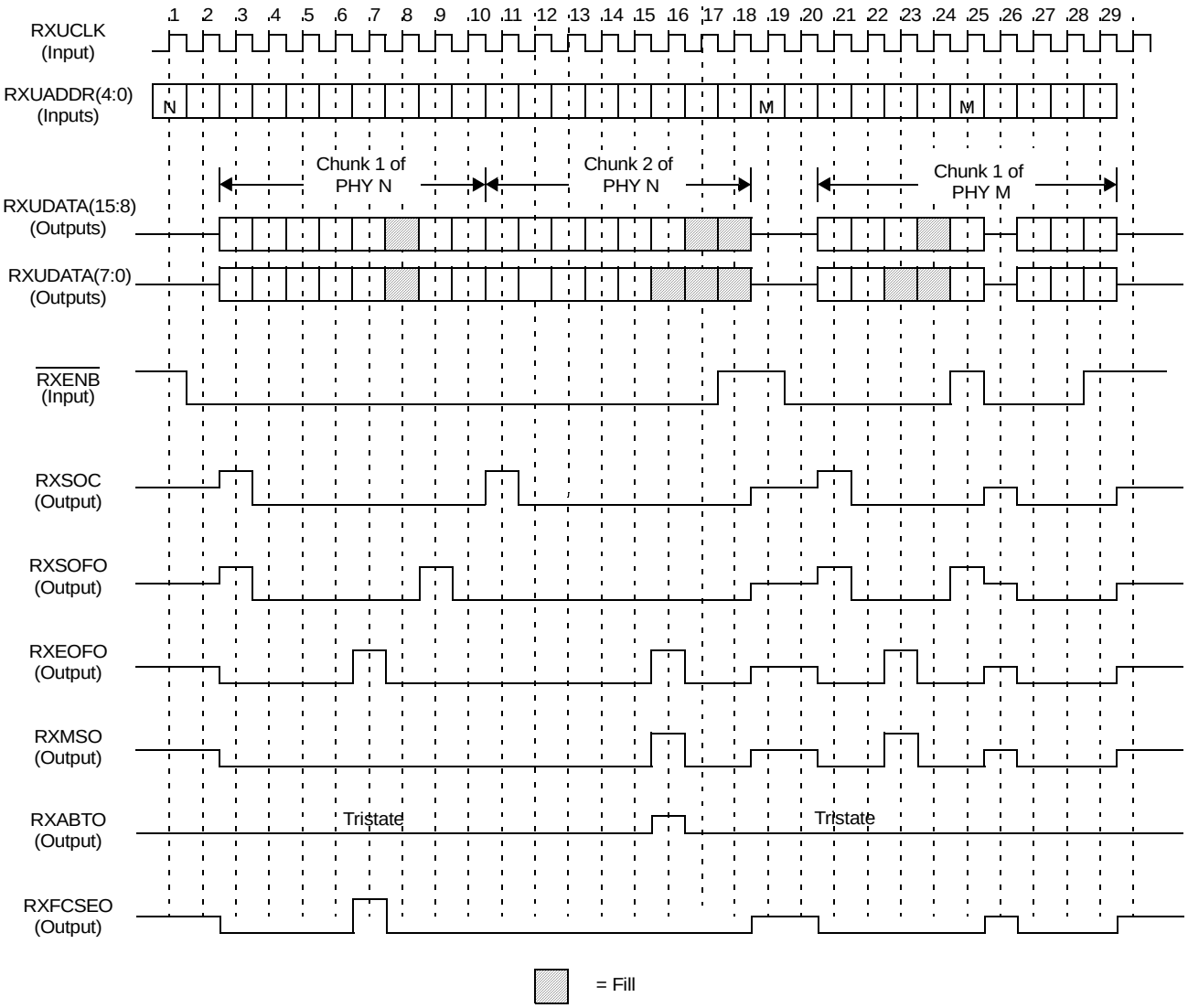


Figure 16. Receive UTOPIA Level 2P Interface Operation for Non-transparent Mode (16-byte chunks)

Figure 16 shows the transfer of frames across the receive UTOPIA Level 2P Interface. The RPAVO, and RXPRTY signals are omitted to avoid clutter. The polling and selection of PHYs is identical to that in the ATM mode of operation which is also described in [UL2v1]. Therefore, the RXUADDR(4:0), RXENB, RPAVO, RXSOC and RXPRTY behave in the same way as their ATM counterparts, but with the exception that RPAVO indicates that the PHAST-12E has at least a complete chunk of data to transfer. As stated earlier, a chunk is analogous to a cell. Chunk size is programmable to be either 16, 32, 48, or 64 bytes. Figure 16 shows the transfer of two blocks of frame data (of 10 bytes and 15 bytes before aborting the frame, respectively) as back-to-back chunks across PHY N and one complete 5-byte block and a partial block of frame data across PHY M. The chunk size in this case is 16 bytes (with RXENB low). The first block of frame data transferred across PHY N on clock edges 3-7 had an FCS error, which is flagged at the end of the frame data by the RXEOFO

and RXFCSEO signals being asserted. The second block of frame data being transferred across PHY N starts in chunk 1 of PHY N but is aborted in chunk 2 of PHY N. All aborts are signaled by the simultaneous assertion of the RXEOFO, RXMSO, and RXABTO signals (if the FCSABT control bit is 0) or by the simultaneous assertion of the RXEOFO, RXMSO, and RXFCSEO signals (if the FCSABT control bit is 1). The abort could have occurred due to any of the conditions listed below:

- Receive FIFO overflow
- An illegal sequence (7D7E H) was detected in the data stream
- A frame was received that was below the minimum frame length as defined by the MINFL(6:0) bits when DMINF is set to 1
- A frame was received that equaled or exceeded the maximum frame length defined by the MAXFL(15:0) bits

Another block of frame data is transferred across PHY M on clock edges 21-23. The RXMSO signal is asserted with the RXEOFO coincident with clock edge 23 to indicate that the last byte of the block of frame data is in the Most Significant Byte of that word. A word of fill is present on clock edge 24. There can be any number of fill words between frames in a chunk. Since the PHAST-12E device only transfers complete chunks, fill is added to a chunk after the end of a frame to fill out the chunk in lieu of frame data as shown in Figure 16 above. That is, after the end of a frame, fill is inserted into the chunk until either new frame data is received or until the end of the chunk occurs. A chunk will never start with fill. If a block of frame data ended in a chunk that was being transferred across PHY X, and that chunk ended before another block of frame data started, then the start of the next block of frame data across PHY X will start in the first word of the next chunk transferred across PHY X.

If an abort occurs, the rest of the aborted frame data will be used as fill. This fill will only be used to fill the current chunk until a new frame is received. If the end of the chunk occurs before a new frame is received, the rest of the data will be discarded and the next chunk transferred across that PHY will contain the next received frame. A frame always starts on the Most Significant Byte of a word.

An important note on the RXABTO lead: When FCSABT is set to 0, the RXABTO lead indicates detection of one of the abort conditions listed above. In MPHY mode, if an abort condition is detected in a PHY, say PHY N, while PHY M is being accessed, the RXABTO indication for PHY N will not be output until PHY N is selected. When an abort condition occurs, the rest of the received frame is ignored and used to fill up the chunk until the end of the chunk is reached or until a new frame is received. When FCSABT is set to 1, the RXABTO lead is forced low and the RXFCSEO lead is used to indicate both FCS errors and aborts. The abort signalling described above is the same except that the abort is signalled on the RXFCSEO lead.

TELECOM BUS INTERFACE

The PHAST-12E device contains four full duplex Telecom Bus interfaces, numbered 1 through 4. There is one Telecom Bus for each STM-1/STS-3c in 4 x STM-1/STS-3c mode, or one Telecom Bus for each AU-4 that may be contained in an STM-4/STS-12 signal. When STM-4c or STS-12c payloads are processed, the four Telecom Bus interfaces act in unison as a 32-bit wide Telecom Bus interface.

POH processing is not performed when the PHAST-12E is operating in Telecom Bus mode. All POH bytes in the transmit direction are derived from what is input at the transmit Telecom Bus inputs. All POH bytes at the receive Telecom Bus interface are derived directly from the receive line.

In the transmit direction the Telecom Bus interface supports either AU-n or VC-n formats on a per Telecom Bus basis, where n=4 for 4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes, or n=4-4c for STM-4c/STS-12c modes. When the AU-n format is selected, pointer retiming is disabled and the device driving the transmit Telecom Bus must supply (depending on the mode of operation) either an AU-3, an AU-4, or an AU-4-4c. The PHAST-12E will use all of the H1-H3 pointer bytes supplied to it and pass them on to the transmit line. It should be noted that H1-H3 must be supplied in this mode. When the VC-n format is selected, the PHAST-12E performs pointer retiming where it calculates and inserts a pointer value into the outgoing SONET/SDH Frame.

In the receive direction, the entire received payload is passed, unmodified, to the Receive Telecom Bus. Therefore, in 4 x STM-1/STS-3c mode, each STM-1/STS-3c frame is passed to its corresponding Telecom Bus Interface. In STM-4/STS-12 mode, all of the data from column 1 in the received frame is passed to receive Telecom Bus 1, all of the data from column 2 in the received frame is passed to receive Telecom Bus 2, etc. In STM-4c/STS-12c mode the same principle of operation applies as in the case of the STM-4/STS-12 mode, except that the RXTB#SPE, RXTB#J0J1, and RXTB#FAIL outputs have identical signals on them, where # = 1,2,3,4.

Individual SONET/SDH payloads cannot be assigned to individual Telecom Buses in either the TX or RX directions. For 4 x STM-1/STS-3c mode, the VC-4 or AU-4 data put into TX Telecom Bus 1 goes out on STM-1/STS-3c 1, the VC-4 or AU-4 data put into TX Telecom Bus 2 goes out on STM-1/STS-3c 2, etc. For 1 x STM-4/STS-12 mode the VC-4 or AU-4 data put into TX Telecom Bus 1 goes out on AU-4 1, the VC-4 or AU-4 data put into TX Telecom Bus 2 goes out on AU-4 2, etc. For 1 x STM-4c/STS-12c mode the data put into TX Telecom Bus 1 goes out on AU-4-4c slot 1, the data put into TX Telecom Bus 2 goes out on AU-4-4c slot 2, etc. The same correspondence also exists in the RX direction of the PHAST-12E.

The PHAST-12E device's Telecom Bus interface supports the following features:

- Option to enable/disable parity checking.
- Option to select if parity is calculated/checked over data only or over data and SPE and J0J1 and FAIL signals.
- Option to select if odd or even parity is used.
- 8 kHz transmit frame pulse and complementary transmit reference clock outputs are provided to synchronize transmit data into the PHAST-12E in AU-n mode. These signals are also available when the UTOPIA Level 2 or UTOPIA Level 2P Interface is used.
- Pointer retiming, or retiming for short, can be activated on any transmit Telecom Bus (1-4) on a per Telecom Bus basis.

Transmit Telecom Bus

There are four transmit Telecom Bus interfaces, numbered 1 - 4, allowing the back-to-back connection of PHAST-12E devices (if retiming is turned on), or connections to TranSwitch's POP-12 device. Other devices like PHAST-3N, SOT-3, or L4M may be connected to the transmit Telecom Bus interfaces.

Each transmit Telecom Bus interface of the PHAST-12E device consists of the following inputs: 8-bit data bus (TXTB#DATA(7:0)), clock (TXTB#CLK), SPE indication (TXTB#SPE), J0J1 indication (TXTB#J0J1), parity (TXTB#PAR), and a failure indication (TXTB#FAIL). The PHAST-12E also provides a common set of reference timebase signals for synchronizing the data input to each of the Telecom Bus ports for the cases where transmit retiming is not enabled. This reference timebase interface consists of the following outputs: a Transmit Reference Clock and its complement (TXCCLK and $\overline{\text{TXCCLK}}$) and a transmit Reference Frame Pulse (TXCFRM).

All of the Telecom Bus ports operate at 19.44 Mbyte/s. Furthermore, the option to support either a VC-n (Transmit Retiming On) or AU-n (Transmit Retiming Off) format is provided via the GContTx#(1:0) (#=1-4) control bits in the GContTx register. Retiming of the transmit Telecom Bus signal is performed when the VC-n signal format is selected. Retiming is the process of calculating the pointer value based on the phase difference of the input VC-n and the output frame. That is, pointer adjustments are allowed to occur to compensate for the phase changes between the input VC-n signal and the phase of the transmit SONET/SDH frame that may occur due to clock offsets.

Transmit retiming is enabled on a per Telecom Bus basis by setting the corresponding GContTx#(1:0) bits to VC-n Mode. When transmit retiming is enabled on a particular Telecom Bus, its transmit signals (clock, data, SPE etc.) only need to be synchronous to its TXTB#CLK and not to the TXCCLK signal. The J0 and J1 pulses in the TXTB#J0J1 signal are mandatory for the Telecom Bus channels where transmit retiming is enabled. The PHAST-12E will calculate a pointer and insert it into the outgoing SDH stream. The PHAST-12E will cause pointer adjustments to occur to compensate for the difference in the frequencies between the TXTB#CLK and

TXCCLK clocks. Furthermore, the PHAST-12E can accept pointer adjustments on its transmit Telecom Bus input and still perform retiming in an error-free fashion. Figure 18 shows functional timing of the TX Telecom Bus signals when TX Retiming is enabled.

When transmit retiming is disabled, the transmit Telecom Bus device that is providing data to the PHAST-12E must supply an AU-n, that is a VC-n with valid payload pointer bytes including concatenation indication bytes as applicable. Again, n=4 for 4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes, or n=4-4c for STM-4c/STS-12c modes. Additionally, multiple STS-3 applications (3 byte interleaved AU-3s) can be supported in 4xSTM-1/STS-3c mode by using the AU-n mode setting and supplying three byte interleaved AU-3s to the PHAST-12E. This mode of operation can be used to transport multiple STS-3 signals consisting of three STS-1s each. Figure 17 shows functional timing of the TX Telecom Bus signals when TX Retiming is disabled.

When the PHAST-12E is processing an STM-4c/STS-12c signal, all four Telecom Bus ports operate in parallel as one 32-bit wide Telecom Bus. All input signals must be driven (i.e., all clock, all SPE, all J0J1, etc.). In this case the transmit Telecom Bus data needs to be double-word aligned. The receive Telecom Bus data is provided double-word aligned.

The following paragraphs summarize the functionality of the Telecom Bus interface signals.

TXCCLK and $\overline{\text{TXCCLK}}$ are provided as a reference clock for devices to put data out onto the Telecom Bus ports of the PHAST-12E. These signals are 19.44 MHz for all modes. An 8 kHz pulse (TXCFRM) is output on the falling edge of TXCCLK once every frame period and is one TXCCLK clock cycle wide. It is used to synchronize the data arriving at the TXTB#DATA(7:0) inputs of the PHAST-12E if transmit retiming is not performed. If transmit retiming is not selected via the GContTx#(1:0) control bits then TXCFRM and either TXCCLK or $\overline{\text{TXCCLK}}$ must be used to source the data to be transmitted on the appropriate Telecom Bus. Figure 17 below shows the relationship between the Input Telecom Bus Data and the TXCFRM signal when TX Retiming is disabled. The EFRM control bit enables the TXCFRM pulse to come out one cycle earlier to allow more time for the device(s) transmitting on the Telecom Bus to supply the J0 byte.

The transmit Telecom Bus clock input (TXTB#CLK where # = 1-4) is used to clock the transmit Telecom Bus input signals into the PHAST-12E. It should be noted that when an STM-4c/STS-12c payload is being processed, so that the four transmit Telecom Bus interfaces act as a single 32-bit wide interface, all four TXTB#CLK inputs must be identical.

Each Telecom Bus port has an 8-bit wide data bus that accepts byte-aligned data from the transmitting Telecom Bus device. The data on this bus must have proper alignment with respect to the transmit reference frame pulse TXCFRM if transmit retiming is not performed. Figure 17 shows the required alignment when transmit retiming is not performed. Note that the TXTB#CLK signal must be frequency synchronous with TXCCLK if transmit retiming is not performed. However, any phase relationship may exist between TXCCLK and TXTB#CLK as long as the J0 byte is clocked into the PHAST-12E by the TXTB#CLK signal no later than $3*t_{CYC}$ - 22 ns after the occurrence of the rising edge of TXCCLK that is coincident with TXCFRM being high as shown by the parameter t in Figure 17. For all modes t_{CYC} is the period of the 19.44 MHz byte clock derived from the TX reference clock.

Control bit EFRM allows the TXCFRM pulse to occur one cycle earlier as indicated by the dashed line in Figure 17 for the TXCFRM signal. This will allow an extra clock cycle for a device on the Telecom Bus to put out its J0 byte if need be. It is extremely important to note that the J0 byte must be clocked into the PHAST-12E within the window defined by t in Figure 17 regardless of whether or not the TXCFRM pulse is provided one cycle earlier (i.e., the window is always measured with respect to the original position that TXCFRM has when the EFRM control bit is set to 0).

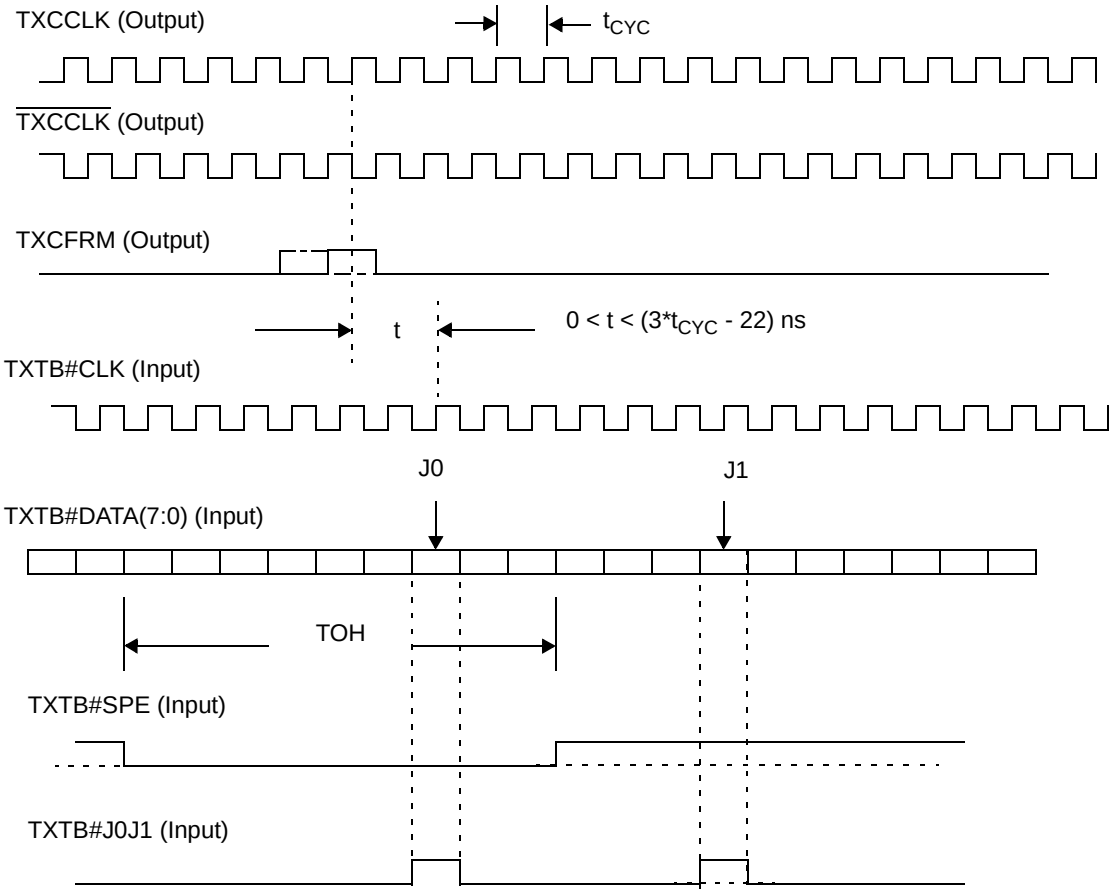
The TXTB#DATA(7:0) stream must contain valid pointer bytes (including concatenation indication, if applicable) when the PHAST-12E is not performing transmit retiming. All other TOH bytes are overwritten by the PHAST-12E. The device transmitting on the Telecom Bus must also supply the POH regardless of whether retiming is enabled or not. The PHAST-12E will not perform any transmit POH processing while in the Telecom Bus mode of operation. Even if Ring Port operation is enabled while in Telecom Bus mode, the PHAST-12E will ignore POH information from the mating PHAST-12E.

It should be noted that when an STM-4c/STS-12c payload is being processed, so that the four transmit Telecom Bus interfaces act as a single 32-bit wide interface, the TXTB1DATA(7:0) bus contains the most significant byte of the 32-bit double word of data, i.e., TXTB1DATA(7) is the first bit transmitted while TXTB4DATA(0) is the last bit transmitted.

As stated earlier, individual SONET/SDH payloads cannot be assigned to individual Telecom Buses in either the TX or RX directions.

While transmit retiming is disabled, and the TXTB#SPE input is low, the corresponding J0 pulse in the TXTB#J0J1 signal is used as a required slot identifier signal rather than a J0 byte identifier. A set of control bits FRM_SLT_SEL(1:0) in the OT#Conf11 registers is used to tell the PHAST-12E which slot the J0 pulse is located in. Figure 17 shows an example. When transmit retiming is enabled the pulses on the TXTB#J0J1 signal lead must be both present and coincident with the J0 and J1 bytes in the TXTB#DATA(7:0) signals. It should be noted that when an STM-4c/STS-12c payload is being processed, so that the four transmit Telecom Bus interfaces act as a single 32-bit wide interface, all four TXTB#J0J1 inputs must be identical.

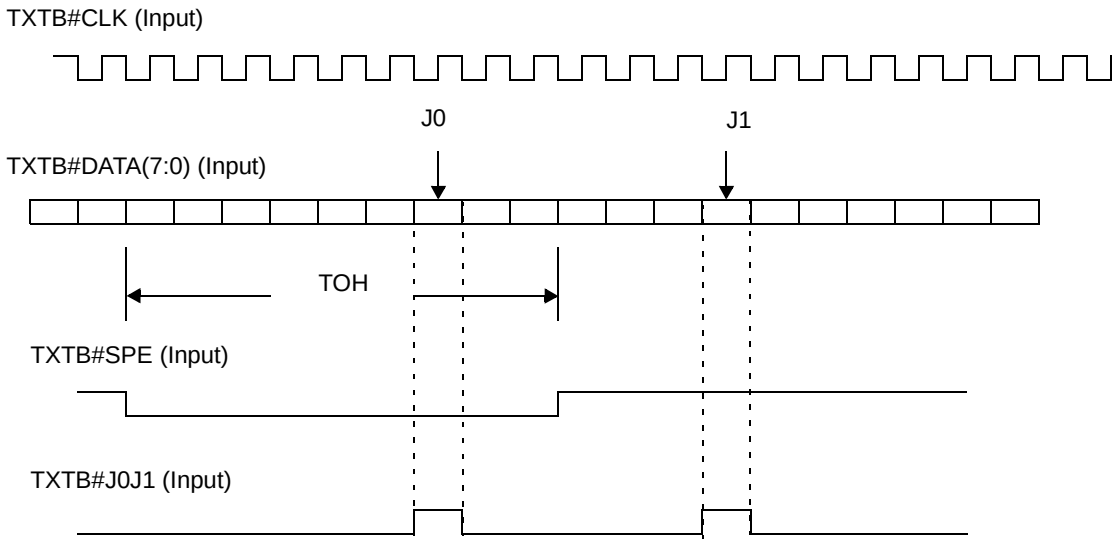
The transmit Telecom Bus SPE input (TXTB#SPE, #=1-4) should be low during TOH time slots, and should be high during SPE time slots, in each subframe while retiming is enabled. This includes cases where pointer adjustments are performed and the VC needs to be adjusted about the H3 byte(s). For example, the H3 byte(s) become payload during the frame in which a pointer decrement occurs, therefore the TXTB#SPE signal should be high coincident with the corresponding H3 byte(s). Also in the frame where a pointer increment occurs, the corresponding stuff opportunity byte(s) after the H3 byte(s) become stuff, therefore the TXTB#SPE signal must be low for those bytes. The TXTB#SPE signal can be tied low if no-retiming is done and the TXTB#J0J1 signal has only one pulse. It should be noted that when an STM-4c/STS-12c payload is being processed, so that the four transmit Telecom Bus interfaces act as a single 32-bit wide interface, all four TXTB#SPE inputs must be identical. When retiming is disabled, the TX#TBSPE signal can optionally be tied low if the TXTB#J0J1 signal contains only a slot identification pulse. Otherwise, the TXTB#SPE signal should be low during the time that the TXTB#J0J1 signal contains a slot identification pulse and should be high during the time that the TXTB#J0J1 signal contains a J1 pulse.



Notes:

1. Parity and Failure inputs are not shown.
2. TXTB#J0J1 does not need to be aligned under the J0 byte in the TXTB#DATA(7:0) signal while retiming is disabled. When retiming is disabled, the TXTB#J0J1 signal is used as a slot identification pulse. There are three slots (1-3) in a SONET/SDH frame. The 1st, 4th, 7th,... etc., column of the SONET/SDH frame is slot 1. The 2nd, 5th, 8th,... etc., column of the SONET/SDH frame is slot 2. The 3rd, 6th, 9th,... etc., column of the SONET/SDH frame is slot 3. The pulse on TXTB#J0J1 can be in any slot (1-3) provided that the FRM_SLT_SEL(1:0) bits in the OT#Conf11 registers are set accordingly, where # = 1-4. In this example, the slot identification pulse is in slot 1. The slot identification pulse needs to repeat once every 125 microseconds. Furthermore, if retiming is not enabled, the J1 pulse does not need to be present. However, the TXTB#SPE signal needs to be low during the time that the TXTB#J0J1 contains the slot identification pulse and should be high during the time that the TXTB#J0J1 contains a J1 pulse. If the TXTB#J0J1 signal contains only a slot identification pulse, then the TXTB#SPE signal can be tied low as shown by the dashed lines in the TXTB#SPE and TXTB#J0J1 signals.
3. The relationship between the J1 and the SPE signals is shown for illustration purposes only, and will be a function of pointer offset. The J1 pulse is not required or used by the PHAST-12E when Transmit Retiming is disabled.
4. When Transmit Retiming is disabled, while in STM-1/STS-3c or STM-4/STS-12 modes, the TXTB#DATA(7:0) bus must contain a valid AU-4 or three byte interleaved AU-3s.
5. When Transmit Retiming is disabled, while in STM-4c/STS-12c mode, the TXTB#DATA(7:0) bus must contain a valid AU-4-4c.

Figure 17. Functional Relationship of the Transmit Telecom Bus Signals when Transmit Retiming is not Performed (subframe 1 is shown)



Notes:

1. Parity and Failure inputs are not shown.
2. The relationship between the J1 and the SPE signals is shown for illustration purposes only, and will be a function of pointer offset.
3. When retiming is enabled, the J0 and J1 pulses in the TXTB#J0J1 signal are mandatory.
4. TXTB#SPE needs to be high during the STS-3c-SPE/STS-12c-SPE/VC-4/VC-4-4c byte times, including during pointer adjustments when the H3 stuff opportunity bytes or the bytes after them may or may not contain STS-3c-SPE, VC-4, STS-12c-SPE, or VC-4-4c data, and should be low during the Transport Overhead (TOH) byte times.
5. In 1xSTM-4c/STS-12c mode, the J1 byte can only exist on Telecom Bus 1. However, the TXTB#J0J1 signal must be asserted accordingly on all four transmit Telecom Buses.

Figure 18. Functional Relationship of the Transmit Telecom Bus Signals when Transmit Retiming is Performed (subframe 1 is shown)

The Telecom Bus checks the value of the transmit Telecom Bus parity input (TXTB#PAR) against an internally calculated value. The parity calculations that the PHAST-12E performs can be configured on a per Telecom Bus basis through the use of the PAR_EVEN, PAR_EN, and PAR_FULL control bits in the OT#Conf11 registers. If the TXTB#PAR signal indicates a different value than the PHAST-12E expects, the PHAST-12E will indicate an alarm through the PAR_ERR interrupt request bits in the OT#IRQ2 registers. Interrupt mask bits for the PAR_ERR interrupt request bits are provided in the OT#M_IRQ2 registers. The PAR_ERR interrupt mask bits will enable an interrupt request to be generated if its corresponding PAR_ERR interrupt request bit is set. The parity is checked on a per Telecom Bus basis regardless of whether or not the Telecom Bus interfaces work individually or as a single bus.

The transmit Telecom Bus failure input (TXTB#FAIL) is generated by the transmit Telecom Bus device to the PHAST-12E to tell the PHAST-12E to generate AIS-P in the STM-1/STS-3c for which the alarm occurs, regardless of whether retiming is turned on or off. This lead has an internal pull-up resistor to allow automatic AIS generation if a board failure occurs, such as when the driving signal to this lead is removed such that it is left floating. If this lead is not used it should be tied to ground. It should be noted that when an STM-4c/STS-12c payload is being processed, so that the four transmit Telecom Bus interfaces act as a single 32-bit wide interface, all four TXTB#FAIL inputs must be activated simultaneously.

Receive Telecom Bus

There are four receive Telecom Bus interfaces, numbered 1 - 4, allowing the back-to-back connection of PHAST-12E devices (if retiming is enabled in the transmit direction), or connections to other TranSwitch devices. Other devices may be connected to the receive Telecom Bus interfaces but it is up to the end user to determine their suitability.

Each receive Telecom Bus interface of the PHAST-12E device consists of the following outputs: 8-bit data bus (RXTB#DATA(7:0)), clock (RXTB#CLK), SPE indication (RXTB#SPE), J0J1 indication (RXTB#J0J1), parity (RXTB#PAR), and a failure indication (RXTB#FAIL), where # = 1-4 for 4xSTM-1/STS-3c, 1xSTM-4/STS-12, and 1x STM-4c/STS-12c modes. All of the receive Telecom Bus ports operate at 19.44 Mbyte/s.

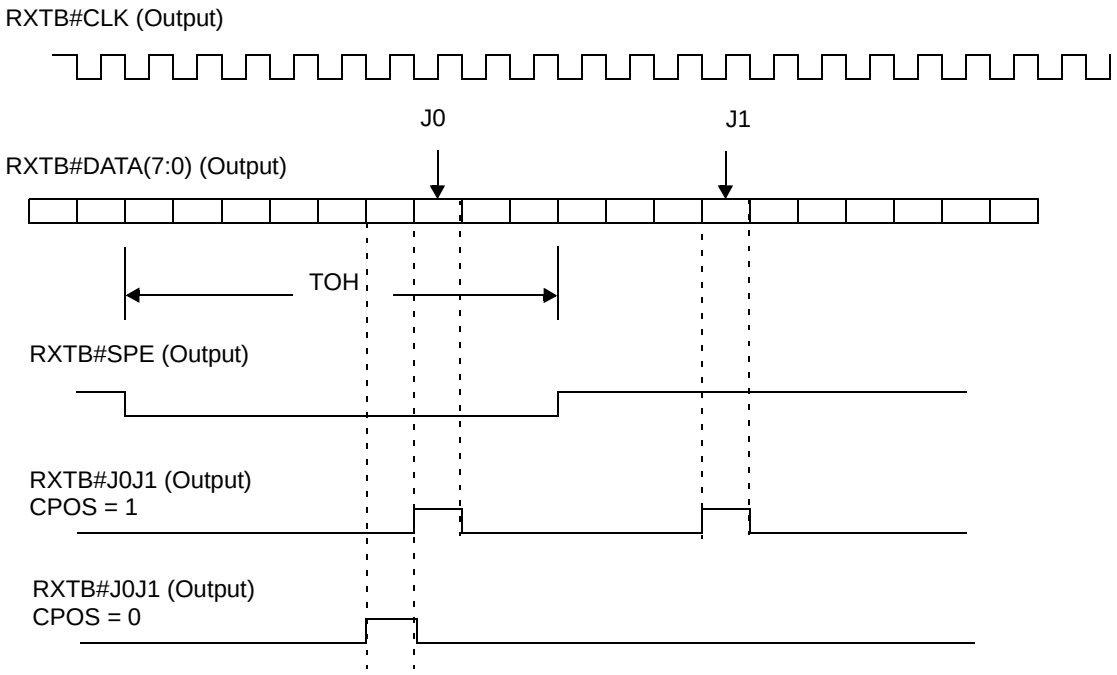
When an STM-4c or STS-12c is processed, the four receive Telecom Buses operate in unison as one Telecom Bus interface. The J0J1, SPE, clock, and FAIL outputs are identical. RXTB1DATA(7) is the MSB and is the first bit received, while RXTB4DATA(0) is the LSB and is the last bit received.

The following paragraphs summarize the functionality of the receive Telecom Bus interface signals.

The receive Telecom Bus clock output (RXTB#CLK) is used to clock out the receive Telecom Bus output signals from the PHAST-12E. The clock edge on which the Telecom Bus signals are clocked out is programmable on a per Telecom Bus basis via the CKINV# control bits. Figure 19 shows the functional relationship of the receive Telecom Bus signals.

Each receive Telecom Bus port has an 8-bit wide data bus that outputs the frame data from the 622.08 Mbit/s or 155.52 Mbit/s line input to receive Telecom Bus #. The receive Telecom Bus data is byte-aligned and the entire payload, including TOH and POH, is passed through the PHAST-12E device. In the case of STM-4/STM-4c/STS-12/STS-12c operation, the received frame is byte demuxed in 1:4 fashion. That is, the data from slot 1 is output on RX Telecom Bus 1, the data from slot 2 is output on Telecom Bus 2, etc. When processing an STM-4c/STS-12c the four receive Telecom Buses act as a single Telecom Bus, where RXTB1DATA(7) is the MSB and is the first bit received, while RXTB4DATA(0) is the LSB and is the last bit received.

The receive Telecom Bus J0J1 output (RXTB#J0J1) can be provisioned to provide two different types of indications, on a per Telecom Bus basis, depending on the setting of the CPOS control bits in the OR#Conf13 registers. When CPOS is set to 1, the corresponding RXTB#J0J1 signal provides two pulses. One pulse is coincident with the J0 byte (RXTB#J0J1 is high and RXTB#SPE is low) and the other is coincident with the J1 byte (RXTB#J0J1 is high and RXTB#SPE is high). The J1 pulse will track the J1 byte position as the PHAST-12E receives pointer adjustments. When CPOS is set to 0, the J1 pulse is eliminated and the J0 pulse is coincident with the third A2 byte. Figure 19 shows this operation.



Notes:

1. Parity and Failure outputs are not shown.
2. The relationship between the J1 pulse and the SPE signals is shown for reference purposes only, and will be a function of the pointer offset.
3. There is a CPOS control bit for each receive Telecom Bus in the OR#Conf13 registers.

Figure 19. Functional Relationship of the Receive Telecom Bus Signals (subframe 1 is shown)

For all subframes, the receive Telecom Bus SPE output (RXTB#SPE) is low during the TOH byte times in the RXTB#DATA(7:0) stream and is high during the SPE/VC byte times. This includes cases where pointer adjustments are performed and the SPE/VC needs to be adjusted about the H3 bytes. For example, in 4xSTM-1/STS-3c, 1xSTM-4/STS-12, or 1xSTM-4c/STS-12c modes, the H3 bytes are payload bytes during the frame in which a pointer decrement occurs, therefore the RXTB#SPE signal will be high coincident with the H3 bytes for that frame. Also in the frame where a pointer increment occurs, the bytes after the H3 bytes become stuff, therefore the RXTB#SPE signal will be low for those bytes.

The parity checking that the PHAST-12E performs can be configured on a per Telecom Bus basis through the use of the PAR_EVEN and PAR_FULL control bits in the OR#Conf13 registers. Parity is calculated on a per Telecom Bus basis regardless of whether the interfaces work individually or as a single bus.

The receive Telecom Bus failure output (RXTB#FAIL) is generated by PHAST-12E in response to an alarm condition that will cause all 1s AIS to be generated downstream, to tell the downstream device to generate AIS-P in the channel in which the alarm occurred. The RXTB#FAIL output will remain active for the duration of the alarm condition that causes it to become set. See Figure 58 on page 157 for details.

RING PORT

A Ring Port, also known as an Alarm Indication Port (AIP), is provided on the PHAST-12E for ring applications where line and path information need to be passed between PHAST-12E devices. The following line and path information are exchanged:

- Path RDI and FEBE
- Line RDI indication and FEBE
- Debounced K1 byte and inconsistent K1 byte Indication
- Debounced K2 byte and New APS Indication
- Debounced K3 byte and New K3 byte indication

The above alarm information is output on the RX Ring Port interface when the corresponding LineRING and PathRING control bits are set. However, when in Telecom Bus mode, the POH alarms (Path RDI and FEBE and Debounced K3 byte and New K3 byte indication) are not output or accepted by the RING Port. The TX Ring Port interface of the PHAST-12E can be configured to accept either the line alarm information or the path alarm information or both from its TX Ring Port interface instead of generating them locally.

e.g.: Consider the node of a Unidirectional Path Switched Ring (UPSR) Composed of two PHAST-12E devices as shown in Figure 20. B2 errors are detected by PHAST-12E East on its RX OC-12 East line. A Line FEBE needs to be sent back towards the originating signal on the TX OC-12 West line. This is automatically accomplished through the Ring Ports. Since PHAST-12E East is configured for Ring mode, instead of sending the line FEBE out on its TX OC-12 East line, it passes the line FEBE information over its RX Ring Port to PHAST-12E West (which is also configured for RING mode), which then transmits the Line FEBE on TX OC-12 West.

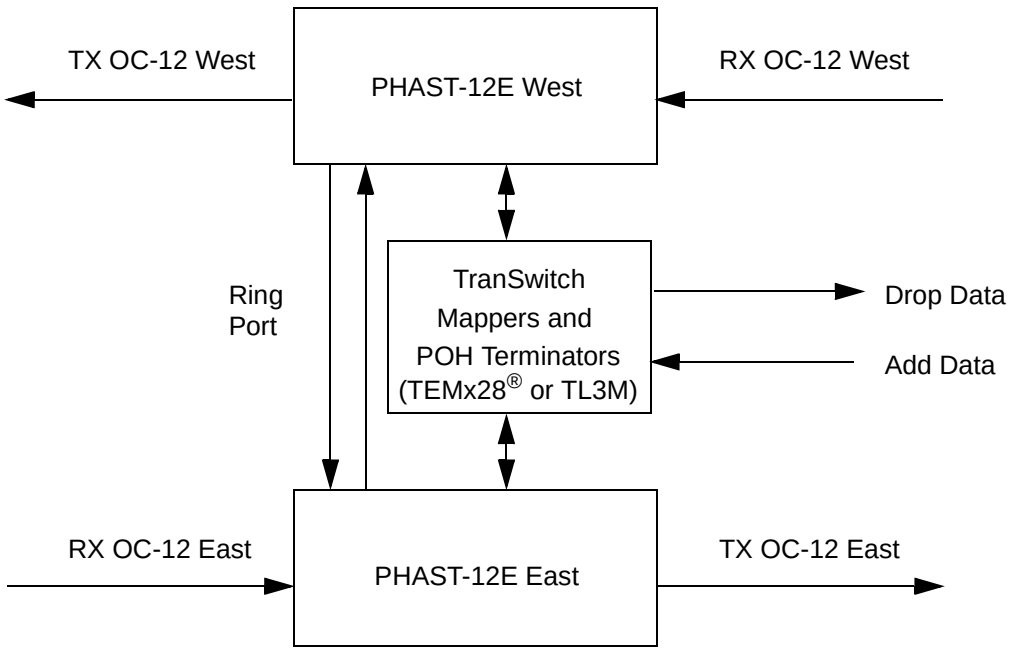


Figure 20. OC-12 UPSR Ring Port Example

DCC PORTS

There are four transmit DCC Ports and four receive DCC Ports. Each port consists of a clock output and a corresponding data input for transmit and corresponding data output for receive. The Regenerator Section (RS) DCC bytes D1-D3 or the MS DCC bytes D4-D12 can be processed by these ports via software control. All four ports are used in 4xSTM-1/STS-3c mode, and only the first ports should be used in 1xSTM-4/STS-12 and 1xSTM-4c/STS-12c modes; the other ports can be used in these modes but they contain the “dummy” DCC bytes. Optionally, the DCC bytes can be transmitted/received from the on-chip RAM.

MICROPROCESSOR INTERFACE

The PHAST-12E has a built-in microprocessor interface which is compatible with the Motorola 68360 microprocessor bus and is adaptable to be compatible with the Intel microprocessor bus. Interrupt capability is provided via interrupt mask bits. Access to the various configuration registers, counters, control, and status registers is provided via this interface.

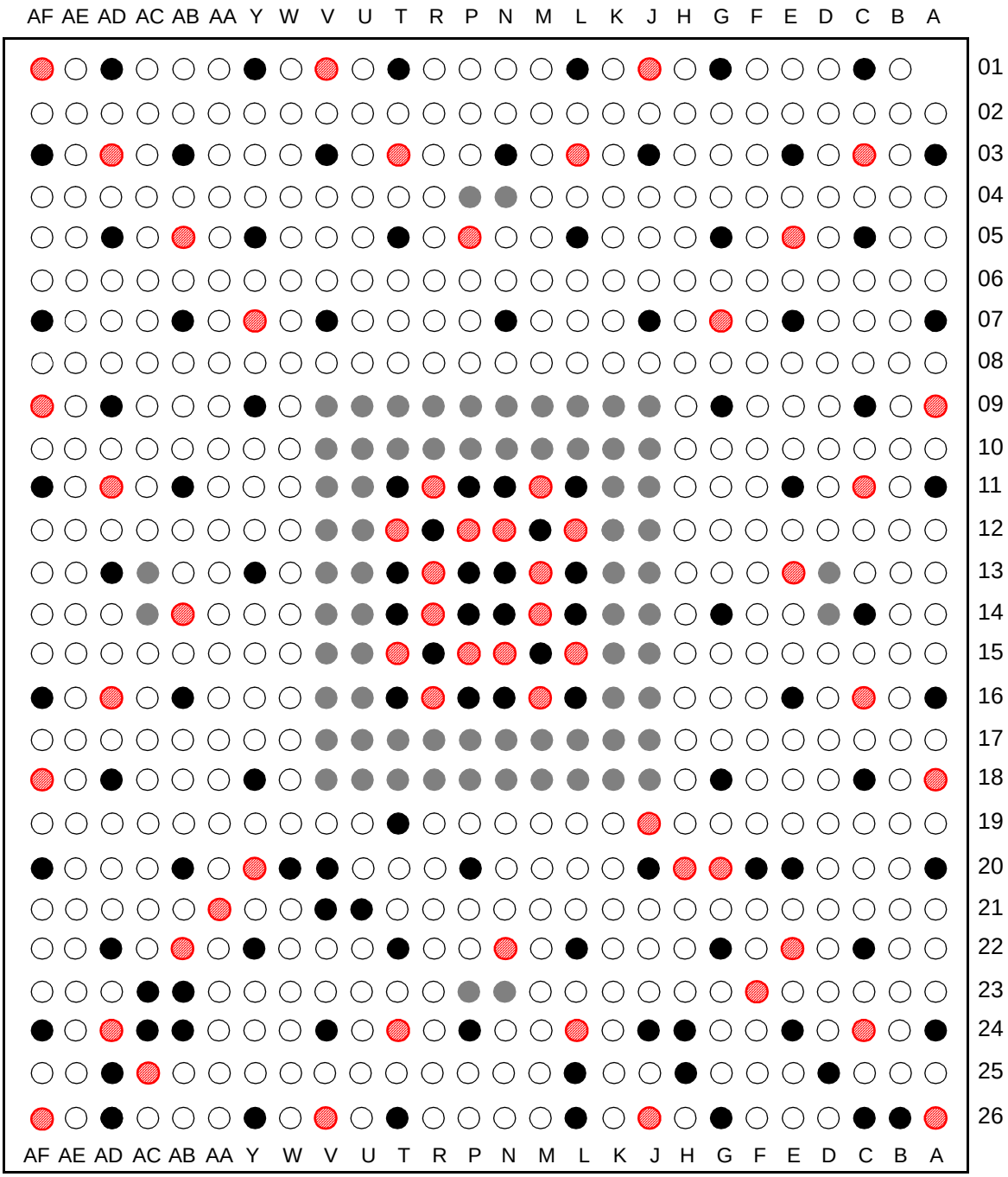
There are four operating modes available:

- Motorola synchronous
- Intel synchronous
- Motorola asynchronous
- Intel asynchronous

BOUNDARY SCAN

The Boundary Scan Port includes a five-lead TAP (Test Access Port) that conforms to the IEEE 1149.1-1994 standard for JTAG testing. This TAP provides external boundary scan to read and write the PHAST-12E input and output leads from the TAP for board and component testing.

LEAD DIAGRAM



Digital +2.5 V Power VDD, 56 places (VDD2-VDD5 and VDDP leads are not shown)

Ground, 106 places

No Connect, 72 places

Note: Diagram viewed from top of package.

Figure 21. PHAST-12E TXC-06212 Lead Diagram for the 675-Lead Enhanced PBGA Package

LEAD DESCRIPTIONS

Please note that none of these leads are 5 V tolerant and that two of them ($\overline{\text{FRESET}}$ and EN_COMBUS) are 2.5 V inputs and are not 3.3V tolerant.

The electrical characteristics of the I/O types (e.g., LVTTL, LVTTLp, etc.) can be found in the section "Input, Output and Input/output Parameters" on page 96.

POWER AND GROUND LEADS

Lead Name	Lead No.	Lead Description
GND	A03, A07, A11, A16, A20, A24, B26, C01, C05, C09, C14, C18, C22, C26, D25, E03, E07, E11, E16, E20, E24, F20, G01, G05, G09, G14, G18, G22, G26, H24, H25, J03, J07, J20, J24, L01, L05, L11, L13, L14, L16, L22, L25, L26, M12, M15, N03, N07, N11, N13, N14, N16, P11, P13, P14, P16, P20, P24, R12, R15, T01, T05, T11, T13, T14, T16, T19, T22, T26, U21, V03, V07, V20, V21, V24, W20, Y01, Y05, Y09, Y13, Y18, Y22, Y26, AB03, AB07, AB11, AB16, AB20, AB23, AB24, AC23, AC24, AD01, AD05, AD09, AD13, AD18, AD22, AD25, AD26, AF03, AF07, AF11, AF16, AF20, AF24	**Ground:** 0-volt reference.
VDD	A09, A18, A26, C03, C11, C16, C24, E05, E13, E22, F23, G07, G20, H20, J01, J19, J26, L03, L12, L15, L24, M11, M13, M14, M16, N12, N15, N22, P05, P12, P15, R11, R13, R14, R16, T03, T12, T15, T24, V01, V26, Y07, Y20, AA21, AB05, AB14, AB22, AC25, AD03, AD11, AD16, AD24, AF01, AF09, AF18, AF26	**Power (Digital):** +2.5V ± 5% power supply (for the internal logic of the PHAST-12E and IPECL inputs; APECL inputs are not included). Power must be supplied to these leads first before power is supplied to any of the other power leads.
VDD2	E25, E26, G24, H21, J22, J25, K21, K22, K26, L19, L20, L23, M23, M24, N26, T20, V22, W26, Y24, AA22, AB26	**Power (Analog):** +2.5V ± 5% power supply (for analog circuits, PLLs, and APECL inputs). This supply should be filtered very carefully since the quality of this voltage determines the jitter performance of the PLLs. Use of a linear, non-switching, regulator is mandatory.
VDD3	Y11, Y16, AB09, AB18, AD07, AD20, AF05, AF14, AF22	**Power (Digital):** +3.3V ± 5% power supply for the 3.3V LVTTL I/Os. VDD3, VDD4, and VDD5 must all be tied together.
VDD4	E01, G03, J05, L07, P01, T07, V05, Y03, AB01	**Power (Digital):** +3.3V ± 5% power supply for the 3.3V LVTTL I/Os. VDD3, VDD4, and VDD5 must all be tied together.
VDD5	A05, A13, A22, C07, C20, E09, E18, G11, G16	**Power (Digital):** +3.3V ± 5% power supply for the 3.3V LVTTL I/Os. VDD3, VDD4, and VDD5 must all be tied together.

Lead Name	Lead No.	Lead Description
VDDP	F25, J21, K23, N21, P19, U24, W21, Y25	**Power (Analog):** +3.3V ± 5% power supply (for Transmit analog circuits, PLLs, and APECL outputs). This supply should be filtered very carefully since the quality of this voltage determines the jitter performance of the PLLs. Use of a linear, non-switching, regulator is mandatory.
NC	D13, D14, J09, J10, J11, J12, J13, J14, J15, J16, J17, J18, K09, K10, K11, K12, K13, K14, K15, K16, K17, K18, L09, L10, L17, L18, M09, M10, M17, M18, N04, N09, N10, N17, N18, N23, P04, P09, P10, P17, P18, P23, R09, R10, R17, R18, T09, T10, T17, T18, U09, U10, U11, U12, U13, U14, U15, U16, U17, U18, V09, V10, V11, V12, V13, V14, V15, V16, V17, V18, AC13, AC14	**No Connect:** NC leads are not to be connected, not even to another NC lead, but must be left floating. Connection of NC leads may impair performance or cause damage to the device. If future revisions of the device are made, then these leads may have functions associated with them.

JTAG / LSSD / ANALOG TEST INTERFACE LEADS

Lead Name	Lead No.	I/O	Type	Lead Description
TEST_PU2	D26, F24 G21, H22 Y23, AA26 AC26	I		**Test Leads with Internal Pull-Up:** Used for factory test of the device. These inputs are connected to a pull-up resistor in the chip. They can be left unconnected. If it is desired to tie these leads to a known voltage, then they can be tied to +2.5V (VDD) via a pull-up resistor of not more than 10 kΩ.
TEST_PU3	C06	I		**Test Lead with Internal Pull-Up:** Used for factory test of the device. This input is connected to a pull-up resistor in the chip. It can be left unconnected. If it is desired to tie this lead to a known voltage, then it can be tied to +3.3V (VDD3, VDD4 or VDD5) via a pull-up resistor of not more than 10 kΩ.
TEST_PD	G23, M26 P26, AE25	I		**Test Leads with Internal Pull-Down:** Used for factory test of the device. The inputs are connected to a pull-down resistor in the chip. They can be left unconnected. If it is desired to tie these leads to a known voltage, then they can be tied to 0 V via a pull-down resistor of not more than 1 kΩ.
TEST_A TEST_E	AB21, AE26	I		**Test Lead:** Used for factory test of the device. An external pull-up resistor of not more than 10 kΩ MUST be used to tie each lead high to 2.5V (i.e., VDD).

Lead Name	Lead No.	I/O	Type	Lead Description
TEST_B	M22, M25 N25, P21 P22, R22 R23, R24 R25, R26 T23, T25 U22, V23	O		**Test Leads:** Used for factory test of the device. These leads must be left unconnected.
TEST_C	U23 V25	I		**Test Leads:** Used for factory test of the device. These leads should be connected to ground (GND).
TEST_D	N24	I		**Test Lead:** Used for factory test of the device. This lead should be connected to VDD2.
$\overline{\text{FRESET}}$	F26	I	LVCMOS2p	**Chip Reset:** (Active low) The use of this lead at power-up is mandatory. Holding this lead low causes all the registers in the device to be reset. The minimum reset pulse width is 4 microseconds. The power and the GPPCLK clock input must be stable during the low to high transition of this lead. The reset pulse applied to the $\overline{\text{FRESET}}$ lead is recommended to have a rise time less than or equal to 5 ns. This lead is not 3.3 V tolerant.
TCK	D23	I	LVTTLp	**JTAG TAP Test Clock:** Clock input for JTAG boundary scan testing. This input is connected to a pull-up resistor in the chip. It should be left unconnected if no JTAG test is required.
$\overline{\text{TRST}}$	A25	I	LVTTLp	**JTAG TAP Reset:** (Active low). Resets the JTAG TAP controller. This input is connected to a pull-up resistor in the chip. If the boundary scan is not used then this lead must be tied low. This lead must be held low for at least 50 ns and then brought high at power-up.
TMS	D22	I	LVTTLp	**JTAG Test Mode Select:** Mode selection for JTAG TAP controller. This input is connected to a pull-up resistor in the chip. It should be left unconnected if no JTAG test is required.
TDI	B23	I	LVTTLp	**JTAG Test Data Input:** Input port for serial scan data. This input is connected to a pull-up resistor in the chip. It should be left unconnected if no JTAG test is required.
TDO	F21	O	LVTTL	**JTAG Test Data Output:** Output port for serial scan data. This lead should be left unconnected if no JTAG test is required.

SYSTEM LEADS

Lead Name	Lead No.	I/O	Type	Lead Description
ACHCLK	AF13	I	LVTTLp	**ATM Cell Handler PPP Handler Clock:** This clock can have a maximum frequency of 25 MHz, but cannot go below the TX SFH byte clock frequency (19.44 MHz). Also, ACHCLK bust be synchronous to the UTOPIA clock divided by two (example: if UTOPIA clock is 50 MHz, ACHCLK will run at 25 MHz, synchronous to UTOPIA clock). The 19.44 MHz clock that is used by the transmit SFH blocks is derived from either the REFCLKT or REFCLKE(0:1) leads, or if in loop timing mode, it can be derived from one of the recovered clocks from the RX SONET/SDH lines. If some of the TX SFH blocks are running in loop timing and others are running off of the TCS logic, then the lowest frequency of the ACHCLK clock is limited to the highest SFH byte clock frequency. The ACHCLK clock is always required, even for Telecom Bus mode, in which case the frequency can be between 19.44 MHz (as used by the TX SFH blocks) and 25 MHz; as before the 19.44 MHz clocks here are the byte clocks used by the TX SFH blocks. If the APS Interface ports are used, a common ACHCLK is required between PHAST-12E devices.
ADDR(2) ADDR(1) ADDR(0)	D24 E23 C25	I	LVCMOSd	These leads must always be tied to ground (GND).

SONET / SDH LEADS

Lead Name	Lead No.	I/O	Type	Lead Description
TXSDAT1(0) TXSDAT1(1)	U19 U20	O	APECL	**Serial SONET/SDH Transmit Data 1:** (0=true, 1=inverted) 622.08/155.52 Mbit/s bit-serial data to electro/optical transceivers. Only TXSDAT1 is valid for STS-12/12c and STM-4/4c modes.
TXSDAT2(0) TXSDAT2(1)	AB25 AA25	O	APECL	**Serial SONET/SDH Transmit Data 2:** (0=true, 1=inverted) 155.52 Mbit/s bit-serial data to electro/optical transceivers. Not valid for STS-12/12c and STM-4/4c modes.
TXSDAT3(0) TXSDAT3(1)	J23 H23	O	APECL	**Serial SONET/SDH Transmit Data 3:** (0=true, 1=inverted) 155.52 Mbit/s bit-serial data to electro/optical transceivers. Not valid for STS-12/12c, and STM-4/4c modes.
TXSDAT4(0) TXSDAT4(1)	M19 M20	O	APECL	**Serial SONET/SDH Transmit Data 4:** (0=true, 1=inverted) 155.52 Mbit/s bit-serial data to electro/optical transceivers. Not valid for STS-12/12c and STM-4/4c modes.
TXPDAT(7) TXPDAT(6) TXPDAT(5) TXPDAT(4) TXPDAT(3) TXPDAT(2) TXPDAT(1) TXPDAT(0)	AB19 AC20 AA20 AF21 AD21 AE22 AF23 AE23	O	LVTTLp	These leads must be left unconnected.
TX_BYCLKINT	AD23	I	LVTTLp	This lead must be left unconnected.
TX_BYCLKINE(0) TX_BYCLKINE(1)	AE24 AF25	I	IPECL	These leads are not used and must be terminated as shown in Figure 47.
REFCLKT	P25	I	LVCMOSd	**Transmit Reference Clock LVCMOS:** Reference clock input for the transmit clock generation system in the PHAST-12E when not in loop timing mode. The frequency of this clock can be selected via control bits to be either 19.44, 38.88, 51.84 or 77.76 MHz. The frequency tolerance for this clock is ± 20 ppm. The maximum allowed jitter on this clock should be confined to the same limits as indicated below for the REFCLKE(0:1) leads. **Note:** REFCLKT must be present when the PHAST-12E is powered up. After the Auto Trim process is completed, REFCLKT can be replaced by REFCLKE and bit 4 of register PIMTConf1 must be set accordingly.

<table>
<tr><th>Lead Name</th><th>Lead No.</th><th>I/O</th><th>Type</th><th>Lead Description</th></tr>
<tr><td>REFCLKE(0)
REFCLKE(1)</td><td>M21
L21</td><td>I</td><td>IPECL</td><td>Transmit Reference Clock PECL: (0=true, 1=inverted)
Reference clock inputs for the transmit clock generation system in the PHAST-12E.
The frequency of this clock can be selected via control bits to be 19.44, 38.88, 51.84, or 77.76 MHz. The frequency tolerance for this clock is ± 20 ppm.
The maximum allowed jitter on this clock should be confined to a bandwidth of 5 kHz - 5 MHz and to the values shown below depending on the selected frequency, as indicated:
4 x 155 Mbit/s or 1 x 622 Mbit/s Operation Maximum Reference Clock Jitter.
Note: REFCLKT must be present when the PHAST-12E is powered up. After the Auto Trim process is completed, REFCLKT can be replaced by REFCLKE and bit 4 of register PIMTConf1 must be set accordingly.

<table>
<tr><th rowspan="2">Applied Reference Clock Frequency (MHz)</th><th colspan="2">Maximum Reference Clock Jitter</th></tr>
<tr><th>ps RMS</th><th>ps pp</th></tr>
<tr><td>19.44</td><td>7</td><td>50</td></tr>
<tr><td>38.88</td><td>9</td><td>65</td></tr>
<tr><td>51.84</td><td>9</td><td>65</td></tr>
<tr><td>77.76</td><td>9</td><td>65</td></tr>
</table>

No internal 100 Ω resistor exists for these leads.</td></tr>
<tr><td>TXDCLKT</td><td>G19</td><td>O</td><td>LVTTL</td><td>Transmit Divided Clock:
Programmable external clock output with nominal 50% duty cycle. This lead is always enabled.
The output frequency is selectable via control bits. Frequencies of 19.44, 38.88, 51.84 and 77.76 MHz are available. This clock will become indeterminate if the selected transmit reference clock is not present.</td></tr>
<tr><td>TXLPOW1</td><td>AA24</td><td>I</td><td>LVCMOS</td><td>Transmitter Low Power 1: (Active high)
This lead is used for monitoring the low power output indication from the external optical transmitter for line 1. It can be used to monitor other signals if desired.</td></tr>
<tr><td>TXLPOW2</td><td>W23</td><td>I</td><td>LVCMOS</td><td>Transmitter Low Power 2: (Active high)
This lead is used for monitoring the low power output indication from the external optical transmitter for line 2. It can be used to monitor other signals if desired.</td></tr>
<tr><td>TXLPOW3</td><td>AA23</td><td>I</td><td>LVCMOS</td><td>Transmitter Low Power 3: (Active high)
This lead is used for monitoring the low power output indication from the external optical transmitter for line 3. It can be used to monitor other signals if desired.</td></tr>
</table>

Lead Name	Lead No.	I/O	Type	Lead Description
TXLPOW4	A23	I	LVCMOS	**Transmitter Low Power 4:** (Active high) This lead is used for monitoring the low power output indication from the external optical transmitter for line 4. It can be used to monitor other signals if desired.
TXSDOWN1	B22	O	LVTTL	**Transmitter Shut Down 1:** (Active high) Used to shut down the optical transmitter for line 1. The level on this lead (0 or 1) depends on a control bit setting. This lead can be used to control other devices if desired.
TXSDOWN2	A12	O	LVTTL	**Transmitter Shut Down 2:** (Active high) Used to shut down the optical transmitter for line 2. The level on this lead (0 or 1) depends on a control bit setting. This lead can be used to control other devices if desired.
TXSDOWN3	E21	O	LVTTL	**Transmitter Shut Down 3:** (Active high) Used to shut down the optical transmitter for line 3. The level on this lead (0 or 1) depends on a control bit setting. This lead can be used to control other devices if desired.
TXSDOWN4	F19	O	LVTTL	**Transmitter Shut Down 4:** (Active high) Used to shut down the optical transmitter for line 4. The level on this lead (0 or 1) depends on a control bit setting. This lead can be used to control other devices if desired.
RXSDAT1(0) RXSDAT1(1)	U25 U26	I	APECL	**Serial SONET/SDH Receive Data 1:** (0=true, 1=inverted) The supported data rates on RXSDAT1 are 155.52 and 622.08 Mbit/s. An external 100 Ω resistor is required as close as possible to the PHAST-12E device. This line input can be used in 4xSTM-1/STS-3c, 1xSTM-4/STS-12, and 1xSTM-4c/STS-12c modes.
RXSDAT2(0) RXSDAT2(1)	V19 W19	I	APECL	**Serial SONET/SDH Receive Data 2:** (0=true, 1=inverted) The supported data rate on RXSDAT2 is 155.52 Mbit/s. An external 100 Ω resistor is required as close as possible to the PHAST-12E device. This line input can be used in 4xSTM-1/STS-3c mode.
RXSDAT3(0) RXSDAT3(1)	K20 K19	I	APECL	**Serial SONET/SDH Receive Data 3:** (0=true, 1=inverted) The supported data rate on RXSDAT3 is 155.52 Mbit/s. An external 100 Ω resistor is required as close as possible to the PHAST-12E device. This line input can be used in 4xSTM-1/STS-3c mode.

Lead Name	Lead No.	I/O	Type	Lead Description
RXSDAT4(0) RXSDAT4(1)	K24 K25	I	APECL	**Serial SONET/SDH Receive Data 4:** (0=true, 1=inverted) The supported data rate on RXSDAT4 is 155.52 Mbit/s. An external 100 Ω resistor is required as close as possible to the PHAST-12E device. This line input can be used in 4xSTM-1/STS-3c mode.
RXPDAT(7) RXPDAT(6) RXPDAT(5) RXPDAT(4) RXPDAT(3) RXPDAT(2) RXPDAT(1) RXPDAT(0)	AF19 AE19 AD19 AC19 AE20 AE21 AC21 AC22	I	LVTTLd	These leads must be left unconnected.
RXBYCLK	Y21	I	LVTTLp	This lead must be left unconnected.
RXDCLKT1	B24	O	LVTTL	**Receive Divided Clock 1:** Programmable clock output derived from the serial data stream on channel 1. Clock rates are 19.44, 38.88, 51.84 and 77.76 MHz. This clock will be indirectly derived from the TX reference clock through the RX clock recovery PLL 1 when the RX clock recovery PLL 1 is in frequency acquisition mode. This lead is always enabled.
RXDCLKT2	C23	O	LVTTL	**Receive Divided Clock 2:** Programmable clock output derived from the serial data stream on channel 2. Clock rates are 19.44, 38.88, 51.84 and 77.76 MHz. This clock will be indirectly derived from the TX reference clock through the RX clock recovery PLL 2 when the RX clock recovery PLL 2 is in frequency acquisition mode. This lead is always enabled.
RXDCLKT3	D21	O	LVTTL	**Receive Divided Clock 3:** Programmable clock output derived from the serial data stream on channel 3. Clock rates are 19.44, 38.88, 51.84 and 77.76 MHz. This clock will be indirectly derived from the TX reference clock through the RX clock recovery PLL 3 when the RX clock recovery PLL 3 is in frequency acquisition mode. This lead is always enabled.
RXDCLKT4	C21	O	LVTTL	**Receive Divided Clock 4:** Programmable clock output derived from the serial data stream on channel 4. Clock rates are 19.44, 38.88, 51.84 and 77.76 MHz. This clock will be indirectly derived from the TX reference clock through the RX clock recovery PLL 4 when the RX clock recovery PLL 4 is in frequency acquisition mode. This lead is always enabled.

Lead Name	Lead No.	I/O	Type	Lead Description
LOCKDET	B25	I	LVTTLd	**Lock Detect:** (Active high) A “1” applied to this lead causes an interrupt request bit to become set. This lead can be used to monitor other signals.
LOSSSIG1	B21	I	LVTTLp	**Loss of Signal 1:** (Active high) Signal from optical receiver for line 1 indicating loss of signal. The polarity of this input is configurable via software. When a logic level is applied to this lead that indicates a Loss of Signal has occurred, then the corresponding RX clock recovery PLL is forced to the frequency acquisition state where it will try and lock to the selected Transmit Reference Clock input (REFCLKE or REFCLKT).
LOSSSIG2	D19	I	LVTTLp	**Loss of Signal 2:** (Active high) Signal from optical receiver for line 2 indicating loss of signal. The polarity of this input is configurable via software. When a logic level is applied to this lead that indicates a Loss of Signal has occurred, then the corresponding RX clock recovery PLL is forced to the frequency acquisition state where it will try and lock to the selected Transmit Reference Clock input (REFCLKE or REFCLKT).
LOSSSIG3	A21	I	LVTTLp	**Loss of Signal 3:** (Active high) Signal from optical receiver for line 3 indicating loss of signal. The polarity of this input is configurable via software. When a logic level is applied to this lead that indicates a Loss of Signal has occurred, then the corresponding RX clock recovery PLL is forced to the frequency acquisition state where it will try and lock to the selected Transmit Reference Clock input (REFCLKE or REFCLKT).
LOSSSIG4	D20	I	LVTTLp	**Loss of Signal 4:** (Active high) Signal from optical receiver for line 4 indicating loss of signal. The polarity of this input is configurable via software. When a logic level is applied to this lead that indicates a Loss of Signal has occurred, then the corresponding RX clock recovery PLL is forced to the frequency acquisition state where it will try and lock to the selected Transmit Reference Clock input (REFCLKE or REFCLKT).
OOF	H19	O	LVTTLd	This lead must be left unconnected.
FP	F22	I	LVTTLd	This lead must be left unconnected.
RSTCREC	E19	O	LVTTL	**Reset Deserializer:** Signal that can be used to control any other device. The state of this lead is set through software control.

PHY LAYER INTERFACE LEADS

Lead Name	Lead No.	I/O	Type	Lead Description
TXUCLK	Y06	I	LVTTLp	**Transmit UTOPIA Clock:** The data and control signals are transferred on the rising edge of this clock. **UTOPIA Level 2:** This clock is used for the transmit UTOPIA Level 2 Interface. Maximum clock frequency is 50 MHz for 16-bit mode and 25 MHz for 8-bit mode. **UTOPIA Level 2P:** This clock is used for the transmit UTOPIA Level 2P Interface. Maximum clock frequency is 50 MHz.
TXUDATA(15) TXUDATA(14) TXUDATA(13) TXUDATA(12) TXUDATA(11) TXUDATA(10) TXUDATA(9) TXUDATA(8) TXUDATA(7) TXUDATA(6) TXUDATA(5) TXUDATA(4) TXUDATA(3) TXUDATA(2) TXUDATA(1) TXUDATA(0)	AA02 Y02 W02 V02 U03 U04 U05 R06 T06 U06 V06 W06 W07 U07 U08 T08	I	LVTTLp	**Transmit Data In:** 16-bit cell data input, valid when $\overline{\text{TXENB}}$ is asserted low. Bit 0 is the LSB. **UTOPIA Level 2:** TXUDATA(15:0) is the word input for the transmit UTOPIA Level 2 interface. Bit 15 is the most significant bit and is transmitted first. TXUDATA (15:8) are used in 8-bit mode. In 8-bit mode, bit 15 is the most significant bit and is transmitted first and bit 8 is the least significant bit and is transmitted last. **UTOPIA Level 2P:** TXUDATA(15:0) is the word input for the transmit UTOPIA Level 2P interface. Bit 15 is the most significant bit and is transmitted first.
TXUADDR(4) TXUADDR(3) TXUADDR(2) TXUADDR(1) TXUADDR(0)	W03 Y04 W04 V04 W05	I	LVTTLp	**Transmit Physical Device Address:** Four five-bit wide address for the for UTOPIA Level 2P and Level 2 interface ports. Bit 0 is the LSB. If single-PHY operation is performed, such as when STM-4c or STS-12c frames are processed, then these leads should be set to 0.
TXPRTY	AD02	I	LVTTLd	**Transmit Parity Input:** (Active high) Odd parity bit for UTOPIA Level 2 and Level 2P interfaces. Parity can be calculated over data, or data and control signals, depending on a control bit setting. The PHAST-12E only checks the TXPRTY in those TXUCLK cycles where the $\overline{\text{TXENB}}$ is asserted low.
TXSOC	AA04	I	LVTTLd	**Transmit Start of Cell/Chunk Input:** (Active high) Indicates the start of cell/chunk for UTOPIA Level 2 and Level 2P interfaces.
TXSOFI	AC02	I	LVTTLd	**Transmit Start-of-Frame Input:** (Active high) Used only during UTOPIA Level 2P operation, this lead indicates the start-of-frame data. This lead is ignored during ATM mode operation.
$\overline{\text{TXENB}}$	AB02	I	LVTTLp	**Transmit Read Enable Input:** (Active low) Read enable signal for cell/chunk input for UTOPIA Level 2 and Level 2P interfaces.

Lead Name	Lead No.	I/O	Type	Lead Description
TXCLAV(0)/TPAVO TXCLAV(1) TXCLAV(2) TXCLAV(3)	AE01 AC01 AA01 W01	O	LVTTL	**Transmit Cell/ Chunk Available Indicator**: TXCLAV/TPAVO indicates that the PHAST-12E can accept a complete cell or chunk in accordance with the UTOPIA Level 2 specification. TXCLAV(0) is associated with macro 1. The TXCLAV/TPAVO signals are not active for those streams terminated into the Port Handler Cross Connect (PHCC) since they are not terminated into the UTOPIA Level 2/2P interface. **UTOPIA Level 2:** TXCLAV(3:0) are the cell available indications for the transmit UTOPIA Level 2 interface. TXCLAV(3:0) can be configured for direct status (TXCLAV(0) only or TXCLAV(3:0)) or multiplexed status (TXCLAV(0) only or TXCLAV(3:0)) via the SIndT1(1:0) bits. **UTOPIA Level 2P:** TPAVO is the chunk available indication for the transmit UTOPIA Level 2P interface. TPAVO can only be configured for multiplexed status (TXCLAV(3:1) are not used). Chunks are analogous to cells. TPAVO functions exactly the same way as in ATM mode, except that TPAVO indicates the PHAST-12E's ability to accept chunks instead of cells.
TXEOFI	AA07	I	LVTTLd	**Transmit End-of-Frame Input:** (Active high) Used only during UTOPIA Level 2P operation, this lead indicates the end of frame data input. This lead is ignored during ATM mode operation.
TXMSI	AA03	I	LVTTLd	**Transmit Most Significant Byte Input:** (Active high) Used only during UTOPIA Level 2P operation, this lead indicates the frame data ends on the MSByte of the current word transfer. This lead is ignored during ATM mode operation.
TXABTO	V08	O	LVTTL	**Transmit Frame Abort Output:** (Active high) Used only during UTOPIA Level 2P operation, this lead indicates that a transmit FIFO has underflowed during the middle of the transfer of the "HDLC-like" frame and subsequently, an illegal sequence, 7D7E H, was transmitted. In MPHY mode, if a transmit abort occurs in a macro, say macro n, while macro m is being accessed, the TXABTO indication for macro n will not be output until macro n is selected. This lead is tristated until an abort is output (while a PHY port is selected). Therefore an external 1-3 kΩ pull-down resistor is required for this lead to ensure that the TXABTO lead is pulled to its inactive state in a timely manner in order to avoid functional problems.

Lead Name	Lead No.	I/O	Type	Lead Description
RXUCLK	AF02	I	LVTTLp	**Receive UTOPIA Clock:** The data and control signals are transferred on the rising edge of this clock. **UTOPIA Level 2:** This clock is used for the receive UTOPIA Level 2 Interface. Maximum clock frequency is 50 MHz for 16-bit mode and 25 MHz for 8-bit mode. **UTOPIA Level 2P:** This clock is used for the receive UTOPIA Level 2P Interface. Maximum clock frequency is 50 MHz.
RXUDATA(15) RXUDATA(14) RXUDATA(13) RXUDATA(12) RXUDATA(11) RXUDATA(10) RXUDATA(9) RXUDATA(8) RXUDATA(7) RXUDATA(6) RXUDATA(5) RXUDATA(4) RXUDATA(3) RXUDATA(2) RXUDATA(1) RXUDATA(0)	AA06 AB06 AF08 AE08 AD08 AC08 AB08 AA08 Y08 W08 AE09 AC09 AA09 W09 Y10 W10	O	LVTTL	**Receive Data Out:** Tristateable 16-bit cell data output bus, enabled only in cycles following those with RXENB asserted low. Bit 0 is the LSB. **UTOPIA Level 2:** RXUDATA(15:0) is the word output for the receive UTOPIA Level 2 interface. Bit 15 is the most significant bit and is the first bit received. RXUDATA(15:8) are used in 8-bit mode. In 8-bit mode, bit 15 is the most significant bit and is received first and bit 8 is the least significant bit and is received last. **UTOPIA Level 2P:** RXUDATA(15:0) is the word input for the receive UTOPIA Level 2P interface. Bit 15 is the most significant bit and is the first bit received.
RXUADDR(4) RXUADDR(3) RXUADDR(2) RXUADDR(1) RXUADDR(0)	AF06 AE06 AD06 AC06 AC07	I	LVTTLp	**Receive Physical Device Address:** Four five-bit wide address for the for UTOPIA Level 2P and Level 2 interface ports. Bit 0 is the LSB. If single-PHY operation is performed, such as when STM-4c or STS-12c frames are processed, then these leads should be set to 0.
RXPRTY	AE03	O	LVTTL	**Receive Parity Output:** (Active high) Odd parity bit for UTOPIA Level 2P and Level 2 interfaces. Parity can be generated over data, or over data and control signals, depending on a control bit setting. This is a tristateable output, enabled only in cycles following those with RXENB asserted low.
RXSOC	AE07	O	LVTTL	**Receive Start of Cell/Chunk Output:** (Active high) RXSOC indicates the start of each chunk or ATM cell for UTOPIA Level 2P and Level 2 interfaces. This is a tristateable output, enabled only in cycles following those with RXENB asserted low.
RXSOFO	AE02	O	LVTTL	**Receive Start-of-Frame Output:** (Active high) Used only during UTOPIA Level 2P operation, this lead indicates the start of a new block of frame data. This is a tristateable output, enabled only in cycles following those with RXENB asserted low.

Lead Name	Lead No.	I/O	Type	Lead Description
$\overline{\text{RXENB}}$	AC03	I	LVTTLp	**Receive Read Enable Input:** (Active low) Read enable input signal for UTOPIA Level 2P and Level 2 interfaces. Data and control outputs, except for the RXCLAV(3:0) signals, are enabled on the clock cycle following the assertion of this signal low for both Multi PHY and single PHY modes of operation.
RXCLAV(0)/RPAVO RXCLAV(1) RXCLAV(2) RXCLAV(3)	AF04 AE04 AD04 AE05	O	LVTTL	**Receive Cell/Chunk Available Indicator Output:** (Active high) Tristateable output signal that indicates that a complete chunk or cell is available for transfer. RXCLAV(3:0)/RPAVO operates per the UTOPIA Level 2 specification. RXCLAV(0) is associated with macro 1. The RXCLAV/RPAVO signals are not active for those streams terminated into the Port Handler Cross Connect (PHCC) since they are not terminated into the UTOPIA Level 2/2P interface. **UTOPIA Level 2:** RXCLAV(3:0) are the cell available indications for the receive UTOPIA Level 2 interface. RXCLAV(3:0) can be configured for direct status (RXCLAV(0) only or RXCLAV(3:0)) or multiplexed status (RXCLAV(0) only or RXCLAV(3:0)) via the SIndR1(1:0) bits. **UTOPIA Level 2P:** RPAVO is the chunk available indication for the receive UTOPIA Level 2P interface. RPAVO can only be configured for multiplexed status (RXCLAV(3:1) are not used). Chunks are analogous to cells. RPAVO functions exactly the same way as in ATM mode, except that RPAVO indicates that the PHAST-12E has at least one chunk to transfer (as opposed to having cells to transfer).
RXEOFO	AA05	O	LVTTL	**Receive End-of-Frame Output:** (Active high) Used only during UTOPIA Level 2P operation, this lead indicates the end of a block of frame data. This is a tristateable output, enabled only in cycles following those with $\overline{\text{RXENB}}$ asserted low.
RXMSO	AB04	O	LVTTL	**Receive Most Significant Byte Output:** (Active high) Used only during UTOPIA Level 2P operation, this lead indicates the frame data ends on the MSByte of the current word transfer. This is a tristateable output, enabled only in cycles following those with $\overline{\text{RXENB}}$ asserted low.

Lead Name	Lead No.	I/O	Type	Lead Description
RXFCSEO	AC05	O	LVTTL	**Receive Frame FCS Error Output:** (Active high) Used only during UTOPIA Level 2P operation, this lead indicates that an FCS error has been detected on the current frame being transferred over the interface. When FCSABT control bit is set to a 1 this lead will also indicate when an ABORT sequence (i.e., an illegal sequence of 7D7E H) is detected in the current frame or if the RX FIFO of the currently selected PHY has overflowed or if the PPP chiplet was disabled through its enable bit. When this lead indicates an abort, the RXEOFO and RXMSO leads are asserted at the same time that this lead is asserted, and the abort indication is only output when the PHY that detected the abort is selected. This is a tristateable output, enabled only in cycles following those with RXENB asserted low.
RXABTO	AC04	O	LVTTL	**Receive Abort Output:** This lead is used only during UTOPIA Level 2P operation. When the FCSABT bit is set to 0, this lead is an active high output signal that indicates that an ABORT condition (i.e., illegal sequence of 7D7E H) has been detected on the current frame being transferred over the interface, or that the receive ACB FIFO of the currently selected PHY has overflowed, or if the PPP chiplet was disabled through its enable bit. When FCSABT is set to 1, this lead is forced low. In MPHY mode, if a receive abort condition occurs in a macro, say macro n, while macro m is being accessed, the RXABTO indication for macro n will not be output until macro n is selected. Also, the RXEOFO and RXMSO leads are asserted at the same time that this lead is asserted. This lead is tristated until an abort is output (while a PHY port is selected). Therefore an external 1-3 kΩ pull-down resistor is required for this lead to ensure that the RXABTO lead is pulled to its inactive state in a timely manner in order to avoid functional problems.

TELECOM BUS INTERFACE LEADS[1]

Lead Name	Lead No.	I/O	Type	Lead Description
TXCCLK	F11	O	LVTTL	**Transmit Reference Clock:** TXCCLK is provided as a transmit reference timebase for devices connected to the transmit Telecom Bus interface. TXCCLK is configured to be 19.44 MHz for STM-1/STS-3c/STM-4/ STS-12/STM-4c/STS-12c operation. TXCFRM along with either TXCCLK or $\overline{\text{TXCCLK}}$ must be used to synchronize the data that is input to the Telecom Bus ports when TX Retiming is turned off i.e., when AU-n mode is enabled.

Lead Name	Lead No.	I/O	Type	Lead Description
$\overline{\text{TXCCLK}}$	F12	O	LVTTL	**Transmit Reference Clock Complement:** TXCCLK is the complement of TXCCLK and is provided to support devices that may have different timing requirements for clocking in the TXCFRM signal. $\overline{\text{TXCCLK}}$ is configured to be 19.44 MHz for STM-1/STS-3c/STM-4/STS-12/STM-4c/STS-12c operation. TXCFRM along with either TXCCLK or $\overline{\text{TXCCLK}}$ must be used to synchronize the data that is input to the Telecom Bus ports when TX Retiming is turned off i.e., when AU-n mode is enabled.
TXCFRM	H11	O	LVTTL	**Transmit Reference Frame Pulse:** TXCFRM along with either TXCCLK or $\overline{\text{TXCCLK}}$ must be used to synchronize the data that is input to the Telecom Bus ports when TX Retiming is turned off i.e., when AU-n mode is enabled. When TX Retiming is enabled, i.e., VC-n mode enabled, then this lead does not have to be used. This signal is synchronous to TXCCLK. n=4 for 4xSTM-1/STS-3c and 1xSTM-4/STS-12 modes, and n=4-4c for 1xSTM-4c/STS-12c modes.
TXTB1DATA(7) TXTB1DATA(6) TXTB1DATA(5) TXTB1DATA(4) TXTB1DATA(3) TXTB1DATA(2) TXTB1DATA(1) TXTB1DATA(0)	U01 T02 R01 R03 P02 N01 M01 M03	I	LVTTLp	**Telecom Bus 1 Transmit Input Data:** This data is clocked into the PHAST-12E on the rising edge of TXTB1CLK. Bit 7 is the MSB and is transmitted first. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** 19.44 Mbyte/s AU-4 (transmit retiming turned off) or VC-4 (TX retiming turned on) data input on these leads is inserted into the outgoing STM-1 1/STS-3c 1. **1xSTM-4c/STS-12c modes:** This bus contains the MSByte to be transferred first. The 19.44 Mbyte/s data can be in either AU-4-4c format (transmit retiming turned off) or in the VC-4-4c format (TX retiming turned on).
TXTB1CLK	N05	I	LVTTLp	**Telecom Bus 1 Transmit Input Clock:** All of the signals for Telecom Bus 1 are clocked into the PHAST-12E on the rising edge of this clock. TXTB1CLK **must** be frequency locked to either TXCCLK or $\overline{\text{TXCCLK}}$ if transmit retiming is not performed. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** The clock frequency is 19.44 MHz ± 20ppm. **1xSTM-4c/STS-12c modes:** The clock frequency is 19.44 MHz ± 20ppm.

1. When STM-4c or STS-12c frames are processed, the four transmit and four receive Telecom Buses operate in parallel as two 32-bit wide Telecom Buses.

Lead Name	Lead No.	I/O	Type	Lead Description
TXTB1J0J1	P08	I	LVTTLd	**Telecom Bus 1 Transmit Input Slot Indication:** When the TXTB1SPE signal is high, TXTB1J0J1 indicates the position of the J1 byte on Telecom Bus 1. When the TXTB1SPE signal is low, TXTB1J0J1 indicates the position of the J0 byte. The J1 and J0 pulses are required if transmit retiming is turned on. If transmit retiming is turned off then this signal becomes a slot identifier. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** The TXTB1J0J1 can be independent of the other TXTB#J0J1 leads. **1xSTM-4c/STS-12c modes:** TXTB1J0J1, TXTB2J0J1, TXTB3J0J1, and TXTB4J0J1 must all be asserted and deasserted together.
TXTB1SPE	R07	I	LVTTLd	**Telecom Bus 1 Transmit Input Synchronous Payload Envelope Signal:** This signal is high for the SPE bytes and is low for the TOH bytes on Telecom Bus 1. If transmit retiming is turned off, and no J1 pulse is present in TXTB1J0J1, then this lead can be tied low. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** The TXTB1SPE can be independent of the other TXTB#SPE leads. **1xSTM-4c/STS-12c modes:** TXTB1SPE, TXTB2SPE, TXTB3SPE, and TXTB4SPE must all be asserted and deasserted together.
TXTB1PAR	R05	I	LVTTLp	**Telecom Bus 1 Transmit Input Parity:** Parity for the signals of Telecom Bus1. It should be calculated by the transmitting device according to the settings of the PAR_FULL, PAR_EVEN, and PAR_EN control bits in the OT1Conf11 register. Parity errors are reported via the PAR_ERR interrupt request bit in the OT1IRQ2 register, but no actions are taken.
TXTB1FAIL	P07	I	LVTTLp	**Telecom Bus 1 Transmit Input Failure Indication:** TXTB1FAIL indicates that a failure has occurred on the device transmitting on Telecom Bus 1. This lead has no effect in ATM/PPP mode. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** When TXTB1FAIL goes high, AIS-P is transmitted on STM-1 1/STS-3c 1. **1xSTM-4c/STS-12c modes:** TXTB1FAIL, TXTB2FAIL, TXTB3FAIL, and TXTB4FAIL must all be asserted and deasserted together to cause AIS-P to be transmitted or terminated in the TX STM-4c/STS-12c signal.

Lead Name	Lead No.	I/O	Type	Lead Description
TXTB2DATA(7) TXTB2DATA(6) TXTB2DATA(5) TXTB2DATA(4) TXTB2DATA(3) TXTB2DATA(2) TXTB2DATA(1) TXTB2DATA(0)	L02 K01 K03 K05 J02 H01 H03 H05	I	LVTTLp	**Telecom Bus 2 Transmit Input Data:** This data is clocked into the PHAST-12E on the rising edge of TXTB2CLK. Bit 7 is the MSB and is transmitted first. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** 19.44 Mbyte/s AU-4 (transmit retiming turned off) or VC-4 (TXC retiming turned on) data input on these leads is inserted into the outgoing STM-1 2/STS-3c 2. **1xSTM-4c/STS-12c modes:** This bus contains the 2nd MSByte to be transferred. The 19.44 Mbyte/s data can be in either AU-4-4c format (transmit retiming turned off) or in the VC-4-4c format (TXC retiming turned on).
TXTB2CLK	J06	I	LVTTLp	**Telecom Bus 2 Transmit Input Clock:** All of the signals for Telecom Bus 2 are clocked into the PHAST-12E on the rising edge of this clock. TXTB2CLK **must** be frequency locked to either TXCCLK or $\overline{\text{TXCCLK}}$ if transmit retiming is not performed. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** The clock frequency is 19.44 MHz ± 20ppm. **1xSTM-4c/STS-12c modes:** The clock frequency is 19.44 MHz ± 20ppm.
TXTB2J0J1	K08	I	LVTTLd	**Telecom Bus 2 Transmit Input Slot Indication:** When the TXTB2SPE signal is high, TXTB2J0J1 indicates the position of the J1 byte on Telecom Bus 2. When the TXTB2SPE signal is low, TXTB2J0J1 indicates the position of the J0 byte. The J1 and J0 pulses are required if transmit retiming is turned on. If transmit retiming is turned off then this signal becomes a slot identifier. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** The TXTB2J0J1 can be independent of the other TXTB#J0J1 leads. **1xSTM-4c/STS-12c modes:** TXTB1J0J1, TXTB2J0J1, TXTB3J0J1, and TXTB4J0J1 must all be asserted and deasserted together.
TXTB2SPE	M08	I	LVTTLd	**Telecom Bus 2 Transmit Input Synchronous Payload Envelope Signal:** This signal is high for the SPE bytes and is low for the TOH bytes on Telecom Bus 2. If transmit retiming is turned off, and no J1 pulse is present in TXTB2J0J1, then this lead can be tied low. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** The TXTB2SPE can be independent of the other TXTB#SPE leads. **1xSTM-4c/STS-12c modes:** TXTB1SPE, TXTB2SPE, TXTB3SPE, and TXTB4SPE must all be asserted and deasserted together.

Lead Name	Lead No.	I/O	Type	Lead Description
TXTB2PAR	M06	I	LVTTLp	**Telecom Bus 2 Transmit Input Parity:** Parity for the signals of Telecom Bus 2. It should be calculated by the transmitting device according to the settings of the PAR_FULL, PAR_EVEN, and PAR_EN control bits in the OT2Conf11 register. Parity errors are reported via the PAR_ERR interrupt request bit in the OT2IRQ2 register, but no actions are taken.
TXTB2FAIL	L06	I	LVTTLp	**Telecom Bus 2 Transmit Input Failure Indication:** TXTB2FAIL indicates that a failure has occurred on the device transmitting on Telecom Bus 2. This lead has no effect in ATM/PPP mode. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** When TXTB2FAIL goes high, AIS-P is transmitted on STM-1 2/STS-3c 2. **1xSTM-4c/STS-12c modes:** TXTB1FAIL, TXTB2FAIL, TXTB3FAIL, and TXTB4FAIL must all be asserted and deasserted together to cause AIS-P to be transmitted or terminated in the TX STM-4c/STS-12c signal.
TXTB3DATA(7) TXTB3DATA(6) TXTB3DATA(5) TXTB3DATA(4) TXTB3DATA(3) TXTB3DATA(2) TXTB3DATA(1) TXTB3DATA(0)	G02 F01 D01 E02 D03 B01 B03 A02	I	LVTTLp	**Telecom Bus 3 Transmit Input Data:** This data is clocked into the PHAST-12E on the rising edge of TXTB3CLK. Bit 7 is the MSB and is transmitted first. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** 19.44 Mbyte/s AU-4 (transmit retiming turned off) or VC-4 (TXC retiming turned on) data input on these leads is inserted into the outgoing STM-1 3/STS-3c 3. **1xSTM-4c/STS-12c modes:** This bus contains the 3rd MSByte to be transferred. The 19.44 Mbyte/s data can be in either AU-4-4c format (transmit retiming turned off) or in the VC-4-4c format (TXC retiming turned on).
TXTB3CLK	F03	I	LVTTLp	**Telecom Bus 3 Transmit Input Clock:** All of the signals for Telecom Bus 3 are clocked into the PHAST-12E on the rising edge of this clock. TXTB3CLK **must** be frequency locked to either TXCCLK or $\overline{\text{TXCCLK}}$ if transmit retiming is not performed. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** The clock frequency is 19.44 MHz ± 20ppm. **1xSTM-4c/STS-12c modes:** The clock frequency is 19.44 MHz ± 20ppm.

Lead Name	Lead No.	I/O	Type	Lead Description
TXTB3J0J1	C04	I	LVTTLd	**Telecom Bus 3 Transmit Input Slot Indication:** When the TXTB3SPE signal is high, TXTB3J0J1 indicates the position of the J1 byte on Telecom Bus 3. When the TXTB3SPE signal is low, TXTB3J0J1 indicates the position of the J0 byte. The J1 and J0 pulses are required if transmit retiming is turned on. If transmit retiming is turned off then this signal becomes a slot identifier. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** The TXTB3J0J1 can be independent of the other TXTB#J0J1 leads. **1xSTM-4c/STS-12c modes:** TXTB1J0J1, TXTB2J0J1, TXTB3J0J1, and TXTB4J0J1 must all be asserted and deasserted together.
TXTB3SPE	E06	I	LVTTLd	**Telecom Bus 3 Transmit Input Synchronous Payload Envelope Signal:** This signal is high for the SPE bytes and is low for the TOH bytes on Telecom Bus 3. If transmit retiming is turned off, and no J1 pulse is present in TXTB3J0J1, then this lead can be tied low. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** The TXTB3SPE can be independent of the other TXTB#SPE leads. **1xSTM-4c/STS-12c modes:** TXTB1SPE, TXTB2SPE, TXTB3SPE, and TXTB4SPE must all be asserted and deasserted together.
TXTB3PAR	G06	I	LVTTLp	**Telecom Bus 3 Transmit Input Parity:** Parity for the signals of Telecom Bus 3. It should be calculated by the transmitting device according to the settings of the PAR_FULL, PAR_EVEN, and PAR_EN control bits in the OT3Conf11 register. Parity errors are reported via the PAR_ERR interrupt request bit in the OT3IRQ2 register, but no actions are taken.
TXTB3FAIL	F05	I	LVTTLp	**Telecom Bus 3 Transmit Input Failure Indication:** TXTB3FAIL indicates that a failure has occurred on the device transmitting on Telecom Bus 3. This lead has no effect in ATM/PPP mode. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** When TXTB3FAIL goes high, AIS-P is transmitted on STM-1 3/STS-3c 3. **1xSTM-4c/STS-12c modes:** TXTB1FAIL, TXTB2FAIL, TXTB3FAIL, and TXTB4FAIL must all be asserted and deasserted together to cause AIS-P to be transmitted or terminated in the TX STM-4c/STS-12c signal.

Lead Name	Lead No.	I/O	Type	Lead Description
TXTB4DATA(7) TXTB4DATA(6) TXTB4DATA(5) TXTB4DATA(4) TXTB4DATA(3) TXTB4DATA(2) TXTB4DATA(1) TXTB4DATA(0)	D08 B08 H09 D09 H10 F10 D10 B10	I	LVTTLp	**Telecom Bus 4 Transmit Input Data:** This data is clocked into the PHAST-12E on the rising edge of TXTB4CLK. Bit 7 is the MSB and is transmitted first. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** 19.44 Mbyte/s AU-4 (transmit retiming turned off) or VC-4 (TXC retiming turned on) data input on these leads is inserted into the outgoing STM-1 4/STS-3c 4. **1xSTM-4c/STS-12c modes:** This bus contains the LSByte to be transferred. The 19.44 Mbyte/s data can be in either AU-4-4c format (transmit retiming turned off) or in the VC-4-4c format (TXC retiming turned on).
TXTB4CLK	B07	I	LVTTLp	**Telecom Bus 4 Transmit Input Clock:** All of the signals for Telecom Bus 4 are clocked into the PHAST-12E on the rising edge of this clock. TXTB4CLK **must** be frequency locked to either TXCCLK or $\overline{\text{TXCCLK}}$ if transmit retiming is not performed. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** The clock frequency is 19.44 MHz ± 20ppm. **1xSTM-4c/STS-12c modes:** The clock frequency is 19.44 MHz ± 20ppm.
TXTB4J0J1	D06	I	LVTTLd	**Telecom Bus 4 Transmit Input Slot Indication:** When the TXTB4SPE signal is high, TXTB4J0J1 indicates the position of the J1 byte on Telecom Bus 4. When the TXTB4SPE signal is low, TXTB4J0J1 indicates the position of the J0 byte. The J1 and J0 pulses are required if transmit retiming is turned on. If transmit retiming is turned off then this signal becomes a slot identifier. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** The TXTB4J0J1 can be independent of the other TXTB#J0J1 leads. **1xSTM-4c/STS-12c modes:** TXTB1J0J1, TXTB2J0J1, TXTB3J0J1, and TXTB4J0J1 must all be asserted and deasserted together.
TXTB4SPE	E08	I	LVTTLd	**Telecom Bus 4 Transmit Input Synchronous Payload Envelope Signal:** This signal is high for the SPE bytes and is low for the TOH bytes on Telecom Bus 4. If transmit retiming is turned off, and no J1 pulse is present in TXTB4J0J1, then this lead can be tied low. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** The TXTB4SPE can be independent of the other TXTB#SPE leads. **1xSTM-4c/STS-12c modes:** TXTB1SPE, TXTB2SPE, TXTB3SPE, and TXTB4SPE must all be asserted and deasserted together.

Lead Name	Lead No.	I/O	Type	Lead Description
TXTB4PAR	H08	I	LVTTLp	**Telecom Bus 4 Transmit Input Parity:** Parity for the signals of Telecom Bus 4. It should be calculated by the transmitting device according to the settings of the PAR_FULL, PAR_EVEN, and PAR_EN control bits in the OT4Conf11 register. Parity errors are reported via the PAR_ERR interrupt request bit in the OT4IRQ2 register, but no actions are taken.
TXTB4FAIL	F07	I	LVTTLp	**Telecom Bus 4 Transmit Input Failure Indication:** TXTB4FAIL indicates that a failure has occurred on the device transmitting on Telecom Bus 4. This lead has no effect in ATM/PPP mode. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** When TXTB4FAIL goes high, AIS-P is transmitted on STM-1 4/STS-3c 4. **1xSTM-4c/STS-12c modes:** TXTB1FAIL, TXTB2FAIL, TXTB3FAIL, and TXTB4FAIL must all be asserted and deasserted together to cause AIS-P to be transmitted or terminated in the TX STM-4c/STS-12c signal.
RXTB1DATA(7) RXTB1DATA(6) RXTB1DATA(5) RXTB1DATA(4) RXTB1DATA(3) RXTB1DATA(2) RXTB1DATA(1) RXTB1DATA(0)	U02 T04 R02 R04 P03 N02 M02 M04	O	LVTTL	**Telecom Bus 1 Receive Data:** Bit 7 is the MSB and is received first. Bit 0 is the LSB and is received last. All TOH and SPE data are passed out of the PHAST-12E and are not modified. The data on these leads are clocked out of the PHAST-12E on either the rising or falling edge of RXTB1CLK depending on the setting of the CKINV1 control bit. The RX Telecom Bus 1 outputs can be tristated through software control or through the EN_COMBUS lead. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** SPE and TOH data from received STM-1 1/STS-3c 1 are output. **1xSTM-4c/STS-12c modes:** SPE and TOH data from the MSByte of the received STM-4c/STS-12c are output.
RXTB1CLK	M05	O	LVTTL	**Telecom Bus 1 Receive Clock:** All Telecom Bus 1 receive signals are clocked out of the PHAST-12E on the falling edge of RXTB1CLK when the CKINV1 control bit is set to 0. If CKINV1 is set to 1, the Telecom Bus 1 receive signals are clocked out on the rising edge of RXTB1CLK. The RX Telecom Bus 1 outputs can be tristated through software control or through the EN_COMBUS lead. **4xSTM-1/STS-3c mode:** This clock is 19.44 MHz and is asynchronous with respect to the other RXTB#CLK outputs. **1xSTM-4/STS-12 mode:** This clock is 19.44 MHz and is frequency synchronous with respect to the other RXTB#CLK outputs. **1xSTM-4c/STS-12c modes:** This clock is 19.44 MHz and is synchronous with respect to the other RXTB#CLK outputs.

Lead Name	Lead No.	I/O	Type	Lead Description
RXTB1J0J1	N08	O	LVTTL	**Telecom Bus 1 Receive J0J1 Signal:** The RX Telecom Bus 1 outputs can be tristated through software control or through the EN_COMBUS lead. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** When the CPOS control bit in the OR1Conf13 register is set to 1, this signal identifies the first J0 byte in the RXTB1DATA(7:0) stream when RXTB1J0J1 is high and RXTB1SPE is low, while the J1 byte in the RXTB1DATA(7:0) stream is identified when RXTB1J0J1 and RXTB1SPE are high. When CPOS is set to 0, RXTB1J0J1 goes high only during the last A2 byte time of the RXTB1DATA(7:0) signal. This signal is independent of the other RXTB#J0J1 signals. **1xSTM-4c/STS-12c modes:** When the control bit CPOS is set to 1, this signal identifies the first J0 byte in the RXTB1DATA(7:0) stream when RXTB1J0J1 is high and RXTB1SPE is low, while the J1 byte in the RXTB1DATA(7:0) stream is identified when RXTB1J0J1 and RXTB1SPE are high. When CPOS is set to 0, RXTB1J0J1 goes high only during the last A2 byte time of the RXTB1DATA(7:0) signal. When CPOS is set to 0, RXTB1J0J1 goes high only during the last A2 byte time of the RXTB1DATA(7:0) signal. RXTB2J0J1, RXTB3J0J1, and RXTB4J0J1 all follow RXTB1J0J1.

Lead Name	Lead No.	I/O	Type	Lead Description
RXTB1SPE	R08	O	LVTTL	**Telecom Bus 1 Receive SPE Signal:** RXTB1SPE is high during the SPE bytes of RXTB1DATA(7:0) and is low otherwise. The RX Telecom Bus 1 outputs can be tristated through software control or through the EN_COMBUS lead. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** If a pointer decrement occurs, RXTB1SPE will go high coincident with the three H3 bytes in RXTB1DATA(7:0). If a pointer increment occurs, RXTB1SPE will go low coincident with the three SPE bytes immediately after the H3 bytes in the RXTB1DATA(7:0) stream. This signal is independent of the other RXTB#SPE signals. **1xSTM-4c/STS-12c modes:** If a pointer decrement occurs, RXTB1SPE will go high coincident with the three H3 bytes in RXTB1DATA(7:0), RXTB2SPE will go high coincident with the three H3 bytes in RXTB2DATA(7:0), RXTB3SPE will go high coincident with the three H3 bytes in RXTB3DATA(7:0), and RXTB4SPE will go high coincident with the three H3 bytes in RXTB4DATA(7:0). If a pointer increment occurs, RXTB1SPE will go low coincident with the three SPE bytes immediately after the last H3 byte in the RXTB1DATA(7:0) stream, RXTB2SPE will go low coincident with the three SPE bytes immediately after the last H3 byte in the RXTB2DATA(7:0) stream, RXTB3SPE will go low coincident with the three SPE bytes immediately after the last H3 byte in the RXTB3DATA(7:0) stream, and RXTB4SPE will go low coincident with the three SPE bytes immediately after the last H3 byte in the RXTB4DATA(7:0) stream. RXTB#SPE are set identically.
RXTB1PAR	P06	O	LVTTL	**Telecom Bus 1 Receive Parity Signal:** Parity for the receive signals of Telecom Bus 1. It is calculated by the PHAST-12E according to the settings of the PAR_FULL and PAR_EVEN bits in the OR1Conf13 register. The RX Telecom Bus 1 outputs can be tristated through software control or through the EN_COMBUS lead.

Lead Name	Lead No.	I/O	Type	Lead Description
RXTB1FAIL	N06	O	LVTTL	**Telecom Bus 1 Receive Failure Indication:** RXTB1FAIL goes high when the PHAST-12E detects errors that would cause an all 1s AIS to be generated. RXTB1FAIL will stay active as long as the failure condition exists. This lead will also operate in ATM/PPP mode. The RX Telecom Bus 1 outputs can be tristated through software control or through the EN_COMBUS lead. **4xSTM-1/STS-3c mode:** All 1s AIS is generated in RXTB1DATA(7:0) when one of the conditions shown in Figure 58 on page 157 occurs. This signal is independent of the other RXTB#FAIL signals. **1xSTM-4/STS-12 mode:** All 1s AIS is generated in RXTB#DATA(7:0) (#=1-4 for all 1s AIS generated by line alarms; for all 1s AIS generated by a path Alarm, # corresponds to the channel that detected the alarm) when one of the conditions shown in Figure 58 on page 157 occurs. **1xSTM-4c/STS-12c modes:** All 1s AIS is generated in RXTB#DATA(7:0) (#=1-4) when one of the conditions shown in Figure 58 on page 157 occurs. All of the RXTB#FAIL leads are asserted and deasserted together.
RXTB2DATA(7) RXTB2DATA(6) RXTB2DATA(5) RXTB2DATA(4) RXTB2DATA(3) RXTB2DATA(2) RXTB2DATA(1) RXTB2DATA(0)	L04 K02 K04 K06 J04 H02 H04 H06	O	LVTTL	**Telecom Bus 2 Receive Data:** Bit 7 is the MSB and is received first. Bit 0 is the LSB and is received last. All TOH and SPE data are passed out of the PHAST-12E and are not modified. The data on these leads are clocked out of the PHAST-12E on either the rising or falling edge of RXTB2CLK depending on the setting of the CKINV2 control bit. The RX Telecom Bus 2 outputs can be tristated through software control or through the EN_COMBUS lead. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** SPE and TOH data from received STM-1 2/STS-3c 2 are output. **1xSTM-4c/STS-12c modes:** SPE and TOH data from the 2nd MSByte of the received STM-4c/STS-12c are output.
RXTB2CLK	H07	O	LVTTL	**Telecom Bus 2 Receive Clock:** All Telecom Bus 2 receive signals are clocked out of the PHAST-12E on the falling edge of RXTB2CLK when the CKINV2 control bit is set to 0. If CKINV2 is set to 1, the Telecom Bus 2 receive signals are clocked out on the rising edge of RXTB2CLK. The RX Telecom Bus 2 outputs can be tristated through software control or through the EN_COMBUS lead. **4xSTM-1/STS-3c mode:** This clock is 19.44 MHz and is asynchronous with respect to the other RXTB#CLK outputs. **1xSTM-4/STS-12 mode:** This clock is 19.44 MHz and is frequency synchronous with respect to the other RXTB#CLK outputs. **1xSTM-4c/STS-12c modes:** This clock is 19.44 MHz and is synchronous with respect to the other RXTB#CLK outputs.

Lead Name	Lead No.	I/O	Type	Lead Description
RXTB2J0J1	J08	O	LVTTL	**Telecom Bus 2 Receive J0J1 Signal:** The RX Telecom Bus 2 outputs can be tristated through software control or through the EN_COMBUS lead. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** When the CPOS control bit in the OR2Conf13 register is set to 1, this signal identifies the first J0 byte in the RXTB2DATA(7:0) stream when RXTB2J0J1 is high and RXTB2SPE is low, while the J1 byte in the RXTB2DATA(7:0) stream is identified when RXTB2J0J1 and RXTB2SPE are high. When CPOS is set to 0, RXTB2J0J1 goes high only during the last A2 byte time of the RXTB2DATA(7:0) signal. This signal is independent of the other RXTB#J0J1 signals. **1xSTM-4c/STS-12c modes:** RXTB2J0J1, RXTB3J0J1, and RXTB4J0J1 all follow RXTB1J0J1.
RXTB2SPE	L08	O	LVTTL	**Telecom Bus 2 Receive SPE Signal:** RXTB2SPE is high during the SPE bytes of RXTB2DATA(7:0) and is low otherwise. The RX Telecom Bus 2 outputs can be tristated through software control or through the EN_COMBUS lead. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** If a pointer decrement occurs, RXTB2SPE will go high coincident with the three H3 bytes in RXTB2DATA(7:0). If a pointer increment occurs, RXTB2SPE will go low coincident with the three SPE bytes immediately after the H3 bytes in the RXTB2DATA(7:0) stream. This signal is independent of the other RXTB#SPE signals. **1xSTM-4c/STS-12c modes:** If a pointer decrement occurs, RXTB1SPE will go high coincident with the three H3 bytes in RXTB1DATA(7:0), RXTB2SPE will go high coincident with the three H3 bytes in RXTB2DATA(7:0), RXTB3SPE will go high coincident with the three H3 bytes in RXTB3DATA(7:0), and RXTB4SPE will go high coincident with the three H3 bytes in RXTB4DATA(7:0). If a pointer increment occurs, RXTB1SPE will go low coincident with the three SPE bytes immediately after the last H3 byte in the RXTB1DATA(7:0) stream, RXTB2SPE will go low coincident with the three SPE bytes immediately after the last H3 byte in the RXTB2DATA(7:0) stream, RXTB3SPE will go low coincident with the three SPE bytes immediately after the last H3 byte in the RXTB3DATA(7:0) stream, and RXTB4SPE will go low coincident with the three SPE bytes immediately after the last H3 byte in the RXTB4DATA(7:0) stream. RXTB#SPE are all set identically.
RXTB2PAR	M07	O	LVTTL	**Telecom Bus 2 Receive Parity Signal:** Parity for the receive signals of Telecom Bus 2. It is calculated by the PHAST-12E according to the settings of the PAR_FULL and PAR_EVEN bits in the OR2Conf13 register. The RX Telecom Bus 2 outputs can be tristated through software control or through the EN_COMBUS lead.

Lead Name	Lead No.	I/O	Type	Lead Description
RXTB2FAIL	K07	O	LVTTL	**Telecom Bus 2 Receive Failure Indication:** RXTB2FAIL goes high when the PHAST-12E detects errors that would cause an all 1s AIS to be generated. RXTB2FAIL will stay active as long as the failure condition exists. This lead will also operate in ATM/PPP mode. The RX Telecom Bus 2 outputs can be tristated through software control or through the EN_COMBUS lead. **4xSTM-1/STS-3c mode:** All 1s AIS is generated in RXTB2DATA(7:0) when one of the conditions shown in Figure 58 on page 157 occurs. This signal is independent of the other RXTB#FAIL signals. **1xSTM-4/STS-12 mode:** All 1s AIS is generated in RXTB#DATA(7:0) (#=1-4 for all 1s AIS generated by line alarms; for all 1s AIS generated by a path Alarm, # corresponds to the channel that detected the alarm) when one of the conditions shown in Figure 58 on page 157 occurs. **1xSTM-4c/STS-12c modes:** All 1s AIS is generated in RXTB#DATA(7:0) (#=1-4) when one of the conditions shown in Figure 58 on page 157 occurs. All of the RXTB#FAIL leads are asserted and deasserted together.
RXTB3DATA(7) RXTB3DATA(6) RXTB3DATA(5) RXTB3DATA(4) RXTB3DATA(3) RXTB3DATA(2) RXTB3DATA(1) RXTB3DATA(0)	G04 F02 F04 D02 D04 B02 B04 A04	O	LVTTL	**Telecom Bus 3 Receive Data:** Bit 7 is the MSB and is received first. Bit 0 is the LSB and is received last. All TOH and SPE data are passed out of the PHAST-12E and are not modified. The data on these leads are clocked out of the PHAST-12E on either the rising or falling edge of RXTB3CLK depending on the setting of the CKINV3 control bit. The RX Telecom Bus 3 outputs can be tristated through software control or through the EN_COMBUS lead. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** SPE and TOH data from received STM-1 3/STS-3c 3 are output. **1xSTM-4c/STS-12c modes:** SPE and TOH data from the 3rd MSByte of the received STM-4c/STS-12c are output.
RXTB3CLK	C02	O	LVTTL	**Telecom Bus 3 Receive Clock:** All Telecom Bus 3 receive signals are clocked out of the PHAST-12E on the falling edge of RXTB3CLK when the CKINV3 control bit is set to 0. If CKINV3 is set to 1, the Telecom Bus 3 receive signals are clocked out on the rising edge of RXTB3CLK. The RX Telecom Bus 3 outputs can be tristated through software control or through the EN_COMBUS lead. **4xSTM-1/STS-3c mode:** This clock is 19.44 MHz and is asynchronous with respect to the other RXTB#CLK outputs. **1xSTM-4/STS-12 mode:** This clock is 19.44 MHz and is frequency synchronous with respect to the other RXTB#CLK outputs. **1xSTM-4c/STS-12c modes:** This clock is 19.44 MHz and is synchronous with respect to the other RXTB#CLK outputs.

Lead Name	Lead No.	I/O	Type	Lead Description
RXTB3J0J1	B05	O	LVTTL	**Telecom Bus 3 Receive J0J1 Signal:** The RX Telecom Bus 3 outputs can be tristated through software control or through the EN_COMBUS lead. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** When the CPOS control bit in the OR3Conf13 register is set to 1, this signal identifies the first J0 byte in the RXTB3DATA(7:0) stream when RXTB3J0J1 is high and RXTB3SPE is low, while the J1 byte in the RXTB3DATA(7:0) stream is identified when RXTB3J0J1 and RXTB3SPE are high. When CPOS is set to 0, RXTB3J0J1 goes high only during the last A2 byte time of the RXTB3DATA(7:0) signal. This signal is independent of the other RXTB#J0J1 signals. **1xSTM-4c/STS-12c modes:** RXTB2J0J1, RXTB3J0J1, and RXTB4J0J1 all follow RXTB1J0J1.
RXTB3SPE	D05	O	LVTTL	**Telecom Bus 3 Receive SPE Signal:** RXTB3SPE is high during the SPE bytes of RXTB3DATA(7:0) and is low otherwise. The RX Telecom Bus 3 outputs can be tristated through software control or through the EN_COMBUS lead. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** If a pointer decrement occurs, RXTB3SPE will go high coincident with the three H3 bytes in RXTB3DATA(7:0). If a pointer increment occurs, RXTB3SPE will go low coincident with the three SPE bytes immediately after the H3 bytes in the RXTB3DATA(7:0) stream. This signal is independent of the other RXTB#SPE signals. **1xSTM-4c/STS-12c modes:** If a pointer decrement occurs, RXTB1SPE will go high coincident with the three H3 bytes in RXTB1DATA(7:0), RXTB2SPE will go high coincident with the three H3 bytes in RXTB2DATA(7:0), RXTB3SPE will go high coincident with the three H3 bytes in RXTB3DATA(7:0), and RXTB4SPE will go high coincident with the three H3 bytes in RXTB4DATA(7:0). If a pointer increment occurs, RXTB1SPE will go low coincident with the three SPE bytes immediately after the last H3 byte in the RXTB1DATA(7:0) stream, RXTB2SPE will go low coincident with the three SPE bytes immediately after the last H3 byte in the RXTB2DATA(7:0) stream, RXTB3SPE will go low coincident with the three SPE bytes immediately after the last H3 byte in the RXTB3DATA(7:0) stream, and RXTB4SPE will go low coincident with the three SPE bytes immediately after the last H3 byte in the RXTB4DATA(7:0) stream. RXTB#SPE are all set identically.
RXTB3PAR	F06	O	LVTTL	**Telecom Bus 3 Receive Parity Signal:** Parity for the receive signals of Telecom Bus 3. It is calculated by the PHAST-12E according to the settings of the PAR_FULL and PAR_EVEN bits in the OR3Conf13 register. The RX Telecom Bus 3 outputs can be tristated through software control or through the EN_COMBUS lead.

Lead Name	Lead No.	I/O	Type	Lead Description
RXTB3FAIL	E04	O	LVTTL	**Telecom Bus 3 Receive Failure Indication:** RXTB3FAIL goes high when the PHAST-12E detects errors that would cause an all 1s AIS to be generated. RXTB3FAIL will stay active as long as the failure condition exists. This lead will also operate in ATM/PPP mode. The RX Telecom Bus 3 outputs can be tristated through software control or through the EN_COMBUS lead. **4xSTM-1/STS-3c mode:** All 1s AIS is generated in RXTB3DATA(7:0) when one of the conditions shown in Figure 58 on page 157 occurs. This signal is independent of the other RXTB#FAIL signals. **1xSTM-4/STS-12 mode:** All 1s AIS is generated in RXTB#DATA(7:0) (#=1-4 for all 1s AIS generated by line alarms; for all 1s AIS generated by a path Alarm, # corresponds to the channel that detected the alarm) when one of the conditions shown in Figure 58 on page 157 occurs. **1xSTM-4c/STS-12c modes:** All 1s AIS is generated in RXTB#DATA(7:0) (#=1-4) when one of the conditions shown in Figure 58 on page 157 occurs. All of the RXTB#FAIL leads are asserted and deasserted together.
RXTB4DATA(7) RXTB4DATA(6) RXTB4DATA(5) RXTB4DATA(4) RXTB4DATA(3) RXTB4DATA(2) RXTB4DATA(1) RXTB4DATA(0)	C08 A08 F09 B09 G10 E10 C10 A10	O	LVTTL	**Telecom Bus 4 Receive Data:** Bit 7 is the MSB and is received first. Bit 0 is the LSB and is received last. All TOH and SPE data are passed out of the PHAST-12E and are not modified. The data on these leads are clocked out of the PHAST-12E on either the rising or falling edge of RXTB4CLK depending on the setting of the CKINV4 control bit. The RX Telecom Bus 4 outputs can be tristated through software control or through the EN_COMBUS lead. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** SPE and TOH data from received STM-1 4/STS-3c 4 are output. **1xSTM-4c/STS-12c modes:** SPE and TOH data from the LSByte of the received STM-4c/STS-12c are output.
RXTB4CLK	A06	O	LVTTL	**Telecom Bus 4 Receive Clock:** All Telecom Bus 4 receive signals are clocked out of the PHAST-12E on the falling edge of RXTB4CLK when the CKINV4 control bit is set to 0. If CKINV4 is set to 1, the Telecom Bus 4 receive signals are clocked out on the rising edge of RXTB4CLK. The RX Telecom Bus 4 outputs can be tristated through software control or through the EN_COMBUS lead. **4xSTM-1/STS-3c mode:** This clock is 19.44 MHz and is asynchronous with respect to the other RXTB#CLK outputs. **1xSTM-4/STS-12 mode:** This clock is 19.44 MHz and is frequency synchronous with respect to the other RXTB#CLK outputs. **1xSTM-4c/STS-12c modes:** This clock is 19.44 MHz and is synchronous with respect to the other RXTB#CLK outputs.

Lead Name	Lead No.	I/O	Type	Lead Description
RXTB4J0J1	B06	O	LVTTL	**Telecom Bus 4 Receive J0J1 Signal:** The RX Telecom Bus 4 outputs can be tristated through software control or through the EN_COMBUS lead. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** When the CPOS control bit in the OR4Conf13 register is set to 1, this signal identifies the first J0 byte in the RXTB4DATA(7:0) stream when RXTB4J0J1 is high and RXTB4SPE is low, while the J1 byte in the RXTB4DATA(7:0) stream is identified when RXTB4J0J1 and RXTB4SPE are high. When CPOS is set to 0, RXTB4J0J1 goes high only during the last A2 byte time of the RXTB4DATA(7:0) signal. This signal is independent of the other RXTB#J0J1 signals. **1xSTM-4c/STS-12c modes:** RXTB2J0J1, RXTB3J0J1, and RXTB4J0J1 all follow RXTB1J0J1.
RXTB4SPE	D07	O	LVTTL	**Telecom Bus 4 Receive SPE Signal:** RXTB4SPE is high during the SPE bytes of RXTB4DATA(7:0) and is low otherwise. The RX Telecom Bus 4 outputs can be tristated through software control or through the EN_COMBUS lead. **4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes:** If a pointer decrement occurs, RXTB4SPE will go high coincident with the three H3 bytes in RXTB4DATA(7:0). If a pointer increment occurs, RXTB4SPE will go low coincident with the three SPE bytes immediately after the H3 bytes in the RXTB4DATA(7:0) stream. This signal is independent of the other RXTB#SPE signals. **1xSTM-4c/STS-12c modes:** If a pointer decrement occurs, RXTB1SPE will go high coincident with the three H3 bytes in RXTB1DATA(7:0), RXTB2SPE will go high coincident with the three H3 bytes in RXTB2DATA(7:0), RXTB3SPE will go high coincident with the three H3 bytes in RXTB3DATA(7:0), and RXTB4SPE will go high coincident with the three H3 bytes in RXTB4DATA(7:0). If a pointer increment occurs, RXTB1SPE will go low coincident with the three SPE bytes immediately after the last H3 byte in the RXTB1DATA(7:0) stream, RXTB2SPE will go low coincident with the three SPE bytes immediately after the last H3 byte in the RXTB2DATA(7:0) stream, RXTB3SPE will go low coincident with the three SPE bytes immediately after the last H3 byte in the RXTB3DATA(7:0) stream, and RXTB4SPE will go low coincident with the three SPE bytes immediately after the last H3 byte in the RXTB4DATA(7:0) stream. RXTB#SPE are all set identically.
RXTB4PAR	G08	O	LVTTL	**Telecom Bus 4 Receive Parity Signal:** Parity for the receive signals of Telecom Bus 4. It is calculated by the PHAST-12E according to the settings of the PAR_FULL and PAR_EVEN bits in the OR4Conf13 register. The RX Telecom Bus 4 outputs can be tristated through software control or through the EN_COMBUS lead.

Lead Name	Lead No.	I/O	Type	Lead Description
RXTB4FAIL	F08	O	LVTTL	**Telecom Bus 4 Receive Failure Indication:** RXTB4FAIL goes high when the PHAST-12E detects errors that would cause an all 1s AIS to be generated. RXTB4FAIL will stay active as long as the failure condition exists. This lead will also operate in ATM/PPP mode. The RX Telecom Bus 4 outputs can be tristated through software control or through the EN_COMBUS lead. **4xSTM-1/STS-3c mode:** All 1s AIS is generated in RXTB4DATA(7:0) when one of the conditions shown in Figure 58 on page 157 occurs. This signal is independent of the other RXTB#FAIL signals. **1xSTM-4/STS-12 mode:** All 1s AIS is generated in RXTB#DATA(7:0) (#=1-4 for all 1s AIS generated by line alarms; for all 1s AIS generated by a path Alarm, # corresponds to the channel that detected the alarm) when one of the conditions shown in Figure 58 on page 157 occurs. **1xSTM-4c/STS-12c modes:** All 1s AIS is generated in RXTB#DATA(7:0) (#=1-4) when one of the conditions shown in Figure 58 on page 157 occurs. All of the RXTB#FAIL leads are asserted and deasserted together.
EN_COMBUS	W22	I	LVCMOS 2d	**Telecom Bus Enable Signal:** This lead is used in conjunction with the CB_RX#_En bits in the CBConf2 register to enable the RX Telecom Bus Outputs. A high on this lead enables the RX Telecom Bus outputs to be tristated or enabled through the CB_RX#_En bits. A low on this lead causes the RX Telecom Bus outputs to become tristated regardless of the settings of the CB_RX#_En control bits. The RX Telecom Bus outputs will be disabled if this lead is left floating. This lead is not 3.3 V tolerant.

MICROPROCESSOR INTERFACE LEADS

Lead Name	Lead No.	I/O	Type	Lead Description
INTFMODE	AF15	I	LVTTLd	**Interface Mode:** Selects the mode of operation of the microprocessor interface. INTFMODE is set high for synchronous mode. INTFMODE is set low for asynchronous mode.
INTFSELECT	W18	I	LVTTLd	**Interface Select:** Selects the type of microprocessor interface. INTFSELECT is set high for the Intel microprocessor interface. INTFSELECT is set low for the Motorola microprocessor interface.

Lead Name	Lead No.	I/O	Type	Lead Description
GPPCLK	AE15	I	LVTTLp	**GPP Clock:** Clock for the microprocessor interface in the PHAST-12E device. This clock is always required, regardless of whether an asynchronous or synchronous interface is selected via the INTFMODE lead. When an asynchronous type interface is selected, this clock can have a maximum frequency of 50 MHz. When a synchronous interface is selected, this clock can have a maximum frequency of 33.3 MHz. All signals are transferred on the falling edge of this clock when the synchronous interface is selected. For the asynchronous mode of operation, the lowest frequency that this clock can have is either 10 MHz or the frequency of the microprocessor clock, whichever is higher.
GPDATA(7) GPDATA(6) GPDATA(5) GPDATA(4) GPDATA(3) GPDATA(2) GPDATA(1) GPDATA(0)	AE14 AD14 AD15 AE16 AF17 AE17 AD17 AE18	I/O	LVTTL	**GPP Data:** (true) Bidirectional bus for data to/from the PHAST-12E GPP interface. Bit (0) is the LSB.
GPADDR(13) GPADDR(12) GPADDR(11) GPADDR(10) GPADDR(9) GPADDR(8) GPADDR(7) GPADDR(6) GPADDR(5) GPADDR(4) GPADDR(3) GPADDR(2) GPADDR(1) GPADDR(0)	AA14 AB15 AA15 Y15 W15 AC16 AA16 W16 AC17 AB17 AA17 AC18 AA18 AA19	I	LVTTL	**GPP Address:** The 14-bit address of the location within the PHAST-12E device that is to be read or written. Bit (0) is the LSB.
GPR/$\overline{W}$, $\overline{GPWR}$	Y17	I	LVTTLp	**GPP Read/Write [R/$\overline{W}$] (Motorola Mode) or Write [$\overline{WR}$] (Intel Mode):** Data transfer control signal. **Motorola Mode:** This signal is high during a data read operation and is low for a data write operation. A low enables data from the GPDATA(7:0) bus to be written into the addressed location. A high enables data to be read from the addressed location. **Intel Mode:** This signal is high during a data read operation and is low for a data write operation. A low enables data from the GPDATA(7:0) bus to be written into the addressed location.

Lead Name	Lead No.	I/O	Type	Lead Description
GPDS, GPRD	Y14	I	LVTTLp	**GPP Data Strobe [DS] (Motorola Mode) or Read [RD] (Intel Mode):** (Active low) **Motorola Mode:** When asserted low during a read cycle, this signal indicates that the PHAST-12E is to put data out on the GPDATA(7:0) bus. When asserted low during a write cycle this signal tells the PHAST-12E that there is valid data on the GPDATA(7:0) bus. **Intel Mode:** This signal is high during a data write operation and is low during a data read operation. A low enables data to be read from the addressed location.
GPDTACK, GPRDY	W17	O	LVTTL	**Data Acknowledge [DTACK] (Motorola Mode) or Ready [RDY] (Intel Mode):** (Active low) Tristate acknowledge signal. For either Intel or Motorola Mode this signal is asserted low to tell the external microprocessor that it can end the bus cycle. An external 1-3 kΩ pull-up resistor is required for this lead to ensure that the GPDTACK, GPRDY lead is pulled to its inactive state in a timely manner in order to avoid functional problems.
GPSEL	Y19	I	LVTTLp	**PHAST-12E Chip Select:** (Active low) Enable signal used to validate the address bus for read and write transfers from/to this particular PHAST-12E device.
GPINT	AC15	O	LVTTL	**Interrupt:** (Active low) Interrupt to microprocessor. For either Intel or Motorola mode, GPINT is an active low output. In the inactive state this output is tristated. An external 1-3 kΩ pull-up resistor is required for this lead to ensure that the GPINT lead is pulled to its inactive state in a timely manner in order to avoid functional problems.

SERIAL DCC INTERFACE LEADS

Lead Name	Lead No.	I/O	Type	Lead Description
TDATA1	A14	I	LVTTLd	**DCC Transmit Data 1:** Bit-serial data from an external LAPD interface controller or similar device to SFH block 1 in the PHAST-12E device. This data can optionally be provided as the D1-D3 or D4-D12 bytes as selected by a control bit. The data on this lead is sampled with the TDCLK1 clock. **4xSTM-1/STS-3c mode:** The DCC bytes for TX SONET/SDH Line 1 are accepted at this input. **1xSTM-4c/STS-12c or 1xSTM-4/STS-12 modes:** The DCC bytes for TX SONET/SDH Line 1 are accepted at this input.

Lead Name	Lead No.	I/O	Type	Lead Description
TDATA2	A15	I	LVTTLd	**DCC Transmit Data 2:** Bit-serial data from an external LAPD interface controller or similar device to SFH block 2 in the PHAST-12E device. This data can optionally be provided as the D1-D3 or D4-D12 bytes as selected by a control bit. The data on this lead is sampled with the TDCLK2 clock. **4xSTM-1/STS-3c mode:** The DCC bytes for TX SONET/SDH Line 2 are accepted at this input. **1xSTM-4c/STS-12c or 1xSTM-4/STS-12 modes:** The first set of “dummy” DCC bytes for TX SONET/SDH Line 1 are accepted at this input.
TDATA3	B15	I	LVTTLd	**DCC Transmit Data 3:** Bit-serial data from an external LAPD interface controller or similar device to SFH block 3 in the PHAST-12E device. This data can optionally be provided as the D1-D3 or D4-D12 bytes as selected by a control bit. The data on this lead is sampled with the TDCLK3 clock. **4xSTM-1/STS-3c mode:** The DCC bytes for TX SONET/SDH Line 3 are accepted at this input. **1xSTM-4c/STS-12c or 1xSTM-4/STS-12 modes:** The 2nd set of “dummy” DCC bytes for TX SONET/SDH Line 1 are accepted at this input.
TDATA4	C15	I	LVTTLd	**DCC Transmit Data 4:** Bit-serial data from an external LAPD interface controller or similar device to SFH block 4 in the PHAST-12E device. This data can optionally be provided as the D1-D3 or D4-D12 bytes as selected by a control bit. The data on this lead is sampled with the TDCLK4 clock. **4xSTM-1/STS-3c mode:** The DCC bytes for TX SONET/SDH Line 4 are accepted at this input. **1xSTM-4c/STS-12c or 1xSTM-4/STS-12 modes:** The 3rd set of “dummy” DCC bytes for TX SONET/SDH Line 1 are accepted at this input.
TDCLK1	D15	O	LVTTL	**DCC Transmit Clock 1:** The signals on TDATA1 are sampled with this clock. This is a bit clock for clocking either the D1-D3 or the D4-D12 DCC data bytes out of an external LAPD controller or similar device into SFH 1 of the PHAST-12E. The clock edge used for data sampling is selectable via a control bit.
TDCLK2	E15	O	LVTTL	**DCC Transmit Clock 2:** The signals on TDATA2 are sampled with this clock. This is a bit clock for clocking either the D1-D3 or the D4-D12 DCC data bytes out of an external LAPD controller or similar device into SFH 2 of the PHAST-12E. The clock edge used for data sampling is selectable via a control bit.

Lead Name	Lead No.	I/O	Type	Lead Description
TDCLK3	F15	O	LVTTL	**DCC Transmit Clock 3:** The signals on TDATA3 are sampled with this clock. This is a bit clock for clocking either the D1-D3 or the D4-D12 DCC data bytes out of an external LAPD controller or similar device into SFH 3 of the PHAST-12E. The clock edge used for data sampling is selectable via a control bit.
TDCLK4	G15	O	LVTTL	**DCC Transmit Clock 4:** The signals on TDATA4 are sampled with this clock. This is a bit clock for clocking either the D1-D3 or the D4-D12 DCC data bytes out of an external LAPD controller or similar device into SFH 4 of the PHAST-12E. The clock edge used for data sampling is selectable via a control bit.
RDATA1	H14	O	LVTTL	**DCC Receive Data 1:** Bit-serial D1-D3 or D4-D12 data from SFH 1 of the PHAST-12E device to an external LAPD controller device. The data on this lead is output with the RDCLK1 clock. **4xSTM-1/STS-3c mode:** The DCC bytes for RX SONET/SDH Line 1 are output on this lead. **1xSTM-4c/STS-12c or 1xSTM-4/STS-12 modes:** The DCC bytes for RX SONET/SDH Line 1 are output on this lead.
RDATA2	F14	O	LVTTL	**DCC Receive Data 2:** Bit-serial D1-D3 or D4-D12 data from SFH 2 of the PHAST-12E device to an external LAPD controller device. The data on this lead is output with the RDCLK2 clock. **4xSTM-1/STS-3c mode:** The DCC bytes for RX SONET/SDH Line 2 are output on this lead. **1xSTM-4c/STS-12c or 1xSTM-4/STS-12 modes:** The 1st set of “dummy” DCC bytes for RX SONET/SDH Line 1 are output on this lead.
RDATA3	E14	O	LVTTL	**DCC Receive Data 3:** Bit-serial D1-D3 or D4-D12 data from SFH 3 of the PHAST-12E device to an external LAPD controller device. The data on this lead is output with the RDCLK3 clock. **4xSTM-1/STS-3c mode:** The DCC bytes for RX SONET/SDH Line 3 are output on this lead. **1xSTM-4c/STS-12c or 1xSTM-4/STS-12 modes:** The 2nd set of “dummy” DCC bytes for RX SONET/SDH Line 1 are output on this lead.
RDATA4	B14	O	LVTTL	**DCC Receive Data 4:** Bit-serial D1-D3 or D4-D12 data from SFH 4 of the PHAST-12E device to an external LAPD controller device. The data on this lead is output with the RDCLK4 clock. **4xSTM-1/STS-3c mode:** The DCC bytes for RX SONET/SDH Line 4 are output on this lead. **1xSTM-4c/STS-12c or 1xSTM-4/STS-12 modes:** The 3rd set of “dummy” DCC bytes for RX SONET/SDH Line 1 are output on this lead.

Lead Name	Lead No.	I/O	Type	Lead Description
RDCLK1	B13	O	LVTTL	**DCC Receive Clock 1:** A bit clock from the PHAST-12E device for clocking the data on the RDATA1 lead into an external LAPD controller or similar device. The clock edge used for output of the RDATA1 signal is selectable via a control bit.
RDCLK2	C13	O	LVTTL	**DCC Receive Clock 2:** A bit clock from the PHAST-12E device for clocking the data on the RDATA2 lead into an external LAPD controller or similar device. The clock edge used for output of the RDATA2 signal is selectable via a control bit.
RDCLK3	F13	O	LVTTL	**DCC Receive Clock 3:** A bit clock from the PHAST-12E device for clocking the data on the RDATA3 lead into an external LAPD controller or similar device. The clock edge used for output of the RDATA3 signal is selectable via a control bit.
RDCLK4	G13	O	LVTTL	**DCC Receive Clock 4:** A bit clock from the PHAST-12E device for clocking the data on the RDATA4 lead into an external LAPD controller or similar device. The clock edge used for output of the RDATA4 signal is selectable via a control bit.

APS INTERFACE LEADS

Lead Name	Lead No.	I/O	Type	Lead Description
TXAPSDAT(8) TXAPSDAT(7) TXAPSDAT(6) TXAPSDAT(5) TXAPSDAT(4) TXAPSDAT(3) TXAPSDAT(2) TXAPSDAT(1) TXAPSDAT(0)	AD12 AC12 AB12 AA12 Y12 W12 W13 AA13 AB13	I/O I/O I/O I/O I/O I/O I/O I/O I/O	LVTTLd	**Transmit APS Data:** Bit (0) is the LSB. This is a bidirectional bus. When the PHAST-12E is configured to output data on the transmit APS interface, these leads are outputs. When the PHAST-12E is configured to accept data at it's transmit APS interface, these leads are inputs. This data bus is used to pass transmit C-4 (VC-4) data from one PHAST-12E device to another. These signals are not used in 1xSTM-4/STS-12 or 1xSTM-4c/STS-12c modes.
TXAPSPAR	W11	I/O	LVTTLd	**Transmit APS Parity:** This is a bidirectional lead. When the PHAST-12E is configured to output data on the transmit APS interface, this lead is an output and provides parity for the TXAPSDAT(8:0) bus. When the PHAST-12E is configured to accept data at it's transmit APS interface, this lead is an input and can accept parity from the PHAST-12E device that is driving the transmit APS Interface. This signal is not used in 1xSTM-4/STS-12 or 1xSTM-4c/STS-12c modes.

Lead Name	Lead No.	I/O	Type	Lead Description
TXAPSDAVA	W14	I/O	LVTTLd	**Transmit APS Provided Data Valid:** This is a bidirectional lead. When the PHAST-12E is configured to output data on the transmit APS interface, this lead is an output and indicates when data on the TXAPSDAT(8:0) bus is valid. A high means that data is valid on the considered clock edge. A low means that data is not valid. When the PHAST-12E is configured to accept data at it's transmit APS interface, this lead is an input and tells the PHAST-12E if the data being received on the TXAPSDAT(8:0) bus is valid or not. A high means that data is valid on the considered clock edge. A low means that data is not valid. This signal is not used in 1xSTM-4/STS-12 or 1xSTM-4c/STS-12c modes.
TXAPSDARQ	AE13	I/O	LVTTLd	**Transmit APS Data Request:** This is a bidirectional lead. When the PHAST-12E is configured to output data on the Transmit APS interface, this lead is an input and tells the PHAST-12E that one of the PHAST-12E devices is requesting data. A high means that data is being requested. A low means that no data is requested. When the PHAST-12E is configured to accept data from the transmit APS interface, this lead is an output and indicates when this PHAST-12E is requesting data. A high means that data is being requested. A low means that no data is requested. This signal is not used in 1xSTM-4/STS-12 or 1xSTM-4c/STS-12c modes.
RXAPSDAT(8) RXAPSDAT(7) RXAPSDAT(6) RXAPSDAT(5) RXAPSDAT(4) RXAPSDAT(3) RXAPSDAT(2) RXAPSDAT(1) RXAPSDAT(0)	AA10 AB10 AC10 AD10 AE10 AF10 AE11 AC11 AA11	I/O I/O I/O I/O I/O I/O I/O I/O I/O	LVTTLd	**Receive APS Data:** Bit (0) is the LSB. This is a bidirectional bus. When the PHAST-12E is configured to output data on the receive APS interface, these leads are outputs. When the PHAST-12E is configured to accept data from the receive APS interface, these leads are inputs. This data bus is used to pass receive C-4 (VC-4) data from one PHAST-12E device to another. These signals are not used in 1xSTM-4/STS-12 or 1xSTM-4c/STS-12c modes.
RXAPSPAR	AF12	I/O	LVTTLd	**Receive APS Parity:** This is a bidirectional lead. When the PHAST-12E is configured to output data on the receive APS interface, this lead is an output and provides parity for the RXAPSDAT(8:0) bus. When the PHAST-12E is configured to accept data from the receive APS interface, this lead is an input and accepts parity from the PHAST-12E device that is driving the receive APS Interface. This signal is not used in 1xSTM-4/STS-12 or 1xSTM-4c/STS-12c modes.

Lead Name	Lead No.	I/O	Type	Lead Description
RXAPSDAVA	AE12	I/O	LVTTLd	**Receive APS Provided Data Valid:** This is a bidirectional lead. When the PHAST-12E is configured to output data on the receive APS interface, this lead is an output and indicates when data on the RXAPSDAT(8:0) bus is valid. A high means that data is valid on the considered clock edge. A low means that data is not valid. When the PHAST-12E is configured to accept data from the receive APS interface, this lead is an input and tells the PHAST-12E if the data being received on the RXAPSDAT(8:0) bus is valid or not. A high means that data is valid on the considered clock edge. A low means that data is not valid. This signal is not used in 1xSTM-4/STS-12 or 1xSTM-4c/STS-12c modes.

EXPANSION INTERFACE LEADS

Lead Name	Lead No.	I/O	Type	Lead Description
TXEXPIN	H12	I	LVTTLd	**Expansion Interface Control:** This lead is not used, and must be left unconnected.
TXEXPOUT	D12	O	LVTTL	**Expansion Interface Control:** This lead is not used, and must be left unconnected.
RXEXPIN	H13	I	LVTTLd	**Expansion Interface Control:** This lead is not used, and must be left unconnected.
RXEXPOUT	C12	O	LVTTL	**Expansion Interface Control:** This lead is not used, and must be left unconnected.
TXFRMIN	B20	I	LVTTLd	**Expansion Interface Control:** This lead is not used, and must be left unconnected.
TXFRMOUT	B12	O	LVTTL	**Expansion Interface Control:** This lead is not used, and must be left unconnected.

RING PORT INTERFACE LEADS

Lead Name	Lead No.	I/O	Type	Lead Description
TXRINGCLK	D11	I	LVTTLd	**Transmit Ring Port Clock Input:** This signal is connected to the RXRINGCLK output of a mating PHAST-12E. TXRINGD data is clocked into the PHAST-12E on the rising edge of this clock.
TXRINGD	B11	I	LVTTLd	**Transmit Ring Port Data Input:** A serial input that is connected to a mating PHAST-12E device's RXRINGD signal to allow communication of the debounced K1, K2 and K3 bytes, Path REI and 3-Bit Path RDI, Line RDI and Line REI, New K3 Indication, Inconsistent K1 Indication, and New APS Indication for all four STM-1/STS-3cs, or the single STM-4/STS-12, or the single STM-4c/STS-12c to facilitate Ring mode operation. The data on this lead is clocked into the PHAST-12E on the rising edge of the TXRINGCLK signal. ***Please note that POH information is not transferred for those channels that are operating in Telecom Bus mode.***
RXRINGCLK	E12	O	LVTTL	**Receive Ring Port Clock Output:** RXRINGD data is output on the falling edge of this clock, which is derived from the Transmit Line Reference Clock. This clock is 19.44 MHz.
RXRINGD	G12	O	LVTTL	**Receive Ring Port Data Output:** A serial output that provides the debounced K1, K2, and K3 bytes, Path REI and 3-Bit Path RDI, Line RDI and Line REI, New K3 Indication, Inconsistent K1 Indication, and New APS Indication for all four STM-1/STS-3cs, or the single STM-4/STS-12, or the single STM-4c/STS-12c to facilitate Ring mode operation. A start sequence and an address field is used to delineate the information contained on this signal output. RXRINGD is output on the falling edge of RXRINGCLK. The data on this lead is output if the LineRING or the PathRING bits are set to 1. ***Please note that POH information is not provided for those channels that are operating in Telecom Bus mode.***

MISCELLANEOUS LEADS

Lead Name	Lead No.	I/O	Type	Lead Description
ALARM1(0) ALARM1(1) ALARM1(2) ALARM1(3) ALARM1(4)	H15 H16 F16 D16 B16	O O O O O	LVTTL	**Alarm Leads for Receive SFH 1:** The ALARM1(0:4) outputs are controlled real time by the same internal control signals that also cause the corresponding microprocessor interrupt. The alarm conditions that are output on these leads are as follows: ALARM1(0) = Loss of Signal in SFH 1 ALARM1(1) = Loss of Frame in SFH 1 ALARM1(2) = Loss of Pointer in SFH 1 ALARM1(3) = Pointer AIS in SFH 1 ALARM1(4) = Line AIS in SFH 1

Lead Name	Lead No.	I/O	Type	Lead Description
ALARM2(0) ALARM2(1) ALARM2(2) ALARM2(3) ALARM2(4)	H17 G17 F17 E17 D17	O O O O O	LVTTL	**Alarm Leads for Receive SFH 2:** The ALARM2(0:4) outputs are controlled real time by the same internal control signals that also cause the corresponding micro-processor interrupt. The alarm conditions that are output on these leads are as follows: ALARM2(0) = Loss of Signal in SFH 2 ALARM2(1) = Loss of Frame in SFH 2 ALARM2(2) = Loss of Pointer in SFH 2 ALARM2(3) = Pointer AIS in SFH 2 ALARM2(4) = Line AIS in SFH 2 These leads are not used in 1xSTM-4c/STS-12c mode. ALARM2(0), ALARM2(1), and ALARM2(4) are not used in 1xSTM-4/STS-12 mode.
ALARM3(0) ALARM3(1) ALARM3(2) ALARM3(3) ALARM3(4)	C17 B17 A17 H18 F18	O O O O O	LVTTL	**Alarm Leads for Receive SFH 3:** The ALARM3(0:4) outputs are controlled real time by the same internal control signals that also cause the corresponding micro-processor interrupt. The alarm conditions that are output on these leads are as follows: ALARM3(0) = Loss of Signal in SFH 3 ALARM3(1) = Loss of Frame in SFH 3 ALARM3(2) = Loss of Pointer in SFH 3 ALARM3(3) = Pointer AIS in SFH 3 ALARM3(4) = Line AIS in SFH 3 These leads are not used in 1xSTM-4c/STS-12c mode. ALARM3(0), ALARM3(1), and ALARM3(4) are not used in 1xSTM-4/STS-12 mode.
ALARM4(0) ALARM4(1) ALARM4(2) ALARM4(3) ALARM4(4)	D18 B18 C19 B19 A19	O O O O O	LVTTL	**Alarm Leads for Receive SFH 4:** The ALARM4(0:4) outputs are controlled real time by the same internal control signals that also cause the corresponding micro-processor interrupt. The alarm conditions that are output on these leads are as follows: ALARM4(0) = Loss of Signal in Macro 4 ALARM4(1) = Loss of Frame in Macro 4 ALARM4(2) = Loss of Pointer in Macro 4 ALARM4(3) = Pointer AIS in Macro 4 ALARM4(4) = Line AIS in Macro 4 These leads are not used in 1xSTM-4c/STS-12c modes. ALARM4(0), ALARM4(1), and ALARM4(4) are not used in 1xSTM-4/STS-12 mode.

ANALOG SIM INPUT/OUTPUT LEADS

Lead Name	Lead No.	I/O	Type	Lead Description
RXCAP1P RXCAP1N	T21 R21	I I		**On-Board Capacitor for Receive PLL 1:** A high quality 68nF or 56nF capacitor should be connected across and as close as possible to these leads. The two legs of the traces that connect the capacitor to these leads should be equal. Either a 68nF or 56nF capacitor can be used regardless of operating mode.
RXCAP2P RXCAP2N	W25 W24	I I		**On-Board Capacitor for Receive PLL 2:** A high quality 68nF or 56nF capacitor should be connected across and as close as possible to these leads. The two legs of the traces that connect the capacitor to these leads should be equal. Either a 68nF or 56nF capacitor can be used regardless of operating mode.
RXCAP3P RXCAP3N	G25 H26	I I		**On-Board Capacitor for Receive PLL 3:** A high quality 68nF or 56nF capacitor should be connected across and as close as possible to these leads. The two legs of the traces that connect the capacitor to these leads should be equal. Either a 68nF or 56nF capacitor can be used regardless of operating mode.
RXCAP4P RXCAP4N	N19 N20	I I		**On-Board Capacitor for Receive PLL 4:** A high quality 68nF or 56nF capacitor should be connected across and as close as possible to these leads. The two legs of the traces that connect the capacitor to these leads should be equal. Either a 68nF or 56nF capacitor can be used regardless of operating mode.
TXCAPP TXCAPN	R20 R19	I I		**On-Board Capacitor for the Transmit PLL:** A high quality 68nF or 56nF capacitor should be connected across and as close as possible to these leads. The two legs of the traces that connect the capacitor to these leads should be equal. Either a 68nF or 56nF capacitor can be used regardless of operating mode.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply Voltage - digital core	VDD	-0.5	3.0	V	Note 1
Supply Voltage - analog	VDD2	-0.5	3.0	V	Note 1
Supply Voltage - digital I/O	VDD3	-0.5	3.8	V	Notes 1, 5
Supply Voltage - digital I/O	VDD4	-0.5	3.8	V	Notes 1, 5
Supply Voltage - digital I/O	VDD5	-0.5	3.8	V	Notes 1, 5
Supply Voltage - analog	VDDP	-0.5	3.8	V	Note 1
Input Voltage (LVTTL)	V_{IN1}	-0.6	VDD3,4,5 + 0.6	V	Notes 1, 2
Input Voltage (LVCMOS)	V_{IN2}	-0.6	VDD3,4,5 + 0.6	V	Notes 1, 2
Input Voltage (LVCMOS2)	V_{IN3}	-0.6	VDD + 0.6	V	Notes 1, 2
Input Voltage (IPECL)	V_{IN4}	-0.6	VDD + 0.6	V	Notes 1, 6
Input Voltage (APECL)	V_{IN5}	-0.6	VDD2 + 0.6	V	Notes 1, 6
Storage Temperature	T_S	-65	150	^oC	Note 1
Ambient operating temperature range	T_A	-40	85	^oC	Note 3
Operating junction temperature range	T_J	-55	115	^oC	Note 1
Moisture Exposure level	ME		5	Level	Per JEDEC A112
Relative Humidity, during assembly	RH	30	60	%	Note 4
Relative Humidity, in-circuit	RH	8	80	%	non-condensing
ESD Classification	ESD	absolute value 2000		V	JESD22-A114-B (Human Body Model)

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. For this parameter, maximum value applies to overshoot, minimum value applies to undershoot.
3. With 0 ft/min. linear airflow and a suitable heat sink attached to the package. See the "Power Requirements, on Page 93' section below for information on operating conditions that may require the use of a heat sink.
4. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
5. VDD3, VDD4, and VDD5 should all be tied together to keep their voltage levels the same.
6. The ESD input protection diodes inside of the PHAST-12E will become activated at voltages near these levels.

TEMPERATURE LIMITATIONS / BOARD PROCESSING

The PHAST-12E's package is compatible with existing surface mount assembly tools and procedures. Typical process conditions are shown in the table below:

Process	Conditions
PCB Assembly	Infrared reflow/convection
PCB clean process	No clean solder paste
PCB rework	Remove/replace
Max placement force	300 gram*meter typical; do not exceed 600 gram*meter
Bakeout	125^{o}C/24 hours

THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Thermal Resistance - junction to ambient	θ_{JA}			19.0	^{o}C/W	0 ft/min. linear airflow
Thermal Resistance - junction to ambient	θ_{JA}			17.0	^{o}C/W	100 ft/min. linear airflow
Thermal Resistance - junction to ambient	θ_{JA}			15.0	^{o}C/W	200 ft/min. linear airflow
Thermal Resistance - junction to ambient	θ_{JA}			14.0	^{o}C/W	300 ft/min. linear airflow
Thermal Resistance - junction to ambient	θ_{JA}			13.0	^{o}C/W	400 ft/min. linear airflow
Thermal Resistance - junction to ambient	θ_{JA}			13.0	^{o}C/W	500 ft/min. linear airflow
Thermal Resistance - junction to ambient	θ_{JA}			12.0	^{o}C/W	600 ft/min. linear airflow
Thermal Resistance - junction to case	θ_{JC}			2.0	^{o}C/W	0 ft/min. linear airflow. Maximum junction temperature must be limited to 115 ^{o}C.

Notes:

1. Estimates based on CFD FlothermTM computer model results
2. 101.5 x 114.5 JEDEC 2S2P thermal test card based on document JC-15-98-69
3. Sea level conditions
4. Capped, full array modules
5. No heat sink

POWER REQUIREMENTS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (see Notes 4 and 5)	VDD,VDD2	2.38	2.50	2.62	V
Supply Voltage (see Notes 4 and 5)	VDD3, VDD4, VDD5, VDDP	3.14	3.30	3.46	V
Power Dissipation - 4 x STM-1/STS-3c (See Notes 1, 2 and 3)	P_{DD}			2.2	W
Power Dissipation - STM-4/STM-4c/STS-12/STS-12c (See Notes 1, 2 and 3)	P_{DD}			1.5	W

Notes:

1: A heat sink is required if the ambient air temperature may go above 73 ^{o}C with 0 ft/min. linear air flow.

2: The power dissipation of the PHAST-12E may be higher than expected if redundant transmit and receive PLLs are not turned off, since the device powers up with all PLLs active as a default condition. This situation may occur when operating in the STM-4/4c and STS-12/12c modes. Since this situation could occur inadvertently due to an application software hang-up or error, possibly causing overheating and damage to the PHAST-12E or surrounding components, use of a suitable heat sink is strongly recommended for all applications to prevent overheating if it does occur. Also refer to note 1 directly above. Refer to the Rx#_Enable bit description in the SIMR#Conf1 register and the Tx_Enable bit description in the SIMTConf1 register.

3: Please contact the TranSwitch Applications Engineering Department for assistance in selecting a heat sink that is suitable for the specific circumstances of your intended application. Also see application note AN-535 which can be found on the TranSwitch Internet Web Site at www.transwitch.com.

4: To ensure low output jitter, the noise on the analog power supply leads (VDD2 and VDDP) must follow the requirements listed in the table below. The output jitter of the PHAST-12E is especially dependent on the power supply noise in the 10-50 kHz range. The actual amount of filtering needed will depend on the overall board design. Other steps that can be taken to help meet jitter requirements are to separate the digital and analog power planes on the board and to use linear (non-switched) DC/DC converters to derive the 3.3 volt and 2.5 volt analog and digital chip supplies separately from a common 5 volt board supply.

5: Power must be supplied to the VDD leads before power is supplied to any of the other power leads (VDD2-5 and VDDP).

ANALOG POWER SUPPLY NOISE REQUIREMENTS

VDD2/VDDP Noise Frequency	Max	Unit
500 Hz to 5 MHz	± 5	mVpp
5 MHz to 50 MHz	+20 dB/decade slope	mVpp
Over 50 MHz	± 50	mVpp

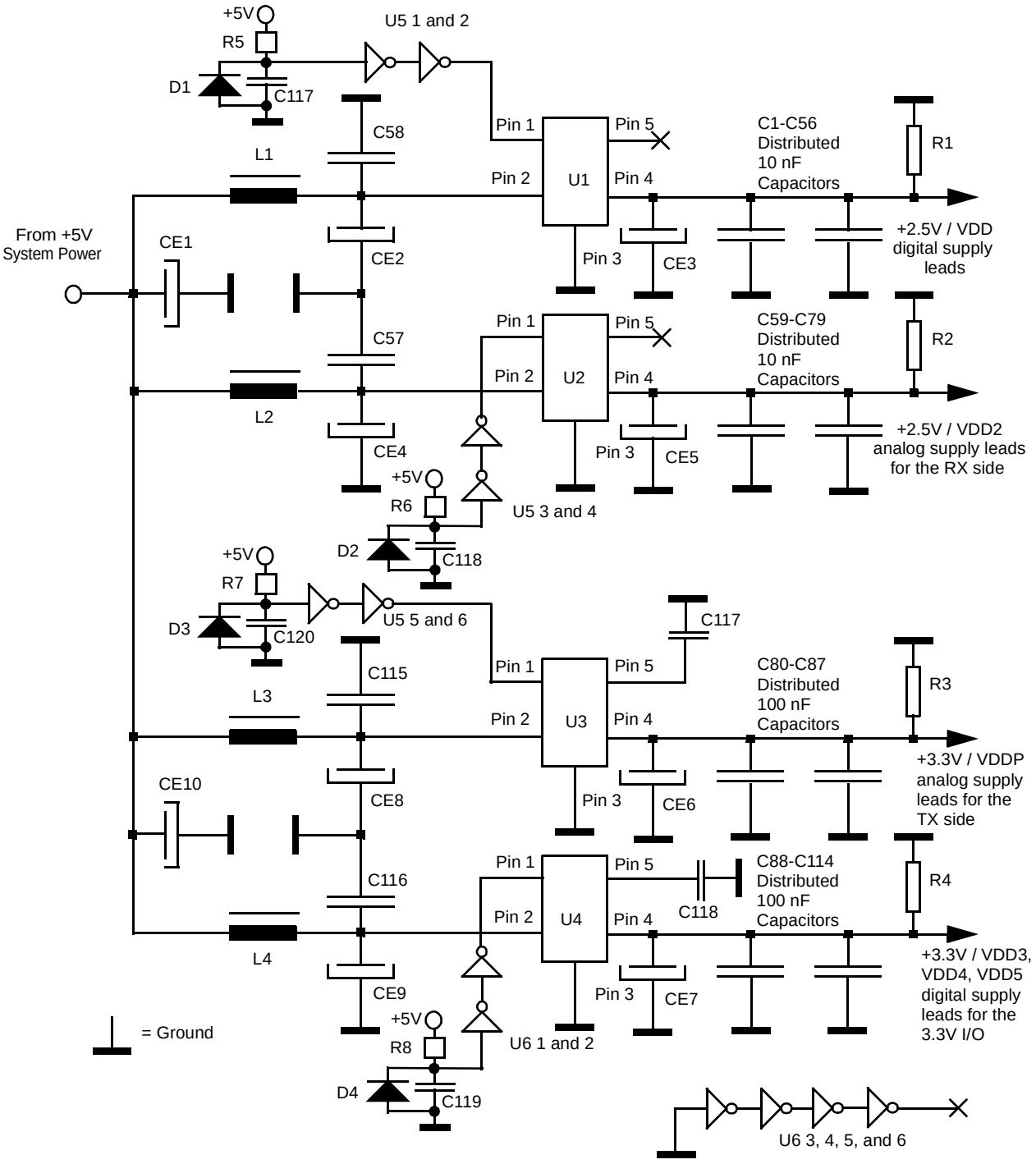


Figure 22. Power supply filter and decoupling for PHAST-12E

- L1- L4: Phillips components, wide band RF choke, catalogue number 4312 020 36643 or WBC2.5/A-3S4.
- CE1-CE5, CE8-CE10: Tantalum capacitor, low ESR type 47µF / 16V
- CE6, CE7: Tantalum capacitor, 47µF / 16V, ESR of 5Ω, and resonant frequency above 1 MHz.
- C1-C56 and C59-C79: Ceramic chip capacitors, 10nF. These capacitors are to be placed as close to the associated power leads as possible.
- C57, C58, and C80-C116: Ceramic chip capacitors, 100nF
- C117, 118: Ceramic chip capacitor, 470 pF
- U1 and U2 are low drop linear voltage regulators from Micrel, MIC39151-2.5BU. These are high quality fixed output voltage regulators with low noise, 2% accuracy / maximum 1.5A. U3 and U4 are low drop out, low noise, linear voltage regulators from Micrel, MIC5209-3.3BU, 2% accuracy / maximum 500mA. U1, U2, U3, and U4 should be supplied with adequate heat sinks per the manufacturer's requirements.
- For purposes of calculating current draw and hence selection of a heat sink for the voltage regulators, 400 mA is expected to be the maximum current drawn from VDD, 450 mA is expected to be the maximum current drawn from VDD2, and 70 mA is expected to be the maximum current drawn from VDDP. The maximum current drawn from VDD3, VDD4, and VDD5 is expected to be 220 mA.
- R1 and R2: Resistors of 220 Ω, 5% Tolerance, 1/4W guarantee a minimum load of 10mA.
- R3 and R4: Placeholders in case a different regulator is used in a future design. This resistor is not needed when the MIC5209-3.3BU is used.
- R5/C117/D1, R6/C118/D2, R7/C120/D3, and R8/C119/D4 are selected such that VDD is turned on first, a 10 microseconds delay occurs, then the other supplies (VDD2, VDD3, VDD4, VDD5, and VDDP) can be turned on in any order. i.e., The Time constant of R5 and C117 must be smaller than the time constants of the other RC networks.
- U5 and U6 are Schmitt Triggers (74HCT14) and are used to create clean transitions on the enable signals.
- D1 - D4 are 1N4001 diodes.
- Voltage regulator manufacturer's recommendations should be followed for board layout and input/output capacitor placement.

INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

For I/Os that have internal pull up resistors, a logic 1 is guaranteed to be applied at the internal circuit if the corresponding lead is left open. However, this does not mean that a logic 1 will be present at that lead. If it is required to have a logic 1 at such a floating lead, then an external pull-up will need to be supplied. On-chip pull-up resistors are about 14 kΩ and on chip pull-down resistors are about 12 kΩ. This implies that pulling the lead voltage up or down requires hundreds of nanoseconds. Transitions will be slower with large capacitive loads. For outputs where a slow transition might cause functional problems, a supplementary external 1 to 3 kΩ pull-up or pull-down resistor should be used.

When connecting any LVTTL lead that does not have an internal pull resistor to another LVTTL lead that has an internal pull-down resistor, an external pull-down resistor of 1 to 3 kΩ should be added to ensure that the signal is pulled to the appropriate logic level when the driving signal goes tristate. This only applies to connections having output signals that go to the tristate condition, where it is necessary to ensure that a valid logic level is present on the signals. An example of this would be when two PHAST-12E's are connected back-to-back across their Telecom Bus interfaces. The signals that would need the external pull-ups are the TXTB#SPE to RXTB#SPE connections and the TXTB#J0J1 to RXTB#J0J1 connections.

Input Parameters for LVTTL (3.3 Volt compatible LVTTL input or LVTTL input/output when in input mode)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.00		VDD3,4,5	V	Notes 1,10
V_{IL}	0.00		0.80	V	Note 1
Input leakage current	0		0	µA	Note 3
Input capacitance			4	pF	

Input Parameters for LVTTLp (3.3 Volt compatible LVTTL input with internal pull-up resistor)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.00		VDD3,4,5	V	Notes 1,10
V_{IL}	0.00		0.80	V	Note 1
Input leakage current	-250		0	µA	Note 3
Input capacitance			4	pF	

Input Parameters for LVTTLd (3.3 Volt compatible LVTTL input with internal pull-down resistor or LVTTL input/output with internal pull-down resistor when in input mode)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.00		VDD3,4,5	V	Notes 1,10
V_{IL}	0.00		0.80	V	Note 1
Input leakage current	0		400	µA	Note 3
Input capacitance			4	pF	

Input Parameters for LVCMOS (3.3 Volt compatible 2.5 Volt CMOS input)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	1.7		VDD3,4,5	V	
V_{IL}	0.00		0.70	V	
Input leakage current	0		0	µA	
Input capacitance			4	pF	

Input Parameters for LVCMOSd (3.3 Volt compatible 2.5 Volt CMOS input with internal pull-down resistor)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	1.7		VDD3,4,5	V	
V_{IL}	0.00		0.70	V	
Input leakage current	0		400	µA	
Input capacitance			4	pF	

Input Parameters for LVCMOS2p (2.5 Volt CMOS input with internal pull-up resistor)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	1.7		VDD	V	Note 2
V_{IL}	0.00		0.70	V	Note 2
Input leakage current	-250		0	µA	
Input capacitance			4	pF	

Input Parameters for LVCMOS2d (2.5 Volt CMOS input with internal pull-down resistor)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	1.7		VDD	V	Note 2
V_{IL}	0.00		0.70	V	Note 2
Input leakage current	0		400	µA	
Input capacitance			4	pF	

Input Parameters for IPECL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DIFF}	± 0.25	0.5	VDD+0.5	V	Note 4
V_{CM} (common mode)	0.55		2.35	V	Note 5
Input capacitance				pF	
V_{IH}			2.75	V	Note 13
V_{IL}	0.9			V	Note 13
Pulse Width Degradation			10	%	

Input Parameters for APECL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DIFF}	± 0.15		± 0.6	V	
V_{CM} (common mode)	1.125		2.1	V	
V_{IH}			2.7	V	Note 13
V_{IL}	0.9			V	Note 13
Input Differential Impedance	90		110	Ω	External 100Ω resistor installed. Otherwise, input impedance can be considered to be infinite.
Input capacitance			5	pF	
Differential Input Slew Rate	2.0			V/ns	Note 6
Pulse Width Degradation			± 120	ps	Note 7

Output Parameters for LVTTL (3.3 Volt LVTTL output or LVTTL input/output when in output mode)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4		VDD3,4,5	V	Note 10
V_{OL}	0.00		0.4	V	
I_{OL}		8		mA	Note 11
I_{OH}		12		mA	Note 12
Tristate leakage current			±25	µA	Worst case
Slew rate of output			70	mA/ns	
Output impedance		50		Ω	
Output capacitance				pF	

Output Parameters for LVTTLp (3.3 Volt LVTTL output with internal pull-up resistor)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4		VDD3,4,5	V	Note 10
V_{OL}	0.00		0.4	V	
I_{OL}		8		mA	Note 11
I_{OH}		12		mA	Note 12
Tristate leakage current			±100	µA	Worst case
Slew rate of output			70	mA/ns	
Output impedance		50		Ω	
Output capacitance				pF	

Output Parameters for LVTTLd (3.3 Volt LVTTL output with internal pull-down resistor or LVTTL input/output with internal pull-down resistor when in output mode)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4		VDD3,4,5	V	Note 10
V_{OL}	0.00		0.4	V	
I_{OL}		8		mA	Note 11
I_{OH}		12		mA	Note 12
Tristate leakage current			±100	µA	Worst case
Slew rate of output			70	mA/ns	
Approximate output impedance		50		Ω	
Output capacitance				pF	

Output Parameters for APECL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.14		2.75	V	Notes 8, 9 and 14
V_{OL}	1.55		1.75	V	Notes 8, 9 and 15
V_{OCM}	1.84		2.22	V	Notes 8, 9 and 16
V_{ODIFF}	± 0.58		± 1.08	V	Notes 8, 9 and 17
output slew rate, 2 pF	2.4		9.3	V/ns	Note 10
output slew rate, 8 pF	1.7		5.7	V/ns	Note 10

Notes:

1: Cell functionality is maintained when V_{IN} is maintained between 0.00 V and VDD3,4,5.

2: Cell functionality is maintained when V_{IN} is maintained between 0.00 V and VDD.

3: Min is tested at $V_{IN}=V_{IL(min)}$ and Max is tested at $V_{IN}=V_{IH(max)}$.

4: Minimum value is the absolute minimum input differential voltage swing.

5: This is the average differential voltage with respect to the receiver ground measured at the differential voltage crosspoint, at 200 MHz.

6: Measured at ± 200 mV differential swing.

7: Under worst case conditions (115 ^{o}C (junction temperature), 3.0V) with worst case process, and the smallest input signal (that is, 1.25 ± 0.15V and 2V/ns).

8: Minimum, Maximum values from 0 ^{o}C to 115 ^{o}C (junction temperature) 3.0V to 3.6V supply and process variation. A 100 Ω line to line resistor is assumed to be connected across the differential outputs.

9: Signal levels to temperature dependency are almost negligible.

10: VDD3,4,5 = 3.0V - 3.6V.

11: V_{OL}= 0.4V, VDD3,4,5 = 3.0V, junction temperature = 100 ^{o}C.

12: V_{OH}= 2.4V, VDD3,4,5 = 3.0V, junction temperature = 100 ^{o}C.

13: Input voltage levels must be within these bounds for optimum performance. To reduce sensitivity to jitter, it is recommended to provide a $V_{DIFF(minimum)}$ of ± 0.5, and a maximum input transition speed of 1 ns (20/80%), 2 V_{DIFF}/ns minimum around the zero crossing is preferred.

14: Voltage dependency is 0.85 V/V. $V_{OH(nom.)}$ = 2.43V. See example below.

15: Voltage dependency is 0.45 V/V. $V_{OL(nom.)}$ = 1.65V. See example below.

16: Voltage dependency is 0.67 V/V. $V_{OCM(nom.)}$ = 2.04V. See example below.

17: Voltage dependency is 0.41 V/V. $V_{ODIFF(nom.)}$ = ± 0.77V. See example below.

Example of how to use voltage dependency numbers:

Suppose it is desired to know what $V_{OH(max.)}$ would be at 3.465V (see Note 14 above).

Simply perform the following calculation:

where $V_{OH(nom.)}$ = 2.43V, V_{DDP} = 3.465V, and $V_{DDP(nom.)}$ = 3.3V

$V_{OH(max.)} = V_{OH(nom.)} + 0.85\ V/V \times (V_{DDP} - V_{DDP(nom.)})$

$V_{OH(max.)} = 2.43 + 0.85\ V/V \times (3.465 - 3.3)$

$V_{OH(max.)}$ = 2.57 Volts

TIMING CHARACTERISTICS

This section presents the detailed timing characteristics for the PHAST-12E in Figures 23 through 40. The load capacitances for the output times are indicated in each Figure as applicable. Unless otherwise indicated, timing parameters are measured at specific signal voltage levels:

1. TTL Inputs - 0.80V / 2.00V
2. TTL Outputs - 0.80V / 2.00V
3. IPECL Inputs - V-crosspoint to V-crosspoint
4. APECL Inputs - V-crosspoint to V-crosspoint
5. APECL Outputs - V-crosspoint to V-crosspoint

The specifications given in this section cover the following environmental condition:

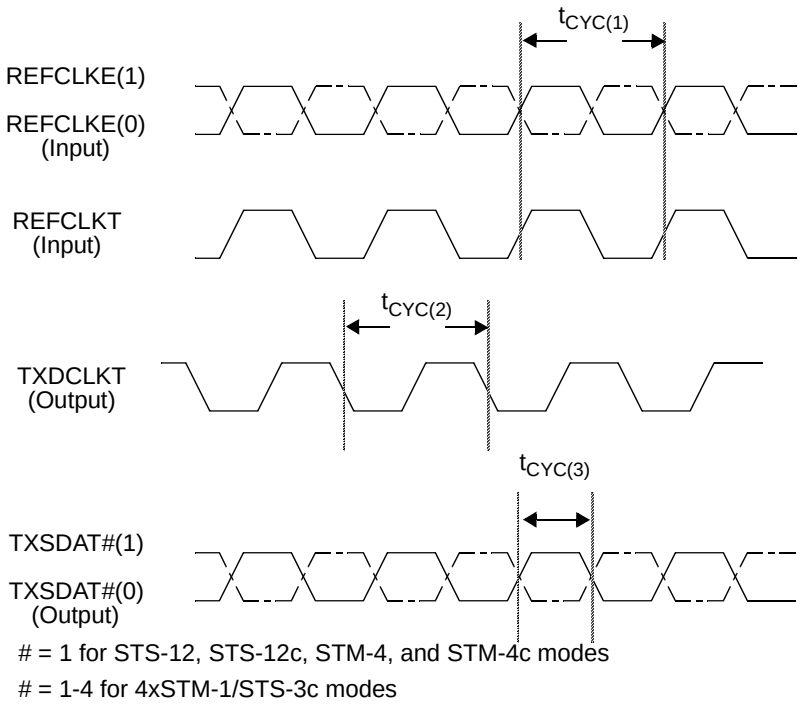
T_j = -40 ^{o}C to +115 ^{o}C, VDD = 2.5/3.3 V ± 5%

Measurements assume input rise and fall times of 2 ns (except REFCLKT/REFCLKE/RXSDAT1(0:1)). Lower and upper limits for the lead capacitance CL at the outputs are specified for each interface. All drivers are 50 Ω source-terminated. Impedance-matched interconnections are assumed.

In all timing diagrams the # symbol is used as an index and can take on the values from 1 up to 4. For instance, TDCLK# is used to compactly represent TDCLK1, TDCLK2, TDCLK3, and T1DCLK4.

Output rise and fall times are measured between 20% and 80% of the output voltage swing.

Figure 23. Serial Transmit Line Interface Timing



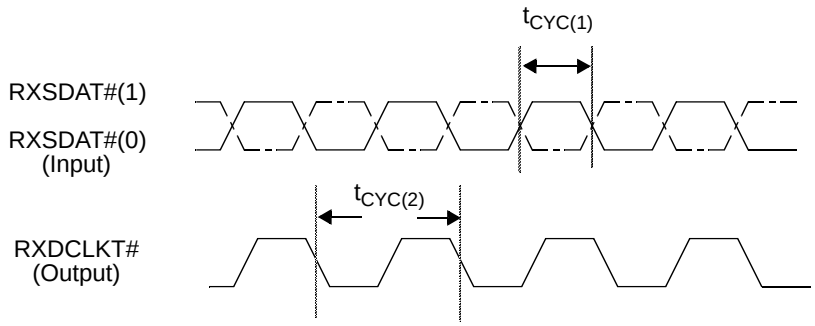
CL at outputs: 3 pF - 15 pF

Parameter	Symbol	Min	Typ	Max	Unit
REFCLKT clock period	$t_{CYC(1)}$	12.86		51.44	ns
REFCLKE clock period	$t_{CYC(1)}$	12.86		51.44	ns
REFCLKT/REFCLKE clock duty cycle		40	50	60	%
REFCLKT/REFCLKE input rise/fall time				0.5	ns
TXDCLKT clock period	$t_{CYC(2)}$	12.86		51.44	ns
TXSDAT1 period	$t_{CYC(3)}$		1.61		ns
TXSDAT2-4 period	$t_{CYC(3)}$		6.43		ns
TXSDAT1-4 output rise/fall times	t_r,t_f	0.3		0.9	ns
TXDCLKT output rise/fall times	t_{rC},t_{fC}	1.0		4.2	ns

Notes:

1. Frequencies for REFCLKT and REFCLKE inputs are selected via the Ref_Freq(1:0) configuration bits.
2. Frequency for TXDCLKT output is selected via the Tx_Div_Freq(2:0) configuration bits.
3. No phase relationship is indicated between REFCLKT/REFCLKE, TXDCLKT, or TXSDAT#.
4. TXSDOWN# are asynchronous outputs when using the serial line interface.
5. TXLPOW# are asynchronous inputs and TXSDOWN# are asynchronous outputs. Asynchronous I/O need not be shown on the timing diagrams.
6. REFCLKT/REFCLKE input rise and fall times are measured from 20% to 80% of the voltage swing.

Figure 24. Serial Receive Line Interface Timing



= 1 for STS-12, STS-12c, STM-4, and STM-4c modes
= 1-4 for 4xSTM-1/STS-3c modes

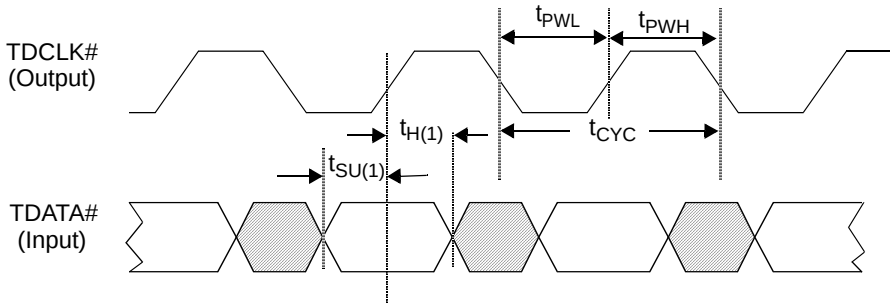
CL at outputs: 3 pF - 15 pF

Parameter	Symbol	Min	Typ	Max	Unit
RXSDAT1 input rise/fall time				0.5	ns
RXSDAT2-4 input rise/fall time				1.0	ns
RXDCLKTn clock period	$t_{CYC(2)}$	12.86		51.44	ns
RXSDAT1 period	$t_{CYC(1)}$		1.61		ns
RXSDAT2-4 period	$t_{CYC(1)}$		6.43		ns
RXDCLKT# output rise/fall times	t_{rC},t_{fC}	1.0		4.2	ns

Notes:

1. Frequencies for the RXDCLKT# outputs are selected via the Rx#_Div_Freq#(2:0) configuration bits.
2. No phase relationship is indicated between RXDCLKT# and RXSDAT#
3. LOSSSIG# are asynchronous inputs. Asynchronous I/O need not be shown on the timing diagrams.

Figure 25. Transmit Serial DCC Interface Timing



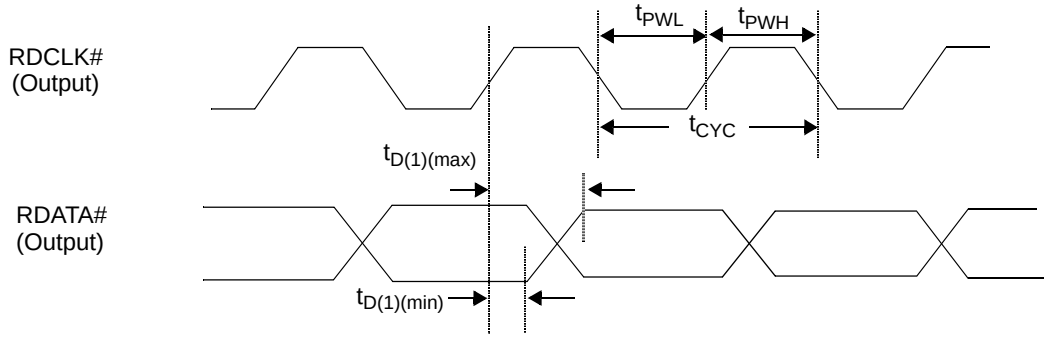
= 1 for STS-12, STS-12c, STM-4, and STM-4c modes
= 1-4 for 4xSTM-1/STS-3c modes

Note: The timing shown is for the EdgeMode bit of the OT#Conf7 register set to 1. The timing parameters remain the same when the EdgeMode bit is set to 0, except that TDATA# is sampled on the falling edge of the corresponding TDCLK#. Each TX Serial DCC Interface can be individually configured.

CL at outputs: 3 pF to 15 pF

Parameter	Symbol	Min	Typ	Max	Unit
TDCLK# clock period for 192 kbit/s D1-D3 channel	t_{CYC}	5.19	5.21	5.25	µs
TDCLK# clock period for 576 kbit/s D4-D12 channel	t_{CYC}	1.7	1.73	1.75	µs
TDCLK# duty cycle	t_{PWH}/t_{CYC}	45		55	%
TDATA# set-up time to TDCLK#↑	$t_{SU(1)}$	103			ns
TDATA# hold time after TDCLK#↑	$t_{H(1)}$	51.5			ns

Figure 26. Receive Serial DCC Interface Timing



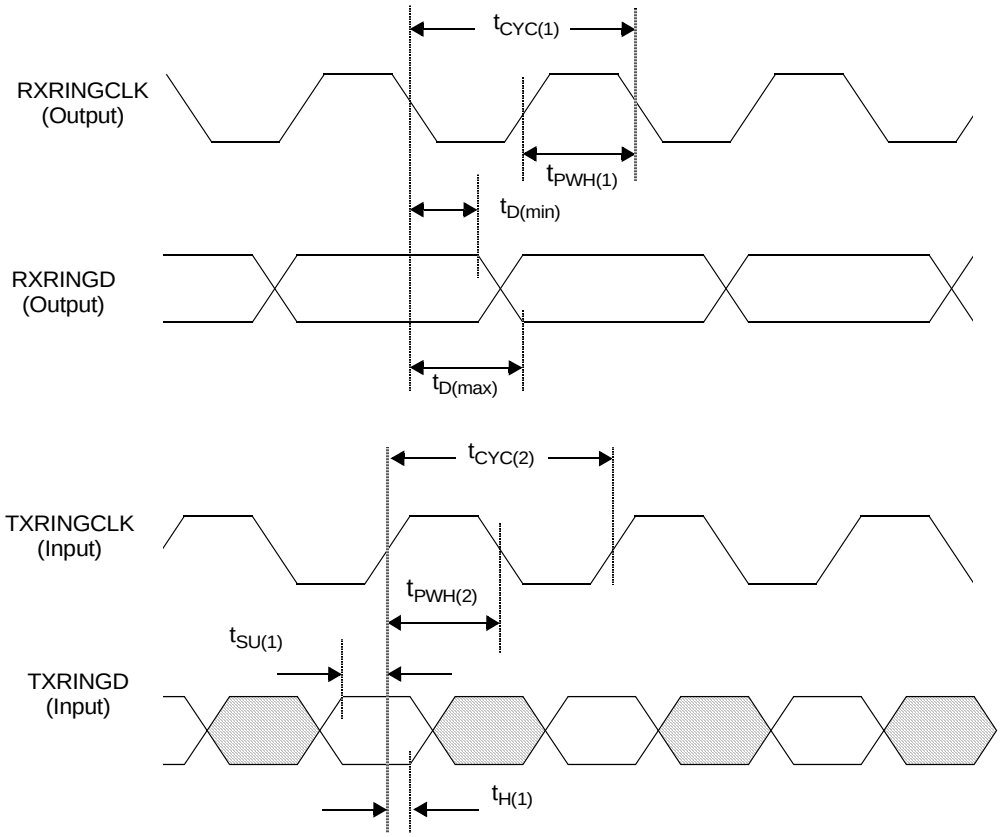
= 1 for STS-12, STS-12c, STM-4, and STM-4c modes
= 1-4 for 4xSTM-1/STS-3c modes

Note: The timing shown is for the EdgeMode bit of the OR#Conf7 register set to 1. The timing parameters remain the same when the EdgeMode bit is set to 0, except that RDATA# is output on the falling edge of the corresponding RDCLK#. Each receive Serial DCC Interface can be individually configured.

CL at outputs: 3 pF to 15 pF

Parameter	Symbol	Min	Typ	Max	Unit
RDCLK# clock period for 192 kbit/s D1-D3 channel	t_{CYC}	5.19	5.21	5.25	µs
RDCLK# clock period for 576 kbit/s D4-D12 channel	t_{CYC}	1.7	1.73	1.75	µs
RDCLK# clock duty cycle	t_{PWH}/t_{CYC}	45		55	%
RDATA# output delay from RDCLK#↑	$t_{D(1)}$	51.44-3.0		51.44+3.0	ns

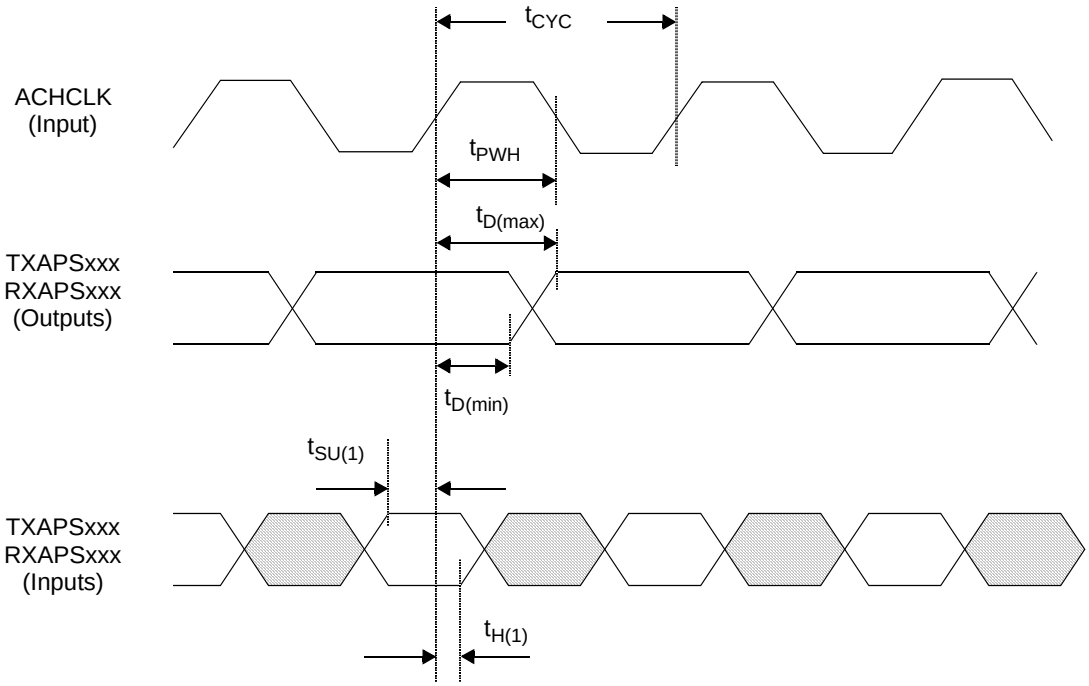
Figure 27. Ring Port Timing



CL at outputs: 3 pF to 25 pF

Parameter	Symbol	Min	Typ	Max	Unit
RXRINGCLK clock period	$t_{CYC(1)}$		51.44		ns
RXRINGCLK clock duty cycle	$t_{PWH(1)}/t_{CYC(1)}$	43		57	%
RXRINGD output delay after RXRINGCLK↓	t_D	1.3		5.6	ns
RXRINGCLK/RXRINGD output rise/fall times	t_r, t_f	1.0		4.2	ns
TXRINGCLK clock period	$t_{CYC(2)}$		51.44		ns
TXRINGCLK clock duty cycle	$t_{PWH(2)}/t_{CYC(2)}$	40		60	%
TXRINGD set-up time to TXRINGCLK↑	$t_{SU(1)}$	0.0			ns
TXRINGD hold time after TXRINGCLK↑	$t_{H(1)}$	0.8			ns

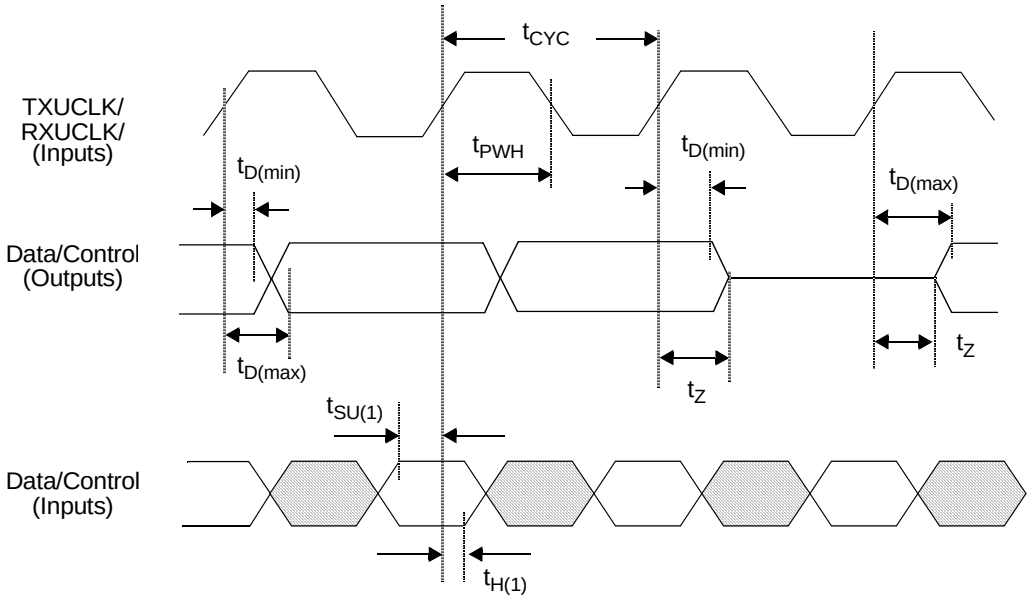
Figure 28. APS Port Timing



CL at outputs: 5 pF to 30pF

Parameter	Symbol	Min	Typ	Max	Unit
ACHCLK clock period	t_{CYC}	38.4	40	Note 1	ns
ACHLK clock duty cycle	t_{PWH}/t_{CYC}	40		60	%
TXAPSxxx/RXAPSxxx output delay after ACHCLK↑	t_D	5.0		18.5	ns
TXAPSxxx/RXAPSxxx set-up time to ACHCLK↑	$t_{SU(1)}$	0.0			ns
TXAPSxxx/RXAPSxxx hold time after ACHCLK↑	$t_{H(1)}$	1.0			ns
TXAPSxxx/RXAPSxxx output rise/fall times	t_r,t_f	0.9		4.8	ns

Figure 29. UTOPIA Level 2 (16-bit) and Level 2P Timing

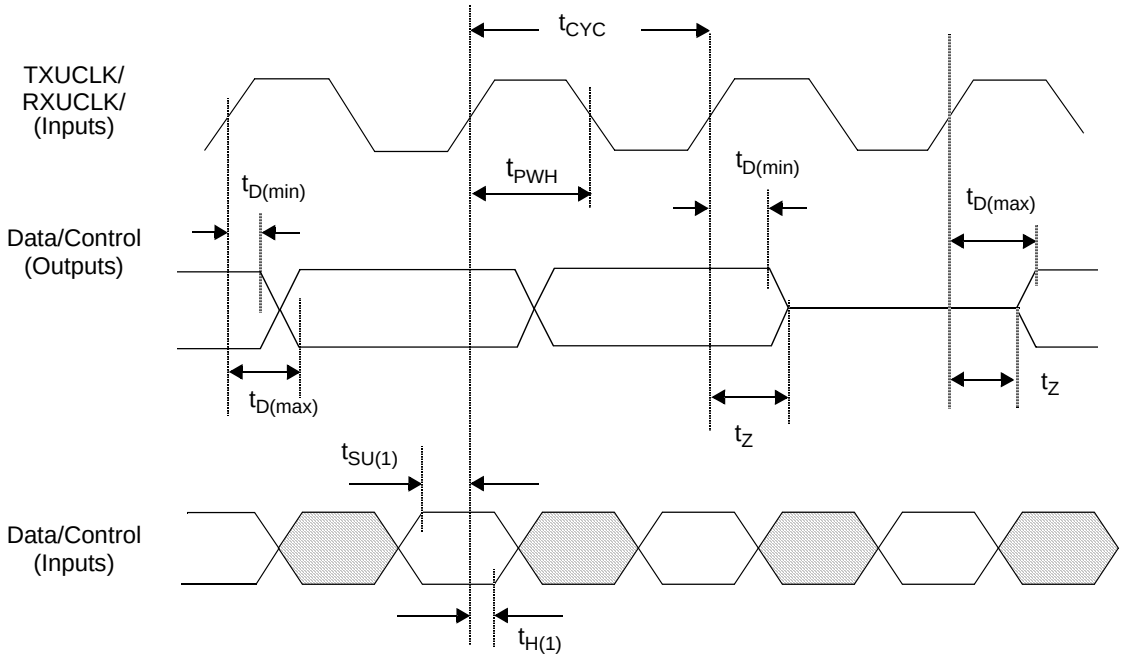


CL at outputs except for TXCLAV/PAVO: 5 pF to 40 pF. CL at TXCLAV/PAVO outputs: 5 pF to 30 pF

Parameter	Symbol	Min	Typ	Max	Unit
TXUCLK/RXUCLK clock period	t_{CYC}	19.2	20		ns
TXUCLK/RXUCLK clock duty cycle	t_{PWH}/t_{CYC}	40		60	%
TXUCLK/RXUCLK peak-to-peak jitter				5	%
TXCLAV/TPAVO tristated/driven after TXUCLK↑	t_Z	5.3		14.2	ns
TXCLAV/TPAVO delay after TXUCLK↑	t_D	4.9		14.9	ns
TXABTO tristated/driven after TXUCLK↑	t_Z	4.8		13.4	ns
TXABTO delay after TXUCLK↑	t_D	4.5		13.4	ns
RXUDATA tristated/driven after RXUCLK↑	t_Z	3.7		11.5	ns
RXUDATA delay after RXUCLK↑	t_D	3.2		11.5	ns
RXABTO/RXMSO/RXFCSEO tristated/driven after RXUCLK↑	t_Z	3.8		11.7	ns
RXABTO/RXMSO/RXFCSEO delay after RXUCLK↑	t_D	3.3		11.7	ns
RXCLAV/RPAVO tristated/driven after RXUCLK↑	t_Z	3.7		11.3	ns
RXCLAV/RPAVO delay after RXUCLK↑	t_D	3.5		11.6	ns
RXPRTY/RXSOC/RXSOFO/RXEOFO tristated/driven after RXUCLK↑	t_Z	3.7		11.3	ns
RXPRTY/RXSOC/RXSOFO/RXEOFO delay after RXUCLK↑	t_D	3.4		11.3	ns
TXUDATA/TXUADDR/TXPRTY/TXSOC/ TXSOFI/TXENB/TXEOFI/TXMSI set-up time to TXUCLK↑	$t_{SU(1)}$	3.9			ns
TXUDATA/TXUADDR/TXPRTY/TXSOC/ TXSOFI/TXENB/TXEOFI/TXMSI hold time from TXUCLK↑	$t_{H(1)}$	0.1			ns
RXUADDR/RXENB set-up time to RXUCLK↑	$t_{SU(1)}$	4.0			ns
RXUADDR/RXENB hold time from RXUCLK↑	$t_{H(1)}$	0.6			ns
UTOPIA interface output rise/fall times	t_r,t_f	1.1		5.9	ns

Note: If the UTOPIA clock frequencies go below 2 MHz the watchdog timer period may need to be changed.

Figure 30. UTOPIA Level 2 (8-bit) Timing

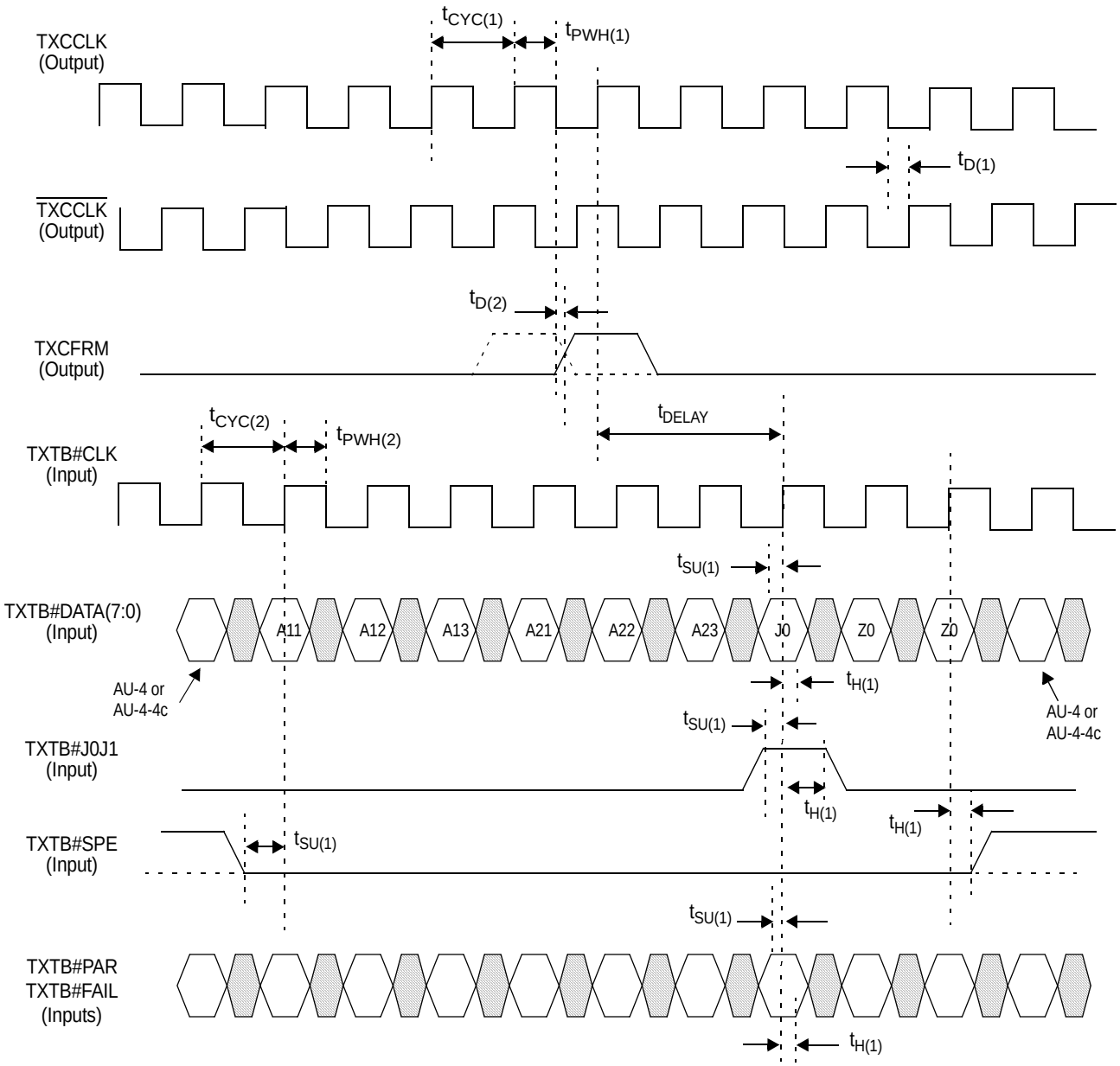


CL at all outputs: 5 pF to 40 pF

Parameter	Symbol	Min	Typ	Max	Unit
TXUCLK/RXUCLK clock period	t_{CYC}	38.4	40		ns
TXUCLK/RXUCLK clock duty cycle	t_{PWH}/t_{CYC}	40		60	%
TXUCLK/RXUCLK peak-to-peak jitter				5	%
TXCLAV tristated/driven after TXUCLK↑	t_Z	5.3		14.2	ns
TXCLAV delay after TXUCLK↑	t_D	4.5		14.9	ns
RXUDATA tristated/driven after RXUCLK↑	t_Z	3.7		11.5	ns
RXUDATA delay after RXUCLK↑	t_D	3.0		11.7	ns
RXPRTY/RXSOC/RXCLAV tristated/driven after RXUCLK↑	t_Z	3.7		11.3	ns
RXPRTY/RXSOC/RXCLAV delay after RXUCLK↑	t_D	3.0		11.7	ns
TXUDATA/TXPRTY/TXSOC/$\overline{\text{TXENB}}$ set-up time to TXUCLK↑	$t_{SU(1)}$	3.9			ns
TXUDATA/TXPRTY/TXSOC/$\overline{\text{TXENB}}$ hold time from TXUCLK↑	$t_{H(1)}$	0.1			ns
$\overline{\text{RXENB}}$ set-up time to RXUCLK↑	$t_{SU(1)}$	4.1			ns
$\overline{\text{RXENB}}$ hold time from RXUCLK↑	$t_{H(1)}$	0.6			ns
UTOPIA interface output rise/fall times	t_r,t_f	1.1		5.9	ns

Note: If the UTOPIA clock frequencies go below 2 MHz the watchdog timer period may need to be changed.

Figure 31. Transmit Telecom Bus (# = 1..4) Timing, AU-4/AU-4-4c Mode



CL at outputs: 3 pF to 25 pF

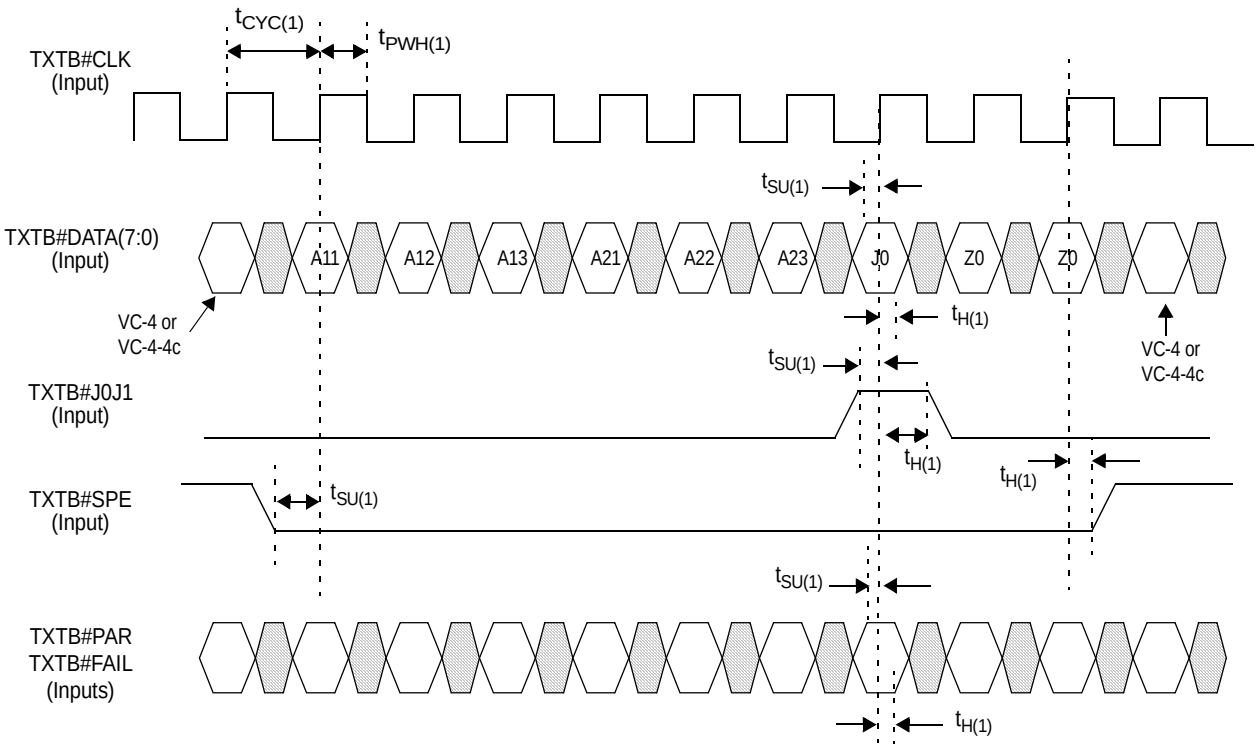
See parameter table on next page.

Parameter	Symbol	Min	Typ	Max	Unit
TXCCLK/$\overline{\text{TXCCLK}}$ clock period	$t_{CYC(1)}$		51.44		ns
TXCCLK/$\overline{\text{TXCCLK}}$ duty cycle	$t_{PWH(1)}$/ $t_{CYC(1)}$	45		55	%
$\overline{\text{TXCCLK}}\uparrow$ delay from TXCCLK$\downarrow$	$t_{D(1)}$	-1.0		1.0	ns
TXCFRM output delay from TXCCLK$\downarrow$	$t_{D(2)}$	-2.5		1.0	ns
TXTB#CLK clock period	$t_{CYC(2)}$		51.44		ns
TXTB#CLK duty cycle	$t_{PWH(2)}$/ $t_{CYC(2)}$	40		60	%
TXTB#DATA(7:0)/TXTB#J0J1/ TXTB#SPE/TXTB#PAR/TXTB#FAIL set-up time to TXTB#CLK$\uparrow$	$t_{SU(1)}$	0.6			ns
TXTB#DATA(7:0)/TXTB#J0J1/ TXTB#SPE/TXTB#PAR/TXTB#FAIL hold time after TXTB#CLK$\uparrow$	$t_{H(1)}$	0.5			ns
Delay from TXCFRM high and TXCCLK$\uparrow$ to J0 byte clocked in by TXTB#CLK	t_{DELAY}	0		3 x $t_{CYC(1)}$ - 22	ns
Transmit Telecom Bus interface output rise and fall times	t_r,t_f	0.9		4.2	ns

Notes:

1. The J1 pulse is not shown in the timing diagram but has the same timing parameters as the J0 pulse. See Figure 17.
2. The dashed line shows the TXCFRM pulse when the EFRM control bit is set to 1. The solid pulse shows the TXCFRM pulse when the EFRM control bit is set to 0. Please be aware that the t_{DELAY} window always exists with respect to the position that TXCFRM/TXCCLK$\uparrow$ has when the EFRM control bit is 0.
3. When in AU-4/AU-4-4c mode (i.e., TX Retiming is off), the J0 pulse in the TXTB#J0J1 signal does not need to be aligned to the J0 byte. In this case it can be aligned to any byte in the frame and is used as a slot identification pulse. This pulse can be in any position in the frame but must not move position (i.e., it needs to be periodic). The FRM_SLT_SEL(1:0) bits need to be programmed accordingly.
4. $t_{D(2)(min)}$ represents the time that the TXCFRM starts to change.
5. $t_{D(2)(max)}$ represents the time for TXCFRM to be stable.
6. The TXTB#SPE signal can be tied low (as shown by the dashed lines in the TXTB#SPE signal in Figure 31) if there is no J1 pulse in the TXTB#J0J1 signal. Otherwise, if there is a J1 pulse in the TXTB#J0J1 signal, then the TXTB#SPE signal needs to be high coincident with the J1 pulse. In either case, the TXTB#SPE signal needs to be low coincident with the slot identification pulse in the TXTB#J0J1 signal.

Figure 32. Transmit Telecom Bus (# = 1..4) Timing, VC-4/VC-4-4c Mode



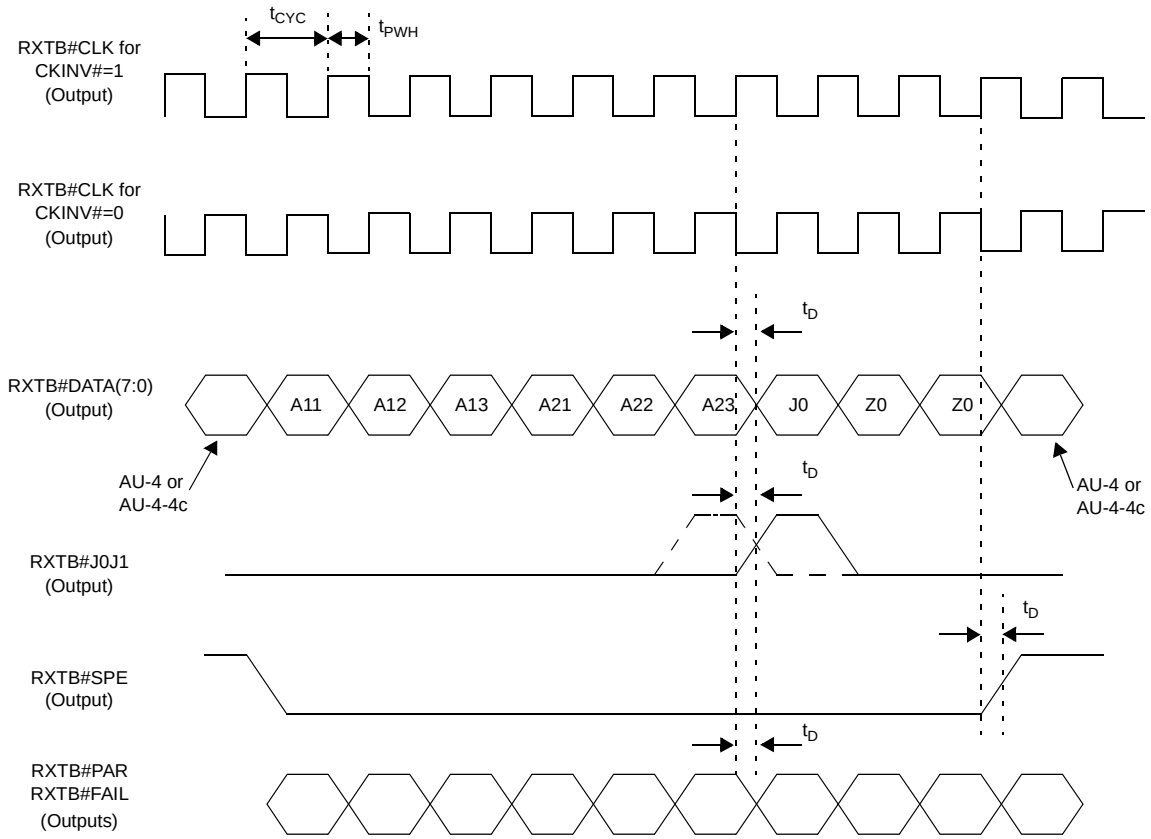
CL at outputs: 3 pF to 25 pF

Parameter	Symbol	Min	Typ	Max	Unit
TXTB#CLK clock period	$t_{CYC(1)}$		51.44		ns
TXTB#CLK duty cycle	$t_{PWH(1)}/t_{CYC(1)}$	40		60	%
TXTB#DATA(7:0)/TXTB#J0J1/ TXTB#SPE/TXTB#PAR/TXTB#FAIL set-up time to TXTB#CLK↑	$t_{SU(1)}$	0.6			ns
TXTB#DATA(7:0)/TXTB#J0J1/ TXTB#SPE/TXTB#PAR/TXTB#FAIL hold time after TXTB#CLK↑	$t_{H(1)}$	0.5			ns
Transmit Telecom Bus interface output rise and fall times	t_r,t_f	0.9		4.2	ns

Notes:

1. The J1 pulse is not shown in the timing diagram but has the same timing parameters as the J0 pulse.
2. The TXCFRM, TXCCLK, and $\overline{\text{TXCCLK}}$ outputs are still active when in VC-4/VC-4-4c mode and can be used if a 19.44 MHz clock and a corresponding frame pulse is needed.
3. The TXTB#SPE signal is required in VC-4/VC-4-4c mode (i.e., TX Retiming is turned on). The TXTB#SPE signal is required to be high during the SPE/VC time periods and is required to be low otherwise.
4. The TXTB#J0J1 pulse is required in VC-4/VC-4-4c mode. The TXTB#J0J1 contains two pulses, one pulse identifies the J0 byte location while the other pulse identifies the J1 byte location. The PHAST-12E uses the TXTB#SPE signal to determine which pulse on the TXTB#J0J1 signal goes with the J0 byte (TXTB#SPE is low) and which pulse on the TXTB#J0J1 signal goes with the J1 byte (TXTB#SPE is high).

Figure 33. Receive Telecom Bus (# = 1..4) Timing



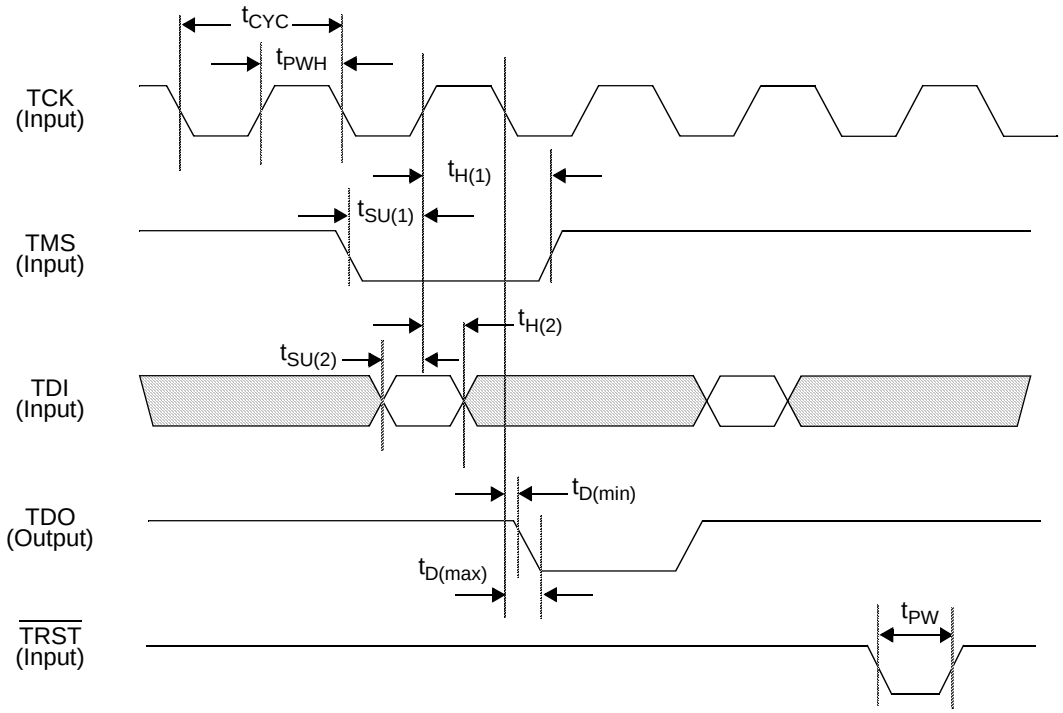
CL at outputs: 3 pF to 25 pF

Parameter	Symbol	Min	Typ	Max	Unit
RXTB#CLK clock period	t_{CYC}		51.44		ns
RXTB#CLK duty cycle	t_{PWH}/t_{CYC}	45		55	%
RXTB#DATA(7:0)/RXTB#J0J1/ RXTB#SPE/RXTB#PAR/RXTB#FAIL delay after RXTB#CLK↑ (CKINV#=1) or after RXTB#CLK↓ (CKINV#=0)	t_D	-1.4		-1.0	ns
Receive Telecom Bus interface output rise and fall times	t_r, t_f	1.3		7.5	ns

Notes:

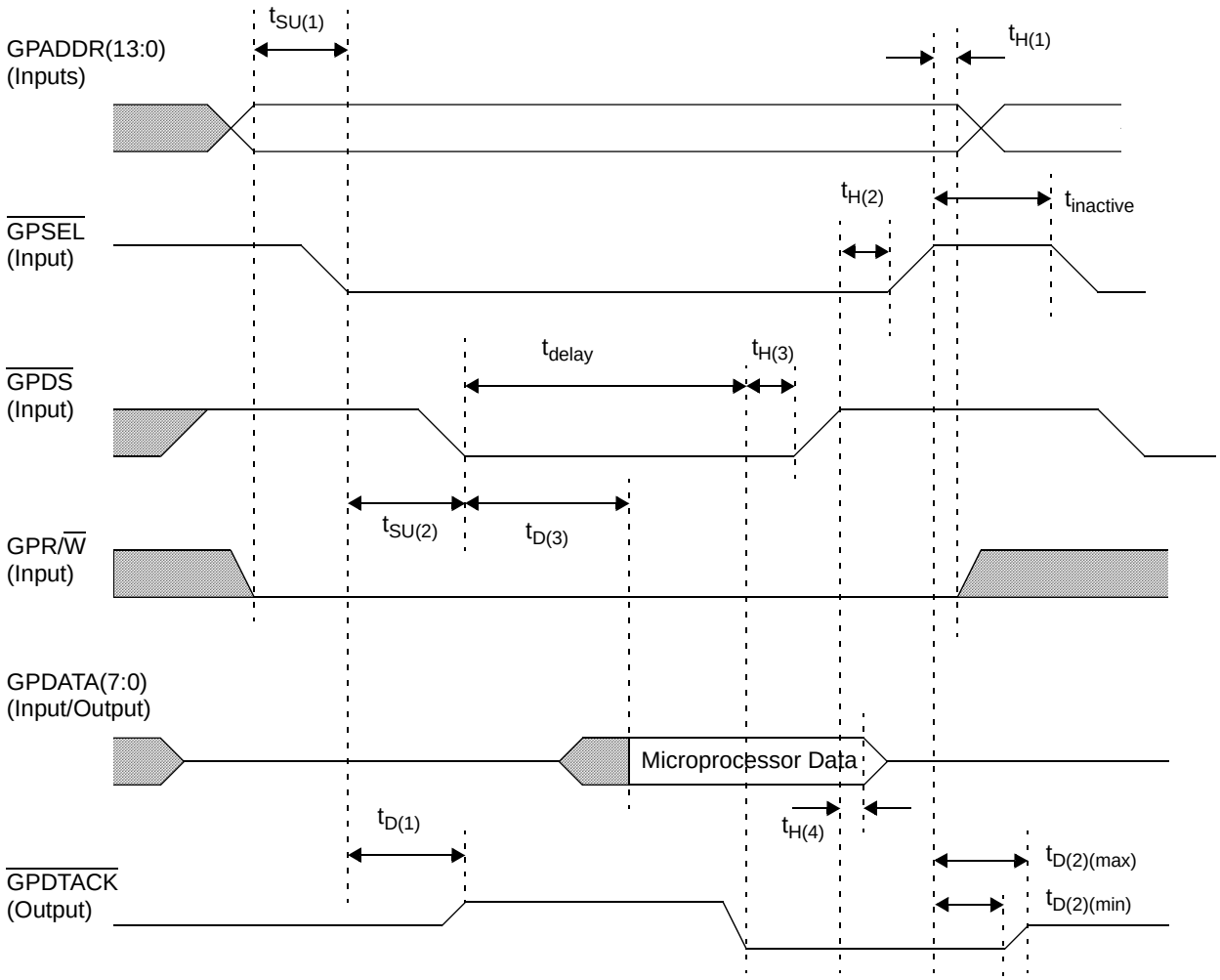
1. The dashed line in the RXTB#J0J1 signal shows the position of the J0 pulse when the corresponding CPOS bit is set to 0. When CPOS is set to 0, the J1 pulse is not present in the corresponding RXTB#J0J1 signal. The solid pulse in the RXTB#J0J1 signal shows the position of the J0 pulse when the corresponding CPOS bit is set to a 1. When CPOS is set to 1, the J1 pulse is present in the corresponding RXTB#J0J1 signal. The J1 pulse is not shown in the timing diagram but has the same timing parameters as the J0 pulse. See Figure 19.
2. $t_{D(min)}$ represents the time that the signal starts to change.
3. $t_{D(max)}$ represents the time that the signal becomes stable.

Figure 34. Boundary Scan Timing



Parameter	Symbol	Min	Max	Unit
TCK clock period	t_{CYC}	50		ns
TCK clock duty cycle	t_{PWH}/t_{CYC}	40	60	ns
TMS setup time to TCK↑	$t_{SU(1)}$	1.0		ns
TMS hold time after TCK↑	$t_{H(1)}$	15		ns
TDI setup time to TCK↑	$t_{SU(2)}$	1.0		ns
TDI hold time after TCK↑	$t_{H(2)}$	15		ns
TDO delay from TCK↓	t_D	4.0	20	ns
$\overline{\text{TRST}}$ pulse width	t_{PW}	50		ns

Figure 35. Asynchronous Microprocessor Interface: Motorola-type Write Cycle Timing



These waveforms apply for control bit settings INTFSELECT=0, INTMODE=0

CL at outputs: 5 pF to 20 pF

See parameter table on next page.

Figure 35. Asynchronous Microprocessor Interface: Motorola-type Write Cycle Timing (cont.)

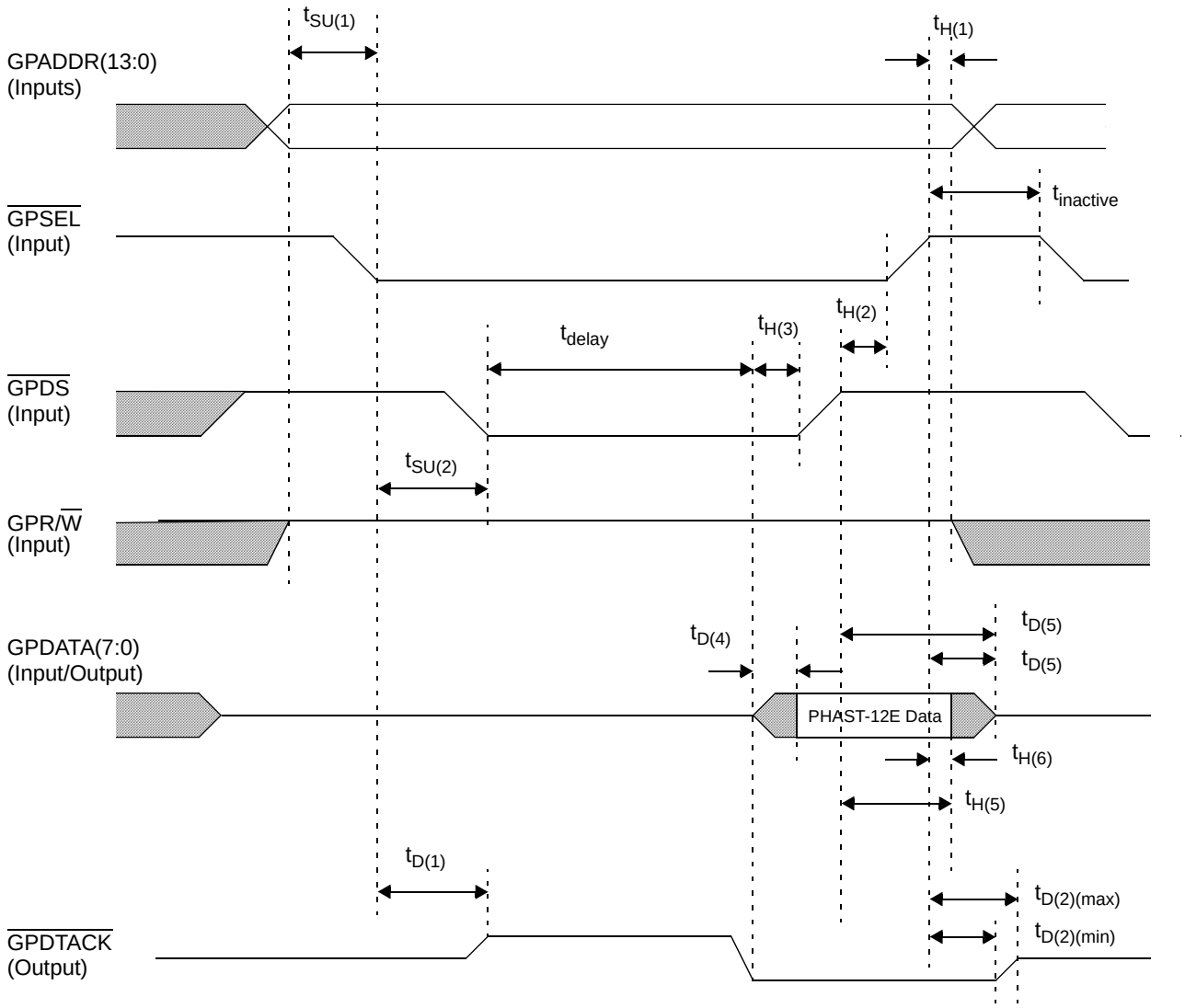
Parameter	Symbol	Min	Typ	Max	Unit
GPPCLK clock period (not shown in diagram)[a]	t_{CYC}	20			ns
GPPCLK duty cycle	t_{PWH}/t_{CYC}	40		60	%
GPADDR(13:0)/GPR/$\overline{W}$ set-up time to $\overline{GPSEL}$ assertion	$t_{SU(1)}$	0			ns
GPADDR(13:0)/GPR/$\overline{W}$ hold time from $\overline{GPSEL}$ de-assertion	$t_{H(1)}$	0			ns
$\overline{GPSEL}$ assertion set-up time to $\overline{GPDS}$ assertion	$t_{SU(2)}$	-1.5			ns
$\overline{GPSEL}$ assertion to $\overline{GPDTACK}$ valid delay	$t_{D(1)}$			12.1	ns
$\overline{GPSEL}$ de-assertion to $\overline{GPDTACK}$ tristate delay[b]	$t_{D(2)}$	3.0		12.1	ns
$\overline{GPSEL}$ de-assertion (high) time between accesses	$t_{inactive}$	t_{CYC}			ns
$\overline{GPSEL}$ hold time from $\overline{GPDS}$ de-assertion	$t_{H(2)}$	0			ns
$\overline{GPDS}$ hold time from $\overline{GPDTACK}$ assertion	$t_{H(3)}$	10			ns
GPDATA(7:0) input valid delay from $\overline{GPDS}$ assertion	$t_{D(3)}$			20	ns
GPDATA(7:0) input valid hold from $\overline{GPDS}$ de-assertion	$t_{H(4)}$	0			ns
$\overline{GPDTACK}$ assertion from $\overline{GPDS}$ assertion[c]	t_{delay}	t_{CYC}		Note c	ns

a. The GPPCLK clock still needs to be applied to the PHAST-12E even if an asynchronous microprocessor interface is used. t_{CYC} must be equal to or smaller than the smaller of 100ns or the microprocessor's clock period but should not go below 20ns. Note, this places a maximum frequency limit of 50 MHz for the microprocessor's bus clock.

b. There might be a de-asserted (high) phase of $\overline{GPDTACK}$ before turning tristate if $\overline{GPDS}$ is de-asserted early.

c. $t_{delay(max)} = 7 \times t_{CYC} + 6 \times t_{min}$ where t_{min} is the cycle time of the lowest-frequency chiplet clock. The lowest frequency of the chiplet clocks is the lower of 19.44 MHz or the UTOPIA interface clock frequencies.

Figure 36. Asynchronous Microprocessor Interface: Motorola-type Read Cycle Timing



These waveforms apply for control bit settings INTFSELECT=0, INTMODE=0

CL at outputs: 5 pF to 20pF

See parameter table on next page.

Figure 36. Asynchronous Microprocessor Interface: Motorola-type Read Cycle Timing (cont.)

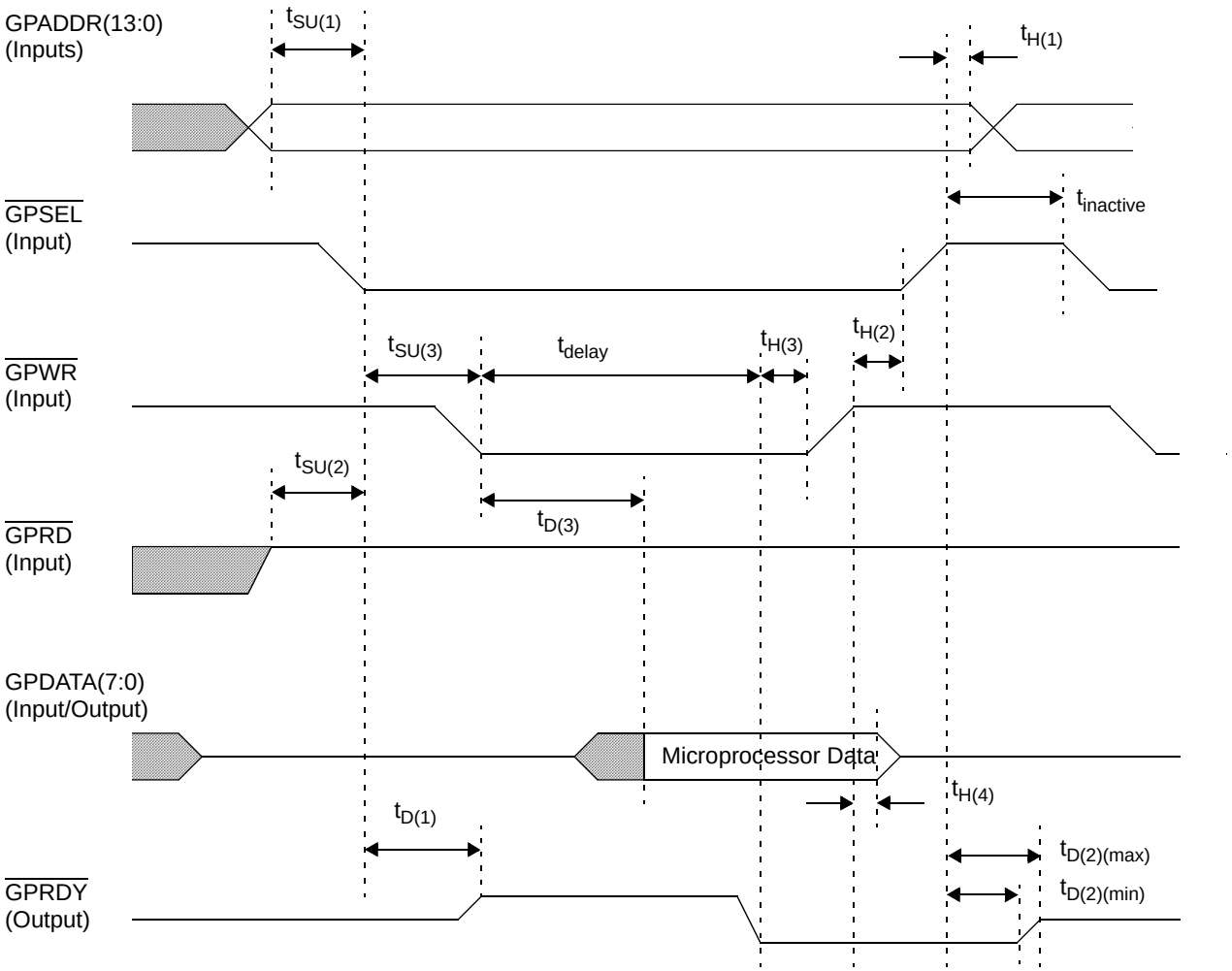
Parameter	Symbol	Min	Typ	Max	Unit
GPPCLK clock period (not shown in diagram)[a]	t_{CYC}	20			ns
GPPCLK duty cycle	t_{PWH}/t_{CYC}	40		60	%
GPADDR/GPR/$\overline{W}$ set-up time to $\overline{GPSEL}$ assertion	$t_{SU(1)}$	0			ns
GPADDR/GPR/$\overline{W}$ hold time from $\overline{GPSEL}$ de-assertion	$t_{H(1)}$	0			ns
$\overline{GPSEL}$ assertion set-up time to $\overline{GPDS}$ assertion	$t_{SU(2)}$	-1.5			ns
$\overline{GPSEL}$ assertion to $\overline{GPDTACK}$ valid delay	$t_{D(1)}$			12.1	ns
$\overline{GPSEL}$ de-assertion to $\overline{GPDTACK}$ tristate delay[b]	$t_{D(2)}$	3.0		12.1	ns
$\overline{GPSEL}$ de-assertion (high) time between accesses	$t_{inactive}$	t_{CYC}			ns
$\overline{GPSEL}$ hold time from $\overline{GPDS}$ de-assertion	$t_{H(2)}$	0			ns
$\overline{GPDS}$ hold time from $\overline{GPDTACK}$ assertion	$t_{H(3)}$	10			ns
$\overline{GPDTACK}$ assertion from $\overline{GPDS}$ assertion[c]	t_{delay}	t_{CYC}		Note c	ns
$\overline{GPDATA(7:0)}$ output valid delay from $\overline{GPDTACK}$ assertion	$t_{D(4)}$			1	ns
GPDATA(7:0) output valid hold from $\overline{GPDS}$ de-assertion	$t_{H(5)}$	3.0			ns
GPDATA output valid hold from $\overline{GPSEL}$ de-assertion	$t_{H(6)}$	3.0			ns
$\overline{GPDATA(7:0)}$ output tristate delay from $\overline{GPDS}$/$\overline{GPSEL}$ de-assertion	$t_{D(5)}$			10	ns
GPDATA(7:0) output rise and fall times	t_r,t_f	1.0		3.7	ns

a. The GPPCLK clock still needs to be applied to the PHAST-12E even if an asynchronous microprocessor interface is used. t_{CYC} must be equal to or smaller than the smaller or 100ns or the microprocessor's clock period but should not go below 20ns. Note, this places a maximum frequency limit of 50 MHz for the microprocessor's bus clock.

b. There might be a de-asserted (high) phase of $\overline{GPDTACK}$ before turning tristate if $\overline{GPDS}$ is de-asserted early.

c. $t_{delay(max)} = 7 \times t_{CYC} + 6 \times t_{min}$ where t_{min} is the cycle time of the lowest-frequency chiplet clock. The lowest frequency of the chiplet clocks is the lower of 19.44 MHz or the UTOPIA interface clock frequencies.

Figure 37. Asynchronous Microprocessor Interface: Intel-type Write Cycle Timing



These waveforms apply for control bit settings INTFSELECT=1, INTFMODE=0

CL at outputs: 5 pF to 20 pF

See parameter table on next page.

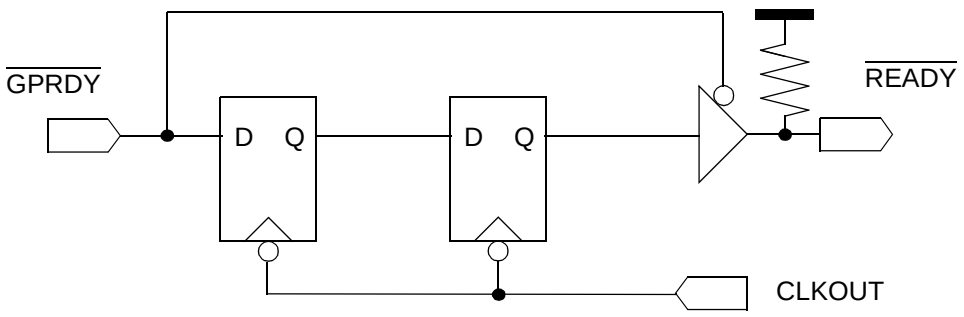
Figure 37. Asynchronous Microprocessor Interface: Intel-type Write Cycle Timing (cont.)

Parameter	Symbol	Min	Typ	Max	Unit
GPPCLK clock period (not shown in diagram)[a]	t_{CYC}	20			ns
GPPCLK duty cycle	t_{PWH}/t_{CYC}	40		60	%
GPADDR(13:0) set-up time to $\overline{\text{GPSEL}}$ assertion	$t_{SU(1)}$	0			ns
GPADDR(13:0) hold time from $\overline{\text{GPSEL}}$ de-assertion	$t_{H(1)}$	0			ns
$\overline{\text{GPRD}}$ de-assertion set-up time to $\overline{\text{GPSEL}}$ assertion	$t_{SU(2)}$	1.5			ns
$\overline{\text{GPSEL}}$ assertion set-up time to $\overline{\text{GPWR}}$ assertion	$t_{SU(3)}$	0			ns
$\overline{\text{GPSEL}}$ assertion to $\overline{\text{GPRDY}}$ valid delay	$t_{D(1)}$			12.1	ns
$\overline{\text{GPSEL}}$ de-assertion to $\overline{\text{GPRDY}}$ tristate delay[b]	$t_{D(2)}$	3.0		12.1	ns
$\overline{\text{GPSEL}}$ de-assertion (high) time between accesses	$t_{inactive}$	t_{CYC}			ns
$\overline{\text{GPSEL}}$ hold time from $\overline{\text{GPWR}}$ de-assertion	$t_{H(2)}$	0			ns
$\overline{\text{GPWR}}$ hold time from $\overline{\text{GPRDY}}$ assertion[c]	$t_{H(3)}$	10			ns
GPDATA(7:0) input valid delay from $\overline{\text{GPWR}}$ assertion	$t_{D(3)}$			13.6	ns
GPDATA(7:0) input valid hold from $\overline{\text{GPWR}}$ de-assertion	$t_{H(4)}$	0			ns
$\overline{\text{GPRDY}}$ assertion from $\overline{\text{GPWR}}$ assertion[d]	t_{delay}	t_{CYC}		Note d	ns

a. The GPPCLK clock still needs to be applied to the PHAST-12E even if an asynchronous microprocessor interface is used. t_{CYC} must be equal to or smaller than the smaller of 100ns or the microprocessor's clock period but should not go below 20ns. Note, this places a maximum frequency limit of 50 MHz for the microprocessor's bus clock.

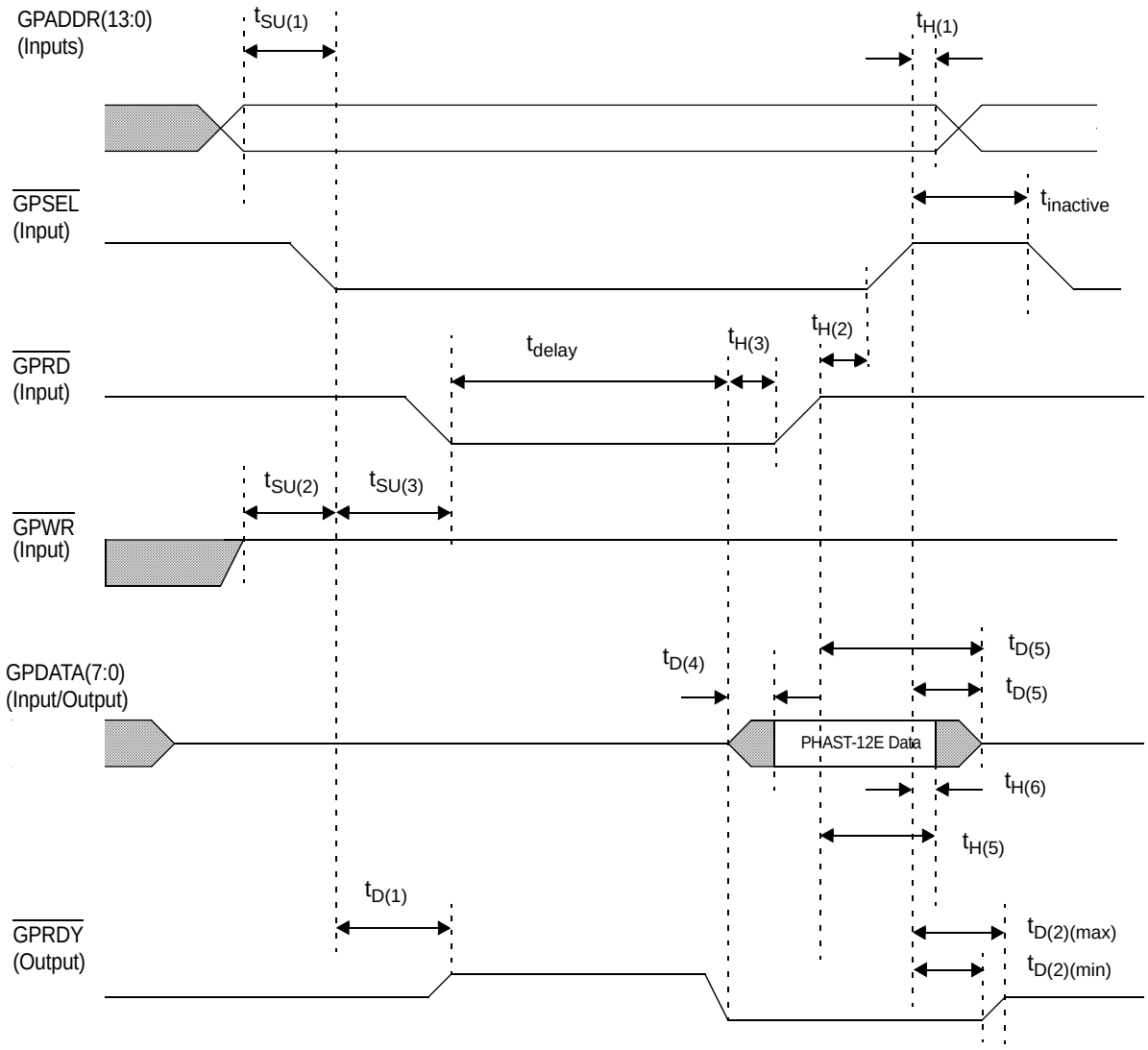
b. There might be a de-asserted (high) phase of $\overline{\text{GPDRDY}}$ before turning tristate if $\overline{\text{GPWR}}$ is de-asserted early.

c. The Intel 286 and 386 microprocessors have synchronous $\overline{\text{READY}}$ inputs, so external synchronization of the $\overline{\text{GPRDY}}$ falling edge to the microprocessor clock is required to avoid metastability problems. Synchronization can be achieved by use of the circuit shown below:



d. $t_{delay(max)} = 7 \times t_{CYC} + 6 \times t_{min}$ where t_{min} is the cycle time of the lowest-frequency chiplet clock. The lowest frequency of the chiplet clocks is the lower of 19.44 MHz or the UTOPIA interface clock frequencies.

Figure 38. Asynchronous Microprocessor Interface: Intel-type Read Cycle Timing



These waveforms apply for control bit settings INTFSELECT=1, INTFMODE=0

CL at outputs: 5 pF to 20 pF

See parameter table on next page.

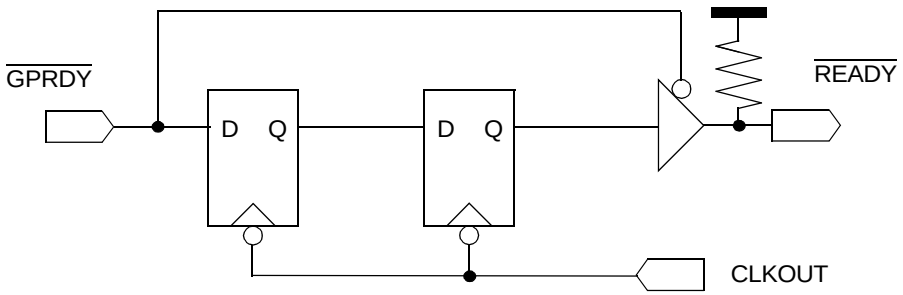
Figure 38. Asynchronous Microprocessor Interface: Intel-type Read Cycle Timing (cont.)

Parameter	Symbol	Min	Typ	Max	Unit
GPPCLK clock period (not shown in diagram)[a]	t_{CYC}	20			ns
GPPCLK duty cycle	t_{PWH}/t_{CYC}	40		60	%
GPADDR(13:0) set-up time to $\overline{\text{GPSEL}}$ assertion	$t_{SU(1)}$	0			ns
GPADDR(13:0) hold time from $\overline{\text{GPSEL}}$ de-assertion	$t_{H(1)}$	0			ns
$\overline{\text{GPWR}}$ de-assertion set-up time to $\overline{\text{GPSEL}}$ assertion	$t_{SU(2)}$	1.5			ns
$\overline{\text{GPSEL}}$ assertion set-up time to $\overline{\text{GPRD}}$ assertion	$t_{SU(3)}$	0			ns
$\overline{\text{GPSEL}}$ assertion to $\overline{\text{GPRDY}}$ valid delay	$t_{D(1)}$			12.1	ns
$\overline{\text{GPSEL}}$ de-assertion to $\overline{\text{GPRDY}}$ tristate delay[b]	$t_{D(2)}$	4.0		12.1	ns
$\overline{\text{GPSEL}}$ de-assertion (high) time between accesses	$t_{inactive}$	t_{CYC}			ns
$\overline{\text{GPSEL}}$ hold time from $\overline{\text{GPRD}}$ de-assertion	$t_{H(2)}$	0			ns
$\overline{\text{GPRD}}$ hold time from $\overline{\text{GPRDY}}$ assertion[c]	$t_{H(3)}$	10			ns
$\overline{\text{GPRDY}}$ assertion from $\overline{\text{GPRD}}$ assertion[d]	t_{delay}	t_{CYC}		Note d	ns
GPDATA(7:0) output valid delay from $\overline{\text{GPRDY}}$ assertion	$t_{D(4)}$			1	ns
GPDATA(7:0) output valid hold from $\overline{\text{GPRD}}$ de-assertion	$t_{H(5)}$	3.0			ns
GPDATA(7:0) output valid hold from $\overline{\text{GPSEL}}$ de-assertion	$t_{H(6)}$	3.0			ns
GPDATA(7:0) output tristate delay from $\overline{\text{GPRD}}$/$\overline{\text{GPSEL}}$ de-assertion	$t_{D(5)}$			10	ns
GPDATA output rise and fall times	t_r,t_f	1.0		3.7	ns

a. The GPPCLK clock still needs to be applied to the PHAST-12E even if an asynchronous microprocessor interface is used. t_{CYC} must be equal to or smaller than the smaller of 100ns or the microprocessor's clock period but should not go below 20ns. Note, this places a maximum frequency limit of 50 MHz for the microprocessor's bus clock.

b. There might be a de-asserted (high) phase of $\overline{\text{GPDRDY}}$ before turning tristate if $\overline{\text{GPRD}}$ is de-asserted early.

c. The Intel 286 and 386 microprocessors have synchronous $\overline{\text{READY}}$ inputs, so external synchronization of the $\overline{\text{GPRDY}}$ falling edge to the microprocessor clock is required to avoid metastability problems. Synchronization can be achieved by use of the circuit shown below:



d. $t_{delay(max)} = 7 \times t_{CYC} + 6 \times t_{min}$ where t_{min} is the cycle time of the lowest-frequency chiplet clock. The lowest frequency of the chiplet clocks is the lower of 19.44 MHz or the UTOPIA interface clock frequencies.

Figure 39. Synchronous Microprocessor Interface: Motorola-type Write and Read Cycle Timing

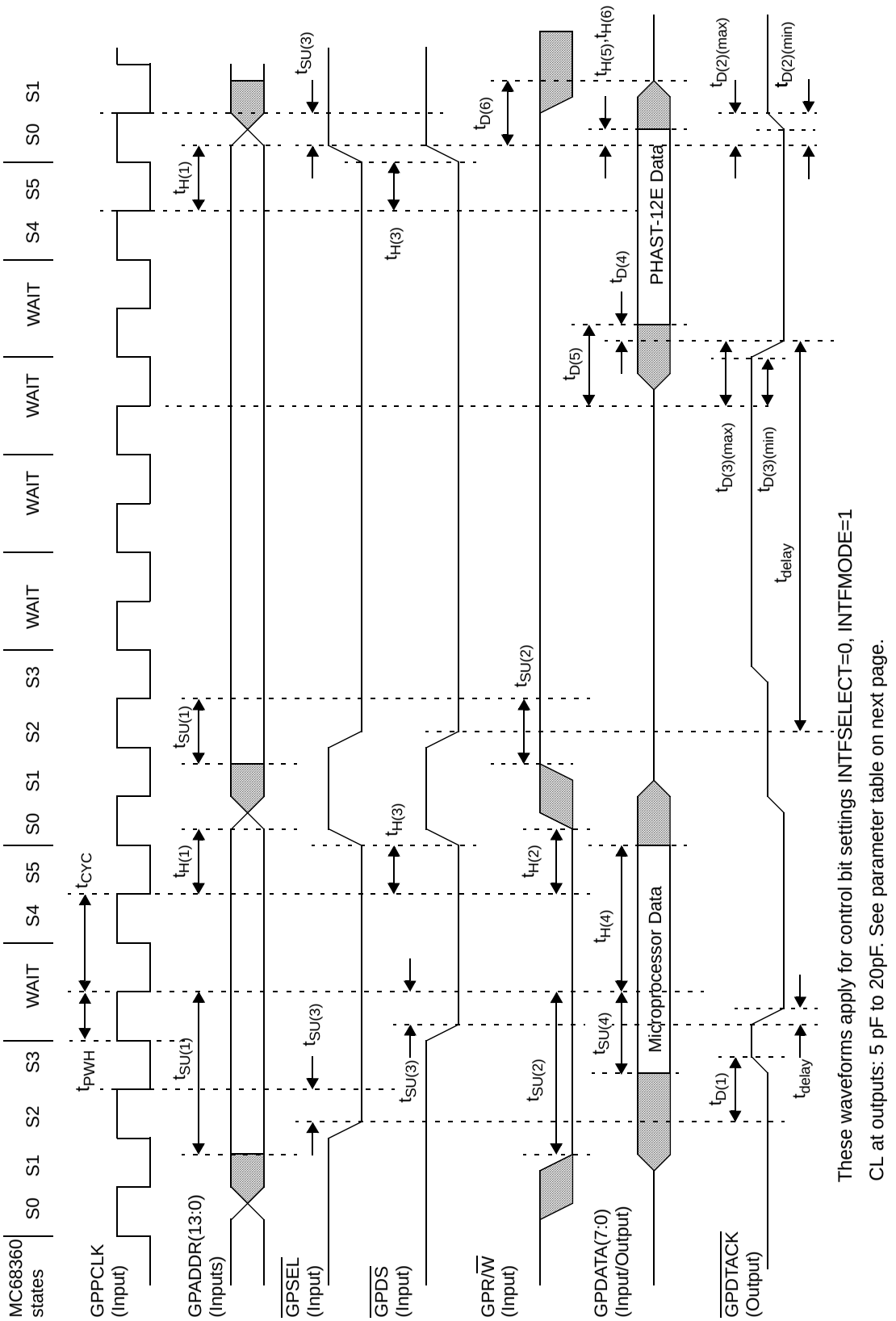


Figure 39. Synchronous Microprocessor Interface: Motorola-type Write and Read Cycle Timing (cont.)

Parameter	Symbol	Min	Typ	Max	Unit
GPPCLK clock period	t_{CYC}	30			ns
GPPCLK duty cycle	t_{PWH}/t_{CYC}	40		60	%
GPADDR(13:0) set-up time to GPPCLK↓[a]	$t_{SU(1)}$	0.3			ns
GPADDR(13:0) hold time from GPPCLK↓[b]	$t_{H(1)}$	0.4			ns
GPR/$\overline{W}$ set-up time to GPPCLK↓[c]	$t_{SU(2)}$	3.6			ns
GPR/$\overline{W}$ hold time from GPPCLK↓[d]	$t_{H(2)}$	0.5			ns
$\overline{GPSEL}$/$\overline{GPDS}$ set-up time to GPPCLK↓	$t_{SU(3)}$	3.6			ns
$\overline{GPSEL}$/$\overline{GPDS}$ hold time from GPPCLK↓	$t_{H(3)}$	0.5			ns
GPDATA(7:0) set-up time to GPPCLK↓[e]	$t_{SU(4)}$	0.1			ns
GPDATA(7:0) hold time from GPPCLK↓[f]	$t_{H(4)}$	0.5			ns
$\overline{GPSEL}$ assertion to $\overline{GPDTACK}$ valid delay[g]	$t_{D(1)}$			12.1	ns
$\overline{GPSEL}$ de-assertion to $\overline{GPDTACK}$ tristate delay[h]	$t_{D(2)}$	3.0		12.1	ns
$\overline{GPDTACK}$ assertion from $\overline{GPDS}$ assertion[i]	t_{delay}	3.0		Note i	ns
$\overline{GPDTACK}$ assertion from $\overline{GPPCLK}$↓[j]	$t_{D(3)}$	3.0		10	ns
GPDATA(7:0) output valid delay from $\overline{GPDTACK}$ assertion	$t_{D(4)}$			1	ns
GPDATA(7:0) output delay from GPPCLK↓[k]	$t_{D(5)}$			11.0	ns
GPDATA(7:0) output valid hold time from $\overline{GPDS}$ de-assertion	$t_{H(5)}$	3.0			ns
GPDATA(7:0) output valid hold from $\overline{GPSEL}$ de-assertion	$t_{H(6)}$	3.0			ns
GPDATA(7:0) output tristate delay from $\overline{GPDS}$/$\overline{GPSEL}$ de-assertion	$t_{D(6)}$			10	ns
GPDATA(7:0) output rise and fall times	t_r,t_f	1.0		3.7	ns

a. This parameter applies to clock transitions during the "$\overline{GPDS}$ asserted" phase only (when the device is selected); asynchronous signals are acceptable if GPADDR(13:0) and GPR/$\overline{W}$ change early in the access cycle.

b. This parameter applies to clock transitions during the "$\overline{GPDS}$ asserted" phase only (when the device is selected); asynchronous signals are acceptable if GPADDR(13:0) and GPR/$\overline{W}$ change early in the access cycle.

c. This parameter applies to clock transitions during the "$\overline{GPDS}$ asserted" phase only (when the device is selected); asynchronous signals are acceptable if GPADDR(13:0) and GPR/$\overline{W}$ change early in the access cycle.

d. This parameter applies to clock transitions during the "$\overline{GPDS}$ asserted" phase only (when the device is selected); asynchronous signals are acceptable if GPADDR(13:0) and GPR/$\overline{W}$ change early in the access cycle.

e. Input data is latched by the PHAST-12E device at the falling clock edge of the last or second to last microprocessor WAIT state (the microprocessor is detecting $\overline{GPDTACK}$ asserted at the same time or t_{CYC} later).

(continued on next page)

f. Input data is latched by the PHAST-12E device at the falling clock edge of the last or second to last microprocessor WAIT state (the microprocessor is detecting $\overline{\text{GPDTACK}}$ asserted at the same time or t_{CYC} later).

g. Depending on the relative speeds of the microprocessor and the PHAST-12E device, $\overline{\text{GPDTACK}}$ might switch from tristate to asserted state directly (applies only to the first write cycle after the interface was idle).

h. There might be a de-asserted (high) phase of $\overline{\text{GPDTACK}}$ before turning tristate if $\overline{\text{GPDS}}$ is de-asserted early.

i. The value shown for $t_{delay(min)}$ applies to the first write cycle after the interface was idle. For all read cycles and for write cycles with more than one microprocessor WAIT cycle $t_{delay(min)} = t_{CYC}$.
$t_{delay(max)} = 5 \times t_{CYC} + 6 \times t_{min}$, where t_{min} is the cycle time of the lowest-frequency chiplet clock. The lowest frequency of the chiplet clocks is the lower of 19.44 MHz or the UTOPIA interface clock frequencies.

j. $t_{D(3)}$ applies to all read cycles and to write cycles with more than one microprocessor WAIT cycle.

k. The microprocessor latches PHAST-12E data at the end of state S4. This is t_{CYC} after detecting $\overline{\text{GPDTACK}}$ asserted.

Note: The PHAST-12E microprocessor interface can be connected to a Motorola MC68360 microprocessor running synchronously at 25 MHz or 33.33 MHz. The connections are as follows:

CLKO1	->	GPPCLK
A(13:0)	->	GPADDR(13:0)
D(31:24)	<->	GPDATA(7:0)
$\overline{\text{CSn}}$	->	$\overline{\text{GPSEL}}$
$\overline{\text{DS}}$	->	$\overline{\text{GPDS}}$
R/$\overline{\text{W}}$	->	GPR/$\overline{\text{W}}$
$\overline{\text{DSACK0}}$	<-	$\overline{\text{GPDTACK}}$
$\overline{\text{IRQx}}$	->	$\overline{\text{GPINT}}$

The following conditions must be established for proper operation:

- Signal delay skew between the MC68360 and PHAST-12E needs to be considered in order to ensure that the timing requirements of both devices are met.
- The PHAST-12E device must be deselected ($\overline{\text{GPSEL}}$ high) between two accesses.

Figure 40. Synchronous Microprocessor Interface: Intel-type Write and Read Cycle Timing

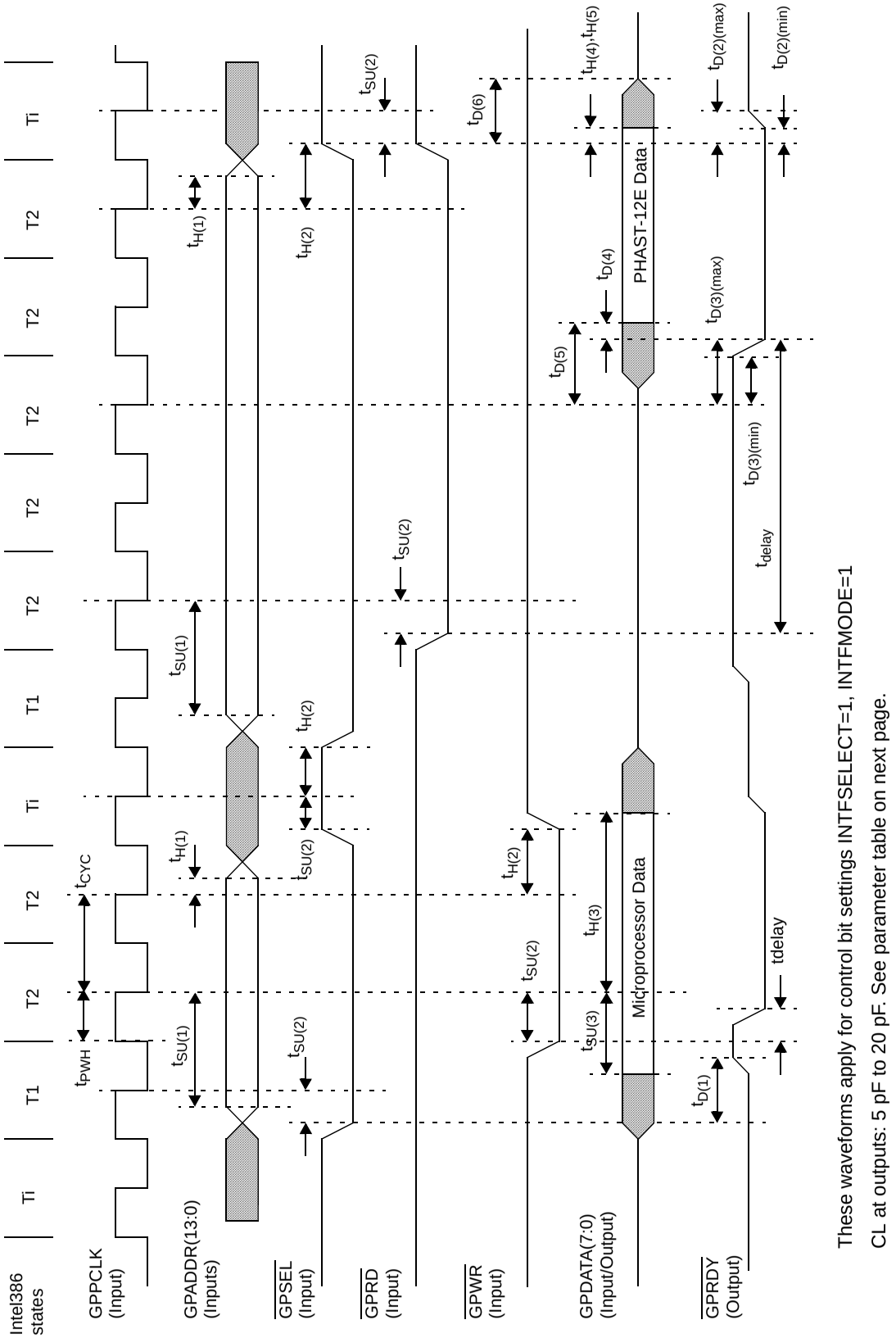


Figure 40. Synchronous Microprocessor Interface: Intel-type Write and Read Cycle Timing (cont.)

Parameter	Symbol	Min	Typ	Max	Unit
GPPCLK clock period	t_{CYC}	30			ns
GPPCLK duty cycle	t_{PWH}/t_{CYC}	40		60	%
GPADDR(13:0) set-up time to GPPCLK↓[a]	$t_{SU(1)}$	0.3			ns
GPADDR(13:0) hold time from GPPCLK↓[b]	$t_{H(1)}$	0.4			ns
$\overline{\text{GPSEL}}$/$\overline{\text{GPWR}}$/$\overline{\text{GPRD}}$ set-up time to GPPCLK↓	$t_{SU(2)}$	3.6			ns
$\overline{\text{GPSEL}}$/$\overline{\text{GPWR}}$/$\overline{\text{GPRD}}$ hold time from GPPCLK↓	$t_{H(2)}$	0.5			ns
GPDATA(7:0) input set-up time to GPPCLK↓	$t_{SU(3)}$	0.1			ns
GPDATA(7:0) input hold time from GPPCLK↓	$t_{H(3)}$	0.5			ns
$\overline{\text{GPSEL}}$ assertion to $\overline{\text{GPRDY}}$ valid delay	$t_{D(1)}$			12.1	ns
$\overline{\text{GPSEL}}$ de-assertion to $\overline{\text{GPRDY}}$ tristate delay[c]	$t_{D(2)}$	3.0		12.1	ns
$\overline{\text{GPRDY}}$ assertion from $\overline{\text{GPWR}}$/$\overline{\text{GPRD}}$ assertion[d]	t_{delay}	3.0		Note d	ns
$\overline{\text{GPRDY}}$ assertion from GPPCLK↓[e]	$t_{D(3)}$	3.0		20.5	ns
GPDATA(7:0) output valid delay from $\overline{\text{GPRDY}}$ assertion	$t_{D(4)}$			15	ns
GPDATA(7:0) output delay from GPPCLK↓	$t_{D(5)}$			11.0	ns
GPDATA(7:0) output valid hold time from $\overline{\text{GPRD}}$ de-assertion	$t_{H(4)}$	3.0			ns
GPDATA(7:0) output valid hold from $\overline{\text{GPSEL}}$ de-assertion	$t_{H(5)}$	3.0			ns
GPDATA(7:0) output tristate delay from $\overline{\text{GPRD}}$/$\overline{\text{GPSEL}}$ de-assertion	$t_{D(6)}$			10	ns
GPDATA(7:0) output rise and fall times	t_r,t_f	1.0		3.7	ns

a. This parameter applies to clock transitions during the "$\overline{\text{GPRD}}$/$\overline{\text{GPWR}}$ asserted" phase only (when the device is selected); asynchronous signals are acceptable if GPADDR(13:0) changes early in the access cycle.

b. This parameter applies to clock transitions during the "$\overline{\text{GPRD}}$/$\overline{\text{GPWR}}$ asserted" phase only (when the device is selected); asynchronous signals are acceptable if GPADDR(13:0) change early in the access cycle.

c. There might be a de-asserted (high) phase of $\overline{\text{GPRDY}}$ before turning tristate if $\overline{\text{GPRD}}$/$\overline{\text{GPWR}}$ is de-asserted early.

d. To avoid a fast path with the Intel 286 and Intel 386 microprocessors, two internal WAIT states will need to be programmed in the device select unit of the microprocessor. Alternatively, the use of a double D-Flip Flop is recommended to delay and re-synchronize the $\overline{\text{GPRDY}}$ falling edge to the microprocessor clock. $t_{delay(max)} = 5 \times t_{CYC} + 6 \times t_{min}$, where t_{min} is the cycle time of the lowest-frequency chiplet clock. The lowest frequency of the chiplet clocks is the lower of 19.44 MHz or the UTOPIA interface clock frequencies.

e. $t_{D(3)}$ applies to all read cycles and to write cycles with more than one microprocessor WAIT cycle.

Note: The PHAST-12E microprocessor interface cannot be directly connected to an Intel 286 or Intel 386 microprocessor at 25 MHz or 33.33 MHz clock frequency in synchronous mode because of the large spread in the timing specifications of these devices. Either device pre-selection for speed, or external re-synchronizing logic, or a reduction of the microprocessor clock frequency is required for proper operation. The PHAST-12E device must be deselected ($\overline{\text{GPSEL}}$ high) between two accesses. It is not recommended to use the synchronous Intel interface due to the requirement for special measures that is indicated above.

OPERATION

This Operation section provides additional detailed information on the operation of the functional units and processes of the PHAST-12E device. It is by no means exhaustive and should be read in conjunction with the information contained in the other sections of this Data Sheet.

It should be noted that interrupt requests are not all rationalized in the PHAST-12E hardware. That is, lower level alarms are not inhibited by higher level alarms except when indicated. The rationalization of alarms needs to be handled in the software that monitors the PHAST-12E device.

The block diagram of the PHAST-12E and a list of the various components are listed here for convenient reference while reading the sections below.

PHAST-12E Chiplets

Chiplet Name	Acronym	General Functions
GPPINT	GPPINT	This chiplet contains global configuration and monitoring functions.
Serial Interface Module	SIM	Provides clock recovery and synthesis. Byte interleaving/deinterleaving.
Overhead Frame Processor	OFP	Processes all Transport Overhead and POH. Please note that POH is not processed in Telecom Bus mode.
SONET/SDH Data Buffer	SDB	Provides elastic store between OFP and either the Telecom Bus interfaces or the APH blocks due to clock differences.
Telecom Bus Interface	TB	Provides byte wide 8-bit or double word wide 32-bit interface to TDM traffic.
Transmit APS Cross Connect	TACC	Allows bridging of either ATM or PPP traffic from one TX ACH/PPP chiplet to a TX SFH block or to the external TX APS port. Also allows data from the TX APS port to be applied to a TX SFH block.
Receive APS Cross Connect	RACC	Allows the output of a RX SFH block to be bridged to an RX ACH/PPP chiplet or to the external RX APS interface. Also allows data from the RX APS port to be applied to an RX ACH/PPP chiplet.
PPP Processor/ATM Processor	PPP/ACH	The PPP Processor performs the “PPP in HDLC-like Framing” indicated in [RFC1662] and PPP over SONET/SDH mapping indicated in [RFC2615]. Monitoring functions are also performed. The ATM Processor performs the ATM Physical layer processing of ATM Cells.
ATM/PPP Cell/Chunk Buffer	ACB	Provides elastic store for ATM cells or PPP chunks.
Port Handler	PH	Provides control and monitoring of the ACBs.
Port Handler Cross Connect	PHCC	Provides RX to TX VC-4 (4xSTM-1/STS-3c and 1xSTM-4/STS-12 modes) loopback function with capability for time slot interchange at the VC-4 level.
ATM/PPP Cell Inlet	ACI	Provides control and monitoring of the UTOPIA Interface.

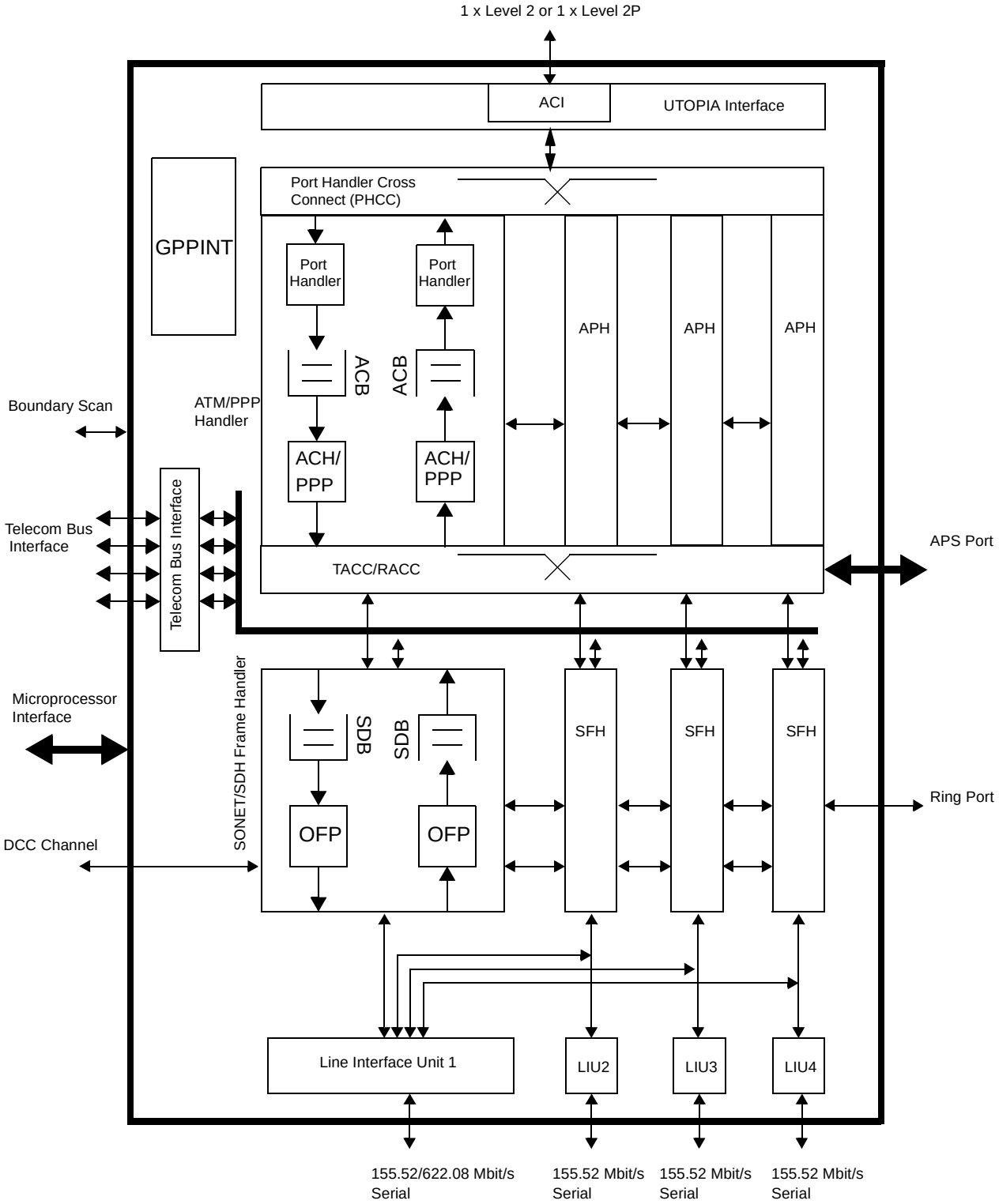
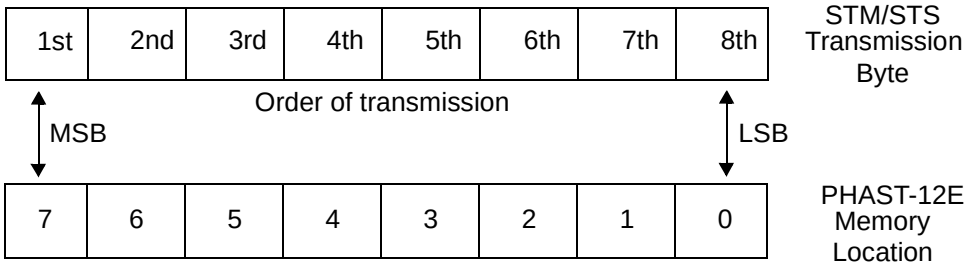


Figure 41. PHAST-12E Block Diagram Showing Chiplets

GENERAL INFORMATION AND MEMORY MAP BIT ORDERING

The memory map of the PHAST-12E device is partitioned into named “chiplet” segments, as shown in Table 4 on page 168. Chiplets are synonymous with “functional sub blocks”. Several chiplets can make up a higher level functional block, like those shown in the Block Diagram. For example, the UTOPIA Level 2/2P block in the Block Diagram is made up of the ACI chiplet, while the APH block is composed of the ACH, PH, and PPP chiplets, not to mention the PHCC and the TACC/RACC. The SFH blocks are composed of the OFP chiplets, the Telecom Bus block is not composed of chiplets but is controlled by the GPPINT and OFP chiplets, the LIU blocks contain the SIM chiplets and are controlled, in part, by the GPPINT chiplet.

Memory map address locations are stated in Hexadecimal (H). The bit placement relationship between a receive and transmit serial SDH/SONET (STM/STS) byte (e.g., J0) and its corresponding storage location in the PHAST-12E memory map is shown below:



CLOCKS

The GPPCLK input signal needs to be present to operate the GPPINT chiplet. The corresponding clocks for the other chiplets need to be present or access to those chiplets via the microprocessor interface will not succeed and will result in the watchdog timer timing out with a corresponding interrupt being issued. The chiplets and the corresponding clocks that need to be present in order to access them are listed below (# can represent values from 1 to 4):

Chiplet / External Interface	Clock
ACI_Tx1	TXUCLK
ACI_Rx1	RXUCLK
PH_Tx#	Depends on the setting of the PHT#(2:0) bits in the PHTXGP1 and PHTXGP2 global configuration registers. The clock can be either TXUCLK or ACHCLK (if the PHCC is used). If the PHT#(2:0) and PHR#(1:0) bits are contradictory, the PHT#(2:0) setting takes priority.
PH_Rx#	Depends on the setting of the PHR#(1:0) bits in the PHRXGP global configuration register. The clock can be either RXUCLK or ACHCLK (if the PHCC is used). If the PHT#(2:0) and PHR#(1:0) bits are contradictory, the PHT#(2:0) setting takes priority.
ACH_Tx#	ACHCLK
ACH_Rx#	ACHCLK
PPP	ACHCLK

OFP_Tx#	Transmit line clock synthesized from REFCLKT/E, or from one of the RX recovered clocks if selected as the TX time-base.
OFP_Rx#	Corresponding recovered receive line clock.
GPPINT	GPPCLK
Transmit Telecom Bus	TXTB#CLK.
Receive Telecom Bus	Corresponding recovered receive line clock.
AIP_TX *	TXRINGCLK
AIP_RX *	Transmit line clock synthesized from REFCLKT/E, or from one of the RX recovered clocks if selected as the TX time-base.
TX SIM	REFCLKT/E, or from one of the RX recovered clocks if selected as the TX timebase.
RX SIM	The RX clock recovery PLLs need the REFCLKT/E signal present in order to operate during frequency acquisition mode.

* External interfaces, part of OFP_xxx chiplets

Other chiplets, or parts of chiplets, have their clocks selected according to global configuration parameter settings. For example, the ACB_Tx# FIFO's write logic has the same clock as the corresponding PH_Tx# port handler, whereas the read logic is always clocked by ACHCLK. The SDB_Tx# FIFO's write port can be driven by TXTB#CLK (if GContTx# ='11') or ACHCLK (GContTx# /='11'[1]), whereas the read logic is always driven by the same clock as OFP_Tx#.

PHAST-12E POWER UP, RESET AND AUTOTRIM SEQUENCE

Figure 42 shows the required power-up and RESET sequence for the PHAST-12E.

For the PHAST-12E Revision C, the "AutoTrim" must be triggered after power-up.

Explanation: the PHAST-12E has one VCO for the synthesis of the transmit clock, and 4 separate VCOs for recovery of the received clocks. The gain center frequency of these VCO can:

- Be adjusted ("trimmed") automatically by the PHAST-12E, or
- Forced, by writing the gain value in control registers SIMTConf2 [3901H],SIMR#Conf4 [390CH, 394CH, 398CH, 39CCH].

Hence, the AutoTrim is inserted in Step 6 of the "Power UP, RESET and AutoTrim Sequence".

1. This does not affect Telecom Bus mode when GContTx# ='10' since in that case, the SDB_Tx# FIFO is bypassed.

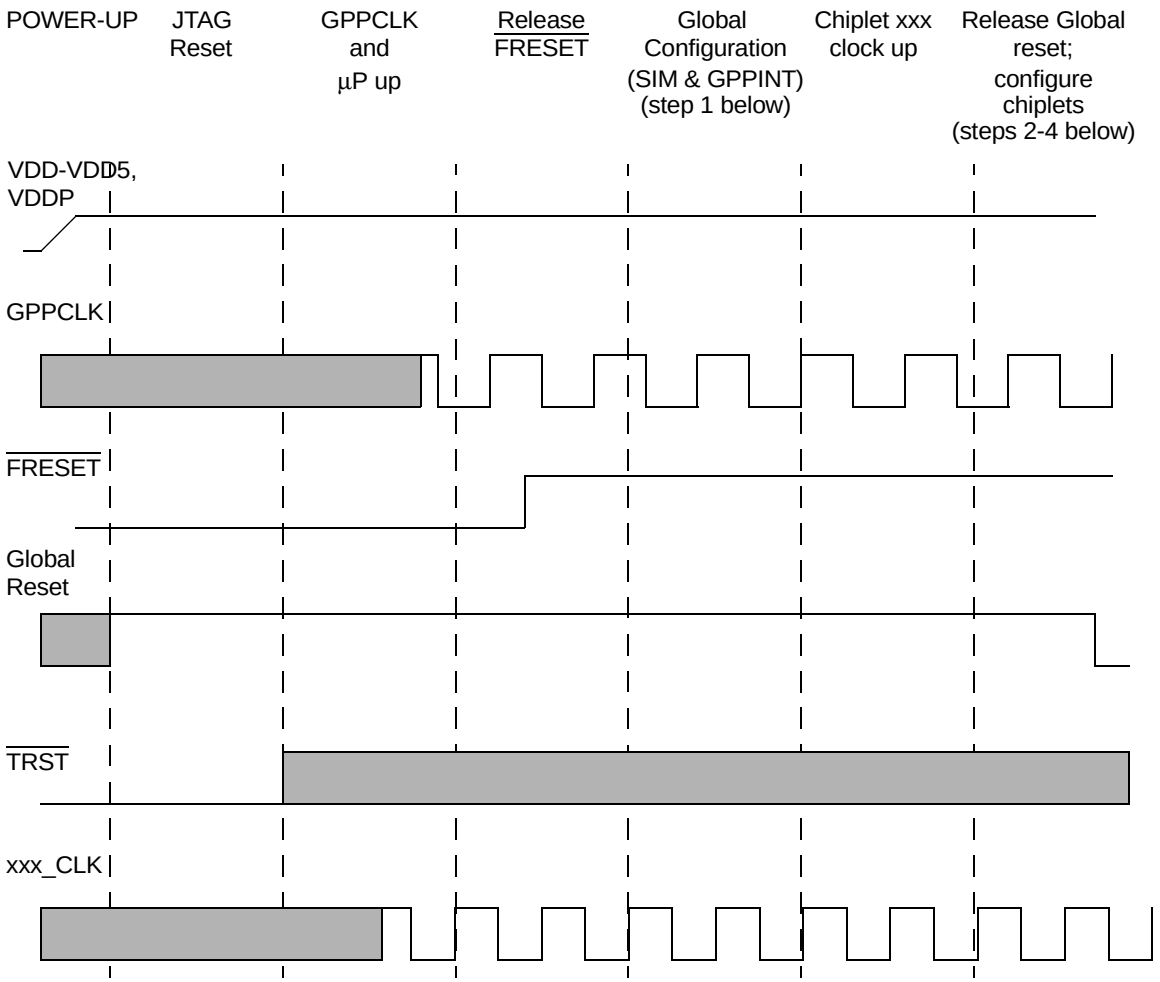


Figure 42. PHAST-12E Power-Up-Reset Sequence

The complete power up, reset and AutoTrim sequence for the PHAST-12E device is as follows:

1. Apply power and $\overline{\text{FRESET}}$ input as shown in Figure 42.

2. Assert the global resets by setting to "1" the reset bits in the RESGP# registers.

3. Configure the parameters in the SIM chiplet first; the main ones are:

Bit Line Rate: Tx#_BLR, Rx#_BLR bits in SIMR#Conf3.

In SIMR#Conf1 #1 only (register 3909 H), TX_Sync_Enable (bit 5) must be set to "0". In SIMR#Conf1 # 2, 3, 4 TX_Sync_Enable must remain to the default value "1".

Reference frequency: Ref_Freq(1:0) in SIMRefFreq (3908 H).

Note that the PLLs current magnitudes in registers 3903 H, 3904 H, as well as in registers SIMR#Conf5, SIMR#Conf6, SIMR#Conf7, SIMR#Conf8 are automatically updated by the selection of Reference frequency and Bit Line Rate.

4. Wait 10 ms. This ensures that the PLL stabilizes its phase and frequency to the reference clock.

5. Set the following registers as shown:

SIMTConf3 [3902 H]=>00
SIMTConf4 [3903 H]=>00
SIMTConf5 [3904 H]=>00
SIMTConf1 [3900 H] =>07

6. Trigger the AutoTrim process: toggle register SIMTConf1 [3900 H] as follows:

SIMTConf1 [3900 H] =>06
SIMTConf1 [3900 H] =>07

7. Read bits 3, 4 of register SIMTrim [3921 H], until they both become set to “11”. These bits attest that the AutoTrim has been initialized.

8. Read bits 2, 1, 0 of register SIMTrim: [3921 H]. If the value reported is “111” or “110” or “010” or “001” or “000”, the AutoTrim must be triggered again: go back to Step 6.

9. Set register SIMTConf3 [3902 H] to "02":

Select again the correct Ref_Freq in register SIMRefFreq [3908 H], same as in step 2. (Note: this will automatically update the registers 3903 H, 3904 H to the appropriate values)

10. Wait 10 ms. Again, this ensures that the PLL stabilize its phase and frequency to the reference clock.

11. If the AutoTrim was performed successfully, bits 2, 1, 0 of registers 3901 H, 390C H, 394C H, 398C H, 39CC H will report the computed VCO trim value; the same values is also reported in bit 2, 1, 0 of register 3921 H.

12. Set the Global Configuration Parameters in the GPPINT chiplet.

13. Remove the global resets by a 1 to 0 transition of the reset bits in the RESGP# registers. Improper operation may result if the Global Static Configuration parameters (in the GPPINT chiplet) are changed on the fly without toggling the corresponding chiplet reset bit(s) in registers 3800 H - 3805 H. The order in which the global resets are deasserted is important. The order in which the global resets are deasserted is as follows: RESGP6, RESGP5, RESGP1, RESGP2, RESGP3, and RESGP4. Leave the unused channels in reset, to reduce power dissipation and prevent cross-talk, (cross talk may increase jitter).

14. Configure the local parameters in each chiplet (i.e., the configuration registers in the local chiplets).

15. Deassert the individual chiplet resets (xx30 H). The sequence for removing the resets of the chiplets is important. A list is given below, showing the order in which the chiplets that are used should be taken out of reset and the values to be written to those chiplets.

For each Tx OFP chiplet, the following must be done:

- After the reset is removed, the corresponding "init" bit must be polled until it becomes set to "1".

Note: at any time a clock is removed from a chiplet and established again, the global reset for that chiplet must be applied (for at least two chiplet clock cycles) and removed to establish local default values in that chiplet and associated state machines.

Appendix 1, on page 338 shows an example of configuration script, written in Pseudo-Code.

Please contact the TranSwitch Applications Engineering Department for availability of more reference scripts for configuring the PHAST-12E to various operating modes.

Table 2. Sequence for Taking Chiplets Out of Reset

Address (Hex)	Value	Chiplet
0130	00	Tx ACI
0530	00	Tx PH 1
0630	00	Tx PH 2
0730	00	Tx PH 3
0830	00	Tx PH 4
1030	00	Tx ACH 4
0F30	00	Tx ACH 3
0E30	00	Tx ACH 2
0D30	00	Tx ACH 1
2430	00	Tx-OFP 4 (Poll init bit in reg. 2433)
2030	00	Tx-OFP 3 (Poll init bit in reg. 2033)
1C30	00	Tx-OFP 2 (Poll init bit in reg. 1C33)
1830	00	Tx-OFP 1 (Poll init bit in reg. 1833)
0330	00	Rx ACI
0930	00	Rx PH 1
0A30	00	Rx PH 2
0B30	00	Rx PH 3
0C30	00	Rx PH 4
1430	00	Rx ACH 4
1330	00	Rx ACH 3
1230	00	Rx ACH 2
1130	00	Rx ACH 1
3430	00	Rx OFP 4
3030	00	Rx OFP 3
2C30	00	Rx OFP 2
2830	00	Rx OFP 1

LINE INTERFACES

Serial Line Interfaces

The PHAST-12E provides four serial line interfaces with differential I/O and integrated clock recovery and synthesis for STM-1/4/4c or STS-3c/12/12c applications. Line Interface Unit 1 can handle 622.08 Mbit/s or 155.52 Mbit/s data rates. Line Interface Units 2 - 4 handle 155.52 Mbit/s data rates. Either of two external reference clock sources (TTL or differential pseudo-ECL) or one of the four receive recovered clocks can be selected as the reference clock source for the transmit clock synthesis block. The Ref_Freq_Sel(2:0) bits in the SIMRefClkSel register and the Tx_RefSIS bit in the PIMTConf1 register are used to select the source. The frequency of the reference clocks can be selected via the Ref_Freq(1:0) control bits in the SIMRefFreq register to be either 19.44 MHz, 38.88 MHz, 51.84 MHz, or 77.76 MHz. Additionally, a divided-down version of the synthesized transmit SONET/SDH clock is provided on the TXDCLKT lead. The frequency of the divided clock on the TXDCLKT lead can be selected via the Tx_Div_Freq(2:0) control bits in the SIMTConf6 register to be either 19.44 MHz, 38.88 MHz, 51.84 MHz, or 77.76 MHz.

In the receive direction, divided-down versions of the recovered clocks from the four LIUs are provided on four leads (RXDCLKT#). The frequencies of the clocks on the RXDCLKT# leads can be individually selected to be either 19.44 MHz, 38.88 MHz, 51.84 MHz, or 77.76 MHz via the Rx#_Div_Freq(2:0) bits in the SIMR#Conf3 registers.

Clock Recovery PLLs

There are four clock recovery PLLs in the PHAST-12E device, one for each RX LIU. These PLLs are used to recover a clock from the received serial SONET/SDH line signals. At power up, the RX PLLs enter into frequency acquisition mode. In frequency acquisition mode, the RX PLLs lock to the REFCLKT/E inputs to bring a scaled down version of the RX Clock Recovery PLL clock to the REFCLKT/E frequency. Once the frequency difference between the divided down RX Clock Recovery PLL clock and the REFCLKT/E is less than 0.05% (which is in close proximity to the nominal frequency of a RX SONET/SDH line) a lock counter (Rx#_Lock_Monitor field in the SIMR#PLLMon registers) is incremented. When a no-lock condition is detected, the lock counter is decremented. Two programmable threshold values, Rx#_LTR_lo(3:0) and Rx#_LTR_hi(3:0) are provided in configuration registers in the SIM chiplet. If the lock counter exceeds the Rx#_LTR_hi(3:0) parameter, the RXPLL switches to data recovery (also known as phase acquisition) mode. If there are data transitions on the corresponding RX SONET/SDH line, then the RX PLL will lock to the phase of the received data stream in about 300 microseconds. If the lock counter goes below the Rx#_LTR_lo(3:0) threshold, such as would occur when data transitions are not present on the RX SONET/SDH line, the RX PLL will lose lock and go into frequency acquisition mode. The LOSSSIG# leads are also capable of starting the frequency acquisition process. When the corresponding LOSSSIG# lead is asserted active, the lock counter is forced to zero, thus forcing the corresponding RX Clock Recovery PLL into frequency acquisition mode. When the LOSSSIG# lead is brought to its inactive state, the corresponding RX Clock Recovery PLL can then begin the locking process as described above.

Receive Jitter Tolerance

The noise on the analog power supply leads must meet the requirements in the “Analog Power Supply Noise Requirements, on Page 93’ section, in order to meet ITU-T and Bellcore jitter tolerance requirements. If the above requirement is met, then the PHAST-12E will be able to tolerate more jitter than required by ITU-T and Bellcore, as indicated by the jitter tolerance graphs in Figures 43 and 44 below.

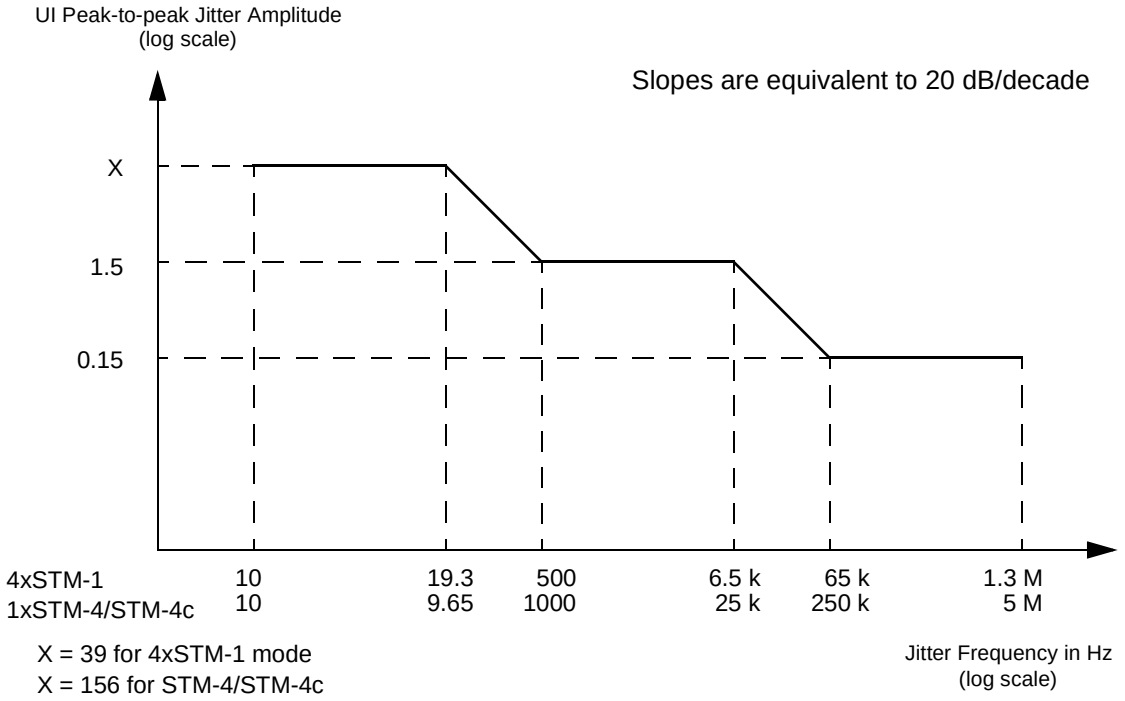


Figure 43. Minimum tolerable input jitter (adapted from figure 2/G.825 (03/93))

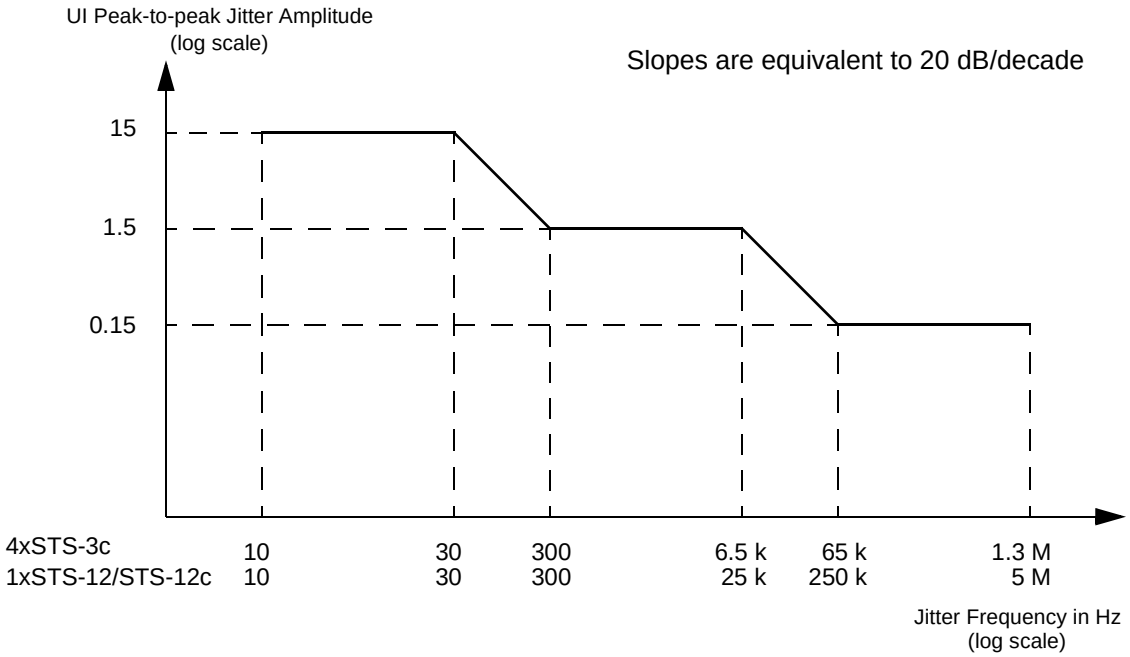


Figure 44. Minimum tolerable input jitter
(adapted from figure 5-28/GR-253-CORE (Revision 2, 01/99))

Clock Synthesis PLL

The clock synthesis PLL is used to synthesize the TX SONET/SDH line clock for all four LIUs. The Transmit Clock Synthesis (TCS) circuit takes an external reference clock from one of the REFCLKT/E inputs and multiplies it up to the appropriate SONET/SDH line frequency. Note that REFCLKT must be present when the PHAST-12E is powered up. After the AutoTrim process is completed, REFCLKT can be replaced by REFCLKE and bit 4 of register PIMTConf1 must be set accordingly. The TCS circuit can accept several reference frequencies from the REFCLKT/E inputs. They are 19.44 MHz, 38.88 MHz, 51.84 MHz, and 77.76 MHz. These frequencies are commonly available frequencies used in SONET/SDH applications. The jitter on the REFCLKT/E inputs must be limited to the values indicated in the “Lead Descriptions, on Page 51’ section, and the noise on the analog power supply leads must meet the requirements in the “Analog Power Supply Noise Requirements, on Page 93’ section, in order to meet Bellcore and ITU-T jitter generation requirements. The clock synthesis PLL also has the ability to take as its reference, one of the recovered clocks or can be bypassed as explained below in “Options for Loop Timing, on Page 138’.

Transmit Jitter Generation

The jitter on the REFCLKT/E inputs must be limited to the values indicated in the “Lead Descriptions, on Page 51’ section, and the noise on the analog power supply leads must meet the requirements in the “Analog Power Supply Noise Requirements, on Page 93’ section, in order to meet ITU-T and Bellcore jitter generation requirements. If the above two requirements are met, then the jitter generation will be under ITU-T and Bellcore jitter generation limits as indicated in the tables below:

ITU-T, Option 1, Jitter Generation Limits (G.813, 08/96, Table 6):

Mode	Maximum Allowed Jitter	Unit	Measurement Filter Bandwidth
4XSTM-1	0.50	UI_{pp}	500 Hz -1.3 MHz
4XSTM-1	0.10	UI_{pp}	65 kHz -1.3 MHz
1XSTM-4 and 1xSTM-4c	0.50	UI_{pp}	1000 Hz - 5 MHz
1XSTM-4 and 1xSTM-4c	0.10	UI_{pp}	250 kHz - 5 MHz

Bellcore Category II Jitter Generation Limits (GR-253-CORE, Revision 2, January 1999, R5-248):

Mode	Maximum Allowed Jitter	Unit	Measurement Filter Bandwidth
4XSTS-3c	0.10	UI_{pp}	12 kHz -1.3 MHz
4XSTS-3c	0.01	UI_{rms}	12 kHz -1.3 MHz
1XSTS-12 and 1xSTS-12c	0.10	UI_{pp}	12 kHz - 5 MHz
1XSTS-12 and 1xSTS-12c	0.01	UI_{rms}	12 kHz - 5 MHz

Options for Loop Timing

The PHAST-12E provides the ability to select, through software control, one of the RX recovered clocks as the transmit timebase. In 622 Mbit/s mode, the RX recovered clock can only be externally looped back, as described in the following section. In 155.52 Mbit/s mode, three options exist. The 1st option allows each RX recovered clock to be used directly as the SONET/SDH transmit clock (i.e., The TCS circuit is bypassed). The 2nd option, allows one of the four RX recovered clocks to be filtered by the TCS circuit and used as the TX timebase for all four TX SONET/SDH lines. The 3rd option allows one of the four RX recovered clocks to be filtered by the TCS circuit and then used as the TX timebase for the corresponding transmit path, while the other three TX paths are driven by their corresponding RX clocks. The generated jitter on the transmit SONET/SDH lines are below the ITU-T and Bellcore jitter generation requirements indicated in the sections above if there is no jitter on the received line signal, the jitter on the REFCLKT/E inputs is limited to the values indicated in the "Lead Descriptions, on Page 51' section, and the noise on the analog power supply leads meet the requirements in the "Analog Power Supply Noise Requirements, on Page 93' section.

Loop Timing in 622 Mbit/s SONET STS-12 Mode

Instead of using the internal timing loopback, filter the external recovered clock from the RXDCLKT1 lead through a PLL and apply the cleaned-up clock to the REFCLKT/E leads through a mux, as shown in Figure 45, below. The mux is controlled by a microprocessor. When the internal RX clock recovery PLL goes out of lock[1], the mux is switched, under microprocessor control, to allow a stable reference clock to be applied to the REFCLKT/E leads. When the LOS indication from the fiber optic module goes inactive, the mux can be switched back to the PLL output. Details of the PLL are being developed. Please contact the TranSwitch Applications Engineering Department for assistance.

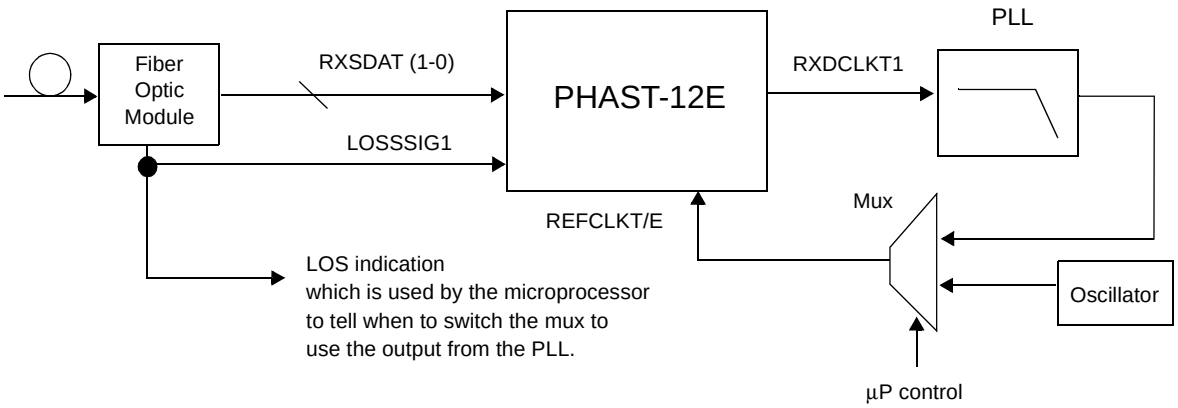


Figure 45. Externally Implemented Timing Loopback.

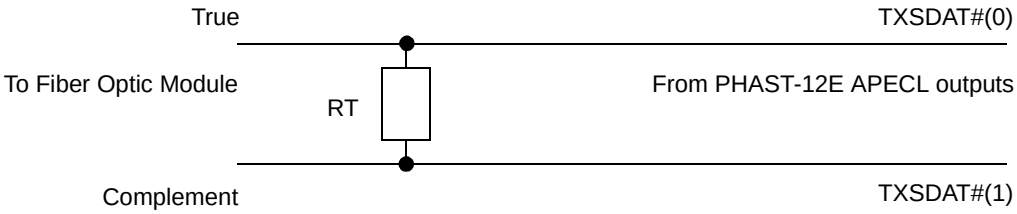
1. Out of lock in this case should be considered to occur when bit 7 of register 3916 H is set to a 1.

Line Interface Controls And Monitoring

Four low power inputs (TXLPOW#) and Loss of Signal inputs (LOSSSIG#) are provided for monitoring external interface circuitry for low power or loss of signal conditions. Also a lock detect status input lead (LOCKDET) is provided to monitor external circuitry. When any of these leads are asserted high, a corresponding maskable interrupt request bit is set. Five control leads (TXSDOWN# and RSTCREC) are provided for controlling external line interface circuitry via the register map of the PHAST-12E. The TXSDOWN# leads can be used to turn the lasers of a fiber optic module on or off. The RSTCREC lead can be used to control an external device.

Line Interface Terminations

Figure 46 shows the suggested termination scheme for the PHAST-12E's transmit APECL serial line interfaces to a 3.3V PECL compatible fiber optic module or similar device. Due to the high speed of the serial interfaces great care should be taken in the layout of the serial line interface signals during the physical design phase of the board. The differential pairs must be routed together and be the same length and have a characteristic impedance of 50Ω on each trace. The differential pairs should also be routed as short as possible and in as straight a path as is possible. Vias should be avoided if practicable.



RT is placed close to the Fiber Optic Module's serial data inputs. RT=100Ω.

Figure 46. TX APECL Terminations

Figure 47 shows how to terminate unused IPECL and APECL inputs.

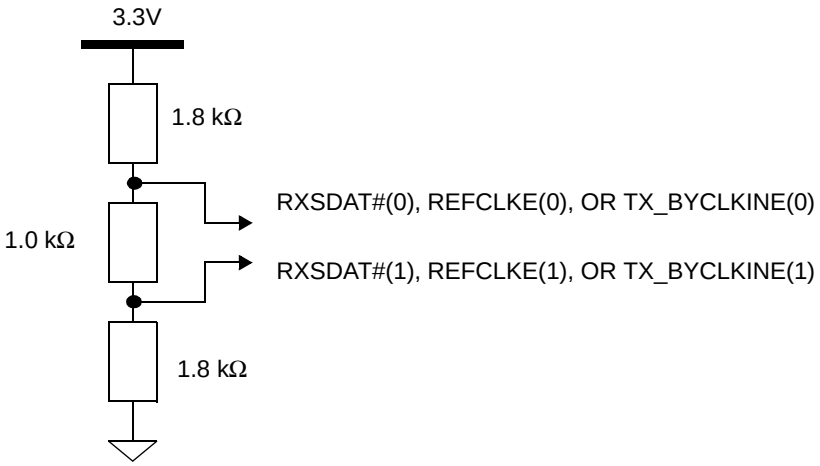


Figure 47. Termination of unused IPECL and APECL inputs

RECEIVE TRANSPORT OVERHEAD BYTE PROCESSING

General

All 81 incoming overhead bytes for each individual STM-1/STS-3c, or the 324 overhead bytes for STM-4/STM-4c/STS-12/STS-12c are written into the OFP_Rx# GRA locations. Each of the four SFH blocks process the TOH associated with its corresponding receive STM-1/STS-3c. When STM-4/4c or STS-12/12c streams are being processed, SFH 1 processes the receive TOH from slot 1 of the frame, SFH 2 processes the receive TOH from slot 2 of the frame, etc. B2 errors are accumulated in SFH 3 since the transmit M1 byte resides in slot 3 of the transmitted frame. B2 errors are accumulated in SFH 3 for 1xSTM-4/STS-12 and 1xSTM-4c/STS-12c modes since the transmit M1 byte resides in slot 3 of the transmitted frame, and in those modes each SFH processes a slot of the overhead. All of the receive SONET/SDH TOH bytes are passed through the PHAST-12E device when operating in the Telecom Bus mode. When processing PPP or ATM data, the TOH is terminated in the PHAST-12E.

RX Descrambling

Descrambling of the line signals can optionally be disabled. The descrambler consists of a frame synchronous descrambler with polynomial of $1+X^6+X^7$.

A1A2 Bytes

The number of consecutive errored framing patterns for OOF can be configured via the Algo#(1:0) control bits in the PIMRConf2 register. Programmable timers OUTnum(1:0) and INnum (0, 1, 2, or 3 ms) are provided for setting the entering or termination of the LOF state. The LOF condition is entered when an internal counter called outcount equals or exceeds the millisecond value indicated by the OUTnum(1:0) bits. Outcount increments each frame while OOF is detected. Outcount is reset if INnum(1:0) consecutive milliseconds of error free frames are received after OOF is cleared. The LOF state is left when another internal counter called incount equals or exceeds the millisecond value indicated by the INnum(1:0) bits. Incount is incremented each frame while the OOF condition does not exist and is reset whenever OOF is detected.

When OOF is detected, the PHAST-12E's SONET/SDH framers do not stay aligned to the last known frame alignment.

J0 Bytes

A 16-byte long J0 message is stored in the receive GRA for each receive line. A maskable interrupt request is generated when the received J0 message does not match a microprocessor-written message. J0 processing can be optionally disabled or enabled via a control bit.

The 16-byte section trace checker for declaring STIM discriminates between two modes: HUNT and REGULAR. The checker is in HUNT mode at start-up time when it has not yet found a correct trace for the first time, or when it has identified a corrupted trace, declared section trace identifier mismatch (STIM), and tries to find another valid trace. In HUNT mode, the checker retrieves the first byte of the expected J0 trace from the RX GRA and compares it with the received J0 bytes. No received J0 bytes are written to the received trace memory area as long as the checker is in HUNT mode. If no match between the first expected byte and the received J0 bytes is found for 17 frames, a STIM alarm is declared and the STIM interrupt request bit is set. If a match between first expected and received J0 byte is found, the checker switches to REGULAR mode. In REGULAR mode, the expected section trace bytes are retrieved on a frame-by-frame basis from GRA and compared against the received J0 bytes. In REGULAR mode, the received J0 bytes are written in the respective memory areas in the on-chip GRA. If the checker had declared a STIM while in the HUNT mode, the STIM alarm is only cleared once 16 consecutive correct matches between expected and received J0 bytes have been found. If no STIM defect is present, a single mismatch between received and expected bytes does not cause an immediate STIM alarm. However, if a second mismatch is found during the next 16 frames, STIM is declared, the STIM interrupt request bit is set and the checker re-enters the HUNT mode to restart a search

for the first expected section trace byte.

For the case where two or more consecutive identical bytes occur in the microprocessor written J0 comparison message, e.g., A, B, C, D, D, E, F, G, H, J, K, M, N, P, Q, R; the microprocessor written J0 comparison message should be written into the PHAST-12E as follows: D, D, E, F, G, H, J, K, M, N, P, Q, R, A, B, C.

B1 Byte

The B1 byte is checked for errors and the errors are counted in a 16-bit counter. Four separate counters are provided for up to 4 x STM-1/STS-3c operation. Separate B1 block error counters are also provided. When in 1xSTM-4/STS-12 mode or 1xSTM-4c/STS-12c mode, only the B1 counters in SFH block one are valid.

B2 Bytes

The PHAST-12E device also performs a B2 BIP-24 parity check. 16-bit counters with two programmable thresholds each (for signal fail and signal degradation detection) are provided for counting B2 BIP-24 bit errors. B2 BIP-24 Block errors are counted in 16-bit performance counters. Two programmable thresholds are provided for each B2 BIP-24 block error counter. The BIP-24 error counts are optionally provided for transmission as line FEBE in the M1 byte. The source is either local, or from the mate PHAST-12E in a ring configuration via the Ring Port. When in STM-4/4c or STS-12/12c modes, the B2 error counter in SFH 3 is where all of the B2 errors are accumulated. In 4xSTM-1/STS-3c mode, there are four B2 error counters which count the B2 errors from their respective STM-1/STS-3c.

K1/K2 Bytes

The K1 byte and 5 MSBits of the K2 byte are debounced and placed in the OT#Stat3 and OT#Stat4 registers. If K1 and the first five MSBs of K2 are equal and new for three consecutive frames, the debounced values in OT#Stat3 and OT#Stat4 are updated and the NewAPS interrupt request bit is set. If no 3 consecutive received K1 bytes of the last 12 successive frames are identical, starting with the last frame containing a previously consistent byte, then an inconsistent K1 byte alarm is declared and the APS_Incon interrupt request bit is set. This inconsistent K1 byte alarm terminates when 3 consecutive received K1 bytes are identical. If the Ring Port is enabled, the new debounced values along with a New APS and Inconsistent K1 Byte Indications are sent to a mate PHAST-12E. In addition, bits 6, 7, and 8 of the K2 byte are monitored for a line RDI (110_2) and a line AIS (111_2) indication. If the Ring Port is enabled, alarm status can be provided, along with interrupt mask bits at the mate PHAST-12E. Line RDI status is also provided for a mate PHAST-12E in a ring configuration (see “Ring port” subsection on page 48) when the Ring Port is enabled. MS-AIS is translated into MS-RDI in the transmit direction within two frames. If enabled by the SFen control bit, excessive error defects can also cause an MS-RDI to be sent in the transmit direction within two frames.

Pointer Bytes

There are four pointer tracking state machines in the PHAST-12E, one in each RX SFH block, for the purpose tracking the SONET/SDH pointers. The H1 and H2 bytes are processed by pointer tracking state machines to determine the location of the J1 byte in the VC/SPE format. The pointer tracking state machine is designed to meet the current ITU-T and Bellcore standards (see “Pointer Tracking Interpretation, on Page 158’ subsection below). In 4xSTM-1/STS-3c mode there is one pointer for each STM-1/STS-3c line; those pointers are processed by their associated SFH blocks. In 1xSTM-4/STS-12 mode, there are four pointers which are processed by SFH blocks 1-4. In 1xSTM-4c/STS-12c mode, there is one pointer which is processed by SFH block 1, and there are three concatenated pointers which are processed by SFH blocks 2-4 according to the state machine shown in G.783 annex C.2.

In addition, when operating with the STS-3c, STS-12, or STS-12c formats, the AIS to LOP transition and the ss-bit checks can be disabled to conform to Bellcore standards. Upon device reset, the pointer tracking state machines are forced to the AIS state. Pointer increments, pointer decrements, and New Data Flag (NDF) indications are counted in their corresponding 8-bit counters. The pointer is also monitored for pointer AIS and

LOP, and interrupt request bits are provided. Pointer AIS is considered to have been detected when the AIS state is entered. Detection of pointer AIS is equivalent to saying path AIS has been detected.

Line FEBE/REI

The M1 byte can be monitored for a line FEBE/REI count in a 16-bit performance counter. A control bit is provided to enable the line FEBE/REI counter to count line FEBE/REI block errors. When operating in 4 x STM-1/STS-3c mode, any counts greater than 18H are counted as 00H. When STM-4/4c or STS-12/12c frames are being processed, counts greater than 60H are counted as 00H.

DCC Bytes

The received Regenerator Section DCC bytes (D1-D3) or the Multiplex Section Regenerator bytes (D4-D12) can be output to an external interface. Four of these interfaces are provided, one for each STM-1/STS-3c or one for each channel of an STM-4/4c or STS-12/12c frame. When a STM-4/4c or STS-12/12c frame is being processed, only DCC port 1 should be used as there is only one set of DCC bytes in the first channel of those frames; the other ports carry the “dummy” DCC bytes.

S1 Byte

The received S1 byte is checked against a microprocessor-written expected value. An interrupt is raised when a mismatch between the microprocessor-written expected value and the received value persists for a number of consecutive frames.

Other Bytes

No processing is performed on the receive E1, E2, or F1 bytes or the TOH bytes that are reserved for national use or international standardization.

TRANSMIT TRANSPORT OVERHEAD BYTE PROCESSING

General

All 81 outgoing overhead bytes for each individual STM-1/STS-3c, or 324 overhead bytes for STM-4/STM-4c/STS-12/STS-12c are stored in the OFP_Tx# GRA locations by internal logic where they are retrieved for transmission or for access by a microprocessor.

TX Scrambling

Scrambling of the line signals is provided and can optionally be disabled. The scrambler consists of a frame synchronous scrambler with polynomial of $1+X^6+X^7$.

J0 Bytes

Additional 16-byte blocks are provided in the transmit GRAs for transmitting a 16-byte long microprocessor-written J0 message. Optionally J0 byte transmission can be performed for STS slot identification purposes instead of the 16-byte J0 message.

B1/B2 Bytes

B1 and B2 byte calculations are performed for either four individual STS-3c/STM-1 streams or for a single STS-12/12c or STM-4/4c stream. B1 and B2 bytes can be corrupted for a single frame by writing to the desired B1 or B2 location in the transmit GRA.

DCC Bytes

Four ports are provided for sourcing either the three Regenerator Section DCC bytes (D1-D3) or the Multiplex Section DCC bytes (D4-D12) associated with the TX SONET/SDH lines. For 1xSTM-4/STS-12 and 1xSTM-4c/STS-12c modes only DCC port 1 should be used as only slot 1 in those frames contain valid DCC byte. All four DCC ports can be used in 4xSTM-1/STS-3c mode. The DCC bytes can also be sourced from the transmit GRA.

Line RDI

When MS-AIS, LOF or LOS is detected in the receive direction it is translated into MS-RDI in the transmit direction within two frames. If enabled by the SFen control bit, excessive receive error defects can also cause an MS-RDI to be sent in the transmit direction within two frames. When MS-RDI is automatically transmitted due to RX alarm conditions, internal logic ensures that it is transmitted for a minimum of 20 SONET/SDH frames. MS-RDI can also be forced via software control. Line RDI is also transmitted if the Line RDI Indication bit on the transmit Ring Port being set to a 1. See Figure 48 for a complete graphical representation of TX MS-RDI generation.

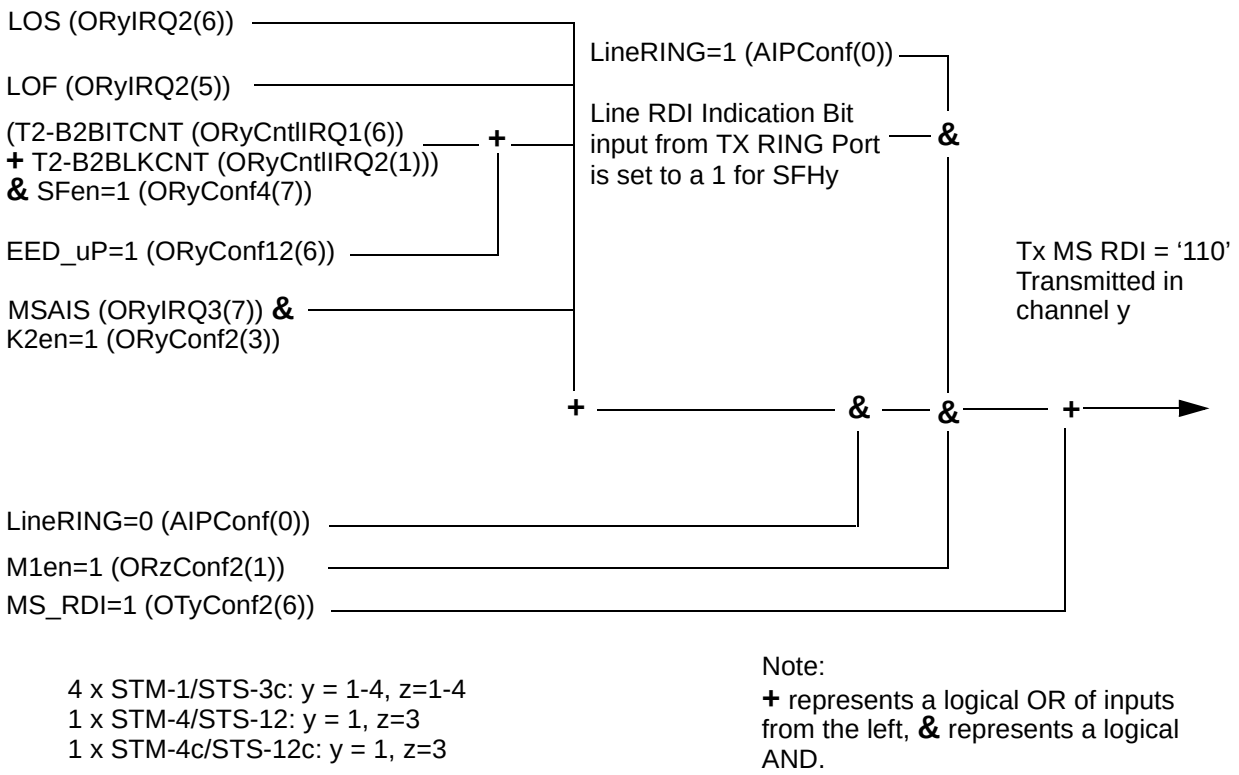


Figure 48. TX Line RDI

Line AIS

MS-AIS can be forced under software control. MS-AIS (also known as line AIS) is all ones in SONET/SDH frame except the first three rows of TOH, which contain valid overhead bytes.

Line FEBE/REI

MS-REI (M1 byte) generation is based on receive B2 errors. For STM-1/STS-3c operation, receive B2 errors are turned around into MS-REI (in the transmit M1 byte as a bit or block count, configurable through software), on a per SFH basis. For STM-4/4c or STS-12/12c operation, the receive B2 errors from all employed SFHs are accumulated and are then turned around into MS-REI (in the transmit M1 byte as a bit or block count, configurable through software) in transmit SFH 3.

Pointer Processing

Outgoing Pointer Adjustment events and NDF events are counted in 8-bit counters. Pointer processing is performed per [G.783], [G.707], and [GR-253]. Pointer adjustments, NDF events, and pointer defect events are counted in 8-bit counters. Optional transmit pointer retiming can be enabled for transmit Telecom Bus, ATM, or PPP applications. For ATM/PPP applications the pointer offset can be fixed to 0. When operating in the Telecom Bus mode, the pointer bytes can be calculated internally (VC-n mode) or can be sourced directly from the Telecom Bus interface (AU-n mode).

Other Bytes

No processing is performed on the receive TOH bytes that are reserved for national use or international standardization. These bytes are just read from the TX GRA and inserted into the TX SONET/SDH signal.

APS FUNCTIONS

An integrated cross connect is provided for APS applications in 4xSTM-1/STS-3c mode only. For single device operation 1:3 multiplex section trail protection can be achieved. If a multi-device configuration is implemented a 1:N (N can range from 1 up to 14) multiplex section trail protection can be realized through the external bidirectional APS interface (see “R/TACC - Receive/Transmit APS Cross Connect” subsection on page 28). Three maskable interrupt request bits are provided for indicating to the external microprocessor that a potential bridge, switch, or switch release is being requested and that the receive K1 and K2 bytes need to be read and interpreted. Based on the receive K1 and K2 bytes the APSSELECT bits in the HT1Conf14 register and the ApsSource bits in the HR1Conf11 register can be written with the appropriate code to cause a bridge to the protection channel as desired. A control bit (Pchan) is provided in each SFH block to enable a particular channel as the protection channel in order to cause the K1 bytes of the working channels to be ignored. An 8-bit counter is provided for counting parity errors that are detected on the APS bus.

TRANSMIT/RECEIVE HIGHER-ORDER PATH CONNECTION FUNCTION LAYER OPTIONS

This function is provided by the PHCC. The PHAST-12E has the ability to fold back received VC-4s in 4xSTM-1/STS-3c and 1xSTM-4/STS-12 modes from any of the four RX SFH blocks and assign them to any TX VC-4 via software control.

RING PORT

The Ring Port is used to communicate K1, K2, K3, Path RDI, Line RDI, Path FEBE, Line FEBE, and the status associated with the K1, K2, and K3 bytes.

The Ring Port is a serial interface that is used to exchange various SONET/SDH-specific alarm, bit error information, and APS information, among PHAST-12E devices when operating in a counter-rotating unidirectional ring network. Thus, the Ring Port replaces the PHAST-12E internal remote alarm, bit error, and APS signaling which is used in bidirectional point-to-point SONET/SDH applications depending on the settings of the LineRING and PathRING control bits. When PathRING is set to 1, path RDI and REI are not inserted into the local transmit SDH stream when local alarms or errors are detected. Instead the Path RDI and REI fields that are transmitted come from those fields that are received over the Ring Port from a mating PHAST-12E. Also, a debounced K3 byte along with a New K3 Byte Indication (when a new debounced K3 byte is received) are written into memory locations for access by the local microprocessor, but are not transmitted on the TX SONET/SDH line. The New K3 Byte Indication can trigger an interrupt request to the local microprocessor if enabled. When PathRING is set to 0, the Path RDI and REI information are not derived from the Ring Port, instead they are derived from locally detected alarms and errors. The K3 byte is not processed and the NewK3 indication is not active. When LineRING is set to 1, line RDI and REI are not inserted into the local transmit SDH stream when local alarms or errors are detected. Instead the Line RDI and REI fields that are transmitted come from those fields that are received over the Ring Port from a mating PHAST-12E. Also, a debounced K1 byte and debounced 5 MSBits of the K2 byte along with a New APS and an Inconsistent K1 Byte indication are written into memory locations for access by the local microprocessor, but are not transmitted on the TX SONET/SDH line. The New APS and Inconsistent K1 Byte Indications can trigger interrupt requests to the local microprocessor if enabled. When LineRING is set to 0, the Line RDI and REI, and K1/K2 byte information are not derived from the Ring Port, instead they are derived from locally detected K1/K2 bytes, alarms, and errors.

When the PHAST-12E is operating in Telecom Bus mode all of the transmit POH information output to the line will be derived from the transmit Telecom Bus inputs and not from the Ring Port regardless of the setting of the PathRING bit. This feature will allow a POH Processor to perform POH processing while the PHAST-12E processes the TOH.

The RXRINGD and RXRINGCLK signals connect directly to their corresponding TXRINGD and TXRINGCLK leads on a mating PHAST-12E. The RXRINGCLK clock is derived from the transmit Line Reference Clock of the PHAST-12E device that is driving that signal. The RXRINGCLK signal is 19.44 MHz ± 20 ppm.

The format of the Ring Port data that is output on the RXRINGD lead is shown in Figure 49, Ring Port Data Structure. The leftmost bit is transmitted first. The information consists of twenty 29-bit fields, one for each of the K1, K2, and K3 bytes, and Line and Path REI values, plus their associated alarms that are processed by each SFH block.

In 4xSTM-1/STS-3c mode, SFH blocks 1-4 process the debounced K1 and K2 bytes, Line REI, Line RDI Indication, the New APS Indication, Inconsistent K1 Byte Indication, Path RDI/REI, debounced K3 byte, and New K3 byte Indication for their corresponding SONET/SDH line.

In 1xSTM-4/STS-12 mode, SFH block 1 processes the debounced K1 and K2 bytes, Line RDI Indication, plus the New APS Indication and Inconsistent K1 Byte Indication. SFH block 3 processes the Line REI. However, please note that the Line RDI bit in the RX Ring Port data is actually output with the Line REI field from SFH block 3. At the TX Ring Port, the Line RDI field from SFH block 3 is used to cause Line RDI to be transmitted in TX SFH block 1 if the LineRING bit is set to 1. Path RDI/REI, debounced K3 byte, and New K3 byte Indication for each of the four VC/SPE are handled by SFH blocks 1-4.

In 1xSTM-4c/STS-12c mode, SFH block 1 processes the debounced K1 and K2 bytes, Line RDI Indication, plus the New APS Indication and Inconsistent K1 Byte Indication. SFH block 3 processes the Line REI. However, please note that the Line RDI bit in the RX Ring Port data is actually output with the Line REI field from SFH block 3. At the TX Ring Port, the Line RDI field from SFH block 3 is used to cause Line RDI to be transmitted in TX SFH block 1 if the LineRING bit is set to 1. Path RDI/REI, debounced K3 byte, and New K3 byte Indication for the VC-4-4c/STS-12c-SPE are handled by SFH block 1.

The functions of the Ring Port are indicated in the subsections below.

The sub-fields of the RXRINGD signal are:

- A 15-bit start sequence consisting of 14 consecutive zeros followed by a 1 (i.e., 0000 0000 0000 001). This field is used by the mating PHAST-12E to determine the location of the address and data fields.
- A 5-bit address field. This field identifies to the mating PHAST-12E what the contents of the 9-bit data field are and from which SFH block it came. The one exception to this is when the PHAST-12E is operating in 1xSTM-4/STM-4c/STS-12/STS-12c mode. In this case the Line RDI field, which is generated by RX SFH block 1 and the M1 byte field from RX SFH block 3 are output together with the 5-bit address field set to indicate SFH block 3. However, TX SFH block 1 will look at the Line RDI field of SFH block 3 on its TX Ring Port to decide when to transmit a Line RDI.
- 9-bit data field. This field will contain one of the following:
  - Debounced K1 byte plus an Inconsistent K1 Byte Indication.
  - Debounced K2 byte plus New APS Indication.
  - Debounced K3 byte plus New K3 Indication.
  - G1 path REI (Path FEBE) plus Path RDI.
  - M1 Line REI (Line FEBE) and Line RDI.
- The PHAST-12E device will not lose data input on its transmit Ring Port interface if the frequency of its transmit Ring Port clock input signal is ± 20 ppm from nominal and its transmit line clock is ± 20 ppm from nominal. This also applies to the receive side. That is, if the receive line frequency is different from the RXRINGCLK frequency (which is derived from the TX reference clock), no data will be lost going from the receive side of the PHAST-12E over to the receive Ring Port interface output.

Start sequence																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	ADDRESS					DATA											
14 CONSECUTIVE 0S															4	3	2	1	0	8	7	6	5	4	3	2	1	0			

Figure 49. Ring Port Data Structure

Figure 50 below indicates the meaning of the bits in the address field while Figure 51, Figure 52, Figure 53, Figure 54, and Figure 55 indicate the formats of the nine-bit data field. The data fields contain information relating only to their corresponding STM-1/STM-4/STM-4c/STS-3c/STS-12/STS-12c.

Address Field					
4	3	2	1	0	
DATA_SEL			section no.		
0	0	0			Data field contains New APS Indication and Debounced K2 Byte.
0	0	1			Data field contains New K3 Indication and Debounced K3 Byte.
0	1	0			Data field contains Line RDI Indication and Line FEBE.
0	1	1			Data field contains Path FEBE and Path RDI.
1	0	0			Data field contains an Inconsistent K1 byte indication and Debounced K1 Byte.
1	0	1			Not Used.
1	1	X			Not Used.
			0	0	Data Field is associated with SFH 1
			0	1	Data Field is associated with SFH 2
			1	0	Data Field is associated with SFH 3
			1	1	Data Field is associated with SFH 4

Figure 50. Address Field Bit Definitions

Inconsistent K1 Byte Indication	DEBOUNCED K1 BYTE							
8	7	6	5	4	3	2	1	0
MSB								LSB

Figure 51. Data field is carrying debounced K1 byte and an Inconsistent K1 Byte Indication

The Inconsistent K1 Byte Indication is set when no three consecutive K1 bytes of the last twelve successive frames are identical, starting with the last frame containing a previously consistent K1 byte. The duration of the Inconsistent K1 Byte Indication is from a minimum of two SONET/SDH frames or for as long as the inconsistent K1 byte condition is detected, whichever is longer.

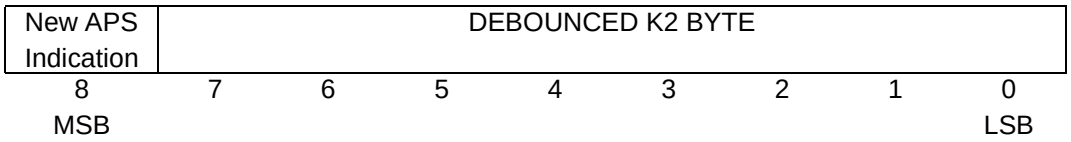


Figure 52. Data field is carrying debounced K2 byte and New APS Indication bit

The New APS Indication bit becomes set when three consecutive and equal new values of K1 plus the five MSBs of K2 are received by the PHAST-12E. The duration of the New APS Indication bit being set is for only one frame.

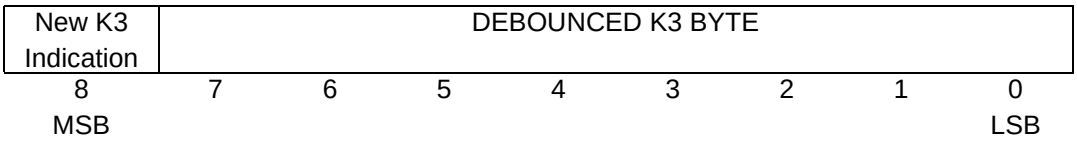


Figure 53. Data field is carrying debounced K3 byte and new K3 Indication bit

The New K3 Indication bit becomes set when three consecutive and equal new values of K3 are received by the PHAST-12E. The duration of the New K3 Indication bit being set is for only one frame.

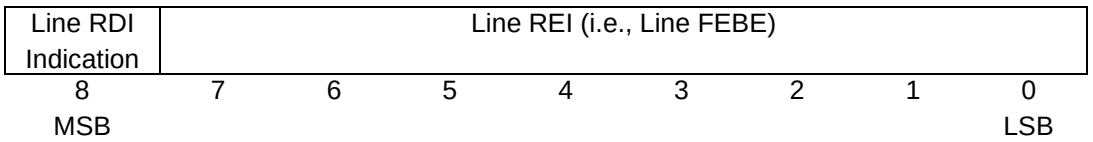


Figure 54. Data field is carrying M1 Line REI and RDI

The Line REI field is set to the number of B2 errors received by the PHAST-12E. The Line RDI bit is generated per Figure 48. The Line RDI bit will persist for at least twenty frames. The line RDI is removed within 2 frames from when the PHAST-12E detects termination of the defect. The mating PHAST-12E will insert these Line RDI and Line REI (bit or block errors, configurable through software) into its transmit K2 and transmit M1 byte stream for the appropriate STM-1, STM-4, STM-4, STM-4c, STS-3c, STS-12, or STS-12c. Again, while LineRING is set to 1, TX Line FEBE and RDI are not derived from locally detected alarms and errors but are instead communicated from a mating PHAST-12E.

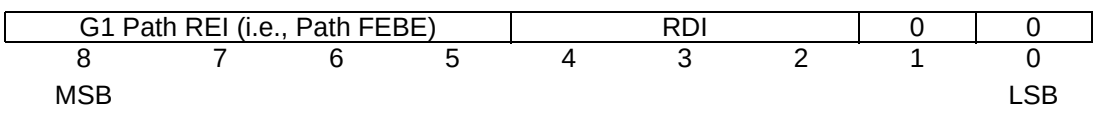


Figure 55. Data field is carrying Path REI and RDI

The G1 path REI field will contain the count of B3 errors received in its corresponding VC-4 or VC-4-4c. The Path RDI is generated immediately after detection of the defect(s) that would cause the PHAST-12E to normally transmit the Path RDI. The path RDI is transmitted for a minimum of ten frames. The Path RDI field is set to indicate no defect detected within two frames from when the PHAST-12E detects termination of the defect. The mating PHAST-12E will insert these path RDI and FEBE (bit or block errors, configurable through software) values into its transmit G1 byte stream for the appropriate VC-4 or VC-4-4c. Again, while PathRING is set to 1, TX path FEBE and RDI are not derived from locally detected alarms and errors but are instead communicated from a mating PHAST-12E.

All of the data fields above are output by the PHAST-12E even if there are no errors or actions to report, provided that the corresponding LineRING or PathRING bits are set to 1.

Please keep in mind that no POH processing (particularly J1, G1 and K3) is performed by the PHAST-12E when the Telecom Bus mode of operation is selected, regardless of the setting of the PathRING bit. Therefore, for the cases below where K3 and G1 processing are mentioned, Telecom Bus mode is assumed to be turned off.

Figure 56 below shows the data flow. The tables that follow Figure 56 summarize, for each mode, which SFH blocks are involved in the processing of the various Ring port data structures.

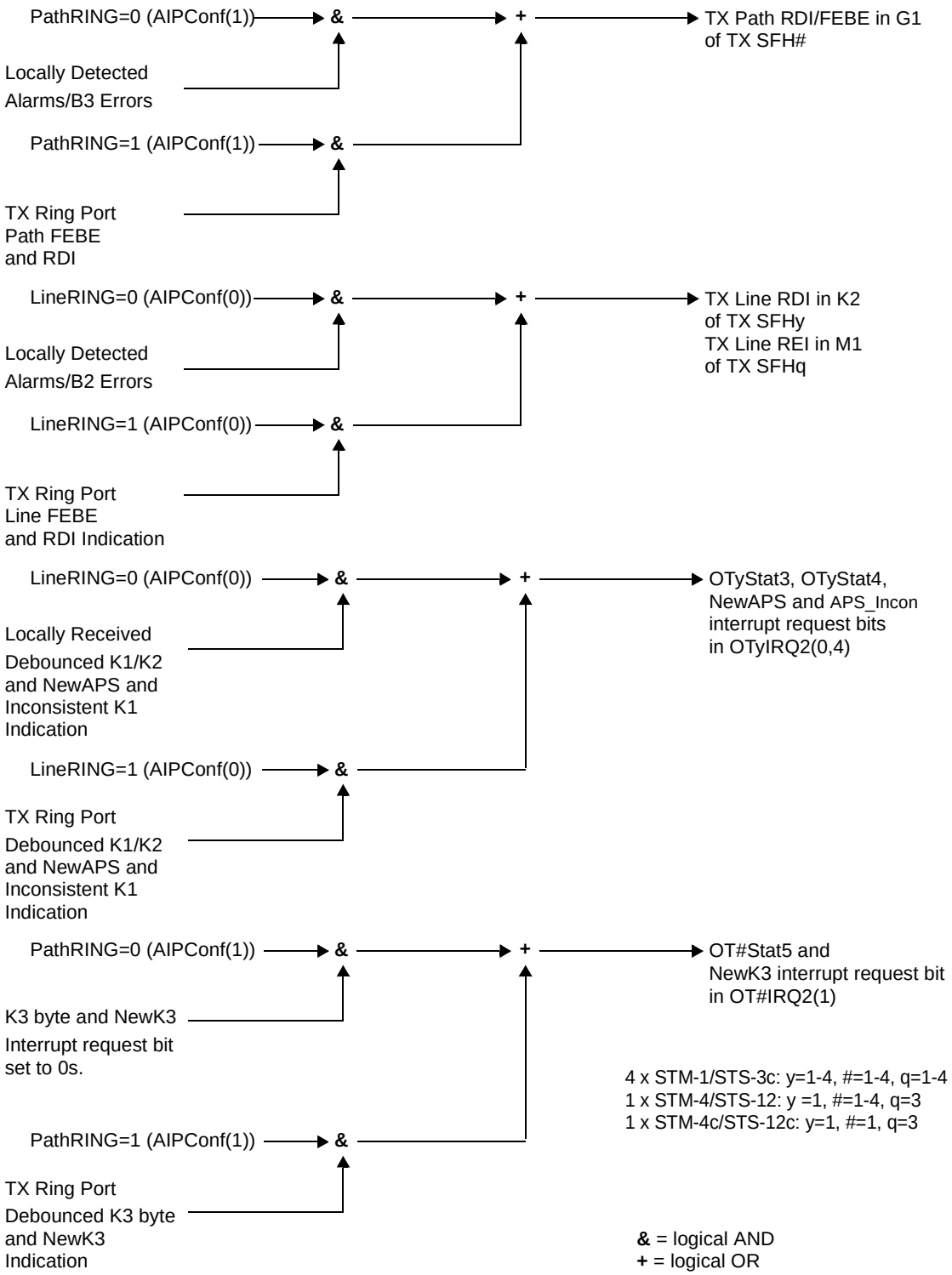


Figure 56. Ring Port Data Flow

Depending upon mode, the SFH blocks process the Ring Port Data Structures per the tables below.

4xSTM-1/STS-3c Mode

Data Structure	SHF1	SFH2	SFH3	SFH4	Comments
STM-1/STS-3c 1: K1 and Inconsistent K1 Indication plus K2 and New APS Indication	X				
STM-1/STS-3c 2: K1 and Inconsistent K1 Indication plus K2 and New APS Indication		X			
STM-1/STS-3c 3: K1 and Inconsistent K1 Indication plus K2 and New APS Indication			X		
STM-1/STS-3c 4: K1 and Inconsistent K1 Indication plus K2 and New APS Indication				X	
STM-1/STS-3c 1: Line RDI Line REI	X				The B2 Errors from the three B2 bytes are summed up in SFH 1 because the M1 byte that is transmitted, resides in SFH 1.
STM-1/STS-3c 2: Line RDI Line REI		X			The B2 Errors from the three B2 bytes are summed up in SFH 2 because the M1 byte that is transmitted, resides in SFH 2.
STM-1/STS-3c 3: Line RDI Line REI			X		The B2 Errors from the three B2 bytes are summed up in SFH 3 because the M1 byte that is transmitted, resides in SFH 3.
STM-1/STS-3c 4: Line RDI Line REI				X	The B2 Errors from the three B2 bytes are summed up in SFH 4 because the M1 byte that is transmitted, resides in SFH 4.
K3 and New K3 Indication for STS-3c-SPE/VC-4 1	X				
K3 and New K3 Indication for STS-3c-SPE/VC-4 2		X			
K3 and New K3 Indication for STS-3c-SPE/VC-4 3			X		
K3 and New K3 Indication for STS-3c-SPE/VC-4 4				X	
G1 (Path RDI and REI) for STS-3c-SPE/VC-4 1	X				
G1 (Path RDI and REI) for STS-3c-SPE/VC-4 2		X			
G1 (Path RDI and REI) for STS-3c-SPE/VC-4 3			X		
G1 (Path RDI and REI) for STS-3c-SPE/VC-4 4				X	

1xSTM-4/STS-12 Mode

Data Structure	SHF1	SFH2	SFH3	SFH4	Comments
K1 and Inconsistent K1 Indication plus K2 and New APS Indication	X				
Line RDI	X				Please note that the RDI field is transferred across the Ring Port interface along with the Line REI field associated with SFH block 3. However, the Line RDI is still processed in TX SFH block 1 and RX SFH block 1 inside of the PHAST-12E.
Line REI			X		The B2 Errors from the twelve B2 bytes are summed up in SFH 3 because the M1 byte that is transmitted, resides in SFH 3.
K3 and New K3 Indication for STS-3c-SPE/VC-4 1	X				
K3 and New K3 Indication for STS-3c-SPE/VC-4 2		X			
K3 and New K3 Indication for STS-3c-SPE/VC-4 3			X		
K3 and New K3 Indication for STS-3c-SPE/VC-4 4				X	
G1 (Path RDI and REI) for STS-3c-SPE/VC-4 1	X				
G1 (Path RDI and REI) for STS-3c-SPE/VC-4 2		X			
G1 (Path RDI and REI) for STS-3c-SPE/VC-4 3			X		
G1 (Path RDI and REI) for STS-3c-SPE/VC-4 4				X	

1xSTM-4c/STS-12c Mode

Data Structure	SHF1	SFH2	SFH3	SFH4	Comments
K1 and Inconsistent K1 Indication plus K2 and New APS Indication	X				
Line RDI	X				Please note that the RDI field is transferred across the Ring Port interface along with the Line REI field associated with SFH block 3. However, the Line RDI is still processed in TX SFH block 1 and RX SFH block 1 inside of the PHAST-12E.

1xSTM-4c/STS-12c Mode

Data Structure	SHF1	SFH2	SFH3	SFH4	Comments
Line REI			X		The B2 Errors from the twelve B2 bytes are summed up in SFH 3 because the M1 byte that is transmitted, resides in SFH 3.
K3 and New K3 Indication for the STS-12c-SPE/VC-4-4c	X				
G1 (Path RDI and REI) for the STS-12c-SPE/VC-4 -4c	X				

TRANSMIT HIGHER-ORDER PATH TERMINATION (HPT) LAYER OPTIONS

General

The PHAST-12E provides the HPT functions for those SONET/SDH streams for which ATM or PPP processing is enabled. POH processing is not performed on the data that is terminated into the Telecom Bus.

All POH (Path Overhead) bytes are stored in on-chip RAM where they are retrieved for transmission or for access by a microprocessor. POH processing is provided for up to four STS-3c-SPE/VC-4s or one STS-12c-SPE/VC-4-4c or three STS-1-SPEs.

J1 Bytes

The J1 path trace can be written by the microprocessor into on-chip RAM (i.e., the transmit GRA) for transmission as a 16 or 64-byte long repeating message.

B3 Byte

The B3 is calculated for each SPE/VC and written into the on-chip RAM for transmission.

C2 Bytes

C2 bytes can be written to on-chip RAM by the microprocessor for transmission. When an unequipped signal is transmitted by setting the HUG bit in the OT#Conf2 register, the transmitted C2 and the C-4 or C-4-4c payload section are forced to all 0s. In this case, the C2 value in the corresponding transmit GRA does not have an effect, but the other POH bytes in the transmit GRA do have an effect.

G1 Byte

Path FEBE is based on received B3 errors and is automatically inserted into the corresponding transmit G1 byte. Path RDI generation per [G.707] and [GR-253] are performed based on mode (SONET or SDH) as follows:

SDH (Bellcore bit = 0):

Interrupt Request or Status Indication	Transmitted RDI Code[a]
PtrAIS, LOP	101
UNEQ, HPTIM[b]	110
LCD_defect[c] (i.e., loss of cell delineation)	010
No defects	001

a. RDI is transmitted for a minimum of 20 frames or until 2 frames after the alarm that caused the path RDI to be transmitted is terminated, whichever is longer.

b. A control bit (TIM_RDI) can be used to disable/enable the HPTIM interrupt request bit from causing TX Path RDI and RX all 1s AIS to be generated.

c. A control bit (LCD_RDI) can be used to enable/disable the LCD_defect alarm from causing TX Path RDI to be generated.

SONET (Bellcore bit = 1):

Interrupt Request or Status Indication	Transmitted RDI Code[a]
PtrAIS, LOP	101
UNEQ, HPTIM[b]	110
LCD_defect[c], SLM[d]	010
No defects	001

a. RDI is transmitted for a minimum of 20 frames or until 2 frames after the alarm that caused the path RDI to be transmitted is terminated, whichever is longer. Also the priority scheme indicated in [GR-253] for deciding which RDI code is transmitted when multiple alarms are detected, is followed. The alarms are listed in order of priority (PtrAIS, LOP are highest priority).

b. A control bit (TIM_RDI) can be used to disable/enable the HPTIM interrupt request bit from causing TX Path RDI and RX all 1s AIS to be generated. This bit is normally set to 0 for Bellcore mode since the PHAST-12E only performs TIM processing on 16-byte messages, and not 64-byte messages. 64-byte messages in Bellcore mode can be processed by software and the TIM_uP can be used to force TX RDI and RX all 1s AIS when the software detects a TIM condition.

c. A control bit (LCD_RDI) can be used to enable/disable the LCD_defect alarm from causing TX Path RDI to be generated.

d. A control bit (SLM_RDI) can be used to disable/enable the SLM interrupt request bit from causing TX Path RDI and RX all 1s AIS to be generated.

The transmitted G1 bytes can be generated from local alarm conditions if the PathRING control bit is set to 0 or can be derived from the Ring Port when the PathRING control bit is set to 1. For data terminated into the Telecom Bus, the TX POH is derived directly from the TX Telecom Bus Interface.

F2, F3, H4, K3, and N1 Bytes

The F2, F3, H4, K3, and N1 bytes can be written to the on-chip RAM by the microprocessor for transmission. These values are static and are not acted upon by the PHAST-12E's transmit logic.

Path AIS

Path AIS can be forced in the transmit direction under software control or by an external Telecom Bus lead (TXTB#FAIL). The TXTB#FAIL lead is only active for TX Telecom Bus interfaces that are terminating data.

RECEIVE HIGHER-ORDER PATH TERMINATION (HPT) LAYER OPTIONS

General

The PHAST-12E provides the HPT functions for those SONET/SDH streams for which ATM or PPP processing is enabled. POH processing is not performed on the data that is terminated into the Telecom Bus. All POH (Path Overhead) bytes are stored in on-chip RAM where they can be observed by the microprocessor.

J1 Bytes

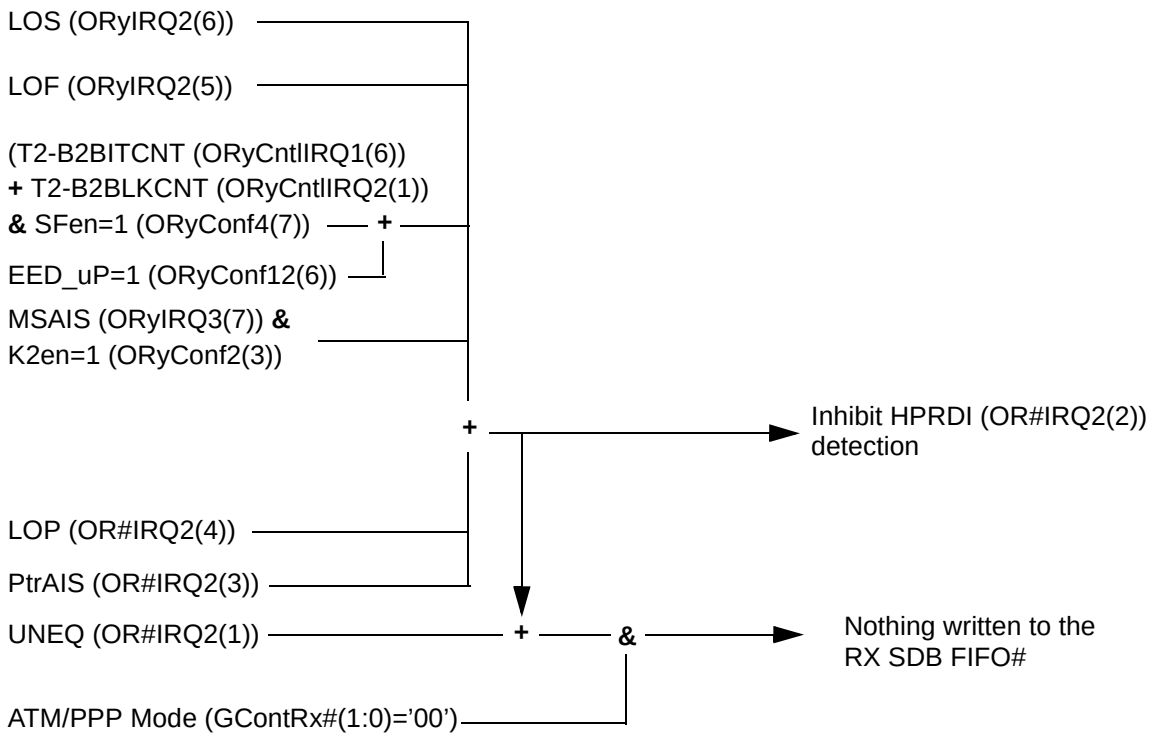
Either 64-byte free form or 16-byte ITU-T G.831-style messages can be received. The received 16-byte J1 message can be compared with a 16-byte microprocessor-written J1 compare message in the receive GRA. A Trace Identifier Mismatch alarm (HPTIM) is raised if no match occurs.

The 16-byte path trace checker for declaring HPTIM discriminates between two modes: HUNT and REGULAR. The checker is in HUNT mode at start-up time when it has not yet found a correct trace for the first time, or when it has identified a corrupted trace, declared higher order path trace identifier mismatch (HPTIM), and tries to find another valid trace. In HUNT mode, the checker retrieves the first byte of the expected J1 trace from the RX GRA and compares it with the received J1 bytes. No received J1 bytes are written to the received trace memory area as long as the checker is in HUNT mode. If no match between the first expected byte and the received J1 bytes are found for 16 frames, a HPTIM alarm is declared and the HPTIM interrupt request bit is set. If a match between first expected and received J1 byte is found, the checker switches to REGULAR mode. In REGULAR mode, the expected path trace bytes are retrieved on a frame-by-frame basis from the GRA and compared against the received J1 bytes. In REGULAR mode, the received J1 bytes are written in the respective memory areas in the on-chip GRA. If the checker had declared a HPTIM while in the HUNT mode, the HPTIM alarm is only cleared once 16 consecutive correct matches between expected and received J1 bytes have been found. If no HPTIM defect is present, a single mismatch between received and expected bytes does not cause an immediate HPTIM alarm. However, if a second mismatch is found during the next 16 frames, HPTIM is declared, the HPTIM interrupt request bit is set and the checker re-enters the HUNT mode to restart a search for the first expected path trace byte.

For the case where two or more consecutive identical bytes occur in the microprocessor written J1 comparison message, e.g., A, B, C, D, D, E, F, G, H, J, K, M, N, P, Q, R; the microprocessor written J1 comparison message should be written into the PHAST-12E as follows: D, D, E, F, G, H, J, K, M, N, P, Q, R, A, B, C.

B3/G1 Bytes

16-bit counters are provided for counting B3 errors, B3 block errors and Path REI for up to four SPE/VC. These counters have programmable threshold overstep registers that cause maskable interrupts to be generated when the counter value equals the programmed threshold. The B3 block error counter increments by one each time an errored B3 byte is received, no matter how many bits are errored. The Path REI counter regards values of 09 H or greater as a count of 0. Maskable interrupt request bits are provided to indicate when HP-RDI is detected in the RX G1 bytes. Figure 57 shows the conditions for which path RDI is inhibited.



NOTES:

+ represents a logical OR of inputs from the left, **&** represents a logical AND.

4 x STM-1/STS-3c: y=1-4, #=1-4
1 x STM-4/STS-12: y=1, #=1-4
1 x STM-4c/STS-12c: y=1, #=1-4

The SDB FIFO can be reset by:
local reset of the corresponding ACH chiplet in STM-1 or STM-4 mode
local reset of ACH chiplet #1 in STM-4C mode

Figure 57. Conditions for which HPRDI Detection is Disabled and Writes are Inhibited to the RX SDB FIFOs

C2 Bytes

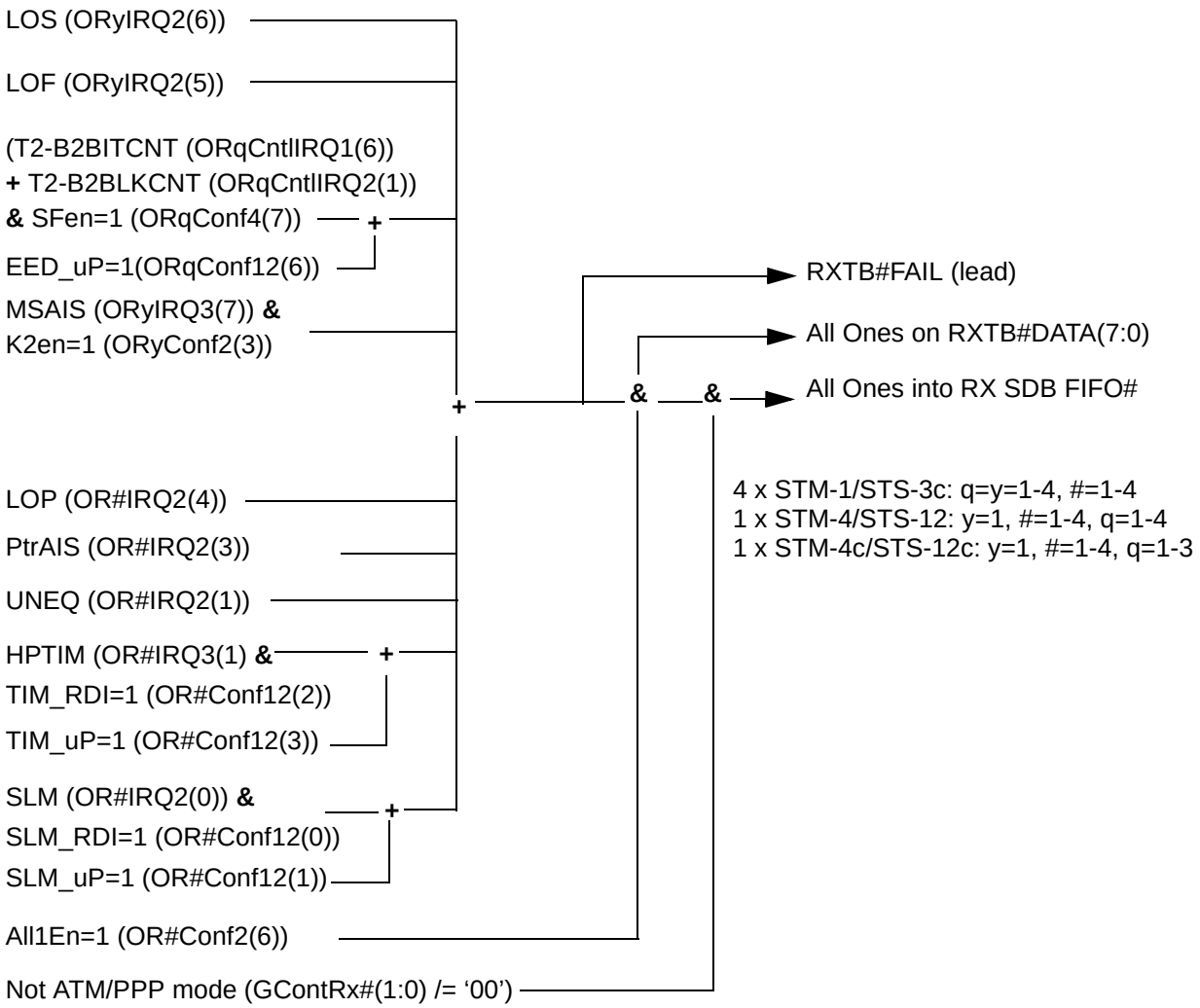
The Unequipped defect (UNEQ) detection is performed on the received C2 bytes. If the received C2 bytes are set to 0 for five consecutive frames then the UNEQ interrupt request bit is set to a 1. If the received C2 byte is not 0 for five consecutive frames the Unequipped defect will be terminated. Path Signal Label mismatch detection is performed against a microprocessor-written expected C2 byte and an internal 01 H value. If a mismatch occurs between the received C2 byte and either the expected C2 byte or the internal 01 H value, the SLM interrupt request bit becomes set to a 1. It should be noted that an unequipped condition does not cause the SLM interrupt request bit to go active. Also, the UNEQ defect does not inhibit path RDI detection.

F2, F3, H4, K3, and N1 Bytes

The F2, F3, H4, K3, and N1 bytes are written to the on-chip RAM for observation by the microprocessor.

All 1s AIS

Figure 58 shows, in graphical form, the conditions for generating RX all 1s AIS in the PHAST-12E device.



NOTES:

+ represents a logical OR of inputs from the left, **&** represents a logical AND.

If GcontRx#(1:0) = 00 and RX all 1s AIS is generated and All1En =1, then nothing gets written into the RX SDB FIFO#.

The SDB FIFO can be reset by:

local reset of the corresponding ACH chiplet in STM-1 or STM-4 mode

local reset of ACH chiplet #1 in STM-4C mode

Figure 58. RX All 1s AIS Generation and Write Inhibit to RX SDB FIFOs

TRANSMIT/RECEIVE PATH ADAPTATION FUNCTIONS

In ATM/PPP mode the transmit ATM/PPP streams are mapped into either a C-4 (4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes), or a C-4-4c (1xSTM-4c/STS-12c mode) and the receive ATM/PPP streams are extracted from the C-4 or C-4-4c per [G.707] and [RFC-2615]. The PHAST-12E supports multiservice applications where one or more payloads can contain ATM cells, others can contain “PPP in HDLC-like Framing”, and still others can contain TDM traffic.

POINTER TRACKING INTERPRETATION

The pointer tracking algorithm implemented in the PHAST-12E device is illustrated in Figure 59. Please refer to [G.783] and [GR-253] for definitions of the transitions. The pointer tracking state machine is based on the pointer tracking state machine found in the ITU-T requirements, and is also valid for Bellcore. The AIS to LOP transition of the state machine does not occur in Bellcore mode (i.e., Bellcore = 1).

Four pointer tracking state machines are employed. In 4xSTM-1/STS-3c and 1xSTM-4/STS-12 modes, the four pointer tracking state machines are used to track the four pointers. In 1xSTM-4c/STS-12c mode, the first pointer tracking state machine is used to track the pointer; the concatenated pointers where AU-4 pointers 2-4 would be, are tracked by three concatenated pointer tracking state machines. See Figure 59 and Figure 60 for details. The pointer tracking state machine uses the H1n and H2n bytes, where n=1-4. The pointer is extracted from the concatenation of the H1n and H2n bytes, and is interpreted as follows:

H1n Byte								H2n Byte							
1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
N	N	N	N	ss-bits		I	D	I	D	I	D	I	D	I	D

NNNN = New Data Flag Bits. This is interpreted as enabled = 1001 or 0001/1101/1011/1000, and normal or disabled = 0110 or 1110/0010/0100/0111 (i.e., a single-bit error is tolerated).

ss = Size bits used in pointer tracking state machine interpretation if enabled by Bellcore control bit being set to 0. When Bellcore is set to 1 these bits are ignored, but when it is set to 0 these bits are expected to be 10.

I = Increment Bits defined as bit 7 of H1n and bits 1, 3, 5 and 7 of H2n.

D = Decrement Bits defined as bit 8 of H1n and bits 2, 4, 6 and 8 of H2n.

Negative Justification: Inverted 5 D-bits and accept majority rule. The 8 of 10 objective of O3-94 in [GR-253] can be enabled by setting the JusITU bit in OR#Conf3 to 0.

Positive Justification: Inverted 5 I-bits and accept majority rule. The 8 of 10 objective of O3-94 in [GR-253] can be enabled by setting the JusITU bit in OR#Conf3 to 0.

For STM-1/STS-3c operation, the pointer is a binary number with the range of 0 to 782 (decimal). It is a 10-bit value derived from the concatenation of the two least significant bits of the H11 byte with the H21 byte, to form an offset in 3-byte counts from the last H3 byte location. For example, for an STM-1 signal, a pointer value of 0 indicates that the VC-4 starts in the byte location 3 bytes after the first H3 byte, whereas an offset of 87 indicates that the VC-4 starts three bytes after the K2 byte.

In STM-4/STS-12 modes there are four byte-interleaved AU-4s, so there are four H1/H2 byte pairs for determining the beginning (i.e., the J1 byte location) of their respective VC-4s. The operation of the four pointer tracking state machines in this case is identical to that for 4 x STM-1/STS-3c operation, where the four STM-1/STS-3cs are byte-interleaved to form the STM-4/STS-12.

When dealing with STS-12c/STM-4c, the pointer tracking state machine for SFH block 1 is used to locate the beginning of the VC-4-4c. The pointer tracking uses the H11 and H21 bytes. The pointer is extracted from the

concatenation of the H11 and H21 bytes, and is interpreted as shown above. However, the offset that is formed represents the number of 12-byte counts from the last H3 byte location. For example, for an STS-12c signal, a pointer value of 0 indicates that the VC-4 starts in the byte location twelve bytes after the first H3 byte, whereas an offset of 87 indicates that the VC-4 starts twelve bytes after the K2 byte.

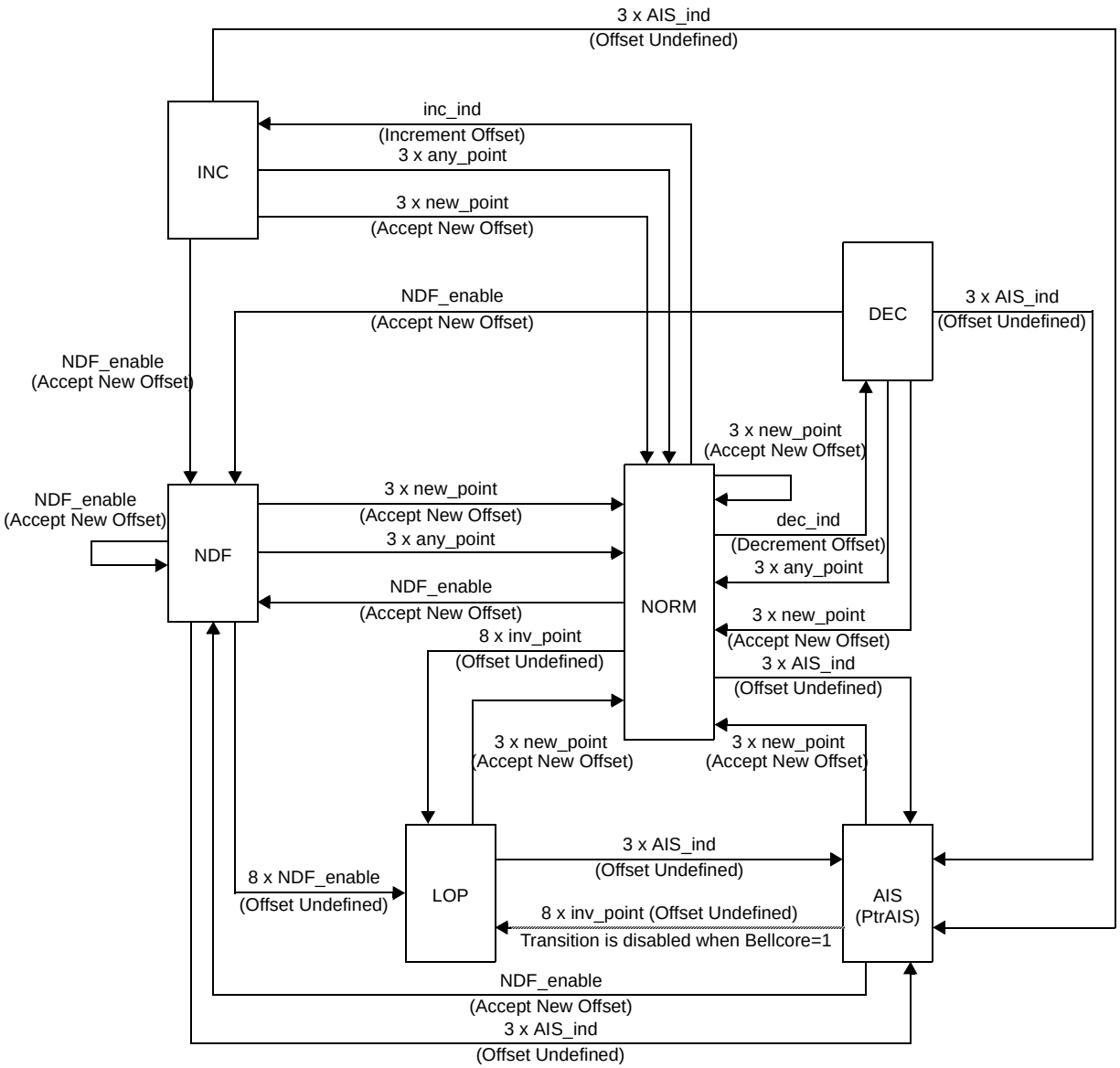


Figure 59. PHAST-12E Pointer Tracking State Machine

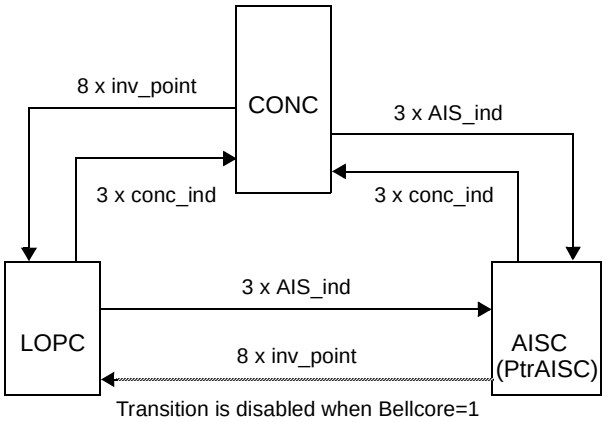


Figure 60. Concatenation Indication State Machine

8-bit counters are provided for counting positive and negative justification events, as well as NDF events. Status bits are provided for indicating the detection of negative justification, positive justification, NDF, invalid pointer, new pointer and concatenation indication.

In STM-4c and STS-12c modes, the pointer bytes for slots 2, 3, and 4 are examined for the concatenation indication bytes, and are monitored for LOP and PtrAIS in corresponding SFH blocks 2-4, per the state machine in Annex C of [G.783]. Figure 60 illustrates the concatenation indicator state machine diagram in the PHAST-12E. Please refer to [G.783] for definitions of the transitions. The AISC to LOPC transition of the state machine does not occur in Bellcore mode (i.e., Bellcore = 1). The pointer bytes for slot 1, are always monitored in SFH block 1, by the pointer tracking state machine shown in Figure 59.

When the LOP or LOPC states are entered as indicated in Figures 59 and 60, the LOP condition is reported in the LOP interrupt request bits in the OR#IRQ2 registers. Similarly, if the AIS or AISC states are entered, the PtrAIS interrupt request bits in the OR#IRQ2 registers will become set.

TRANSMIT ATM FUNCTIONS

The transmit ATM Transmission Convergence Sublayer Functions (TCSF) are performed in the transmit APH blocks. The four transmit APH blocks can process up to four individual C-4 streams, such as in STM-4/STS-12 or 4xSTM-1/STS-3c modes. In STM-4c/STS-12c mode the four transmit APH blocks work in parallel as a single transmit APH block to process a single C-4-4c stream. A four-cell-deep elastic store (i.e., the ACB) is provided between each transmit APH Block and the UTOPIA Level 2/2P interface.

Scrambler

A self- synchronous scrambler of polynomial $1+X^{43}$ is provided to scramble the payloads of the transmitted cells.

Cell Processing

When an STM-4c/STS-12c frame is being generated, the four transmit APH blocks work in parallel as a single transmit APH block, otherwise the Transmit APH blocks work independently. Idle cells per [I.432] or unassigned cells per [I.361] are provided towards the MSA Layer (i.e., the SFH blocks) when no ATM cells are available. Generation of Idle/Unassigned cells can be enabled or disabled via a control bit. The header bytes of Idle/Unassigned Cells can be programmed via on-chip registers. Payload of Idle/Unassigned cells can be programmed such that:

- each payload byte of a cell is the same value in the range 0-255, and is configured through the microprocessor interface
- an incrementing pattern is placed in all the payload bytes of each cell, e.g., all of the payload bytes in a cell are M, all of the payload bytes in the next cell are M+1, etc.,
- An incrementing pattern can be placed in each payload byte of a cell where each successive payload byte contains a value that is one greater than the value of the previous byte.

The HEC calculation for Idle/Unassigned or ATM layer Cells can be enabled or disabled via software control. The HEC can be corrupted under microprocessor control via on-chip mask registers for test purposes.

Counters

24-bit counters are provided to count generated idle/unassigned cells and ATM Layer cells read from the elastic store (i.e., ACB FIFO). An 8-bit counter is provided for counting corrupted ATM Layer cells read from the elastic store.

RECEIVE ATM FUNCTIONS

The receive ATM Transmission Convergence Sublayer Functions (TCSF) are performed in the receive APH blocks. The four receive APH blocks can process up to four individual C-4 streams, such as in STM-4/STS-12 or 4xSTM-1/STS-3c modes. In STM-4c/STS-12c mode the four receive APH blocks work in parallel as a single receive APH block to process a single C-4-4c. A four-cell-deep elastic store (i.e., the ACB) is provided between each receive APH Block and the UTOPIA Level 2/2P interface. The ACB FIFO can be reset by local reset of the corresponding ACH chiplet in STM-1 or STM-4 mode, or local reset of ACH chiplet #1 in STM-4C mode.

Descrambling

Self-synchronizing cell descrambling is performed per [I.432.1]. The descrambler polynomial is $1+X^{43}$.

Cell Processing

The ATM TCSF functions in the receive ATM/PPP Handler are implemented per [I.432.1]. ATM cell delineation is performed according to [I.432.1]. Programmable ALPHA and DELTA registers are provided to allow users to program the thresholds for leaving and entering the SYNC state. Status bits are provided for indicating the transition from the SYNC to the HUNT state and for indicating that the cell delineation state machine is in the HUNT, PRESYNC, or SYNC modes of operation. A control bit (LCD_RDI) can be used to enable automatic Path RDI generation in the transmit G1 byte when loss of cell delineation is detected. The ATM cell header is checked and error detection/correction is performed according to [I.432.1]. Single-bit errors can be corrected or not as enabled via a control bit (NCorHECEr). The coset (i.e., offset) byte of the HEC is user programmable and defaults to 01010101. Provision is made for additional control bits:

- enabling the HEC checking state machine to stay in Correction mode until the SYNC state is left, or to transition to the Detection mode when a HEC error is detected and corrected
- allow/prevent IDLE cells to be written to the ACB FIFOs
- enable/disable ATM cell payload descrambler

An Idle/Unassigned cell filter is provided whereby the five header bytes can be defined so that cells that meet the criteria are identified as Idle/Unassigned cells and can be optionally discarded.

Counters

Two 24-bit long counters are provided for counting received idle cells and ATM cells. Three 16-bit long counters with programmable thresholds (to signal an interrupt when the respective counters equal the threshold) are provided for counting uncorrected HEC errors, corrected HEC errors, and ATM cells that were discarded due to the receive ACB FIFO not being able to accept a complete cell.

PPP FUNCTIONS

Four independent PPP chiplets can be used to map/extract PPP into/from SONET/SDH payloads per [RFC2615] and [RFC1662] for STM-1, STS-3c, STM-4c, and STS-12c applications. Additionally, PPP Payloads can be mapped into and extracted from the payloads of STS-12 and STM-4 signals. A frame interface called UTOPIA Level 2P based on the existing UTOPIA Level 2 interface is provided for transferring frame data on a single-PHY or multi-PHY interface between the PHAST-12E and a packet switch. Frames are transferred across the UTOPIA Level 2P interface in programmable length chunks.

Transmit PPP Functions

Transmitted frame data is processed as follows:

- Optional scrambler ($1+X^{43}$ polynomial) can be used to scramble the HDLC stream before insertion into transmit SONET/SDH frame per [RFC2615]
- Either a 16-bit or 32-bit FCS is calculated over the frame data per [RFC1662] on a per TX PPP chiplet basis
- FCS calculation can be disabled through control bits on a per TX PPP chiplet basis
- Transparent mode can be enabled where chunks are mapped directly into the transmit SONET/SDH frame
- Flag (7E H) and Control Escape (7D H) characters in the data plus FCS are stuffed per section 4.2 of [RFC1662]
- Frame delineation flags are inserted around the frame. At least one or at least two frame delineation flags can be inserted between transmitted frames as selected by a control bit (MFLAG)
- Transmit ACB FIFO underrun in the middle of a frame transfer causes an illegal sequence (7D7E H) to be transmitted
- Inter frame flag fill is added per section 4.4.1 of [RFC1662] to fill space between frames
- Transmit C2 and H4 bytes can be programmed to appropriate values to satisfy [RFC2615]
- PPP frames are mapped into SONET/SDH payload per [RFC2615]

Receive PPP Functions

Received frame data is processed as follows:

- The received frame data extracted from the SONET/SDH payload can optionally be descrambled with a descrambler ($1+X^{43}$ polynomial) per [RFC2615]
- Frame delineation is performed by examining the payload stream for flag characters (7E H) per section 4.1 of [RFC1662]. All flags are discarded
- All control escape sequences are processed (i.e., destuffed) per section 4.2 of [RFC1662]
- Either a 16-bit or 32-bit FCS is checked over the frame data per [RFC1662] on a per RX PPP chiplet basis. The FCS is not discarded
- FCS errors are detected and registered in interrupt request bits, counted in an 8-bit combined Abort/FCS error counter, and signaled on an external FCS error lead
- FCS check on a per RX PPP chiplet basis, can be disabled through control bits. In this case, counters, interrupt request bits, and the FCS error lead are not active when the corresponding PHY is selected
- Transparent mode can be enabled where chunks are passed directly across the UTOPIA Level 2P interface and extracted from the SONET/SDH payload without any frame delineation signals or processing
- When not in transparent mode, frames (after destuffing and including FCS) that are greater than or equal to a user-defined maximum frame length (MAXFL(15:0)) are aborted

- When not in transparent mode, frames (after destuffing and including FCS) that are less than a user-defined minimum frame length (MINFL(6:0)) can optionally be aborted based on a control bit setting (DMINF). This is used to comply with section 4.3 of [RFC1662]
- A control bit is provided (FCSABT) to enable FCS errors and aborts to both be indicated on the FCS error lead, or on their respective leads
- Receive FIFO overflow causes an Abort to be signaled on an external lead
- The remainder of all aborted frames are discarded and not counted as an FCS error
- Illegal sequences that are detected (7D7E H) are registered in an interrupt request bit and are counted in an 8-bit combined Abort/FCS Error counter, and signaled on an external Abort lead
- 8-bit counters are provided for counting frames that are discarded due to being too short or too long

UTOPIA LEVEL 2 INTERFACE ATM FEATURES

The PHAST-12E provides a UTOPIA Level 2, PHY Layer interface with cell level handshaking for ATM applications. The UTOPIA Level 2 interface can support either an 8- or 16-bit data bus. Up to four cell streams can be supported with multi-PHY operation. In 4xSTM-1/STS-3c and 1xSTM-4/STS-12 mode each ATM Cell Stream is contained in a C-4. Single-PHY operation is provided only in STM-4C mode, so that cell streams in a concatenated payload (C-4-4c) are supported. In multi-PHY mode, polling/selection can be controlled by one or four CLAV signals. The valid options for CLAV status indication are shown in Table 3 and are controlled by register ACITXGP and ACIRXGP. The UTOPIA Level 2 clock frequency can range from 2 to 50 MHz when the 16-bit interface is used. The frequency range for the 8-bit interface is from 2 to 25 MHz. A unique port address can be assigned to each of the APH blocks through control registers. Depending on the payload being processed, C-4-4c (1xSTM-4c/STS-12c mode) or C-4 (4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes) the PT#Conf2:NEWCONF, HT#Conf2:ACBTXHPAE, HR#Conf10:PAFT and PR#Conf2:RXTHBUF registers need to be set as indicated in the memory map section of this Data Sheet to ensure the proper operation of the transmit and receive CLAV signals.

Table 3. Valid Options for CLAV Status Indication in ATM Mode

Description	**ACITXGP [3860H] TX Side from ATM Layer to PHAST-12E ACIRXGP [3863H] RX Side from PHAST-12E to ATM Layer**			
PHAST-12E Mode	**Configration Registers 3860H/3863H**	**STM1 UTOPIA 16-bit**	**STM4 UTOPIA 16-bit**	**STM4c UTOPIA 16-bit**
a/ Direct Status Indication with 1 Status Line	06h	**Not Valid**	**Not Valid**	**Not Valid**
	07h	**Not Valid**	**Not Valid**	**Valid**
b/ Direct Status Indication with 4 Status Lines	0Eh	**Valid**	**Valid**	**Not Valid**
	0Fh	**Not Valid**	**Not Valid**	**Not Valid**
c/ Multiplexed Status Indication with 1 Status Line	16h	**Valid**	**Valid**	**Not Valid**
	17h	**Not Valid**	**Not Valid**	**Valid**
d/ Multiplexed Status Indication with 4 Status Lines	1Eh	**Valid**	**Valid**	**Not Valid**
	1Fh	**Not Valid**	**Not Valid**	**Not Valid**

UTOPIA LEVEL 2P INTERFACE PPP FEATURES

The PHAST-12E device provides a PHY Layer interface with “chunk” level handshaking for PPP applications. The data bus is 16 bits wide with a single multiplexed PAVO (chunk available) indication being employed for controlling transfers for both single- and multi-PHY modes. A multi-PHY mode that follows UTOPIA Level 2 style handshaking is provided for terminating up to four C-4 data streams. The method of polling and PHY selection as outlined in [UL2v1] is followed. A single-PHY mode is provided that also provides UTOPIA Level 2 style handshaking for cases where a concatenated payload, such as a C-4-4c, is being terminated. Only complete chunks are transferred. See “UTOPIA Level 2/2P Interface, on Page 35’ for details on the handshaking.

The UTOPIA Level 2P interface is basically a UTOPIA Level 2 interface “plus” some additional signals to facilitate frame delineation. These extra handshaking and status signals are added to indicate start and end of frame, FCS error, abort, last byte of frame is in the most significant byte position, and start of chunk. The frame data is passed across the interface in programmable size data blocks called chunks. Chunks sizes are programmed via the CHNKSZ(2:0) bits in ‘Table 48, ” on page 198. Data from several frame streams can broken up into chunks and multiplexed to/from the appropriate PHY in much the same way that ATM cells are. The advantage to “chunking” the frame data is that short frames on PHY N do not have to wait for a long frame that is currently being transferred on PHY M to be completely transmitted/received. However, it is the responsibility of the “ATM” or controlling layer to ensure that PHYs are not starved or stuffed to overflowing. It is, therefore, strongly suggested that the UTOPIA Level 2P interface clocks be run at, or very near 50 MHz, even though the frequency of the clocks can range down to 2 MHz. A unique port address can be assigned to each of the APH blocks through control registers.

Depending on the payload container being processed, C-4-4c (1xSTM-4c/STS-12c mode) or C-4 (4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes) and the chunk size, the PT#Conf2:NEWCONF, HT#Conf2:ACBTXHPAE, HR#Conf10:PAFT and PR#Conf2:RXTHBUF registers need to be set as indicated in the memory map section of this data sheet to ensure the proper operation of the transmit and receive PAVO signals.

TRANSMIT TELECOM BUS INTERFACE

The transmit Telecom Bus interface of the PHAST-12E device provides an interface for accepting TDM data formatted as either an AU-n or a VC-n signal, where n=4 for 1xSTM-1/STS-3c and 1xSTM-4/STS-12 modes, and n=4-4c for 1xSTM-4c/STS-12c modes. The GContTx#(1:0) bits in the GContTX register are used to select the mode of operation. When AU-n mode is selected, an AU-n is supplied to the PHAST-12E’s transmit Telecom Bus. When AU-n mode is selected, the AU-n that is provided must be aligned to the TXCFRM pulse output and must also be frequency synchronous with either of the TXCCLK or $\overline{\text{TXCCLK}}$ clocks. For more information on the timing modes, see “Transmit Telecom Bus” on page 41. In VC-n mode, a VC-n is supplied to the PHAST-12E; the PHAST-12E calculates a pointer and appends it to the input VC-n, thus creating an AU-n. When VC-n mode is active, it is necessary to have both the J0 and J1 pulses present in the corresponding TXTB#J0J1 signal. The PHAST-12E takes the VC-n and calculates a pointer and appends it to the VC-n, thus creating an AU-n. In 4xSTM-1/STS-3c mode, the MS and RS Overhead are added to the AU-4 by the PHAST-12E and the completed frame is transmitted. In STM-4/STS-12 mode, the AU-4s are byte-interleaved, RS and MS Overhead are added to the multiplexed AU-4s, and the completed STM-4/STS-12 frame is transmitted. When operating in 4 x STM-1/STS-3c mode or STM-4/STS-12 mode, each transmit Telecom Bus interface can be individually configured for AU-4 or VC-4 mode. In STM-4c/STS-12c mode, the four transmit Telecom Buses act as a single transmit Telecom Bus with a 32-bit wide data path. The byte associated with Telecom Bus 1 is the most significant byte and is the first byte that is transmitted. All of the J0J1, SPE, FAIL and clock inputs must be driven with the same signals and the GContTx#(1:0) bits should be set to configure each SFH block for the same mode, either VC-4 or AU-4.

POH processing is not performed when the PHAST-12E is operating in Telecom Bus mode. All POH bytes in the transmit direction are derived from what is input at the transmit Telecom Bus inputs. All POH bytes at the receive Telecom Bus interface are derived directly from the line.

RECEIVE TELECOM BUS INTERFACE

Four output Telecom Buses are provided in the receive direction for interfacing TDM traffic from the line interfaces to path processing devices. Signals are provided for identifying the SPE and J0 plus J1 bytes. Control bits exist to configure each receive Telecom Bus interface individually as to parity calculation, clock edge selection, or J0J1 signal aligned to A23 byte only or to the J0 and J1 bytes.

In 1xSTM-4/STS-12 and 4xSTM-1/STS-3c modes, the Telecom Buses act independently of each other. In STM-4c/STS-12c modes, the four Telecom Buses act in parallel as one Telecom Bus with a 32-bit wide data path. For details refer to, “Receive Telecom Bus” on page 46.

In 1xSTM-4/STS-12 and 1xSTM-4c/STS-12c operation, the received frame is byte demuxed in 1:4 fashion. That is, the data from slot 1 is output on RX Telecom Bus 1, the data from slot 2 is output on Telecom Bus 2, etc.

SIMULTANEOUS TERMINATION OF ATM, PPP, AND TDM TRAFFIC

When the PHAST-12E is configured in either 4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes, the PHAST-12E can support simultaneous processing and termination of ATM, PPP, and TDM data. Each APH block can be individually configured to process ATM or PPP data. When, on the UTOPIA Level 2/2P interface a PHY is selected that corresponds to an APH that is configured for ATM mode, then the UTOPIA Level 2 handshaking is used to transfer the cell or cells. When a PHY is selected that corresponds to an APH that is configured for PPP mode, then the UTOPIA Level 2P handshaking is used to transfer the chunk or chunks of frame data. The payloads that are not terminated into the APH blocks can be terminated into the Telecom Bus Interface. Thus, TDM, ATM, and PPP can be simultaneously supported.

LOOPBACKS

Three loopbacks are supported in the transmit direction and two are supported in the receive direction.

Transmit Loopback Stage 1 is at the ATM Cell Buffer (ACB) interface with the ACH/PPP Chiplets (see Figure 61). As soon as the ACB is not empty, the ACB contents are read and provided to the receive direction. Only the loopback is performed, data is not forwarded to the next level.

Transmit Loopback Stage 2 is at the output of the ACH/PPP Chiplet before the SONET/SDH Frame Handler. The transmit cell stream at the output of the ACH/PPP Chiplet is looped back to the receive side input of the ACH/PPP Chiplet. This cell stream can contain idle/unassigned cells or “PPP in HDLC-like Framing”. Transmit Loopback Stage 2 has two modes. With the first mode, just the loopback is performed and data is not forwarded to the next processing step. The second loopback mode allows data to be forwarded to the next processing step in addition to being looped back.

The third TX Loopback is called the TX Serial Wrap Loopback. This loopback consists of taking the TX serial line output signal and looping it back, internal to the PHAST-12E device, to the RX serial line input. The TX serial line output is still provided to external circuitry while this loopback is enabled.

Receive Loopback Stage 2 causes receive data provided by the SONET/SDH Frame Handler to be looped back towards the transmit direction. There are two modes for this receive loopback, one for loopback only (i.e., no data is passed to the ATM/PPP Handler), and one where data is passed to the ATM/PPP Handler in addition to being looped back. Additionally, when RX Loopback Stage 2 is used, either a C-n or a VC-n (n=4 in 4xSTM-1/STS-3c and 1xSTM-4/STS-12 modes, n=4-4c in 1xSTM-4c/STS-12c mode) can be looped back. When a C-n is looped back, the PHAST-12E adds the POH in the TX direction. When a VC-n is looped back, the PHAST-12E does not touch the POH. Any of the available C-n or VC-n can be individually looped back.

Finally, there is the line RX Parallel Wrap Loopback. This loopback occurs at the boundary between the LIU blocks and the SFH blocks. An entire received frame is looped back towards the transmit direction. The RX parallel data is still supplied to the SFH blocks.

In order for a loopback to be accomplished, the corresponding blocks have to be configured for the same mode of operation. e.g., If it is desired to have a TX Loopback stage 2 performed on channel 2, the TX and RX APH blocks must be configured for the same mode of operation and the SFH blocks should have the same frame format. For instance if TX channel 2 is configured for PPP operation and STM-1 mode, then RX channel 2 must also be configured for PPP operation and STM-1 mode.

Registers GLoopTx1, GLoopTx2, GLoopRx, and SIMR#Conf1 contain the loopback control bits for all five loopbacks.

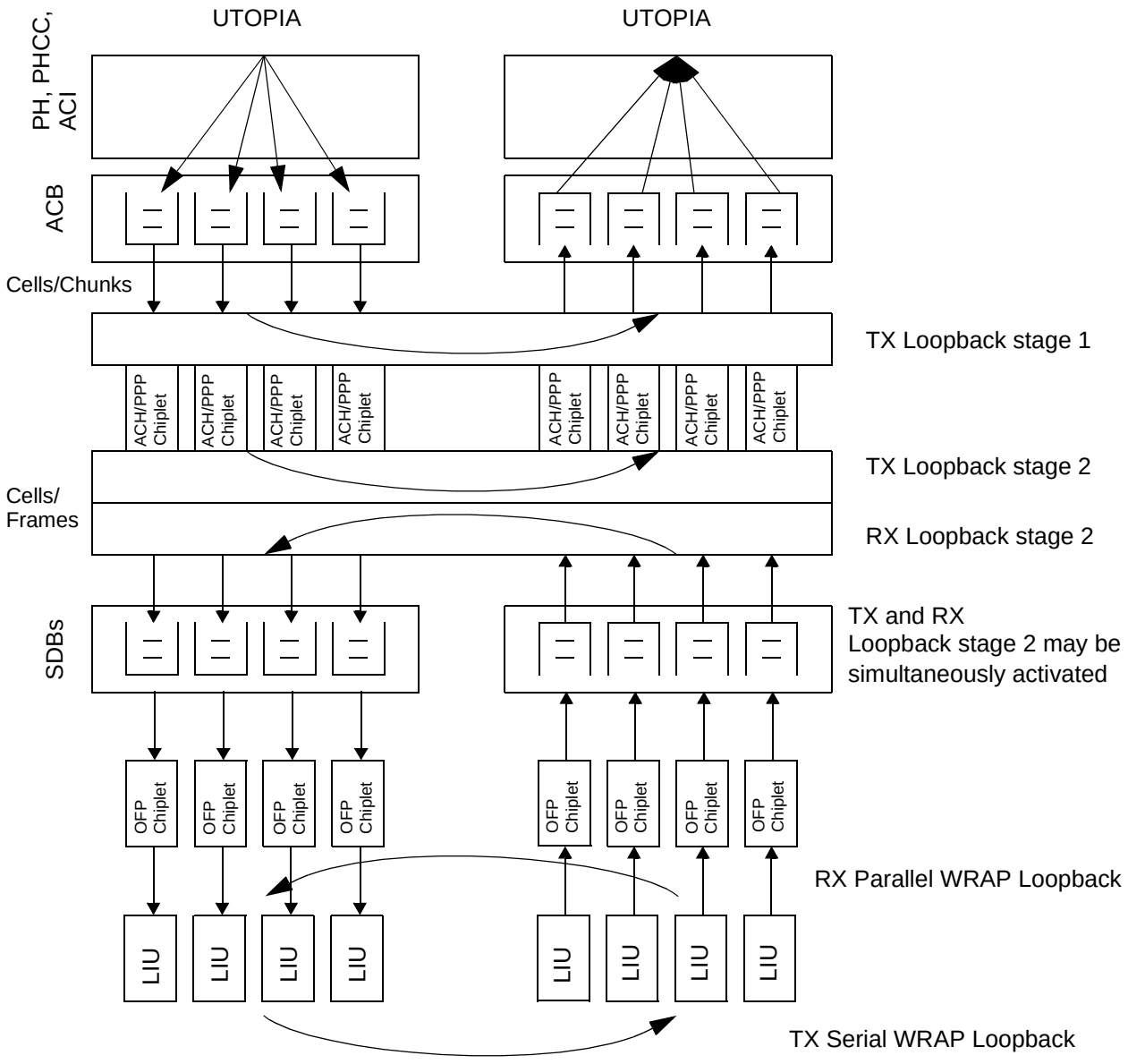


Figure 61. PHAST-12E Loopbacks

MICROPROCESSOR INTERFACE

The PHAST-12E can support either Motorola or Intel microprocessor bus types. The Motorola interface is designed to support a Motorola 68360 microprocessor bus type interface. Either synchronous or asynchronous modes of operation can be selected. In synchronous mode, all of the bus transactions are synchronized to the microprocessor clock. In asynchronous mode, all of the bus transactions are asynchronous with respect to the microprocessor clock and are synchronized internally to the external GPPCLK signal. The Intel-compatible bus interface can also operate in a synchronous or asynchronous mode.

A watchdog timer is provided to allow transactions to a specific block to be terminated when a programmable timer runs out, even if the clock for the block being accessed is not present. If a timeout occurs, an interrupt request bit corresponding to the offending block is set.

BOUNDARY SCAN INTERFACE

A boundary scan interface compliant with IEEE Standard 1149.1-1994 (JTAG) is provided for board level testing of the PHAST-12E. Details of the PHAST-12E boundary scan operation are provided in “Boundary Scan” on page 334.

POWER CONSUMPTION IN VARIOUS MODES

There are five PLLs in the PHAST-12E device associated with the TX and RX line interfaces. One PLL is associated with the TX direction and is used for clock synthesis purposes when any of the TX serial interfaces are used. There are four PLLs in the RX direction, with one PLL associated with each RX serial line interface. These PLLs are used for clock recovery. When operating in STM-4, STM-4c, STS-12 or STS-12c modes and the RX serial line interface is being used, only RX PLL 1 should be enabled. RX PLLs 2-4 must be disabled. Failure to do so, will result in more power being dissipated than specified in “Power Requirements” on page 93. The TX and RX PLLs can be enabled or disabled via the Tx_Enable and Rx#_Enable control bits in the SIMTConf1 and SIMR#Conf1 registers.

THROUGHPUT DELAY

The worst case throughput delays for the PHAST-12E are listed in the table below.

Path that Data Travels	Worst Case Throughput Delay in microseconds
RX Serial Line Input through Port Handler Cross Connect (PHCC) to TX Serial Line output	6.7
RX Serial Line Input to RX Telecom Bus Output	1.0
RX Serial Line Input to RX UTOPIA Bus Output	4.5
TX UTOPIA Bus Input to TX Serial Line Output	13.3
TX Telecom Bus Input to TX Serial Line Output.	5.7

MEMORY MAP

This section contains the address map and register bit descriptions for the internal memory locations of the PHAST-12E device. The Access columns of the tables specify bit access as Read-only (R), Write-only (W) or Read/Write (R/W). When writing to registers that contain bits designated in the following tables as Reserved or Not Used, care should be taken to write those bits with their default values (if specified), or with 0 if no default value is specified.

CHIPLET ADDRESS MAPPING

Table 4. Chiplet Address Mapping

Chiplet Name / Short Name	Chiplet Base Addr.	Chiplet Addr. Range	# of Bytes	See Page
Reserved	0000 H	0000 - 00FF H	256	
ACI_Tx1 / IT1	0100 H	0100 - 01FF H	256	220
Reserved	0200 H	0200 - 02FF H	256	
ACI_Rx1 / IR1	0300 H	0300 - 03FF H	256	226
Reserved	0400 H	0400 - 04FF H	256	
PH_Tx1/ PT1	0500 H	0500 - 05FF H	256	231
PH_Tx2/ PT2	0600 H	0600 - 06FF H	256	231
PH_Tx3/ PT3	0700 H	0700 - 07FF H	256	231
PH_Tx4/ PT4	0800 H	0800 - 08FF H	256	231
PH_Rx1/ PR1	0900 H	0900 - 09FF H	256	234
PH_Rx2/ PR2	0A00 H	0A00 - 0AFF H	256	234
PH_Rx3/ PR3	0B00 H	0B00 - 0BFF H	256	234
PH_Rx4/ PR4	0C00 H	0C00 - 0CFF H	256	234
ACH_Tx1 / HT1	0D00 H	0D00 - 0DFF H	256	236
ACH_Tx2 / HT2	0E00 H	0E00 - 0EFF H	256	248
ACH_Tx3 / HT3	0F00 H	0F00 - 0FFF H	256	248
ACH_Tx4 / HT4	1000 H	1000 - 10FF H	256	248
ACH_Rx1 / HR1	1100 H	1100 - 11FF H	256	255
ACH_Rx2 / HR2	1200 H	1200 - 12FF H	256	266
ACH_Rx3 / HR3	1300 H	1300 - 13FF H	256	266
ACH_Rx4 / HR4	1400 H	1400 - 14FF H	256	266
PPP / PPP	1500 H	1500 - 15FF H	256	275
Reserved	1600 H	1600 - 17FF H	512	

Table 4. Chiplet Address Mapping (Continued)

Chiplet Name / Short Name	Chiplet Base Addr.	Chiplet Addr. Range	# of Bytes	See Page
OFP_Tx1 / OT1	1800 H	1800 - 1BFF H	1024	287
OFP_Tx2 / OT2	1C00 H	1C00 - 1FFF H	1024	287
OFP_Tx3 / OT3	2000 H	2000 - 23FF H	1024	287
OFP_Tx4 / OT4	2400 H	2400 - 27FF H	1024	287
OFP_Rx1 / OR1	2800 H	2800 - 2BFF H	1024	305
OFP_Rx2 / OR2	2C00 H	2C00 - 2FFF H	1024	305
OFP_Rx3 / OR3	3000 H	3000 - 33FF H	1024	305
OFP_Rx4 / OR4	3400 H	3400 - 37FF H	1024	305
GPPINT/ GP	3800 H	3800 - 38FF H	256	171
SIM	3900 H	3900 - 39FF H	256	204
Reserved	3A00 H	3A00 - 3FAF H	1456	
GP Access Protection	3FBF H	3FBF H	1	203
Reserved	3FC0 H	3FC0 - 3FFF H	64	

GPPINT ARCHITECTURE

The General Purpose Processor Interface (GPPINT) provides direct access to registers located in the GPPINT module and direct, but delayed, access to registers and counters located in the GppHandler modules of the various chiplets of PHAST-12E. GPPINT controls the handshaking with the external microprocessor as well as the handshaking with the GppHandlers at the asynchronous chiplet interfaces.

Address decoding is done to the chiplet level in GPPINT. In addition, addresses are decoded to the register level for the local GPPINT registers.

Reset Registers

Each chiplet with the exception of the GPPINT and SIM chiplets is controlled by one reset bit. At power-on, all reset bits are active and the chiplets are disabled. They can be released by the GPP only after all global configuration parameters have been set and the clocks to the chiplets have been established. In addition, there are reset bits for parts of the device that do not have their own GppHandler, like the PIM (Parallel Interface Module) which is part of the LIU. The registers in the GPPINT and SIM chiplets are reset via the $\overline{\text{FRESET}}$ lead.

Interrupt Registers

Figure 62 shows the interrupt structure of the PHAST-12E. The hierarchy used allows the software to quickly pinpoint where an interrupt is coming from by reading the registers pointed to by the interrupt request bits until the source of the interrupt is found. This method enables the software to follow the “trail” to the active interrupt request bit(s) while bypassing inactive registers.

e.g., The software first reads IRQGP1 which points to IRQGP2-5, ClkStat1, or HShake1. The software now goes to the register pointed to by IRQGP1. ClkStat1 and HShake1 point to Interrupt request registers within the GPPINT. IRQGP2-5 point to the Main Chiplet Interrupt Request registers within each individual chiplet.

These main Chiplet Interrupt Request registers point to individual Interrupt Request Registers within their own chiplet, which can then be read by software to identify the cause the interrupt request. Therefore, when an interrupt occurs, instead of reading all of the interrupt request bits, only a small number of accesses are required to pinpoint the cause of an interrupt.

An active bit of the interrupt registers is reset by removing the cause for the request in the corresponding chiplet or by masking the active IRQ (Interrupt Request) bit(s) in the chiplet; therefore, the interrupt registers (including the pointer) are read-only. All interrupt and pointer registers have a corresponding MASK register (Read/Write). Every unmasked, active interrupt bit causes an active pointer bit.

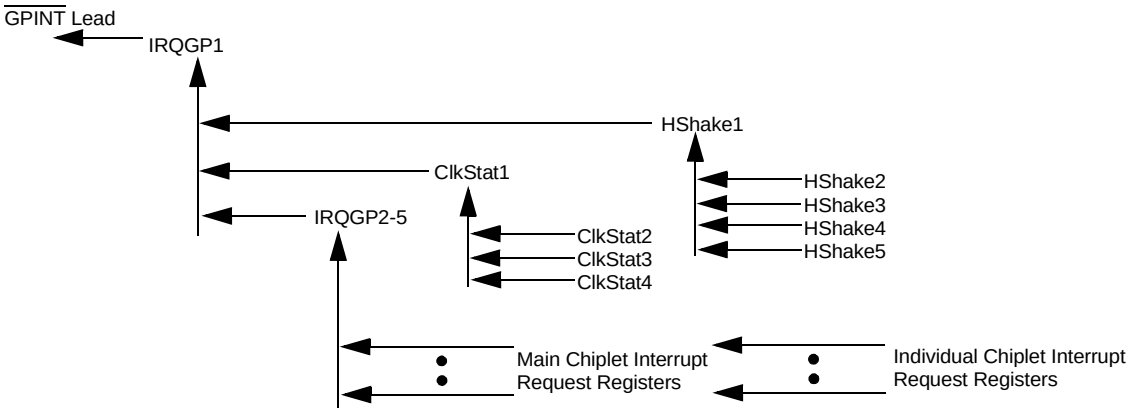


Figure 62. PHAST-12E Interrupt Structure

Handshaking Error Registers

The MAIN handshaking error register (HShake1) is used as a pointer to the other handshaking error registers with pending requests. Each bit of the handshaking error registers indicates a locked interface to one of the GppHandlers. Two additional bits indicate various timeout events. To reset an individual bit of the handshaking error registers the cause for the request must be removed AND a 1 must be written into the bit location of the register (R/W). Reading one of the registers will reset the whole (8-bit) register if the corresponding “clear-register” option is set in the configuration register. All handshaking error indication and pointer registers have a corresponding MASK register (R/W).

Every unmasked, active handshaking error bit causes an active pointer bit. Every unmasked, active pointer bit causes activation of the pointer bit in the MAIN handshaking interrupt register.

Clock Monitor Status Registers

The MAIN clock monitor status register is used as a pointer to the other clock monitor status registers with active error indication bit(s). The clock monitor status register bits indicate the loss of a specific chiplet’s clock. They are set whenever a difference between the clock test signal and the individual chiplets clock acknowledge signal occurs after one clock monitor test period. To reset an individual bit of the clock monitor status registers, the clock of the corresponding chiplet must be restored AND a 1 must be written into the bit location of the register (R/W). Reading one of the registers will reset the whole (8-bit) register if the corresponding “clear-register” option is set in the configuration register. All clock monitor status and pointer registers have a corresponding MASK register (R/W). Every unmasked, active clock monitor status bit causes an active pointer bit. Every unmasked, active pointer bit causes activation of the pointer bit in the MAIN interrupt register.

Local GPPINT Configuration Registers

There are registers (R/W) for the Clock Monitor Test Period, the Watchdog Timer Period and the “clear-register” option.

Global Static Configuration Registers

These registers contain configuration parameters that are shared by many chiplets or that are needed by chiplets that have no GppHandler. The initial values can be modified by the microprocessor after power-up. If these bits are to be changed during normal operation, a global reset should be applied to the affected chiplets, the global static bits should be changed, then the global reset should be removed, and the local chiplet should be configured.

The sequence for setting the global configuration bits and removing the chiplet resets is very important. See Figure 42 on page 132 for the power-up-reset sequence of when the Global Configuration bits should be set and when the Global reset and local reset bits should be de-asserted. The order in which chiplets are brought out of reset is indicated in the “PHAST-12E Power Up, Reset and Autotrim Sequence, on Page 131’ section and must be followed.

Status Registers

These registers provide status information from chiplets that have no GppHandler and are read-only. Presently, there is only one status register for the SIM chiplet (PLL lock status). The bit values follow the driving signal immediately.

GPPINT CHIPLET ADDRESS MAPPING

Chiplet Base Address:

3800 H.

Table 5. GPPINT Chiplet Address Mapping

Register Name	Address Offset (Hex)	Access	Initial Value (binary)	Description (all registers are of 8-bit width)	See Page
RESGP1	00	R/W	11111111	Reset register 1	174
RESGP2	01	R/W	11111111	Reset register 2	175
RESGP3	02	R/W	11111111	Reset register 3	175
RESGP4	03	R/W	11111111	Reset register 4	175
RESGP5	04	R/W	11111111	Reset register 5	176
RESGP6	05	R/W	11000000	Reset register 6	176
	06 - 0F			Reserved	
IRQGP1	10	R	00000000	Chiplet interrupt request register 1	177
IRQGP2	11	R	00000000	Chiplet interrupt request register 2	177
IRQGP3	12	R	00000000	Chiplet interrupt request register 3	177

Table 5. GPPINT Chiplet Address Mapping (Continued)

Register Name	Address Offset (Hex)	Access	Initial Value (binary)	Description (all registers are of 8-bit width)	See Page
IRQGP4	13	R	00000000	Chiplet interrupt request register 4	178
IRQGP5	14	R	00000000	Chiplet interrupt request register 5	178
	15 - 17			Reserved	
IRMGP1	18	R/W	00000000	Chiplet interrupt mask register 1	177
IRMGP2	19	R/W	00000000	Chiplet interrupt mask register 2	177
IRMGP3	1A	R/W	00000000	Chiplet interrupt mask register 3	177
IRMGP4	1B	R/W	00000000	Chiplet interrupt mask register 4	178
IRMGP5	1C	R/W	00000000	Chiplet interrupt mask register 5	178
	1D - 1F			Reserved	
HShake1	20	R/W	00000000	Handshaking error register 1	179
HShake2	21	R/W	00000000	Handshaking error register 2	180
HShake3	22	R/W	00000000	Handshaking error register 3	180
HShake4	23	R/W	00000000	Handshaking error register 4	180
HShake5	24	R/W	00000000	Handshaking error register 5	181
	25 - 27			Reserved	
HSMask1	28	R/W	00000000	Handshaking error mask register 1	179
HSMask2	29	R/W	00000000	Handshaking error mask register 2	180
HSMask3	2A	R/W	00000000	Handshaking error mask register 3	180
HSMask4	2B	R/W	00000000	Handshaking error mask register 4	180
HSMask5	2C	R/W	00000000	Handshaking error mask register 5	181
	2D - 2F			Reserved	
ClkStat1	30	R/W	00000000	Clock status register 1	182
ClkStat2	31	R/W	00000000	Clock status register 2	182
ClkStat3	32	R/W	00000000	Clock status register 3	182
ClkStat4	33	R/W	00000000	Clock status register 4	183
	34 - 37			Reserved	
ClkMask1	38	R/W	00000000	Clock status mask register 1	182
ClkMask2	39	R/W	00000000	Clock status mask register 2	182
ClkMask3	3A	R/W	00000000	Clock status mask register 3	182
ClkMask4	3B	R/W	00000000	Clock status mask register 4	183

Table 5. GPPINT Chiplet Address Mapping (Continued)

Register Name	Address Offset (Hex)	Access	Initial Value (binary)	Description (all registers are of 8-bit width)	See Page
	3C - 47			Reserved	
CMonGP1	48	R/W	00000000	Clock monitor test period	183
WDTGP1	49	R/W	11111111	Watchdog timer period	184
ConfGP1	4A	R/W	11111111	“Clear-register” option register	184
	4B - 4F			Reserved	
VPD	50	R	01000100	TXC Internal Use Register	185
	51 - 57			Reserved	
GContTx	58	R/W	00000000	ATM/Loop/TB static configuration register for transmit	188
GContRx	59	R/W	00000000	ATM/Loop/TB static configuration register for receive	189
GCasc	5A	R/W	10001000	Common Cascading static configuration register	190, 191
GLoopTx1	5B	R/W	00000000	Transmit Loopback 1 static configuration register	191
GLoopTx2	5C	R/W	00000000	Transmit Loopback 2 static configuration register	192
GLoopRx	5D	R/W	00000000	Receive Loopback static configuration register	193
GExtRes	5E	R/W	00000000	External clock recovery circuit reset register	193
	5F			Reserved	
ACITXGP	60	R/W	00010110	ACI_Tx UTOPIA static configuration register	195
PHTXGP1	61	R/W	00010001	ACI_Tx Source selection static configuration register 1	195
PHTXGP2	62	R/W	00010001	ACI_Tx Source selection static configuration register 2	196
ACIRXGP	63	R/W	00010110	ACI_Rx UTOPIA static configuration register	196
PHRXGP	64	R/W	01010101	ACI_Rx Sink selection static configuration register	197
PPPGP1	66	R/W	00000000	PPP static configuration register 1	197
PPPGP2	67	R/W	00000110	PPP static configuration register 2	198
OFPTXGP	68	R/W	00000000	OFP_Tx static configuration register	199
OFPRXGP1	69	R/W	00000000	OFP_Rx static configuration register 1	200

Table 5. GPPINT Chiplet Address Mapping (Continued)

Register Name	Address Offset (Hex)	Access	Initial Value (binary)	Description (all registers are of 8-bit width)	See Page
OFPRXGP2	6A	R/W	00000000	OFP_Rx static configuration register 2	200
AIPConf	6B	R/W	00000000	AIP (Ring Port) configuration register	200
CBConf1	6C	R/W	00000000	Telecom Bus static configuration register 1	194
CBConf2	6D	R/W	00000000	Telecom Bus static configuration register 2	194
	6E - 6F			Reserved	
PIMTConf1	70	R/W	00000001	PIM_Tx static configuration register 1	201
	71			Reserved	
PIMRConf1	72	R/W	00000001	PIM_Rx static configuration register 1	202
PIMRConf2	73	R/W	00000000	PIM_Rx static configuration register 2	202
	74 - 7E			Reserved	
SIMStat	7F	R	0000000x	SIM status register	203
	80-88			Reserved	
	89 - FF			Reserved	

Chiplet Reset Registers

The bits of the chiplet reset registers control the resetting (enabling /disabling) of complete chiplets. If a static control bit for a chiplet is changed after the PHAST-12E has been set up, then the corresponding chiplets in the affected macro must have their chiplet reset through the RESGP1-6 registers below. This, in turn, would necessitate reconfiguration of the affected chiplet(s).

For each bit position:

0: Reset inactive for this chiplet

1: Reset active (chiplet is disabled; DEFAULT)

Table 6. RESGP1 [3800 H]

Signal Name	Bit Pos.	Access	Default	Description
ResPT4	0	R/W	1	Reset to chiplet PH_Tx4
ResPT3	1	R/W	1	Reset to chiplet PH_Tx3
ResPT2	2	R/W	1	Reset to chiplet PH_Tx2
ResPT1	3	R/W	1	Reset to chiplet PH_Tx1

Table 6. RESGP1 [3800 H] (Continued)

Signal Name	Bit Pos.	Access	Default	Description
Reserved	4	R/W	1	Reserved
ResIR1	5	R/W	1	Reset to chiplet ACI_Rx1
Reserved	6	R/W	1	Reserved
ResIT1	7	R/W	1	Reset to chiplet ACI_Tx1

Table 7. RESGP2 [3801 H]

Signal Name	Bit Pos.	Access	Default	Description
ResHT4	0	R/W	1	Reset to chiplet ACH_Tx4
ResHT3	1	R/W	1	Reset to chiplet ACH_Tx3
ResHT2	2	R/W	1	Reset to chiplet ACH_Tx2
ResHT1	3	R/W	1	Reset to chiplet ACH_Tx1
ResPR4	4	R/W	1	Reset to chiplet PH_Rx4
ResPR3	5	R/W	1	Reset to chiplet PH_Rx3
ResPR2	6	R/W	1	Reset to chiplet PH_Rx2
ResPR1	7	R/W	1	Reset to chiplet PH_Rx1

Table 8. RESGP3 [3802 H]

Signal Name	Bit Pos.	Access	Default	Description
ResOT4	0	R/W	1	Reset to chiplet OFP_Tx4
ResOT3	1	R/W	1	Reset to chiplet OFP_Tx3
ResOT2	2	R/W	1	Reset to chiplet OFP_Tx2
ResOT1	3	R/W	1	Reset to chiplet OFP_Tx1
ResHR4	4	R/W	1	Reset to chiplet ACH_Rx4
ResHR3	5	R/W	1	Reset to chiplet ACH_Rx3
ResHR2	6	R/W	1	Reset to chiplet ACH_Rx2
ResHR1	7	R/W	1	Reset to chiplet ACH_Rx1

Table 9. RESGP4 [3803 H]

Signal Name	Bit Pos.	Access	Default	Description
APSRxRes	0	R/W	1	Reset to APS_Rx
APSTxRes	1	R/W	1	Reset to APS_Tx
ResPPP	2	R/W	1	Reset to chiplet PPP
Reserved	3	R/W	1	Reserved
ResOR4	4	R/W	1	Reset to chiplet OFP_Rx4
ResOR3	5	R/W	1	Reset to chiplet OFP_Rx3

Table 9. RESGP4 [3803 H] (Continued)

Signal Name	Bit Pos.	Access	Default	Description
ResOR2	6	R/W	1	Reset to chiplet OFP_Rx2
ResOR1	7	R/W	1	Reset to chiplet OFP_Rx1

Table 10. RESGP5 [3804 H]

Signal Name	Bit Pos.	Access	Default	Description
RxRPIS4	0	R/W	1	Reset to chiplet PIS_Rx4
RxRPIS3	1	R/W	1	Reset to chiplet PIS_Rx3
RxRPIS2	2	R/W	1	Reset to chiplet PIS_Rx2
RxRPIS1	3	R/W	1	Reset to chiplet PIS_Rx1
TxRPIS4	4	R/W	1	Reset to chiplet PIS_Tx4
TxRPIS3	5	R/W	1	Reset to chiplet PIS_Tx3
TxRPIS2	6	R/W	1	Reset to chiplet PIS_Tx2
TxRPIS1	7	R/W	1	Reset to chiplet PIS_Tx1

Table 11. RESGP6 [3805 H]

Signal Name	Bit Pos.	Access	Default	Description
Reserved	5:0	R/W	000000	Reserved
RxRPIM	6	R/W	1	Reset to chiplet PIM_Rx
TxRPIM	7	R/W	1	Reset to chiplet PIM_Tx

Chiplet Interrupt Request and Mask Registers

The chiplet interrupt request registers indicate pending interrupt requests from individual chiplets. An active bit of these registers is reset by removing the cause for the request in the corresponding chiplet or by masking the active IRQ bit(s) in the chiplet; therefore, these registers are read-only.

For each bit position:

0: No chiplet interrupt request pending

1: Chiplet has pending interrupt request(s)

The chiplet interrupt request mask register bits control the propagation of a chiplet interrupt request to the PHAST-12E device interrupt output lead. The mask registers allow read and write access.

For each bit position:

0: The corresponding interrupt request bit is masked (DEFAULT)

1: The corresponding interrupt request bit is active (for IRMGP1: the corresponding interrupt request bit activates the PHAST-12E device Interrupt lead)

Table 12. IRQGP1, IRMGP1 [3810 H Request, 3818 H Mask]

Signal Name	Bit Pos.	Access	Default	Description
FElocHS	0	R	0	Pending handshaking error active. This bit is set when a bit in the HShake1 register and its corresponding interrupt mask bit in the HSMask1 register are both set to 1.
FElocCS	1	R	0	Pending clock status error active. This bit is set when a bit in the ClkStat1 register and its corresponding interrupt mask bit in the ClkMask1 register are both set to 1.
Reserved	2	R	0	Reserved
Reserved	3	R	0	Reserved
IRQGP5	4	R	0	Pending IRQ active in IRQGP5 register.
IRQGP4	5	R	0	Pending IRQ active in IRQGP4 register.
IRQGP3	6	R	0	Pending IRQ active in IRQGP3 register.
IRQGP2	7	R	0	Pending IRQ active in IRQGP2 register.

Table 13. IRQGP2, IRMGP2 [3811 H Request, 3819 H Mask]

Signal Name	Bit Pos.	Access	Default	Description
IRQPT4	0	R	0	IRQ (Interrupt Request) from PH_Tx4
IRQPT3	1	R	0	IRQ from PH_Tx3
IRQPT2	2	R	0	IRQ from PH_Tx2
IRQPT1	3	R	0	IRQ from PH_Tx1
Reserved	4	R	0	Reserved
IRQIR1	5	R	0	IRQ from ACI_Rx1
Reserved	6	R	0	Reserved
IRQIT1	7	R	0	IRQ from ACI_Tx1

Table 14. IRQGP3, IRMGP3 [3812 H Request, 381A H Mask]

Signal Name	Bit Pos.	Access	Default	Description
IRQHT4	0	R	0	IRQ from ACH_Tx4
IRQHT3	1	R	0	IRQ from ACH_Tx3
IRQHT2	2	R	0	IRQ from ACH_Tx2
IRQHT1	3	R	0	IRQ from ACH_Tx1
IRQPR4	4	R	0	IRQ from PH_Rx4
IRQPR3	5	R	0	IRQ from PH_Rx3
IRQPR2	6	R	0	IRQ from PH_Rx2
IRQPR1	7	R	0	IRQ from PH_Rx1

Table 15. IRQGP4, IRMGP4 [3813 H Request, 381B H Mask]

Signal Name	Bit Pos.	Access	Default	Description
IRQOT4	0	R	0	IRQ from OFP_Tx4
IRQOT3	1	R	0	IRQ from OFP_Tx3
IRQOT2	2	R	0	IRQ from OFP_Tx2
IRQOT1	3	R	0	IRQ from OFP_Tx1
IRQHR4	4	R	0	IRQ from ACH_Rx4
IRQHR3	5	R	0	IRQ from ACH_Rx3
IRQHR2	6	R	0	IRQ from ACH_Rx2
IRQHR1	7	R	0	IRQ from ACH_Rx1

Table 16. IRQGP5, IRMGP5 [3814 H Request, 381C H Mask]

Signal Name	Bit Pos.	Access	Default	Description
Reserved	2:0	R	000	Reserved
IRQPPP	3	R	0	IRQ from PPP
IRQOR4	4	R	0	IRQ from OFP_Rx4
IRQOR3	5	R	0	IRQ from OFP_Rx3
IRQOR2	6	R	0	IRQ from OFP_Rx2
IRQOR1	7	R	0	IRQ from OFP_Rx1

Handshaking Error Indication and Mask Registers

The local handshaking error indication registers indicate pending handshaking error requests from the GPPINT chiplet. HShake1 consists of pointer bits that indicate active requests in registers HShake2/3/4/5.

For each bit position:

0: Normal operation of the corresponding chiplet

1: The corresponding chiplet did not assert its DTACK signal before the watchdog timer expired.

Exception: The signals AccViol, TOError and IntError (HShake5(2:0)). TOError and IntError have the following meaning:

Table 17. TOError and IntError meanings

TOError	IntError	Description
0	0	normal operation
0	1	GPP de-asserts strobes without waiting for GPDTACK assertion. This means that the external microprocessor, instead of inserting more wait states, has de-asserted either GPSEL or GPDS (GPRD/GPWR in Intel mode) before the GPDTACK signal was asserted.
1	0	Watchdog Timeout in REST state. A timeout in this state indicates that the chiplet addressed in the current read cycle has a problem.
1	1	Watchdog Timeout in REQ state. A timeout in this state indicates that the PHAST-12E was busy working on the prior read or write transaction when the timeout occurred and the current transaction has also failed. Both accesses must be performed again after the problem(s) that caused the timeout(s) is (are) resolved.

An active bit of the handshaking error indication registers is reset by removing the cause for the malfunctioning of the chiplet and by writing a 1 into the corresponding bit position. Reading one of these registers will reset all bits of this register if the “clear-register” option is set in ConfGP1(2).

Handshake errors occur when a chiplet does not assert its internal DTACK signal before the watchdog timer expires. There can be several causes such as, a clock is missing from a chiplet, or the microprocessor interface handshaking caused the error (see the TOError and IntError bits).

Recovery depends on the type of error. For instance, if a clock was missing from a chiplet, that clock has to be restored, the global reset for that chiplet has to be activated and then deactivated, then the chiplet needs to be reconfigured. If the microprocessor interface handshaking caused the error as indicated by the TOError and IntError bits, the actions indicated in the table 15 will need to be done. If TOError, IntError = 01, then there is a problem with the handshaking on the microprocessor’s bus.

The handshaking error indication mask register bits control the propagation of the GPPINT handshaking error requests to bits 7 to 4 of register HShake1. HSMask1 controls propagation to the signal FElocHS (bit 0 of IRQGP1 register). The mask registers allow read and write access.

For each bit position:

0: The corresponding handshaking error indication bit is masked (DEFAULT)

1: The corresponding request bit is active (for HSMask1: the corresponding request bit activates signal FElocHS (bit 0 of IRQGP1 register)).

HShake1 (HSMask1): “clear-register” option is set in ConfGP1(2)

Table 18. HShake1, HSMask1 [3820 H Error, 3828 H Mask]

Signal Name	Bit Pos.	Access	Default	Description
SIM	0	R/W	0	DTACK from SIM stuck at one
Reserved	1:3	R/W	0000	Reserved (pointers)
HShake5	4	R/W	0	Pending HS error active in HShake5
HShake4	5	R/W	0	Pending HS error active in HShake4
HShake3	6	R/W	0	Pending HS error active in HShake3
HShake2	7	R/W	0	Pending HS error active in HShake2

Table 19. HShake2, HSMask2 [3821 H Error, 3829 H Mask]

Signal Name	Bit Pos.	Access	Default	Description
PH_Tx4	0	R/W	0	DTACK from PH_Tx4 stuck at ONE
PH_Tx3	1	R/W	0	DTACK from PH_Tx3 stuck at ONE
PH_Tx2	2	R/W	0	DTACK from PH_Tx2 stuck at ONE
PH_Tx1	3	R/W	0	DTACK from PH_Tx1 stuck at ONE
Reserved	4	R/W	0	Reserved
ACI-Rx1	5	R/W	0	DTACK from ACI_Rx1 stuck at ONE
Reserved	6	R/W	0	Reserved
ACI-Tx1	7	R/W	0	DTACK from ACI_Tx1 stuck at ONE

Table 20. HShake3, HSMask3 [3822 H Error, 382A H Mask]

Signal Name	Bit Pos.	Access	Default	Description
ACH_Tx4	0	R/W	0	DTACK from ACH_Tx4 stuck at ONE
ACH_Tx3	1	R/W	0	DTACK from ACH_Tx3 stuck at ONE
ACH_Tx2	2	R/W	0	DTACK from ACH_Tx2 stuck at ONE
ACH_Tx1	3	R/W	0	DTACK from ACH_Tx1 stuck at ONE
PH_Rx4	4	R/W	0	DTACK from PH_Rx4 stuck at ONE
PH_Rx3	5	R/W	0	DTACK from PH_Rx3 stuck at ONE
PH_Rx2	6	R/W	0	DTACK from PH_Rx2 stuck at ONE
PH_Rx1	7	R/W	0	DTACK from PH_Rx1 stuck at ONE

Table 21. HShake4, HSMask4 [3823 H Error, 382B H Mask]

Signal Name	Bit Pos.	Access	Default	Description
OFP_Tx4	0	R/W	0	DTACK from OFP_Tx4 stuck at ONE
OFP_Tx3	1	R/W	0	DTACK from OFP_Tx3 stuck at ONE
OFP_Tx2	2	R/W	0	DTACK from OFP_Tx2 stuck at ONE
OFP_Tx1	3	R/W	0	DTACK from OFP_Tx1 stuck at ONE
ACH_Rx4	4	R/W	0	DTACK from ACH_Rx4 stuck at ONE
ACH_Rx3	5	R/W	0	DTACK from ACH_Rx3 stuck at ONE
ACH_Rx2	6	R/W	0	DTACK from ACH_Rx2 stuck at ONE
ACH_Rx1	7	R/W	0	DTACK from ACH_Rx1 stuck at ONE

Table 22. HShake5, HSMask5 [3824 H Error, 382C H Mask]

Signal Name	Bit Pos.	Access	Default	Description
IntError	0	R/W	0	GPP Interface Error (see above)
TOError	1	R/W	0	TimeOut Error of the GPP interface (see above)
AccViol	2	R/W	0	Write access to protected register
PPP	3	R/W	0	DTACK from PPP stuck at ONE
OFP_Rx4	4	R/W	0	DTACK from OFP_Rx4 stuck at ONE
OFP_Rx3	5	R/W	0	DTACK from OFP_Rx3 stuck at ONE
OFP_Rx2	6	R/W	0	DTACK from OFP_Rx2 stuck at ONE
OFP_Rx1	7	R/W	0	DTACK from OFP_Rx1 stuck at ONE

Clock Monitor Status and Mask Registers

The clock monitor status register bits indicate the loss of a specific island's clock. They are set whenever a difference between the clock test signal and the individual island's clock acknowledge signal occurs after the clock monitor test period. ClkStat1 consists of pointer bits that indicate active clock status errors in ClkStat2/3/4.

For each bit position:

0: Normal operation of the corresponding clock island

1: The corresponding island clock is lost

An active bit of these registers is reset by restoring the clock of the corresponding clock island and by writing a 1 into the corresponding bit position. Reading one register will reset all bits of this register if the "clear-register" option is set in bit ConfGP1(3).

The clock monitor mask registers ClkMask2/3/4 control the propagation of active clock monitor status signals to bits 7/6/5 of ClkStat1. ClkMask1 controls propagation to the signal FElocCS (bit 1 of IRQGP1 register). The mask registers allow read and write access.

It is important to note that at any time a clock is removed from a chiplet and established again, the global reset for that chiplet must be applied (for at least two clock cycles for that chiplet) and removed to establish local default values in that chiplet and associated state machines.

For each bit position:

0: The corresponding clock status bit is masked (DEFAULT)

1: The corresponding clock status bit is active (for ClkMask1: the corresponding bit activates the signal FElocCS (bit 1 of IRQGP1 register))

Table 23. ClkStat1, ClkMask1 [3830 H Status, 3838 H Mask]

Signal Name	Bit Pos.	Access	Default	Description
Reserved	4:0	R/W	00000	Reserved
ClkStat4	5	R/W	0	Pending active clock status error indication in ClkStat4 register
ClkStat3	6	R/W	0	Pending active clock status error indication in ClkStat3 register
ClkStat2	7	R/W	0	Pending active clock status error indication in ClkStat2 register

Table 24. ClkStat2, ClkMask2 [3831 H Status, 3839 H Mask]

Signal Name	Bit Pos.	Access	Default	Description
PH_Tx4	0	R/W	0	Clock island PH_Tx4 lost clock
PH_Tx3	1	R/W	0	Clock island PH_Tx3 lost clock
PH_Tx2	2	R/W	0	Clock island PH_Tx2 lost clock
PH_Tx1	3	R/W	0	Clock island PH_Tx1 lost clock
Reserved	4	R/W	0	Reserved
ACI_Rx1	5	R/W	0	Clock island ACI_Rx1 lost clock
Reserved	6	R/W	0	Reserved
ACI_Tx1	7	R/W	0	Clock island ACI_Tx1 lost clock

Table 25. ClkStat3, ClkMask3 [3832 H Status, 383A H Mask]

Signal Name	Bit Pos.	Access	Default	Description
OFP_Rx2	0	R/W	0	Clock island OFP_Rx2 lost clock
OFP_Rx1	1	R/W	0	Clock island OFP_Rx1 lost clock
OFP_Tx	2	R/W	0	Clock island OFP_Tx lost clock
ACHCLK	3	R/W	0	Clock island ACH lost clock
PH_Rx4	4	R/W	0	Clock island PH_Rx4 lost clock
PH_Rx3	5	R/W	0	Clock island PH_Rx3 lost clock
PH_Rx2	6	R/W	0	Clock island PH_Rx2 lost clock
PH_Rx1	7	R/W	0	Clock island PH_Rx1 lost clock

Table 26. ClkStat4, ClkMask4 [3833 H Status, 383B H Mask]

Signal Name	Bit Pos.	Access	Default	Description
Reserved	0	R/W	0	Reserved
COMBUS4	1	R/W	0	Clock island Telecom Bus 4 lost clock
COMBUS3	2	R/W	0	Clock island Telecom Bus 3 lost clock
COMBUS2	3	R/W	0	Clock island Telecom Bus 2 lost clock
COMBUS1	4	R/W	0	Clock island Telecom Bus 1 lost clock
LTRC	5	R/W	0	Clock island AIP lost clock. Either or both of the LineRING or PathRING bits must be set to a 1 in order for this bit to function.
OFP_Rx4	6	R/W	0	Clock island OFP_Rx4 lost clock
OFP_Rx3	7	R/W	0	Clock island OFP_Rx3 lost clock

Clock Monitor Test Period Register

CMonGP1: Divider ratio to derive the clock monitor test period from the GPPCLK clock. Clock monitoring is disabled if equal to 00 H (DEFAULT). A 50 MHz GGPCLK frequency results in a maximum of 5.1 µs for the clock test period. This allows clock islands down to a frequency of 196.078 kHz to be monitored.

Note: If the UTOPIA interface clocks go below 197 kHz when a 50 MHz GPPCLK clock is used and the Clock Monitor Test Period Register is set to FF H, then an interrupt will be generated because the UTOPIA clock period will be smaller than the clock monitor test period. In this case the interrupt could be masked or the Clock Monitor Test Period Register can be set to 00 H.

Table 27. CMonGP1 [3848 H]

Signal Name	Bit Pos.	Access	Default	Description
CMonGP1(7:0)	7:0	R/W	00000000	Number of GPPCLK cycles/test period

Watchdog Timer Period Register

WDTGP1: Divider ratio to derive the interface timeout period from the GPPCLK clock. The value written to this register is reloaded into an internal down-counter each time that the down-counter reaches a count of zero. The purpose of the watchdog timer is to set a limit as to how long an access is allowed to last before that access is terminated by the $\overline{\text{GPDTACK}}$/$\overline{\text{GPRDY}}$ signal being forced active. A maskable interrupt can be generated to the external microprocessor when the watchdog timer times out.

The watchdog timer counts the number of GPPCLK clocks since the time that a register has been accessed. The access will terminate when either of the following two events occurs:

1. The watchdog timer times out (in which case, the $\overline{\text{GPDTACK}}$/$\overline{\text{GPRDY}}$ signal is forced active so that the cycle terminates). In this case the write does not occur or the read does not return valid data.
2. The cycle terminates normally.

Table 28. WDTGP1 [3849 H]

Signal Name	Bit Pos.	Access	Default	Description
WDTGP1(7:0)	7:0	R/W	11111111	Number of GPPCLK clock cycles per timeout period

Local (GPPINT) Configuration Register

ConfGP1: The bits of this local configuration register control the resetting of complete registers upon read access (“clear-register” option).

For each bit position:

0: No action upon read access

1: The corresponding register is reset upon read access (DEFAULT)

Table 29. ConfGP1 [384A H]

Signal Name	Bit Pos.	Access	Default	Description
Reserved	0	R/W	1	Reserved
SIMStat	1	R/W	1	Clear-bit for register SIMStat. When this bit is set to a 1 the bits in the SIMStat register clear on read. When set to a 0, the bits in the SIMStat register do not clear on read. For either setting of this bit, the bits in the SIMStat register can be individually cleared by writing a 1 to them, provided that the alarm condition is removed.
HShake	2	R/W	1	Clear-bit for registers HShake1-5. When this bit is set to a 1 the bits in the HShake1-5 registers clear on read. When set to a 0, the bits in the HShake1-5 registers do not clear on read. For either setting of this bit, the bits in the HShake1-5 registers can be individually cleared by writing a 1 to them, provided that the alarm condition is removed.
ClkStat	3	R/W	1	Clear-bit for registers ClkStat1-4. When this bit is set to a 1 the bits in the ClkStat1-4 registers clear on read. When set to a 0, the bits in the ClkStat1-4 registers do not clear on read. For either setting of this bit, the bits in the ClkStat1-4 registers can be individually cleared by writing a 1 to them, provided that the alarm condition is removed.
Reserved	7:4	R/W	1111	Reserved

TranSwitch Internal Use Register

VPD: This read-only register is for internal TXC use only.

Table 30. VPD [3850 H]

Signal Name	Bit Pos.	Access	Default	Description
TEST	7:0	R	01000100	This register is for TXC internal use. The bits are for internal TXC use.

Static Configuration Registers

Common static configuration data, providing control signals that are distributed to multiple chiplets. This is set once by the GPP before the individual chiplets become enabled and is not normally changed during operation. Mixed mode operation is possible, e.g., some chiplets can be configured for ATM and some can be configured for Telecom Bus mode and some chiplets can be configured for PPP. All three modes at the same time are possible (i.e., PPP, ATM, and Telecom Bus modes at the same time).

When the PHAST-12E is in a multiservice application where any combination of ATM, PPP, and TDM data is processed by a macro, it may be desired to reconfigure a macro to process a different data type. The table below gives the reconfiguration sequence for such cases.

Table 31. In-Service Macro Reconfiguration

Current Data Type	Desired Data Type	Reconfiguration Sequence.
ATM	PPP	• Set the global reset bits for the affected PT#, PR#, HT#, and HR# chiplets. Clear the enable bits in the local PPP chiplet registers for the affected PPP chiplets. • Set the appropriate static configuration registers in the GPPINT chiplet. • Clear the global reset bits for the affected PT#, PR#, HT#, and HR# chiplets. • Configure the affected PPP, PT#, PR#, HT#, and HR# chiplets. • Clear the local chiplet reset registers (xx30 H) of the affected PT#, PR#, HT#, and HR# chiplets. Set the enable bits in the local PPP chiplet registers for the affected PPP chiplets.
ATM	Telecom Bus VC-n mode	• Set the global reset bits for the affected PT#, PR#, HT#, and HR# chiplets. • Set the appropriate static configuration registers in the GPPINT chiplet. • Clear the global reset bits for the affected HT# chiplet. • Configure the affected HT# chiplet. • Clear the local chiplet reset register (xx30 H) of the affected HT# chiplet.

Table 31. In-Service Macro Reconfiguration (Continued)

Current Data Type	Desired Data Type	Reconfiguration Sequence.
ATM	Telecom Bus AU-n mode	• Set the global reset bits for the affected PT#, PR#, HT#, and HR# chiplets. • Set the appropriate static configuration registers in the GPPINT chiplet.
PPP	ATM	• Set the global reset bits for the affected PT#, PR#, HT#, and HR# chiplets. Clear the enable bits in the local PPP chiplet registers for the affected PPP chiplets. • Set the appropriate static configuration registers in the GPPINT chiplet. • Clear the global reset bits for the affected PT#, PR#, HT#, and HR# chiplets. • Configure the affected PT#, PR#, HT#, and HR# chiplets. • Clear the local chiplet reset registers (xx30 H) of the affected PT#, PR#, HT#, and HR# chiplets.
PPP	Telecom Bus VC-n mode	• Set the global reset bits for the affected PT#, PR#, HT#, and HR# chiplets. Clear the enable bits in the local PPP chiplet registers for the affected PPP chiplets. • Set the appropriate static configuration registers in the GPPINT chiplet. • Clear the global reset bits for the affected HT# chiplet. • Configure the affected HT# chiplet. • Clear the local chiplet reset register (xx30 H) of the affected HT# chiplet.
PPP	Telecom Bus AU-n mode	• Set the global reset bits for the affected PT#, PR#, HT#, and HR# chiplets. Clear the enable bits in the local PPP chiplet registers for the affected PPP chiplets. • Set the appropriate static configuration registers in the GPPINT chiplet.
Telecom Bus VC-n mode	ATM	• Set the global reset bits for the affected PT#, PR#, HT#, and HR# chiplets. • Set the appropriate static configuration registers in the GPPINT chiplet. • Clear the global reset bits for the affected PT#, PR#, HT#, and HR# chiplets. • Configure the affected PT#, PR#, HT#, and HR# chiplets. • Clear the local chiplet reset registers (xx30 H) of the affected PT#, PR#, HT#, and HR# chiplets.

Table 31. In-Service Macro Reconfiguration (Continued)

Current Data Type	Desired Data Type	Reconfiguration Sequence.
Telecom Bus VC-n mode	PPP	• Set the global reset bits for the affected PT#, PR#, HT#, and HR# chiplets. Clear the enable bits in the local PPP chiplet registers for the affected PPP chiplets. • Set the appropriate static configuration registers in the GPPINT chiplet. • Clear the global reset bits for the affected PT#, PR#, HT#, and HR# chiplets. • Configure the affected PPP, PT#, PR#, HT#, and HR# chiplets. • Clear the local chiplet reset registers (xx30 H) of the affected PT#, PR#, HT#, and HR# chiplets. Set the enable bits in the local PPP chiplet registers for the affected PPP chiplets.
Telecom Bus VC-n mode	Telecom Bus AU-n mode	• Set the global reset bit for the affected HT# chiplet. • Set the appropriate static configuration registers in the GPPINT chiplet.
Telecom Bus AU-n mode	ATM	• Set the global reset bits for the affected PT#, PR#, HT#, and HR# chiplets. • Set the appropriate static configuration registers in the GPPINT chiplet. • Clear the global reset bits for the affected PT#, PR#, HT#, and HR# chiplets. • Configure the affected PT#, PR#, HT#, and HR# chiplets. • Clear the local chiplet reset registers (xx30 H) of the affected PT#, PR#, HT#, and HR# chiplets.
Telecom Bus AU-n mode	PPP	• Set the global reset bits for the affected PT#, PR#, HT#, and HR# chiplets. Clear the enable bits in the local PPP chiplet registers for the affected PPP chiplets. • Set the appropriate static configuration registers in the GPPINT chiplet. • Clear the global reset bits for the affected PT#, PR#, HT#, and HR# chiplets. • Configure the affected PPP, PT#, PR#, HT#, and HR# chiplets. • Clear the local chiplet reset registers (xx30 H) of the affected PT#, PR#, HT#, and HR# chiplets. Set the enable bits in the local PPP chiplet registers for the affected PPP chiplets.
Telecom Bus AU-n mode	Telecom Bus VC-n mode	• Set the global reset bits for the affected HT# chiplet. • Set the appropriate static configuration registers in the GPPINT chiplet. • Clear the global reset bits for the affected HT# chiplet. • Configure the affected HT# chiplet. • Clear the local chiplet reset register (xx30 H) of the affected HT# chiplet.

GContTx: Container handling in transmit macros. The ACH, PPP, and PH chiplets are affected by these bits.

Table 32. GContTx [3858 H]

Signal Name	Bit Pos.	Access	Default	Description
GContTx1(1:0)	1:0	R/W	00	These bits indicate what type entity, C-4, C-4-4c, or VC-4, VC-4-4c is passed between the TX SDB FIFOs and the TX APH blocks for ATM/PPP modes. In Telecom Bus mode these bits indicate if a VC-4 or VC-4-4c gets passed to the TX SDB FIFOs or if the TX SDB FIFOs are bypassed (AU-n mode). These bits are also used for the PHCC functions when in ATM mode. 00: This setting is used if the SONET/SDH macro is set to ATM/PPP mode (as indicated by the PPPGP1 register at 3866 H) and it is desired to use the TX APH to process the data, or it is desired to use the TACC, or pass a C-n into or out of the TX APS port. The data passed to the SBD FIFO is as follows: C-4 in 4xSTM-1/STS-3c or 1xSTM-4/STS-12 mode, or C-4-4c in 1xSTM-4c/STS-12c mode. Pointer processing must be disabled (see the OFPTXGP register at 3868 H) when the data comes from the TACC or TX APH block. This setting is also used if it is desired to loop back a C-n using the GLoopRx register at 385D H. When using the GLoopRx register to loop back a C-n, or when receiving data from the TX APS port, the TX pointer processing for that channel must be enabled. 01: This setting is used if the SONET/SDH macro is set to ATM mode and it is desired to use the PHCC function, or it is desired to loop back a VC-n using the GLoopRx register at 385D H, or it is desired to pass a VC-n out of or into the TX APS port for multichip PHCC applications. The data passed to the SBD FIFO is as follows: VC-4 in 4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes, or VC-4-4c in 1xSTM-4c/STS-12c mode. Pointer processing must be enabled (see the OFPTXGP register at 3868 H). 10: SONET/SDH macro in TB (Telecom Bus) mode (AU-n mode)*. In this mode transmit retiming is not performed. Therefore, an AU-n (i.e., VC-n with pointers) must be provided to the PHAST-12E's transmit Telecom Bus. The TX SDB FIFOs are bypassed in this mode. The TXCFRM and either the TXCCLK or $\overline{\text{TXCCLK}}$ signals must be used to source data into the transmit Telecom Bus. See Figure 17 and surrounding text for more information. This mode is also useful for transporting 12xAU-3, or quad 3xAU-3 streams. 11: SONET/SDH macro in TB mode (VC-n mode)*. In this mode transmit retiming is performed. *: n= 4 in 4xSTM-1/STS-3c and STM-4/STS-12 modes, n=4-4c in 1xSTM-4c/STS-12c modes. (Please note that the TACC and TX APS Port can only be used in 4xSTM-1/STS-3c mode for payloads terminated into the APH blocks)
GContTx2(1:0)	3:2	R/W	00	
GContTx3(1:0)	5:4	R/W	00	
GContTx4(1:0)	7:6	R/W	00	

GContRx: Container handling in receive macros. The ACH, PPP, and PH chiplets are affected by these bits.

Table 33. GContRx [3859 H]

Signal Name	Bit Pos.	Access	Default	Description
GContRx1(1:0)	1:0	R/W	00	For each macro in the receive direction, these bits indicate what type entity, C-4, C-4-4c, VC-4, or VC-4-4c, is passed between the RX SDB FIFOs and the APH blocks for ATM/PPP Mode. For Telecom Bus operation, the entire received frame is passed from the RX SFH blocks to the RX Telecom Bus interfaces. These bits are also used for the PHCC functions when in ATM/PPP mode. 00: This setting must be used if the SONET/SDH macro is set to ATM/PPP mode (as indicated by the PPPGP1 register at 3866 H) and it is desired to use the RX APH to process the data, or it is desired to use the RACC, or it is desired to pass a C-n into or out of the RX APS port. This setting is also used if it is desired to loop back a C-n using the GLoopRx register at 385D H. The data passed from the SBD FIFO is as follows: C-4 in 4xSTM-1/STS-3c or 1xSTM-4/STS-12 modes, or C-4-4c in 1xSTM-4c/STS-12c mode. 01: This setting is used if the SONET/SDH macro is set to ATM mode and it is desired to use the PHCC function, or it is desired to loop back a VC-n using the GLoopRx register at 385D H, or it is desired to pass a VC-n out of or into the RX APS port. The data passed to the SBD FIFO is as follows: VC-4 in 4xSTM-1/STS-3c or 1xSTM-4/STS-12 mode, or VC-4-4c in 1xSTM-4c/STS-12c mode. 10: SONET/SDH macro in TB mode. 11: Do not use. (Please note that the RACC and RX APS Port can only be used in 4xSTM-1/STS-3c mode for payloads terminated into the APH blocks)
GContRx2(1:0)	3:2	R/W	00	
GContRx3(1:0)	5:4	R/W	00	
GContRx4(1:0)	7:6	R/W	00	

GCasc:

Table 34. GCasc (lower nibble) [385A H]

Signal Name	Bit Pos.	Access	Default	Description
GCascTx(3:0)	3:0	R/W	1000	Defines cascading of SONET/SDH macros and PHAST-12E chips in transmit direction: One PHAST-12E device used, each SONET/SDH macro operates individually: 0001,0111, 1000: up to 4 x STS-3c/STM-1 (4 x 155 Mbit/s) One PHAST-12E device used, three to four SONET/SDH macros operate in parallel: 0010: Do not use. 0011, 1001: 1 x STS-12 /STM-4 (4 x 155 Mbit/s, VC-4 mode for the Telecom Bus is not valid if it is desired to have 12xSTS-1-SPE.) 1010,1101,1110,1111: 1 x STM-4c/STS-12c (1 x 622 Mbit/s) 1011, 1100, 0000, 0100, 0101, 0110: Do Not Use.

An important note regarding the GCascTx and GContTx register setting for Telecom Bus mode operation:

STS-12 mode and VC-4 mode are not a valid combination of modes when using the Telecom Bus interface if the STS-12-SPE contains 12 x STS-1-SPE (i.e., 12 x VC-3). This is because the PHAST-12E only does pointer processing at the AU-4 and AU-4-4c levels in STS-12 mode. However, if the STS-12 contains 4xSTS-3c-SPE then VC-4 or AU-4 mode can be selected for the Telecom Bus. If the STS-12-SPE contains 12xAU-3, then AU-4 mode can be used. An external device can supply the 12xAU-3 to the PHAST-12E which will supply the TOH. The pointer processing and POH processing are configured separately from the GCascTx(1:0) and GCascRx(1:0) bits.

Table 35. GCasc (upper nibble) [385A H]

Signal Name	Bit Pos.	Access	Default	Description
GCascRx(3:0)	7:4	R/W	1000	Defines cascading of SONET/SDH macros and PHAST-12E chips in receive direction: One PHAST-12E device used, each SONET/SDH macro operates individually: 0001,0111, 1000: up to 4 x STS-3c/STM-1 (4 x 155 Mbit/s) One PHAST-12E device used, three to four SONET/SDH macros operate in parallel: 0010: Do not use. 0011, 1001: 1 x STS-12 /STM-4 (4 x 155 Mbit/s, VC-4 mode for the Telecom Bus is not valid if it is desired to have 12xSTS-1-SPE.) 1010,1101,1110,1111: 1 x STM-4c/STS-12c (1 x 622 Mbit/s) 1011, 1100, 0000, 0100, 0101, 0110: Do Not Use.

GLoopTx1: Transmit loopback stage 1 control. When this loopback is enabled, cells/chunks that are put into the transmit ACB (ATM Cell/PPP Chunk Buffer) are looped back to their corresponding receive ACB without TCSF or Packet Over SONET/SDH (POS) processing. Bit positions 7-4 should be set to all 1s to enable loop-back-only mode. Loopback-only mode disables cells/chunks from being transmitted out to the SONET/SDH line, only the loopback function is performed. Figure 61 on page 166 shows the PHAST-12E loopback capabilities.

For bit positions 3 to 0:

0: APH Loopback 1# disabled (DEFAULT)

1: APH Loopback 1# enabled

For bit positions 7 to 4:

0: Do not use this setting.

1: Loopback 1# only

Table 36. GLoopTx1 [385B H]

Signal Name	Bit Pos.	Access	Default	Description
TxLpB11	0	R/W	0	Loopback 1 control, transmit APH 1
TxLpB12	1	R/W	0	Loopback 1 control, transmit APH 2
TxLpB13	2	R/W	0	Loopback 1 control, transmit APH 3
TxLpB14	3	R/W	0	Loopback 1 control, transmit APH 4
TxLpB11only	4	R/W	0	Loopback 1 only, transmit APH 1
TxLpB12only	5	R/W	0	Loopback 1 only, transmit APH 2
TxLpB13only	6	R/W	0	Loopback 1 only, transmit APH 3
TxLpB14only	7	R/W	0	Loopback 1 only, transmit APH 4

GLoopTx2: Transmit loopback stage 2 control. When this loopback is enabled, cells/chunks that are put into the transmit ACB are looped back towards their corresponding receive ACB after the TCSF or POS processing functions are performed by the ACH or PPP chiplets. Bit positions 7-4 set the mode of the respective loopback to on-the-fly monitoring or loopback-only. On-the-fly monitoring allows cells/frames to be transmitted towards the SONET/SDH Line in addition to being looped back towards the receive APH blocks. Loopback-only mode disables cells/frames from being transmitted out to the SONET/SDH line, only the loopback function is performed. See Figure 61 on page 166. This loopback is not operational in PPP Transparent mode.

For bit positions 3 to 0:

0: APH Loopback 2# disabled (DEFAULT)

1: APH Loopback 2# enabled

For bit positions 7 to 4:

0: On-the-fly monitoring (LpB2#)

1: Loopback 2# only

Table 37. GLoopTx2 [385C H]

Signal Name	Bit Pos.	Access	Default	Description
TxLpB21	0	R/W	0	Loopback 2 control, transmit APH 1
TxLpB22	1	R/W	0	Loopback 2 control, transmit APH 2
TxLpB23	2	R/W	0	Loopback 2 control, transmit APH 3
TxLpB24	3	R/W	0	Loopback 2 control, transmit APH 4
TxLpB21only	4	R/W	0	Loopback 2 only, transmit APH 1
TxLpB22only	5	R/W	0	Loopback 2 only, transmit APH 2
TxLpB23only	6	R/W	0	Loopback 2 only, transmit APH 3
TxLpB24only	7	R/W	0	Loopback 2 only, transmit APH 4

GLoopRx: Receive loopback control. Cell/frame/TDM data that are received by the SFH blocks are looped back towards the transmit line as either a C-n or VC-n depending on the GContTx#(1:0) and GContRx#(1:0) bits. Please note that TX pointer processing needs to be enabled in the looped back channel (see the OFPTXGP register). Therefore, the TX and RX ACH chiplets need to be enabled so that the SDB FIFOs are operational. See Figure 61 on page 166.

For bit positions 3 to 0:

0: RX Loopback Stage 2# disabled (DEFAULT)

1: RX Loopback Stage 2# enabled

For bit positions 7 to 4:

0: On-the-fly monitoring (LpB2#)

1: Loopback 2# only

Table 38. GLoopRx [385D H]

Signal Name	Bit Pos.	Access	Default	Description
RxLpB21	0	R/W	0	Loopback 2 control, receive APH 1
RxLpB22	1	R/W	0	Loopback 2 control, receive APH 2
RxLpB23	2	R/W	0	Loopback 2 control, receive APH 3
RxLpB24	3	R/W	0	Loopback 2 control, receive APH 4
RxLpB21only	4	R/W	0	Loopback 2 only, receive APH 1
RxLpB22only	5	R/W	0	Loopback 2 only, receive APH 2
RxLpB23only	6	R/W	0	Loopback 2 only, receive APH 3
RxLpB24only	7	R/W	0	Loopback 2 only, receive APH 4

GExtRes: External clock recovery circuit reset signal. Delivered to external circuit (deserializer) via device lead. The active level depends on the external circuit used. Default value at power-on reset is low.

Table 39. GExtRes [385E H]

Signal Name	Bit Pos.	Access	Default	Description
RSTCREC	0	R/W	0	External clock recovery circuit reset. The state of this bit is driven out onto the RSTCREC lead.
Reserved	7:1	R/W	0000000	Reserved

CBConf1: Static configuration data, providing control signals for chiplets Telecom Bus and controls internal to the PHAST-12E. This is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation.

Table 40. CBConf1 [386C H]

Signal Name	Bit Pos.	Access	Default	Description
CKINV4	0	R/W	0	Telecom Bus 4 output clocking: 0 on the falling edge of RXTB4CLK 1 on the rising edge of RXTB4CLK
CKINV3	1	R/W	0	Telecom Bus 3 output clocking: 0 on the falling edge of RXTB3CLK 1 on the rising edge of RXTB3CLK
CKINV2	2	R/W	0	Telecom Bus 2 output clocking: 0 on the falling edge of RXTB2CLK 1 on the rising edge of RXTB2CLK
CKINV1	3	R/W	0	Telecom Bus 1 output clocking: 0 on the falling edge of RXTB1CLK 1 on the rising edge of RXTB1CLK
Reserved	4	R/W	0	Reserved
EFRM	5	R/W	0	0 normal position of TXCFRM 1 TXCFRM one TXCCLK cycle earlier
Reserved	7:6	R/W	00	Reserved

CBConf2: Static configuration data, providing control signals for Telecom Bus _Rx drivers (tristate control).
0 = corresponding Rx Telecom Bus is tristated.
1 = corresponding Rx Telecom Bus is enabled.

Table 41. CBConf2 [386D H]

Signal Name	Bit Pos.	Access	Default	Description
CB_RX1_En	0	R/W	0	Telecom Bus_Rx1 driver enable. The EN_COMBUS lead has to be set high to enable this bit.
CB_RX2_En	1	R/W	0	Telecom Bus_Rx2 driver enable. The EN_COMBUS lead has to be set high to enable this bit.
CB_RX3_En	2	R/W	0	Telecom Bus_Rx3 driver enable. The EN_COMBUS lead has to be set high to enable this bit.
CB_RX4_En	3	R/W	0	Telecom Bus_Rx4 driver enable. The EN_COMBUS lead has to be set high to enable this bit.
Reserved	7:4	R/W	0000	Reserved

ACITXGP, PHTXGP1, PHTXGP2: Static configuration data, providing control signals for chiplets ACI_Tx1 and PH_Tx#. These are set once by the GPP before the individual chiplets are enabled and are not changed during normal operation.

Table 42. ACITXGP [3860 H]

Signal Name	Bit Pos.	Access	Default	Description
L1L2Tx(2:0)	2:0	R/W	110	Configuration of the ATM Cell interface, transmit direction: 000, 010: all ATM cell interfaces disabled. This mode is not valid for PPP operation. 001, 011: Do not use. 100: all ATM cell interfaces disabled 101: UTOPIA interface active (1 x UTOPIA Level 2, 1 x 8-bit mode), non-STS-12c/STM-4c. This mode is not valid for PPP operation. 110: UTOPIA interface active (1 x UTOPIA Level 2/2P, 1 x 16-bit mode), non-STS-12c/STM-4c. This mode is valid for PPP operation. 111: UTOPIA interface active (1 x UTOPIA Level 2/2P, 1 x 16-bit mode), STS-12c/STM-4c. This mode is valid for PPP operation.
SIndT1(1:0)	4:3	R/W	10	Type of status indication for UTOPIA interface. 10 is the only valid setting when processing PPP data. 00: Direct status indication, one status line only (TXCLAV[0]). (TXCLAV[1:3] always high impedance) 01: Direct status indication, four status lines (TXCLAV[0:3]) 10: Multiplexed status indication, one status line only (TXCLAV[0]/PAVO). (TXCLAV[1:3] always high impedance) 11: Multiplexed status indication, four status lines (TXCLAV[0:3])
Reserved	7:5	R/W	000	Reserved

Table 43. PHTXGP1 [3861 H]

Signal Name	Bit Pos.	Access	Default	Description
PHT1(2:0)	2:0	R/W	001	Source of data/control for Transmit Port Handler chiplet 1: 001: UTOPIA interface (L2 8-bit, L2/2P 16-bit) 010: Do not use. The corresponding GContTx#(1:0) bits in the GContTx register must be set to 01 and the corresponding APH block must be set to ATM[a] mode, if any of the bit settings below are used. 100: SONET/SDH receive macro 1 (cross connect mode) 101: SONET/SDH receive macro 2 (cross connect mode) 110: SONET/SDH receive macro 3 (cross connect mode) 111: SONET/SDH receive macro 4 (cross connect mode) others: No source selected (port handler disabled) Pointer processing must be enabled in the macros that are put into cross connect mode. See the PtrProc(3:0) bits in the OFPTXGP register.
Reserved	3	R/W	0	Reserved

Table 43. PHTXGP1 [3861 H] (Continued)

Signal Name	Bit Pos.	Access	Default	Description
PHT2(2:0)	6:4	R/W	001	Source of data/control for Transmit Port Handler chiplet 2: Same effect as for PHT1 above.
Reserved	7	R/W	0	Reserved

a. Even though the APH block is set to ATM mode, any data type (ATM, PPP, or TDM) can be passed through the PHCC since only VCs are cross connected.

Table 44. PHTXGP2 [3862 H]

Signal Name	Bit Pos.	Access	Default	Description
PHT3(2:0)	2:0	R/W	001	Source of data/control for Transmit Port Handler chiplet 3: Same effect as for PHT1 above.
Reserved	3	R/W	0	Reserved
PHT4(2:0)	6:4	R/W	001	Source of data/control for Transmit Port Handler chiplet 4: Same effect as for PHT1 above.
Reserved	7	R/W	0	Reserved

ACIRXGP, PHRXGP: Static configuration data, providing control signals for chiplet ACI_Rx1. These are set once by the GPP before the individual chiplets are enabled and not changed during normal operation.

Table 45. ACIRXGP [3863 H]

Signal Name	Bit Pos.	Access	Default	Description
L1L2Rx(2:0)	2:0	R/W	110	Configuration of the ATM Cell interface, receive direction: 000, 010: all ATM cell interfaces disabled. This mode is not valid for PPP operation. 001, 011: Do not use. 100: all ATM cell interfaces disabled 101: UTOPIA interface active (1 x UTOPIA Level 2, 1 x 8-bit mode), non-STS-12c/STM-4c. This mode is not valid for PPP operation. 110: UTOPIA interface active (1 x UTOPIA Level 2/2P, 1 x 16-bit mode), non-STS-12c/STM-4c. This mode is valid for PPP operation. 111: UTOPIA interface active (1 x UTOPIA Level 2/2P, 1 x 16-bit mode), STS-12c/STM-4c. This mode is valid for PPP operation.
SIndR1(1:0)	4:3	R/W	10	Type of status indication for UTOPIA interface. 10 is the only valid setting when processing PPP data. 00: Direct status indication, one status line only (RXCLAV[0]). (RXCLAV[1:3] always high impedance) 01: Direct status indication, four status lines (RXCLAV[0:3]). 10: Multiplexed status indication, one status line only (RXCLAV[0]/PAVO). (RXCLAV[1:3] always high impedance) 11: Multiplexed status indication, four status lines (RXCLAV[0:3]).
Reserved	7:5	R/W	000	Reserved

Table 46. PHRXGP [3864 H]

Signal Name	Bit Pos.	Access	Default	Description
PHR1(1:0)	1:0	R/W	01	Sink of data selected for Receive Port Handler chiplet 1: 01: UTOPIA interface 10: Transmit macros (internal cross connect mode). The corresponding GContRx#(1:0) bits in the GContRx register and the corresponding GContTx#(1:0) bits in the GContTx register must be set to 01, and the appropriate bits in the PPPGP1 register must be set to ATM mode. others: No sink selected (port handler disabled)
PHR2(1:0)	3:2	R/W	01	Sink of data selected for Receive Port Handler chiplet 2: Same effect as for PHR1 above.
PHR3(1:0)	5:4	R/W	01	Sink of data selected for Receive Port Handler chiplet 3: Same effect as for PHR1 above.
PHR4(1:0)	7:6	R/W	01	Sink of data selected for Receive Port Handler chiplet 4: Same effect as for PHR1 above.

PPPGP1, PPPGP2: Static configuration data, providing control signals for chiplets PPP, ACI_Rx1, ACI_Tx1 and the Port Handlers. These are set once by the GPP before the individual chiplets are enabled and not changed during normal operation.

PPPGP1: These signals determine whether a port handler is in ATM or in PPP mode.

Table 47. PPPGP1 [3866 H]

Signal Name	Bit Pos.	Access	Default	Description
TxPPP(3:0)	3:0	R/W	0000	B=0: ATM Mode B=1: PPP Bxxx: Mode of transmit Port Handler 1 xBxx: Mode of transmit Port Handler 2 xxBx: Mode of transmit Port Handler 3 xxxB: Mode of transmit Port Handler 4 (Mixed ATM and PPP mode is allowed for PHYs that are terminated into the UTOPIA interface i.e., One or more PHYs can be configured for ATM and the other PHYs be configured for PPP (or Telecom Bus) and all PHYs configured for ATM or PPP can be accessed via the UTOPIA interface. In other words, the PHAST-12E can simultaneously support ATM, TDM, and PPP traffic. That is, some streams can be terminated to the Telecom Bus Interface while some can be terminated to the UTOPIA interface, and those terminated to the UTOPIA interface can be either ATM or PPP where some PHYs can process ATM data and some can process PPP data.)

Table 47. PPPGP1 [3866 H] (Continued)

Signal Name	Bit Pos.	Access	Default	Description
RxPPP(3:0)	7:4	R/W	0000	B=0: ATM Mode B=1: PPP Bxxx: Mode of receive Port Handler 1 xBxx: Mode of receive Port Handler 2 xxBx: Mode of receive Port Handler 3 xxxB: Mode of receive Port Handler 4 (Mixed ATM and PPP mode is allowed for PHYs that are terminated into the UTOPIA interface i.e., One or more PHYs can be configured for ATM and the other PHYs be configured for PPP (or Telecom Bus) and all PHYs configured for ATM or PPP can be accessed via the UTOPIA interface. In other words, the PHAST-12E can simultaneously support ATM, TDM, and PPP traffic. That is, some streams can be terminated to the Telecom Bus Interface while some can be terminated to the UTOPIA interface, and those terminated to the UTOPIA interface can be either ATM or PPP where some PHYs can process ATM data and some can process PPP data.)

Table 48. PPPGP2 [3867 H]

Signal Name	Bit Pos.	Access	Default	Description
CHNKSZ(2:0)	2:0	R/W	110	Chunk Size: 8-64 bytes in increments of 8. Only the chunk sizes below are currently supported. 000 = 64-byte chunk size 001 = do not use 010 = 16-byte chunk size (this setting is not available in STM-4c or STS-12c modes) 011 = do not use 100 = 32-byte chunk size 101 = do not use 110 = 48-byte chunk size 111 = do not use
Reserved	7:3	R/W	00000	Reserved

OFPTXGP: Static configuration data, providing control signals for chiplets OFP_Tx1/2/3/4. This is set once by the GPP before the individual chiplets are enabled and not changed during normal operation.

Table 49. OFPTXGP [3868 H]

Signal Name	Bit Pos.	Access	Default	Description
SDHJ0Tx(3:0)	3:0	R/W	0000	B = 0: C1 byte replaced by 16-byte section trace J0 byte; i.e., the on-chip values in offsets 60 H - 6F H of the OFP_Tx1/2/3/4 GRAs are transmitted in place of the contents of offset 06 H. The contents of 07 H and 08 H are still transmitted as the Z0 bytes. B = 1: Old numbering scheme is used. That is, the on-chip values in offsets 06 H - 08 H of the OFP_Tx1/2/3/4 GRAs are transmitted. Bxxx: OFP_Tx1 numbering scheme info xBxx: OFP_Tx2 numbering scheme info xxBx: OFP_Tx3 numbering scheme info xxxB: OFP_Tx4 numbering scheme info
PtrProc(3:0)	7:4	R/W	0000	B = 0: AU pointer processing disabled in ATM/PPP mode. In this case a pointer with a constant offset of 0 is transmitted. These bits must be set to 0 for the channels that are processing PPP data through the TX PPP chiplet. This carries the implication that when using the APS port and passing data from the TX PPP chiplet to another PHAST-12E, the PHAST-12Es must have the same REFCLKE clock. B = 1: AU pointer processing enabled in ATM/PPP mode. These bits must be set to 1 whenever the corresponding GContTx#(1:0) bits are set to 01 or an RX stage 2 loopback is enabled. Bxxx: OFP_Tx1 pointer processing xBxx: OFP_Tx2 pointer processing xxBx: OFP_Tx3 pointer processing xxxB: OFP_Tx4 pointer processing These bits do not apply to Telecom Bus mode.

OFPRXGP1, OFPRXGP2: Static configuration data, providing control signals for chiplets OFP_Rx1/2/3/4. These are set once by the GPP before the individual chiplets are enabled and not changed during normal operation.

Table 50. OFPRXGP1 [3869 H]

Signal Name	Bit Pos.	Access	Default	Description
SDHJ0Rx(3:0)	3:0	R/W	0000	B = 0: The new numbering scheme is used. A 16-byte J0 message is to be received. B = 1: Old numbering scheme is used. A fixed single J0 byte is received. Bxxx: OFP_Rx1 numbering scheme info xBxx: OFP_Rx2 numbering scheme info xxBx: OFP_Rx3 numbering scheme info xxxB: OFP_Rx4 numbering scheme info
Reserved	7:4	R/W	0000	Reserved

Table 51. OFPRXGP2 [386A H]

Signal Name	Bit Pos.	Access	Default	Description
A2Frm(1:0)	1:0	R/W	00	OFP_Rx1 FP assertion control: 00: FP asserted during 3rd A2 byte. 01: Do not use. 10: Do not use. 11: FP asserted during 1st Payload Byte for STM-4/4c and STS-12/12c modes, otherwise FP is asserted coincident with the 3rd A2 byte.
Reserved	3:2	R/W	00	Reserved
Reserved	5:4	R/W	00	Reserved
Reserved	7:6	R/W	00	Reserved

AIPConf: Ring Port static configuration data. This is set once by the GPP and not changed during normal operation.

Table 52: AIPConf [386B H]

Signal Name	Bit Pos.	Access	Default	Description
LineRING	0	R/W	0	0: Disabled - Line/MS information on the Ring Port input is ignored. TX Line/MS RDI and REI are generated based on local alarms. 1: Enabled - Line/MS information on the Ring Port input is accepted. TX Line/MS RDI and REI are generated based on data from TX Ring Port. See Figure 56 on page 150 for details.

Table 52: AIPConf [386B H] (Continued)

Signal Name	Bit Pos.	Access	Default	Description
PathRING	1	R/W	0	0: Disabled - Path information on the Ring Port input is ignored. TX Path RDI and REI are generated based on local alarms. 1: Enabled - Path information on the Ring Port input is accepted. TX Path RDI and REI are generated based on data from TX Ring Port. See Figure 56 on page 150 for details.
Reserved	7:2	R/W	000000	Reserved

PIMTConf1, PIMRConf1, PIMRConf2: Static configuration data, providing control signals for chiplets PIM_Tx/PIM_Rx. These are set once by the GPP before the individual chiplets are enabled and not changed during normal operation.

Table 53. PIMTConf1 [3870 H]

Signal Name	Bit Pos.	Access	Default	Description
TxLModeP(1:0)	1:0	R/W	01	Mode of operation of PIM: 00: Mode 1 - Do not use. 01: Mode 2 - 4 x 155.52 Mbit/s. 10: Mode 3 -Do not use. 11: Mode 4 - 1 x 622.08 Mbit/s.
TxSePar1	2	R/W	0	Transmit channel #1 mode: 0: Serial operation. Internal byte clock comes from the SIM# chiplet. This bit must always be set to 0.
TxRefSelP	3	R/W	0	Reserved
Tx_RefSlS	4	R/W	0	Select external TX reference clock source: 0: REFCLKT is selected 1: REFCLKE is selected
Reserved	7:5	R/W	000	Reserved

Table 54. PIMRConf1 [3872 H]

Signal Name	Bit Pos.	Access	Default	Description
RxLModeP(1:0)	1:0	R/W	01	Mode of operation of PIM: 00: Mode1 - Do not use. 01: Mode 2 - 4 x 155.52 Mbit/s. 10: Mode 3 - Do not use. 11: Mode 4 - 1 x 622.08 Mbit/s. When RxLModeP(1) is set to a 1, the LOSSSIG1 input is forwarded to all macros.
RxSePar1	2	R/W	0	Receive channel 1 mode: 0: Serial operation. This bit must always be set to 0.
Invert_LOS	3	R/W	0	LOSSSIG# polarity control. When set to 0, the LOS interrupt request bits in OR#IRQ2 will become set when the corresponding LOSSSIG# lead is set high. When set to 1, the LOS interrupt request bits in OR#IRQ2 will become set when the corresponding LOSSSIG# lead is set low.
Reserved	7:4	R/W	0000	Reserved

Table 55. PIMRConf2 [3873 H]

Signal Name	Bit Pos.	Access	Default	Description
Algo1(1:0)	1:0	R/W	00	Selects frame pattern recognition algorithm for SFH block 1: 00: Do not use. 01: The last A1 byte and the first four bits of the first A2 byte checked (12 bits total), maximum four bad frames received will cause the corresponding OOF interrupt request bit to become set. 10: Do not use. 11: The last A1 byte and the first four bits of the first A2 byte checked (12 bits total), maximum five bad frames received will cause the corresponding OOF interrupt request bit to become set. For STM-4/4c and STS-12/12c modes of operation, only this register needs to be set.
Algo2(1:0)	3:2	R/W	00	Selects frame pattern recognition algorithm for SFH block 2: 00: Do not use. 01: 12 bits checked only, maximum 4 bad frames. 10: Do not use. 11: 12 bits checked only, maximum 5 bad frames.
Algo3(1:0)	5:4	R/W	00	Selects frame pattern recognition algorithm for SFH block 3: 00: Do not use. 01: 12 bits checked only, maximum 4 bad frames. 10: Do not use. 11: 12 bits checked only, maximum 5 bad frames.

Table 55. PIMRConf2 [3873 H] (Continued)

Signal Name	Bit Pos.	Access	Default	Description
Algo4(1:0)	7:6	R/W	00	Selects frame pattern recognition algorithm for SFH block 4: 00: Do not use. 01: 12 bits checked only, maximum 4 bad frames. 10: Do not use. 11: 12 bits checked only, maximum 5 bad frames.

SIMStat: Status register, providing the GPP with external PLL lock status. “clear-register” option set in ConfGP1(1).

Table 56. SIMStat [387F H]

Signal Name	Bit Pos.	Access	Default	Description
LOCKDET	0	R	N.A.	0: External PLL is in lock. 1: External PLL is out of lock. This bit monitors the state of the LOCKDET lead.
Reserved	7	R	0000000	Reserved.

GP ACCESS PROTECTION ADDRESS MAPPING

Access Protection Base Address:

3FBF H.

ProtReg: The bits of this configuration register control the Write Access Protection as follows:

ProtReg is 11001100: free read and write access to all PHAST-12E registers (DEFAULT)

ProtReg is not 11001100: free read access to all PHAST-12E registers is disabled; write access to register ProtReg only. If a write to a protected register is attempted an access violation error is generated (AccViol = HShake5(2)).

Table 57. Access Protection Register [3FBF H]

Register Name	Address Offset (Hex)	Access	Initial Value (binary)	Description (all registers are of 8-bit width)
ProtReg	0	R/W	11001100	Write protection control

SIM CHIPLET ADDRESS MAPPING

Chiplet Base Address:

3900 H.

REGISTER TYPES:

C configuration register
S status/event latch register

The initial values shown in the table below will be loaded into the registers after the $\overline{\text{FRESET}}$ lead is deasserted.

Table 58. SIM Chiplet Address Mapping

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
SIMTConf1	0	C 3	111	Transmit Configuration 1 Register	206
SIMTConf2	1	C 3	100	Transmit Configuration 2 Register	206
SIMTConf3	2	C 4	0010	Transmit Configuration 3 Register	207
SIMTConf4	3	C 5	00110	Transmit Configuration 4 Register	207
SIMTConf5	4	C 4	1101	Transmit Configuration 5 Register	208
SIMTConf6	5	C 3	011	Transmit Configuration 6 Register	208
SIMRefClkSel	7	C 3	000	Reference Clock Select	209
SIMRefFreq	8	C 2	11	Reference Frequency	209
SIMR1Conf1	9	C 7	0010011	Receive Channel 1 Configuration 1 Register	210
SIMR1Conf2	A	C 8	01000001	Receive Channel 1 Configuration 2 Register	211
SIMR1Conf3	B	C 5	11011	Receive Channel 1 Configuration 3 Register	212
SIMR1Conf4	C	C 3	100	Receive Channel 1 Configuration 4 Register	212
SIMR1Conf5	D	C 5	00010010	Receive Channel 1 Configuration 5 Register	213
SIMR1Conf6	E	C 5	01000	Receive Channel 1 Configuration 6 Register	213
SIMR1Conf7	F	C 4	1101	Receive Channel 1 Configuration 7 Register	214
SIMR1Conf8	10	C 4	1001	Receive Channel 1 Configuration 8 Register	214
SIMR1Conf9	11	C 4	0010	Receive Channel 1 Configuration 9 Register	215
SIMTPLLMon	14	S 8		Transmit PLL Monitor	215
SIMR1EnMon	15	S 8		Receive channel 1 Enable Monitor	216
SIMR1PLLMon	16	S 8		Receive Channel 1 PLL Monitor	216
SIMR1LtrR	18	C 1	N/A	Receive Channel 1 LTR Reset	217
SIMTrim	21	S 8		VCO Trim	217
SIMR2Conf1	49	C 7	0010011	Receive Channel 2 Configuration 1 Register	210
SIMR2Conf2	4A	C 8	01000001	Receive Channel 2 Configuration 2 Register	211
SIMR2Conf3	4B	C 5	11011	Receive Channel 2 Configuration 3 Register	212
SIMR2Conf4	4C	C 3	100	Receive Channel 2 Configuration 4 Register	212
SIMR2Conf5	4D	C 5	00010010	Receive Channel 2 Configuration 5 Register	213
SIMR2Conf6	4E	C 5	01000	Receive Channel 2 Configuration 6 Register	213
SIMR2Conf7	4F	C 4	1101	Receive Channel 2 Configuration 7 Register	214
SIMR2Conf8	50	C 4	1001	Receive Channel 2 Configuration 8 Register	214
SIMR2Conf9	51	C 4	0010	Receive Channel 2 Configuration 9 Register	215

Table 58. SIM Chiplet Address Mapping (Continued)

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
SIMR2EnMon	55	S 8		Receive channel 2 Enable Monitor	216
SIMR2PLLMon	56	S 8		Receive Channel 2 PLL Monitor	216
SIMR2LtrR	58	C 1	N/A	Receive Channel 2 LTR Reset	217
SIMR3Conf1	89	C 7	0010011	Receive Channel 3 Configuration 1 Register	210
SIMR3Conf2	8A	C 8	01000001	Receive Channel 3 Configuration 2 Register	211
SIMR3Conf3	8B	C 5	11011	Receive Channel 3 Configuration 3 Register	212
SIMR3Conf4	8C	C 3	100	Receive Channel 3 Configuration 4 Register	212
SIMR3Conf5	8D	C 5	00010010	Receive Channel 3 Configuration 5 Register	213
SIMR3Conf6	8E	C 5	01000	Receive Channel 3 Configuration 6 Register	213
SIMR3Conf7	8F	C 4	1101	Receive Channel 3 Configuration 7 Register	214
SIMR3Conf8	90	C 4	1001	Receive Channel 3 Configuration 8 Register	214
SIMR3Conf9	91	C 4	0010	Receive Channel 3 Configuration 9 Register	215
SIMR3EnMon	95	S 8	N/A	Receive channel 3 Enable Monitor	216
SIMR3PLLMon	96	S 8	N/A	Receive Channel 3 PLL Monitor	216
SIMR3LtrR	98	C 1	N/A	Receive Channel 3 LTR Reset	217
SIMR4Conf1	C9	C 7	0010011	Receive Channel 4 Configuration 1 Register	210
SIMR4Conf2	CA	C 8	01000001	Receive Channel 4 Configuration 2 Register	211
SIMR4Conf3	CB	C 5	11011	Receive Channel 4 Configuration 3 Register	212
SIMR4Conf4	CC	C 3	100	Receive Channel 4 Configuration 4 Register	212
SIMR4Conf5	CD	C 5	00010010	Receive Channel 4 Configuration 5 Register	213
SIMR4Conf6	CE	C 5	01000	Receive Channel 4 Configuration 6 Register	213
SIMR4Conf7	CF	C 4	1101	Receive Channel 4 Configuration 7 Register	214
SIMR4Conf8	D0	C 4	1001	Receive Channel 4 Configuration 8 Register	214
SIMR4Conf9	D1	C 4	0010	Receive Channel 4 Configuration 9 Register	215
SIMR4EnMon	D5	S 8		Receive channel 4 Enable Monitor	216
SIMR4PLLMon	D6	S 8		Receive Channel 4 PLL Monitor	216
SIMR4LtrR	D8	C 1	N/A	Receive Channel 4 LTR Reset	217

SIM Configuration Registers:

SIMTConf1: register to control various modes of operation of the Transmit SIM chiplet

Table 59. SIMTConf1: [3900 H]

Signal Name	Bit Pos.	Access	Default	Description
Tx_Enable	0	R/W	1	0: Disables and resets the Transmit SIM. 1: Enable the Transmit SIM. Toggling this bit low and then high while the AT_Enable bit (below) is set to 1 starts the AutoTrim function.
AT_Enable	1	R/W	1	0: Use the Transmit/Receive # VCO trim user default setting for the VCOs 1: Enable the TX/RX VCO AutoTrim feature. If AutoTrim is enabled, the AutoTrim circuit block determines the best VCO trim on the next reset of the Transmit macro (See the Tx_Enable bit above). The trim is then applied to the Transmit and all CDR VCOs. If the AutoTrim function is performed at a certain temperature within the PHAST-12E's operating range of T_A= -45^{O}C to +85^{O}C (provided that a suitable heatsink is attached to the PHAST-12E if needed), the AutoTrim function does not have to be performed again if the temperature varies over the PHAST-12E's operating temperature range unless the device loses power or SIM parameters are changed.
Tx_VCOptc	2	R/W	1	0: No compensation 1: Force positive thermal dependency to bias the VCO to compensate for the VCO center frequency saturation at high temperature. It is recommended that this bit be set to a 1 before the AutoTrim function is performed, and should always be used.
Reserved	7:3			Not used

SIMTConf2: register to control various modes of operation of Transmit SIM chiplet

Table 60. SIMTConf2: [3901 H]

Signal Name	Bit Pos.	Access	Default	Description
Tx_VCOtrim(2:0)	2:0	R/W	111	VCO trim value to use for the Transmit PLL if the AutoTrim feature is disabled
Reserved	7:3			Not used

SIMTConf3: register to control various modes of operation of Transmit SIM chiplet

Table 61. SIMTConf3: [3902 H]

Signal Name	Bit Pos.	Access	Default	Description
Tx_IcpSel(1:0)	1:0	R/W	10	00: Select no Transmit filter capacitor 10: Select on board Transmit filter capacitors X1: Reserved
PCFFD1	2	R/W	0	0: No additional 4pF capacitor for the Transmit VCO. 1: Additional 4pF capacitor for the Transmit VCO. This bit is for internal TranSwitch Corporation use and should not be touched unless directed by TranSwitch Corporation.
PCFFD9	3	R/W	0	0: No additional 8pF capacitor for the Transmit VCO. 1: Additional 8pF capacitor for the Transmit VCO. This bit is for internal TranSwitch Corporation use and should not be touched unless directed by TranSwitch Corporation.
Reserved	7:4			Not used

SIMTConf4: register to control various modes of operation of Transmit SIM chiplet

Table 62. SIMTConf4: [3903 H]

Signal Name	Bit Pos.	Access	Default	Description
Tx_IcpPpgm(4:0)	4:0	R/W	00110	Set the magnitude of the Proportional Charge Pump current computed by the internal logic based on the chosen Reference Frequency. A change of the Ref_Freq(1:0) bits in the SIMRefFreq register, has a direct impact on Tx_IcpPpgm default value: 0X => Tx _IcpPpgm:11111 10 => Tx _IcpPpgm:01111 11 => Tx _IcpPpgm:00110 Although not recommended, these values can be configured by the user as soon as Ref_Freq(1:0), Tx#_BLR, and Rx#_BLR bits are configured first.
Reserved	7:5			Not used

SIMTConf5: register to control various modes of operation of Transmit SIM chiplet

Table 63. SIMTConf5: [3904 H]

Signal Name	Bit Pos.	Access	Default	Description
Tx_IcpIpgm(3:0)	3:0	R/W	1101	Set the magnitude of the Integral Charge Pump current computed by the internal logic based on the chosen Reference Frequency. A change of the Ref_Freq(1:0) bits in the SIMRefFreq register, has a direct impact on the Tx_IcpIpgm default value: 0X => Tx _IcpIpgm:1111 10 => Tx _IcpIpgm:1111 11 => Tx _IcpIpgm:1101 Although not recommended, these values can be configured by the user as soon as Ref_Freq(1:0), Tx#_BLR, and Rx#_BLR bits are configured first.
Reserved	7:4			Not used

SIMTConf6: register to control various modes of operation of Transmit SIM chiplet

Table 64. SIMTConf6: [3905 H]

Signal Name	Bit Pos.	Access	Default	Description
Tx_Div_Freq(2:0)	2:0	R/W	011	Select the frequency of the clock on the TXDCLKT lead: 000: 19.44 MHz 001: 38.88 MHz 010: 51.84 MHz 011: 77.76 MHz 1XX: Do not use
Reserved	7:3			Not used

SIMRefClkSel: register to control various modes of operation of Transmit SIM chiplet

Table 65. SIMRefClkSel: [3907 H]

Signal Name	Bit Pos.	Access	Default	Description
Ref_Freq_Sel(2:0)	2:0	R/W	000	Select the Reference clock for the Transmit clock synthesizer: 0XX: External Reference clock (RECLKT/REFCLKE) 100: Recovered clock 1 101: Recovered clock 2 (not valid for 622 Mbit/s operation) 110: Recovered clock 3 (not valid for 622 Mbit/s operation) 111: Recovered clock 4 (not valid for 622 Mbit/s operation)
Reserved	7:3			Not used

SIMRefFreq: register to control various modes of operation of the SIM chiplet.

Table 66. SIMRefFreq: [3908 H]

Signal Name	Bit Pos.	Access	Default	Description
Ref_Freq(1:0)	1:0	R/W	11	Indicate to the SerDes the frequency of the Reference clock. This register is used by both the Transmit TCS and the four CDR PLLs to center the VCO frequency and optimize the Charge Pump Currents to get a correct PLL behavior: 00: 19.44 MHz 01: 38.88 MHz 10: 51.84 MHz 11: 77.76 MHz When these bits are changed the SIMTConf4, SIMTConf5, SIMR#Conf5, SIMR#Conf6, SIMR#Conf7, and SIMR#Conf8 registers are automatically updated to the appropriate values. This register must always be programmed to the frequency of the TX Reference clock (REFCLKT/E), even if a recovered clock is being used as the input to the TCS circuit.
Reserved	7:2			Not used

SIMR#Conf1: register to control various modes of operation of the Receive SIM chiplet.

Table 67. SIMR#Conf1: [3909 H, 3949 H, 3989 H, 39C9 H]

Signal Name	Bit Pos.	Access	Default	Description
Rx#_Enable	0	R/W	1	0: Disable the CDR Channel # block. The RX clock recovery PLL# is disabled. Rx2_Enable, Rx3_Enable, and Rx4_Enable must be set to 0 when RX LIU1 is used in 1xSTM-4/STS-12, or 1xSTM-4c/STS-12c modes. 1: Enable the CDR Channel # block. The RX clock recovery PLL# is enabled.
Tx#_Drv_Enble	1	R/W	1	0: TXSDAT#(0:1) leads in tristate mode. If the corresponding TX LIU is not being used, then this bit should be set to a 0. 1: Drivers for TXSDAT#(0:1) leads are enabled.
Rx#_ParaWrap	2	R/W	0	RX Parallel Wrap Loopback control. 0: Normal mode 1: Enable the parallel wrap (DES to SER diagnostic loopback). The parallel data presented to RX SFH block# by RX LIU# is looped back towards TX LIU# while still providing the parallel data to RX SFH block#. Data and clock are both looped back.
Tx#_SerialWrap	3	R/W	0	TX Serial Wrap Loopback control. 0: Normal mode 1: Enable the serial wrap (SER to DES diagnostic loopback). The TX serial line output is looped back to the RX serial line input. The TX serial line data is output by the PHAST-12E. The LOSSSIG# lead needs to be in the deasserted state when this diagnostic loopback is enabled to avoid forcing and holding the RX clock recovery PLL# into frequency acquisition mode. If this loopback is enabled during normal operation (i.e., not during device configuration), it is recommended to issue a local reset to the Rx ACH chiplets (registers 1130H, 1230H, 1330H, 1430H).
Tx#_Sync_Enable	4	R/W	1	For SIM chiplet 1 (register 3909 H), this bit must always be set to 0. This bit should be set to a 1 for macros 2, 3, 4.

Table 67. SIMR#Conf1: [3909 H, 3949 H, 3989 H, 39C9 H] (Continued)

Signal Name	Bit Pos.	Access	Default	Description
Rx#_VCOptc	5	R/W	1	0: No compensation 1: Force positive thermal dependency to bias the VCO to compensate for the VCO center frequency saturation at high temperature. This bit must be always set to 1.
Rx#_Ser_Wrap_Clock_Enable	6	R/W	0	0: Normal mode. This bit must always be set to a 0 for 1xSTM-4/STS-12 and 1xSTM-4c/STS-12c modes. 1: Enable the recovered clock of the channel # to be used as the Transmit clock without passing through the TCS. This means the recovered clock is used directly as the transmit clock for channel #.
Reserved	7			Not used

SIMR#Conf2: register to control various modes of operation of the Receive SIM chiplet.

Table 68. SIMR#Conf2: [390A H, 394A H, 398A H, 39CA H]

Signal Name	Bit Pos.	Access	Default	Description
Rx#_LTR_lo(3:0)	3:0	R/W	0001	Set the lock detector hysteresis to pass from Phase Acquisition to Frequency Acquisition modes. The RX Clock Recovery PLL switches to Frequency Acquisition mode when the lock counter is less than this value. A value of 0000 prevents the RX Clock Recovery PLL from going into Frequency Acquisition mode once it is locked.
Rx#_LTR_hi(3:0)	7:4	R/W	0100	Set the lock detector hysteresis to pass from Frequency Acquisition to Phase Acquisition modes. The RX Clock Recovery PLL switches to Phase Acquisition (i.e., Data Recovery) mode as soon as lock counter is greater than this value. A value of 1111 disables the RX Clock Recovery PLL from switching to Data Recovery Mode.

SIMR#Conf3: register to control various modes of operation of the Receive SIM chiplet

Table 69. SIMR#Conf3: [390B H, 394B H, 398B H, 39CB H]

Signal Name	Bit Pos.	Access	Default	Description
Rx#_Div_Freq(2:0)	2:0	R/W	011	Select the RXDCLKT# clock frequency: 000: 19.44 MHz 001: 38.88 MHz 010: 51.84 MHz 011: 77.76 MHz 1XX: Do not use.
Rx#_BLR	3	R/W	1	0: 155 Mbit/s Receive Bit Line Rate 1: 622 Mbit/s Receive Bit Line Rate. A setting of 1 is only valid for Rx1_BLR. When this bit is changed the SIMTConf4, SIMTConf5, SIMR#Conf5, SIMR#Conf6, SIMR#Conf7, and SIMR#Conf8 registers are automatically updated.
Tx#_BLR	4	R/W	1	0: 155 Mbit/s Transmit Bit Line Rate 1: 622 Mbit/s Transmit Bit Line Rate. A setting of 1 is only valid for Tx1_BLR. When this bit is changed the SIMTConf4, SIMTConf5, SIMR#Conf5, SIMR#Conf6, SIMR#Conf7, and SIMR#Conf8 registers are automatically updated.
Reserved	7:5			Not used

SIMR#Conf4: register to control various modes of operation of Receive SIM chiplet

Table 70. SIMR#Conf4: [390C H, 394C H, 398C H, 39CC H]

Signal Name	Bit Pos.	Access	Default	Description
Rx#_VCOtrim(2:0)	2:0	R/W	111	VCO trim value to use for the CDR Channel # PLL if the AutoTrim feature is disabled
Reserved	7:3			Not used

SIMR#Conf5: register to control various modes of operation of Receive SIM chiplet

Table 71. SIMR#Conf5: [390D H, 394D H, 398D H, 39CD H]

Signal Name	Bit Pos.	Access	Default	Description
Rx#_IcpPpgmR(4:0)	4:0	R/W	00010010	Set the magnitude of the Proportional Charge Pump current in Recovery mode computed by the internal logic based on the Receive Bit Line Rate (Rx#_BLR). 0 => Rx# _IcpPpgmR:00110 1 => Rx# _IcpPpgmR:00110 Although not recommended, these values can be configured by the user as soon as Ref_Freq(1:0), Tx#_BLR, and Rx#_BLR bits are configured first.
Reserved	7:5			Not used

SIMR#Conf6: register to control various modes of operation of Receive SIM chiplet

Table 72. SIMR#Conf6: [390E H, 394E H, 398E H, 39CE H]

Signal Name	Bit Pos.	Access	Default	Description
Rx#_IcpPpgmA(4:0)	4:0	R/W	01000	Set the magnitude of the Proportional Charge Pump current in Acquisition mode computed by the internal logic based on the chosen Reference Frequency. A change of the Ref_Freq(1:0) field has a direct impact on the Rx#_IcpPpgmA default value: 00 => Rx# _IcpPpgmA:11010 01 => Rx# _IcpPpgmA:00100 10 => Rx# _IcpPpgmA:10010 11 => Rx# _IcpPpgmA:01000 Although not recommended, these values can be configured by the user as soon as Ref_Freq(1:0), Tx#_BLR, and Rx#_BLR bits are configured first.
Reserved	7:5			Not used

SIMR#Conf7: register to control various modes of operation of Receive SIM chiplet.

Table 73. SIMR#Conf7: [390F H, 394F H, 398F H, 39CF H]

Signal Name	Bit Pos.	Access	Default	Description
Rx#_IcpIpgmR(3:0)	3:0	R/W	1101	Set the magnitude of the Integral Charge Pump current in Recovery mode computed by the internal logic based on the Receive Bit Line Rate (Rx#_BLR). A change of the Rx#_BLR field has a direct impact on the Rx#_IcpIpgmR default value: 0 => Rx# _IcpIpgmR:0001 1 => Rx# _IcpIpgmR:1101 Although not recommended, these values can be configured by the user as soon as Ref_Freq(1:0), Tx#_BLR, and Rx#_BLR bits are configured first.
Reserved	7:4			Not used

SIMR#Conf8: register to control various modes of operation of Receive SIM chiplet

Table 74. SIMR#Conf8: [3910 H, 3950 H, 3990 H, 39D0 H]

Signal Name	Bit Pos.	Access	Default	Description
Rx#_IcpIpgmA(3:0)	3:0	R/W	1001	Set the magnitude of the Integral Charge Pump current in Acquisition mode computed by the internal logic based on the chosen Reference Frequency A change of the Ref_Freq(1:0) field has a direct impact on Rx_IcpIpgmA default value: 00 => Rx# _IcpIpgmA:1111 01 => Rx# _IcpIpgmA:1101 10 => Rx# _IcpIpgmA:0101 11 => Rx# _IcpIpgmA:1001 Although not recommended, these values can be configured by the user as soon as Ref_Freq(1:0), Tx#_BLR, and Rx#_BLR bits are configured first.
Reserved	7:4			Not used

SIMR#Conf9: register to control various modes of operation of Receive SIM chiplet

Table 75. SIMR#Conf9: [3911 H, 3951 H, 3991 H, 39D1 H]

Signal Name	Bit Pos.	Access	Default	Description
Rx#_IcpSel(1:0)	1:0	R/W	10	00: Select no Receive Channel # filter capacitor 10: Select on board Receive Channel # filter capacitors X1: Reserved
PCFFD1	2	R/W	0	0: No additional 4pF capacitor for the Receive Channel # VCO. 1: Additional 4pF capacitor for the Receive Channel # VCO. This bit is for internal TranSwitch Corporation use and should not be touched unless directed by TranSwitch Corporation.
PCFFD9	3	R/W	0	0: No additional 8pF capacitor for the Receive Channel # VCO. 1: Additional 8pF capacitor for the Receive Channel # VCO. This bit is for internal TranSwitch Corporation use and should not be touched unless directed by TranSwitch Corporation.
Reserved	7:4			Not used

SIMTPLLMon: Status register of the Transmit SIM chiplet. These are unlatched status bits that follow the driving signal immediately.

Table 76. SIMTPLLMon: [3914 H]

Signal Name	Bit Pos.	Access	Default	Description
Tx_VCO_Clk_det	0	R	N/A	0: The current frequency of the Transmit VCO is lower than around 10 MHz 1: The current frequency of the Transmit VCO is higher than around 10 MHz
Tx_ZClkEn	1	R	N/A	0: The Transmit VCO clock is driven only inside the Transmit VCO block 1: The Transmit VCO clock is provided to all other Serializer blocks.
Tx_ZEnable	2	R	N/A	This status is a delayed copy of the Tx_Enable bit (bit 0 in register SIMTConf1)
Tx_Lock	3	R	N/A	0: Transmit PLL has been not locked during one period of 4096 Reference clock cycles. If the internally scaled down version of the synthesized TX clock is not within 0.05% of the selected input REFCLKT/E signal, then an out of lock condition has occurred. 1: Transmit PLL has been locked at least during 3 consecutive periods of 4096 Reference clock cycles
Reserved	7:4			Not used

SIMR#EnMon: Status register of the Receive SIM chiplet. These are unlatched status bits that follow the driving signal immediately

Table 77. SIMR#EnMon: [3915 H, 3955 H, 3995 H, 39D5 H]

Signal Name	Bit Pos.	Access	Default	Description
Rx#_VCO_Clk_det	0	R	N/A	0: The current frequency of the Receive Channel # VCO is lower than around 10 MHz 1: The current frequency of the Receive Channel # VCO is higher than around 10 MHz
Rx#_ZClkEn	1	R	N/A	0: The Receive Channel # VCO clock is not oscillating as expected. 1: The Receive Channel # VCO clock is oscillating as expected.
Rx#_ZEnable	2	R	N/A	This status is a delayed copy of the Rx#_Enable bit (bit 0 in register SIMR#Conf1)
Reserved	7:3			Not used

SIMR#PLLMon: Status register of the Receive SIM chiplet. These are status bits that follow the driving signal immediately

Table 78. SIMR#PLLMon: [3916 H, 3956 H, 3996 H, 39D6 H]

Signal Name	Bit Pos.	Access	Default	Description
Rx#_Lock_Monitor	3:0	R	N/A	Value of the lock counter.
Reserved	6:4			Not used
Rx#_Lock	7	R	N/A	0: RX Clock Recovery PLL # is in Data Recovery Mode. 1: RX Clock Recovery PLL # is in Frequency Acquisition Mode. Note: The Lock Detector will remain in Data Recovery Mode up to ± 250 ppm frequency offset.

SIMR#LtrR: register to control various modes of operation of the Receive SIM chiplet.

Table 79. SIMR#LtrR: [3918 H, 3958 H, 3998 H, 39D8 H]

Signal Name	Bit Pos.	Access	Default	Description
Rx#_Ltr_Reset	0	W	N/A	Writing anything to this register causes a Reset Lock to Reference on Receive Channel #. This action could also be initiated by deasserting and reasserting Rx#_Enable field (bit0 in SIMR#Conf1 register), or if the LOSSSIG# lead goes to the active state and then to the inactive state.
Reserved	7:1			Not used

SIMTrim: register to control VCO Trim.

Table 80. SIMTrim: [3921 H]

Signal Name	Bit Pos.	Access	Default	Description
VCO_trim_value	2:0	R	N/A	These bits report the VCOTrim computed values, after the AutoTrim has been performed successfully. If the recommended power up procedure is followed, this same VCOTrim value is valid for all Rx and Tx VCOs.
VCO_trim_status	4:3	R	01	These bits will both be set to 1 when the AutoTrim has been launched.
Reserved	7:5			Not used

GPP HANDLER ARCHITECTURE

All GPP handlers for the various chiplets have the following general register structure:

Table 81. General Register Structure for GPP Handlers

Address Range (Hex)	Register Function
0 - 1	Read-on-the-fly registers
2 - 3	Counter enable registers
4 - 2F	Counters and counter threshold registers
30	Reset register
31 - 32	Command registers
33 - 37	Status and event latch registers
38 - 47	Interrupt registers (even address = interrupt register, following odd address = interrupt mask register)
48 - 57	Configuration registers

Counters

Every counter has an enable bit in the counter enable register (address 2 or 3), and optionally up to two programmable thresholds. Each counter has an interrupt bit for overflow and up to two interrupt bits for threshold detection in the counter interrupt registers. For all counters in one handler there are common “read-on-the-fly registers”, that are used to store the higher-order bytes to obtain a correct readback value for counters larger than 8-bits. Counters are read-only registers, the count enable registers are read/write.

Note on reading counters:

Independent of the counter length, given that a counter has address n as base, reading address n or address n+1 both yield the least significant byte of the counter. Reading address n has no influence on the counter but reading address n+1 will reset the counter after the read. Reading address n or n+1 will always latch the higher-order bytes into the read-on-the-fly registers (before the optional automatic reset). Counters can only be read and not written to. For a 16-bit counter the most significant byte should be read from ROFmid (address 0). For a 24-bit counter, the most significant byte is read from ROFhi (address 1), the next byte from ROFmid (address 0). To completely read a 24-bit counter, first read the least significant byte from counter address n or n+1, followed by reading ROFmid and ROFhi (address 0; address 1).

Reset Registers

Each handler has a one-bit reset register. Bit 0 is the chiplet reset control. This bit is active high after power- on reset, causing the chiplet to be disabled. This is a read/write register. The default chiplet register settings are not affected by the setting of the handler reset bits.

Command Registers

The optional command register(s) will generate events to the chiplet. When a bit is written high by the microprocessor, it will remain high for one chiplet clock cycle. Therefore, reading back a command register will always read back zeros. This is a read/write register.

Status and Event Latch Registers

The value of the optional status registers always follows the driving signal immediately. In contrast, the optional event latch registers remember one or more occurrences of events that happen in a chiplet. This may be considered as a 1-bit saturating counter. Each bit in the register corresponds to an event in the chiplet. Such bits remain high after the event has happened until the microprocessor implicitly or explicitly resets the bit. This is configurable. Implicit reset is done by writing a 1 to the bit that is to be reset. Explicit reset will reset all bits of one register when the register is read. Status bits are read-only latches, whereas event latch bits are read/write. Both kinds of bits can be present in the same 8-bit register.

Interrupt Registers

When there are counters, user interrupts or fatal bits in a chiplet, a Main Interrupt Request register will be present. Bit 0 always is the fatal interrupt bit, which is set as soon as a FSM (Finite State Machine) enters an undefined state. Additionally, in the ACI_Tx1 chiplet, the fatal bit also indicates that a port handler address is changed during the transfer of a cell/chunk. The other bits refer to counters or user interrupt registers, to allow easy determination of the interrupt cause. Each Interrupt register has an interrupt MASK register to enable or disable interrupt. After power-on Reset, interrupts are disabled. The interrupt registers are the same as the event latch registers, with the addition that when an interrupt register bit is set, and the corresponding mask register bit is set, the interrupt signal to the Main Interrupt register is activated. If the corresponding mask bit is set, then a bit is set in the corresponding IRQGP2-5 register of the GPPINT chiplet which will identify the chiplet that is requesting an interrupt. The same mechanism to reset the interrupt register bits is used as for the event latch registers. The interrupt MASK registers are only changed by the microprocessor. The interrupt and interrupt mask registers are read/write.

Configuration Registers

These registers are programmed by the microprocessor with setup information, and are read/write. The first configuration register reserves bits 1 and 0 to configure explicit or implicit reset of the event latch registers and interrupt registers respectively (when such registers are present).

Register Types

F Read-On-The-Fly register

N counter register

R reset register

I interrupt register

C configuration register

X control or mask register

S status/event latch register

O command register

ACI_TX1 CHIPLET ADDRESS MAPPING

Chiplet Base Address:

0100 H.

Table 82. ACI_Tx1 Chiplet Address Mapping

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
IT1ROFmid	0	F 8	00000000	Read-on-the-fly register (Middle Significant Byte)	221
IT1ROFhi	1	F 8	00000000	Read-on-the-fly register (Most Significant Byte)	221
IT1CntEn1	2	X 4	0000	COUNT ENABLE register	222
IT1Cnt1:PACNT	4/5	N 8	00000000	Parity error counter, with threshold	221
IT1Th1:PACNTTh	6	X	01111111	Threshold register for counter PACNT	221
IT1Cnt2:PECNT	8/9	N 8	00000000	Protocol error counter, with threshold	222
IT1Th2:PECNTTh	A	X 8	01111111	Threshold register for counter PECNT	222
IT1Cnt3:ATMCELL	C/D	N 24	000000 H	LSByte of 24-bit ATM cell counter, no threshold	222
IT1Cnt4:CORCELL	E/F	N 8	00000000	Corrupted cell/chunk counter, no threshold	222
IT1RESET	30	R 1	1	Default RESET register	223
IT1MainIRQ	38	I 2		MAIN INTerrupt register	223

Table 82. ACI_Tx1 Chiplet Address Mapping (Continued)

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
IT1M_MainIRQ	39	X 2	00	INT MASK register (for IT1MainIRQ)	223
IT1CntIRQ1	3A	I 6		COUNTER INTerrupt register	224
IT1M_CntIRQ1	3B	X 6	000000	INT MASK register (for IT1CntIRQ1)	224
IT1Conf1	48	C 6	000001	Mode of parity check per PHY port	224
IT1Conf2:ADDR1	49	C 5	00000	PHY port address SONET/SDH macro 1	225
IT1Conf3:ADDR2	4A	C 5	00001	PHY port address SONET/SDH macro 2	225
IT1Conf4:ADDR3	4B	C 5	00010	PHY port address SONET/SDH macro 3	225
IT1Conf5:ADDR4	4C	C 5	00011	PHY port address SONET/SDH macro 4	225

ACI_Tx1 (IT1) Counters

IT1ROFmid, IT1ROFhi: Read-on-the-fly registers.

Table 83. IT1ROFmid, IT1ROFhi [0100 H, 0101 H]

Signal Name	Bit Pos.	Access	Default	Description
IT1ROFmid(7:0)	7:0	R	00000000	Read-on-the-fly register (Middle Significant Byte)
IT1ROFhi(7:0)	7:0	R	00000000	Read-on-the-fly register (Most Significant Byte)

IT1Cnt1:PACNT: Number of parity errors detected on the TX UTOPIA Interface. Counter overflow leads to an interrupt request.

IT1Th1:PACNTTh: Threshold register for number of parity errors detected on the TX UTOPIA Interface; threshold equaled leads to an interrupt request.

Table 84. IT1Cnt1:PACNT, IT1Th1:PACNTTh [0104 H / 0105 H, 0106 H]

Signal Name	Bit Pos.	Access	Default	Description
PACNT(7:0)	7:0	R	00000000	Parity error counter
PACNTTh(7:0)	7:0	R/W	01111111	Threshold register

IT1Cnt2:PECNT: Number of UTOPIA protocol errors detected on the UTOPIA Interface (i.e., UTOPIA L2/2P). The counter value is half the number of clock cycles that a cell/chunk has been transmitted on a PHY where it was not allowed to, due to TXCLAV(#)/PAVO=0, as well as the count of cells/chunks that were missing the SOC indication. Counter overflow leads to an interrupt request.

IT1Th2:PECNTTh: Threshold register for number of protocol errors detected on this UTOPIA Interface; threshold equaled leads to an interrupt request.

Table 85: IT1Cnt2:PECNT, IT1Th2:PECNTTh [0108 H / 0109 H, 010A H]

Signal Name	Bit Pos.	Access	Default	Description
PECNT(7:0)	7:0	R	00000000	Protocol error counter
PECNTTh(7:0)	7:0	R/W	01111111	Threshold register

IT1Cnt3:ATMCELL: Number of cells received by this UTOPIA interface from the ATM layer. No threshold register. Counter overflow leads to an interrupt request.

Table 86. IT1Cnt3:ATMCELL [010C H / 010D H]

Signal Name	Bit Pos.	Access	Default	Description
ATMCELL(7:0)	7:0	R	00000000	ATM cell counter, Least Significant Byte

IT1Cnt4:CORCELL: Number of corrupted cell/chunk errors. This counter counts missing Start of Cell/Chunk occurrences to indicate that there is a problem on the TX UTOPIA L2/2P interface. Counter overflow leads to an interrupt request.

Table 87. IT1Cnt4:CORCELL [010E H / 010F H]

Signal Name	Bit Pos.	Access	Default	Description
CORCELL(7:0)	7:0	R	00000000	ACI_Tx1 Corrupted cell/chunk counter

IT1CntEn1: Counter On/Off control register. For each bit position: 0: Counter is disabled, 1: Counter is enabled

Table 88. IT1CntEn1 [0102 H]

Signal Name	Bit Pos.	Access	Default	Description
EN-PACNT	0	R/W	0	UTOPIA parity error counter enable
EN-PECNT	1	R/W	0	UTOPIA protocol error counter enable
EN-ATMCELL	2	R/W	0	ATM cell counter enable
EN-CORCELL	3	R/W	0	Corrupted cell/chunk counter enable
Reserved	7:4			Not used

ACI_Tx1 (IT1) Reset Register

IT1RESET: Reset chiplet control register. This register is automatically preset to the default value by the reset signal ResIT1 from the GPPINT.

For each bit position:

0: Reset not active,

1: Reset active

Table 89. IT1RESET [0130 H]

Signal Name	Bit Pos.	Access	Default	Description
Reset	0	R/W	1	Reset (disable) ACI_Tx1 chiplet
Reserved	7:1			Not used

ACI_Tx1 Interrupt Request and Mask Registers

IT1MainIRQ: Register to indicate fatal interrupt events and to point to user IRQ registers with active requests; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

IT1M_MainIRQ: Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ (Interrupt Request) to the GPPINT. For each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates signal IRQIT1 to GPPINT

Table 90. IT1MainIRQ, IT1M_MainIRQ [0138 H, 0139 H]

Signal Name	Bit Pos.	Access	Default	Description
Fatal	0	R/W	0	Fatal event occurred or a port handler address was changed during the transfer of a cell
CntIRQ1	1	R/W	0	Active request in IT1CntIRQ1 register
Reserved	7:2			Not used

IT1CntIRQ1: Register to indicate active counter interrupt requests of this chiplet. For each bit position:

0: No interrupt request pending

1: Interrupt request pending

IT1M_CntIRQ1: Register to mask pending counter interrupt requests. For each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in IT1MainIRQ register.

Table 91. IT1CntIRQ1, IT1M_CntIRQ1 [013A H, 013B H]

Signal Name	Bit Pos.	Access	Default	Description
OV-PACNT	0	R/W	0	Overflow parity error counter
TH-PACNT	1	R/W	0	Threshold equaled parity error counter.
OV-PECNT	2	R/W	0	Overflow protocol error counter
TH-PECNT	3	R/W	0	Threshold equaled protocol error counter
OV-ATMCELL	4	R/W	0	Overflow ATM cell counter
OV-CORCELL	5	R/W	0	Overflow Corrupted cell/chunk counter
Reserved	7:6			Not used

ACI_Tx1 Configuration Registers

IT1Conf1: Register to control various modes of operation of this chiplet.

Table 92. IT1Conf1 [0148 H]

Signal Name	Bit Pos.	Access	Default	Description
AutRst_Int	0	R/W	1	0: No action on read access 1: Auto-reset interrupt request registers upon read access. Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a 1 to that bit provided that the corresponding alarm condition is removed.
TMOPAIT	1	R/W	0	Mode for UTOPIA (ATM/PPP) parity error detection: 0: Parity check off 1: Parity check on
TMO-PAITC(3:0)	5:2	R/W	0000	Mode of parity calculation: B=0: Parity calculated over data only B=1: Parity calculated over data and control Bxxx: Mode of transmit Port Handler 1. xBxx: Mode of transmit Port Handler 2. xxBx: Mode of transmit Port Handler 3. xxxB: Mode of transmit Port Handler 4.
Reserved	7:6			Not used

IT1Conf2-5:ADDR1-ADDR4: Registers that control the PHY port addresses according to UTOPIA Level 2.

Used in 1 x UTOPIA Level 2 multi-PHY/multi-port configuration (non-STM-4c/STS-12c), multi-PHY/single-port configuration (STM-4c/STS-12c), MULTIPLEXED status indication; for bit positions (4:0) of each register:

00000 to 11110: valid address for PHY port selection.

11111: PHY port is never selected.

Used in 1 x UTOPIA Level 2 multi-PHY/multi-port configuration (non-STM-4c/STS-12c), multi-PHY/single-port configuration (STM-4c/STS-12c), DIRECT status indication; for bit positions (4:0) of each register:

00000 to 11111: valid address for PHY port selection

Table 93. IT1Conf2-5 [0149 H, 014A H, 014B H, 014C H]

Signal Name	Bit Pos.	Access	Default	Description
ADDR1(4:0)	4:0	R/W	00000	PHY port address of SONET/SDH macro 1 (also port address for STM-4c/STS-12c)
Reserved	7:5			Not used
ADDR2(4:0)	4:0	R/W	00001	PHY port address of SONET/SDH macro 2 (for STM-4c/STS-12c: don't care)
Reserved	7:5			Not used
ADDR3(4:0)	4:0	R/W	00010	PHY port address of SONET/SDH macro 3 (for STM-4c/STS-12c: don't care)
Reserved	7:5			Not used
ADDR4(4:0)	4:0	R/W	00011	PHY port address of SONET/SDH macro 4 (for STM-4c/STS-12c: don't care)
Reserved	7:5			Not used

ACI_RX1 CHIPLET ADDRESS MAPPING

Chiplet Base Address:

0300 H.

Table 94. ACI_Rx1 Chiplet Address Mapping

Register Name	Address Offset (Hex)	Type/ Width	Value (binary)	Description	See Page
IR1ROFmid	0	F 8	00000000	Read-on-the-fly register (Middle Significant Byte)	227
IR1ROFhi	1	F 8	00000000	Read-on-the-fly register (Most Significant Byte)	227
IR1CntEn1	2	X 1	0	COUNT ENABLE register	227
IR1Cnt1:ATMCELL	4/5	N 24	000000 H	LSByte of 24-bit ATM cell counter, no threshold	227
IR1RESET	30	R 1	1	Default RESET register	227
IR1Stat1	33	S 4		Indication of which PHY port is selected	228
IR1Stat2	34	S 5		4:0 = selected UTOPIA Level 2 port address	228
IR1MainIRQ	38	I 2		MAIN INTerrupt register	228
IR1M_MainIRQ	39	X 2	00	INT MASK register (for IR1MainIRQ)	228
IR1CntIRQ1	3A	I 3		COUNTER INTerrupt register	229
IR1M_CntIRQ1	3B	X 3	000	INT MASK register (for IR1CntIRQ1)	229
IR1Conf1	48	C 5	01111	Mode of parity generation per PHY port	229
IR1Conf2:P1ADDR	49	C 5	00000	PHY port address of SONET/SDH macro 1	230
IR1Conf3:P2ADDR	4A	C 5	00001	PHY port address of SONET/SDH macro 2	230
IR1Conf4:P3ADDR	4B	C 5	00010	PHY port address of SONET/SDH macro 3	230
IR1Conf5:P4ADDR	4C	C 5	00011	PHY port address of SONET/SDH macro 4	230

ACI_Rx1 (IR1) Counters

IR1ROFmid, IR1ROFhi: Read-on-the-fly registers.

Table 95. IR1ROFmid, IR1ROFhi [0300 H, 0301 H]

Signal Name	Bit Pos.	Access	Default	Description
IR1ROFmid(7:0)	7:0	R	00000000	Read-on-the-fly register (Middle Significant Byte)
IR1ROFhi(7:0)	7:0	R	00000000	Read-on-the-fly register (Most Significant Byte)

IR1Cnt1:ATMCELL: Number of cells transmitted by this UTOPIA interface towards the ATM layer. Counter overflow leads to an interrupt request.

Table 96. IR1Cnt1:ATMCELL [0304 H / 0305 H]

Signal Name	Bit Pos.	Access	Default	Description
ATMCELL(7:0)	7:0	R	00000000	ATM cell counter, Least Significant Byte

IR1CntEn1: Counter On/Off control register

For each bit position:

0: Counter is disabled

1: Counter is enabled

Table 97. IR1CntEn1 [0302 H]

Signal Name	Bit Pos.	Access	Default	Description
EN-ATM	0	R/W	0	ATM cell counter enable
Reserved	7:1			Not used

ACI_Rx1 (IR1) Reset Register

IR1RESET: Reset chiplet control register. This register is automatically preset to the default value by the reset signal ResIR1 from the GPPINT.

For each bit position:

0: Reset not active

1: Reset active

Table 98. IR1RESET [0330 H]

Signal Name	Bit Pos.	Access	Default	Description
Reset	0	R/W	1	Reset (disable) ACI_Rx1 chiplet
Reserved	7:1			Not used

ACI_Rx1 (IR1) Status Register

IR1Stat1: Status register 1 of this chiplet. These are status bits that follow the driving signal immediately.

Table 99. IR1Stat1 [0333 H]

Signal Name	Bit Pos.	Access	Default	Description
PselIR1	0	R		0: macro 1 is not selected 1: macro 1 selected by PHY port
PselIR2	1	R		0: macro 2 is not selected 1: macro 2 selected by PHY port
PselIR3	2	R		0: macro 3 is not selected 1: macro 3 selected by PHY port
PselIR4	3	R		0: macro 4 is not selected 1: macro 4 selected by PHY port
Reserved	7:4			Not used

IR1Stat2: Status register 2 of this chiplet. These are status bits that follow the driving signal immediately.

Table 100. IR1Stat2 [0334 H]

Signal Name	Bit Pos.	Access	Default	Description
UPaddr	4:0	R		Selected UTOPIA Level 2 port address
Reserved	7:5			Not used

ACI_Rx1 (IR1) Interrupt Request and Mask Registers

IR1MainIRQ: Register to indicate fatal interrupt events and to point to user IRQ registers with active requests; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

IR1M_MainIRQ: Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates signal IRQIR1 to GPPINT

Table 101. IR1MainIRQ, IR1M_MainIRQ [0338 H, 0339 H]

Signal Name	Bit Pos.	Access	Default	Description
Fatal	0	R/W	0	Fatal event occurred
CntIRQ1	1	R/W	0	Active request in IR1CntIRQ1 register
Reserved	7:2			Not used

IR1CntIRQ1: Register to indicate active counter interrupt requests of this chiplet; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

IR1M_CntIRQ1: Register to mask pending counter interrupt requests; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in IR1MainIRQ register

Table 102: IR1CntIRQ1, IR1M_CntIRQ1 [033A H, 033B H]

Signal Name	Bit Pos.	Access	Default	Description
OV-ATM	0	R/W	0	Overflow ATM cell counter
Reserved	7:1			Reserved.

ACI_Rx1 Configuration Registers

IR1Conf1: Register to control various modes of operation of this chiplet.

Table 103. IR1Conf1 [0348 H]

Signal Name	Bit Pos.	Access	Default	Description
AutRst_Int	0	R/W	1	0: No action on read access 1: Auto-reset interrupt request registers upon read access Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a 1 to that bit provided that the corresponding alarm condition is removed.
Reserved	1	R/W	1	Reserved
RX1PAMO	2	R/W	1	Control of UTOPIA (ATM/PPP) parity generation: 0: Parity generation off 1: Parity generation on
RX1PAODD	3	R/W	1	Mode for UTOPIA (ATM/PPP) parity generation: 0: Do not use. 1: Odd parity
RX1PA_ALL	7:4	R/W	0	Mode of parity calculation: B=0: Parity calculated over data only B=1: Parity calculated over data and control Bxxx: Mode of receive Port Handler 1. xBxx: Mode of receive Port Handler 2. xxBx: Mode of receive Port Handler 3. xxxB: Mode of receive Port Handler 4.
Reserved	7:5			Not used

IR1Conf2-5:P1ADDR-P4ADDR: Registers that control the PHY port addresses according to UTOPIA Level 2.

Used in 1 x UTOPIA Level 2 multi-PHY/multi-port configuration (non-STM-4c/STS-12c), multi-PHY/single-port configuration (STM-4c/STS-12c), MULTIPLEXED status indication; for bit positions (4:0) of each register:

00000 to 11110: valid address for PHY port selection

11111: PHY port is never selected

Used in 1 x UTOPIA Level 2 multi-PHY/multi-port configuration (non-STM-4c/STS-12c), multi-PHY/single-port configuration (STM-4c/STS-12c), DIRECT status indication; for bit positions (4:0) of each register:

00000 to 11111: valid address for PHY port selection

Table 104. IR1Conf2-5:P1ADDR-P4ADDR [0349 H, 034A H, 034B H, 034C H]

Signal Name	Bit Pos.	Access	Default	Description
P1ADDR(4:0)	4:0	R/W	00000	PHY port address of SONET/SDH macro 1 (also port address for STM-4c/STS-12c)
Reserved	7:5			Not used
P2ADDR(4:0)	4:0	R/W	00001	PHY port address of SONET/SDH macro 2 (for STM-4c/STS-12c: don't care)
Reserved	7:5			Not used
P3ADDR(4:0)	4:0	R/W	00010	PHY port address of SONET/SDH macro 3 (for STM-4c/STS-12c: don't care)
Reserved	7:5			Not used
P4ADDR(4:0)	4:0	R/W	00011	PHY port address of SONET/SDH macro 4 (for STM-4c/STS-12c: don't care)
Reserved	7:5			Not used

PH_TX1/2/3/4 CHIPLET ADDRESS MAPPING

Chiplet Base Address:

PH_Tx1 0500 H.

PH_Tx2 0600 H.

PH_Tx3 0700 H.

PH_Tx4 0800 H.

The four Port Handler SONET/SDH chiplets are grouped together in the following tables (# = 1,2,3,4). Only the Port Handlers that are to handle ATM or PPP data, or that are involved in PHCC operation, need to be configured. Please note that in 1xSTM-4c/STS-12c mode all four Port Handler chiplets need to be configured if processing ATM or PPP data.

Table 105. PH_Tx1/2/3/4 Chiplet Address Mapping

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
Reset	30	R 1	1	Default RESET register	231
PT#Stat1	33	S 2		0 = FF 1 = PAF	231
PT#MainIRQ	38	I 1		MAIN INTerrupt register	232
PT#M_MainIRQ	39	X 1	0	INT MASK register (for PT#MainIRQ)	232
PT#Conf1:REFSPT1	48	C 2	11	0 = R and R INT 1 = R and R STAT	232
PT#Conf2:NEWCONF	49	C 7	1011111	6:0 = PAF threshold	233

PH_Tx1/2/3/4 (PT1/2/3/4) Reset Registers

PT#RESET: Reset chiplet control register. These registers are automatically preset to the default value by the reset signals ResPT1, ResPT2, ResPT3 and ResPT4, respectively, from the GPPINT.

For each bit position:

0: Reset not active

1: Reset active

Table 106. PT#RESET [0530 H, 0630 H, 0730 H, 0830 H]

Signal Name	Bit Pos.	Access	Default	Description
Reset	0	R/W	1	Reset (disable) PH_Tx1/2/3/4 chiplet
Reserved	7:1			Not used

PH_Tx1/2/3/4 (PT1/2/3/4) Status Registers

PT#Stat1: Status register of this chiplet. Bit 0 is an event latch register. Bit 1 immediately follows the driving signal (static).

Table 107. PT#Stat1 [0533 H, 0633 H, 0733 H, 0833 H]

Signal Name	Bit Pos.	Access	Default	Description
acbtxFF	0	R/W		ACB_Tx FIFO Full flag was set
acbtxPAF	1	R		ACB_Tx FIFO Almost Full flag
Reserved	7:2			Not used

PH_Tx1/2/3/4 Interrupt Request and Mask Registers

PT#MainIRQ: Register to indicate fatal interrupt events; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

PT#M_MainIRQ: Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates signal IRQPT1/2/3/4 to GPPINT

Table 108. PT#MainIRQ, PT#M_MainIRQ [0538 H, 0638 H, 0738 H, 0838 H, 0539 H, 0639 H, 0739 H, 0839 H]

Signal Name	Bit Pos.	Access	Default	Description
Fatal	0	R/W	0	Fatal event occurred
Reserved	7:1			Not used

PH_Tx1/2/3/4 Configuration Registers

PT#Conf1:REFSPT1: Register to control various modes of operation of this chiplet.

Table 109. PT#Conf1:REFSPT1 [0548 H, 0648 H, 0748 H, 0848 H]

Signal Name	Bit Pos.	Access	Default	Description
AutRst_Int	0	R/W	1	0: No action on read access 1: Auto-reset interrupt request register upon read access Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a 1 to that bit provided that the corresponding alarm condition is removed.
AutRst_Sta	1	R/W	1	0: No action on read access 1: Auto-reset bit 0 of the PT#Stat1 status register upon read access
Reserved	7:2			Not used

PT#Conf2:NEWCONF: Threshold for programmable almost full flag for the TX ACB FIFO.

Table 110. PT#Conf2:NEWCONF [0549 H, 0649 H, 0749 H, 0849 H]

Signal Name	Bit Pos.	Access	Default	Description
PAFTh	6:0	R/W	1011111	PAF threshold. This threshold is used to derive the TXCLAV/PAVO signals. All four registers should be set identically according to mode, as follows: ATM: STM-4c/STS-12c 73 H STM-1/ STS-3c/STM-4/STS-12 5F H PPP: STM-4c/STS-12c Chunk Size=32 bytes 76 H Chunk Size=48 bytes 74 H Chunk Size=64 bytes 72 H STM-1/STS-3c/STM-4/STS-12 Chunk Size=16 bytes 72 H Chunk Size=32 bytes 6A H Chunk Size=48 bytes 62 H Chunk Size=64 bytes 5A H Note: An increment of 1 H means that two more bytes are allowed in the FIFO before the acbtxPAF alarm is asserted.
Reserved	7			Not used

PH_RX1/2/3/4 CHIPLET ADDRESS MAPPING

Chiplet Base Address:

PH_Rx1 0900 H.

PH_Rx2 0A00 H.

PH_Rx3 0B00 H.

PH_Rx4 0C00 H.

The four Port Handler SONET/SDH chiplets are grouped together in the following tables (# = 1,2,3,4). Only the Port Handlers that are to handle ATM or PPP data, or that are involved in PHCC operation, need to be configured. Please note that in 1xSTM-4c/STS-12c mode all four Port Handler chiplets need to be configured if pro-

cessing ATM or PPP data.

Table 111. PH_Rx1/2/3/4 Chiplet Address Mapping

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
PR#RESET	30	R 1	1	Default RESET register	234
PR#Stat1	33	S 3		0 = PAE flag 1 = EF flag 2 = CC flag	234
PR#MainIRQ	38	I 1		MAIN INTerrupt register	235
PR#M_MainIRQ	39	X 1	0	INT MASK register (for PR#Main-IRQ)	235
PR#Conf1	48	C 2	11	0 = R and R INT 1 = R and R STAT	235
PR#Conf2:RXTHBUF	49	C 7	0000110	6:0 = PAE threshold	236

PH_Rx1/2/3/4 (PR1/2/3/4) Reset Registers

PR#RESET: Reset chiplet control register. These registers are automatically preset to the default value by the reset signals ResPR1, ResPR2, ResPR3 and ResPR4, respectively, from the GPPINT.

For each bit position:

0: Reset not active

1: Reset active

Table 112. PR#RESET [0930 H, 0A30 H, 0B30 H, 0C30 H]

Signal Name	Bit Pos.	Access	Default	Description
Reset	0	R/W	1	Reset (disable) PH_Rx1/2/3/4 chiplet
Reserved	7:1			Not used

PH_Rx1/2/3/4 Status Registers

PR#Stat1: Status register of this chiplet. Bit 0 immediately follows the driving signal (static). Bits 2 and 1 are event latch registers.

Table 113. PR#Stat1 [0933 H, 0A33 H, 0B33 H, 0C33 H]

Signal Name	Bit Pos.	Access	Default	Description
acbrxPAE	0	R		ACB_Rx FIFO Programmable Almost Empty flag
acbrxEF	1	R/W		ACB_Rx FIFO Empty flag
acbrxCC	2	R/W		A corrupted cell was sent to UTOPIA
Reserved	7:3			Not used

PH_Rx1/2/3/4 Interrupt Request and Mask Registers

PR#MainIRQ: Register to indicate fatal interrupt events; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

PR#M_MainIRQ: Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates signal IRQPR1/2/3/4 to GPPINT

Table 114. PR#MainIRQ, PR#M_MainIRQ [0938 H, 0A38 H, 0B38 H, 0C38 H, 0939 H, 0A39 H, 0B39 H, 0C39 H]

Signal Name	Bit Pos.	Access	Default	Description
Fatal	0	R/W	0	Fatal event occurred
Reserved	7:1			Not used

PH_Rx Configuration Registers

PR#Conf1: Register to control various modes of operation of this chiplet.

Table 115. PR#Conf1 [0948 H, 0A48 H, 0B48 H, 0C48 H]

Signal Name	Bit Pos.	Access	Default	Description
AutRst_Int	0	R/W	1	0: No action on read access 1: Auto-reset interrupt request register upon read access Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a 1 to that bit provided that the corresponding alarm condition is removed.
AutRst_Sta	1	R/W	1	0: No action on read access 1: Auto-reset bits 2 and 1 of the PR#Stat1 status register upon read access
Reserved	7:2			Not used

PR#Conf2:RXTHBUF: Threshold for programmable almost empty flag.

Table 116: PR#Conf2:RXTHBUF [0949 H, 0A49 H, 0B49 H, 0C49 H]

Signal Name	Bit Pos.	Access	Default	Description
PAETh	6:0	R/W	0000110	ACB FIFO PAE threshold. This threshold is used to derive the RXCLAV/PAVO signals. This register should be set according to mode as follows: ATM: STM-4c/STS-12c 07 H STM-1/STS-3c/STM-4/STS-12 1B H PPP: STM-4c/STS-12c Chunk Size=32 bytes 02 H Chunk Size=48 bytes 04 H Chunk Size=64 bytes 06 H STM-1/STS-3c/STM-4/STS-12 Chunk Size=16 bytes 08 H Chunk Size=32 bytes 10 H Chunk Size=48 bytes 18 H Chunk Size=64 bytes 20 H
Reserved	7			Not used

ACH_TX1 CHIPLET ADDRESS MAPPING

Chiplet Base Address:

0D00 H.

Table 117. ACH_Tx1 Chiplet Address Mapping

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
HT1ROFmid	0	F 8	00000000	Read-on-the-fly register (Middle Significant Byte)	238
HT1ROFhi	1	F 8	00000000	Read-on-the-fly register (MSByte)	238
HT1CntEn1	2	X 3	000	COUNT ENABLE register	239
HT1Cnt1:ACBC	4/5	N 8	000000 H	LSByte of 24-bit ACB cell counter, no threshold	238
HT1Cnt2:IUC	6/7	N 8	000000 H	LSByte of 24-bit Idle/Unassigned Cell (IUC) counter, no threshold	238

Table 117. ACH_Tx1 Chiplet Address Mapping (Continued)

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
HT1Cnt3:APSPE	8/9	N 8	00000000	APS parity error counter	239
HT1Th3:APSPETh	A	X 8	01111111	Threshold register for counter APSPE	239
HT1RESET	30	R 1	1	Default RESET register	239
HT1Stat1	33	S 8		Status register 1	240
HT1Stat2	34	S 4		Status register 2	240
HT1MainIRQ	38	I 2		MAIN INTerrupt register	241
HT1M_MainIRQ	39	X 2	00	INT MASK register (for HT1MainIRQ)	241
HT1CntIRQ1	3A	I 4		COUNTER INTerrupt register	241
HT1M_CntIRQ1	3B	X 4	0000	INT MASK register (for HT1CntIRQ1)	241
HT1Conf1: CELLTENABLE	48	C 4	1111	Chiplet configuration register	242
HT1Conf2: ACBTXTHPAE	49	C 7	0011011	Programmable almost empty threshold	243
HT1Conf3: HEADERBYTE1	4A	C 8	00000000	IU (Idle/Unassigned)-cell header byte 1, defaults according to [I.432]	243
HT1Conf4: HEADERBYTE2	4B	C 8	00000000	IU-cell header byte 2, defaults according to [I.432]	243
HT1Conf5: HEADERBYTE3	4C	C 8	00000000	IU-cell header byte 3, defaults according to [I.432]	243
HT1Conf6: HEADERBYTE4	4D	C 8	00000001	IU-cell header byte 4, defaults according to [I.432]	243
HT1Conf7: HEADERBYTE5	4E	C 8	01010010	IU-cell header byte 5	243
HT1Conf8: PAYLOADBYTE	4F	C 8	01101010	IU-cell payload byte	243
HT1Conf9: HECENCTRL	50	C 7	0001100	HEC processing control	244
HT1Conf10: HECOFFSET	51	C 8	01010101	HEC offset pattern register	245
HT1Conf11: HECMASKAND	52	C 8	11111111	HEC error corruption mask (AND)	245
HT1Conf12: HECMASKOR	53	C 8	00000000	HEC error corruption mask (OR)	245
HT1Conf13: SDBTXTHPAF	54	C 6	010011	programmable almost full threshold	243

Table 117. ACH_Tx1 Chiplet Address Mapping (Continued)

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
HT1Conf14: APSELECT	55	C 6	111111	APS select matrix (transmit direction)	246
HT1Conf15: APSCONF	56	C 4	1010	APS parity handling (transmit direction)	248

ACH_Tx1 (HT1) Counters

HT1ROFmid, HT1ROFhi: Read-on-the-fly registers.

Table 118. HT1ROFmid, HT1ROFhi [0D00 H, 0D01 H]

Signal Name	Bit Pos.	Access	Default	Description
HT1ROFmid(7:0)	7:0	R	00000000	Read-on-the-fly register (Middle Significant Byte)
HT1ROFhi(7:0)	7:0	R	00000000	Read-on-the-fly register (Most Significant Byte)

HT1Cnt1:ACBC: Number of cells transmitted from this ATM Cell Buffer (ACB_Tx1). Counter overflow leads to an interrupt request.

Table 119. HT1Cnt1:ACBC [0D04 H / 0D05 H]

Signal Name	Bit Pos.	Access	Default	Description
ACBC(7:0)	7:0	R	00000000	ACB cell counter, Least Significant Byte

HT1Cnt2:IUC: Number of transmitted Idle and Unassigned Cells (IUC). Counter overflow leads to an interrupt request.

Table 120. HT1Cnt2:IUC [0D06 H / 0D07 H]

Signal Name	Bit Pos.	Access	Default	Description
IUC(7:0)	7:0	R	00000000	Idle/unassigned cell count, Least Significant Byte

HT1Cnt3:APSPE: Number of parity errors from Automatic Protection Switching (APS). Counter overflow leads to an interrupt request.

HT1Th3:APSPETh: Threshold for APS parity errors. Threshold equaled leads to an interrupt request.

Table 121. HT1Cnt3:APSPE, HT1Th3:APSPETh [0D08 H / 0D09 H, 0D0A H]

Signal Name	Bit Pos.	Access	Default	Description
APSPE(7:0)	7:0	R	00000000	APS parity error counter
APSPETh(7:0)	7:0	R/W	01111111	Threshold for APS parity error counter

HT1CntEn1: Counter On/Off control register for ACH_Tx1/ACB_Tx1.

For each bit position:

0: Counter is disabled

1: Counter is enabled

Table 122. HT1CntEn1 [0D02 H]

Signal Name	Bit Pos.	Access	Default	Description
EN-ACBC	0	R/W	0	ACB cell counter enable
EN-IUC	1	R/W	0	Idle/unassigned cell counter enable
EN-APSPE	2	R/W	0	APS parity error counter enable
Reserved	7:3			Not used

ACH_Tx1 (HT1) Reset Register

HT1RESET: Reset chiplet control register. This register is automatically preset to the default value by the reset signal ResHT1 from the GPPINT.

For each bit position:

0: Reset not active

1: Reset active

Table 123. HT1RESET [0D30 H]

Signal Name	Bit Pos.	Access	Default	Description
Reset	0	R/W	1	Reset (disable) ACH_Tx1 chiplet
Reserved	7:1			Not used

ACH_Tx1 Status Registers

HT1Stat1: Status register 1 of this chiplet. The bits of this register are event latches.

Table 124. HT1Stat1 [0D33 H]

Signal Name	Bit Pos.	Access	Default	Description
SocMiss	0	R/W		Missing start of cell event
sdbtxFF	1	R/W		FIFO full flag from SDB_Tx1
TxLpB1Fe	2	R/W		Transmit Loopback 1 configuration mismatch (e.g., the TX side is configured to 4 x STM-1 but the RX side is configured to 1 x STM-4 while TX Loopback stage 1 is enabled.)
TxLpB2Fe	3	R/W		Transmit Loopback 2 configuration mismatch (e.g., the TX side is configured to 4 x STM-1 but the RX side is configured to 1 x STM-4 while TX Loopback stage 2 is enabled.)
RxLpB2Fe	4	R/W		Receive Loopback 2 configuration mismatch (e.g., the TX side is configured to 4 x STM-1 but the RX side is configured to 1 x STM-4 while RX Loopback stage 2 is enabled.)
IUCFErr	5	R/W		Unexpected state transition in FSM
ApsFErr	6	R/W		APS fatal error detected
ApsPaErr	7	R/W		Parity error detected at device - external APS interface (input direction)

HT1Stat2: Status register 2 of this chiplet. The bits of this register immediately follow the driving signal.

Table 125. HT1Stat2 [0D34 H]

Signal Name	Bit Pos.	Access	Default	Description
acbtxEF	0	R		FIFO empty flag from ACB_Tx1
acbtxPAE	1	R		Programmable almost empty flag from ACB_Tx1
sdbtxPAF	2	R		Programmable almost full flag from SDB_Tx1
cellgenstatus	3	R		0: Idle/unassigned cell is transmitted 1: ACB cell is transmitted
Reserved	7:4			Not used

ACH_Tx1 Interrupt Request and Mask Registers

HT1MainIRQ: Register to indicate fatal interrupt events and to point to user IRQ registers with active requests; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

HT1M_MainIRQ: Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates signal IRQHT1 to GPPINT

Table 126. HT1MainIRQ, HT1M_MainIRQ [0D38 H, 0D39 H]

Signal Name	Bit Pos.	Access	Default	Description
Fatal	0	R/W	0	Fatal event occurred
CntIRQ1	1	R/W	0	Active request in HT1CntIRQ1 register
Reserved	7:2			Not used

HT1CntIRQ1: Register to indicate active counter interrupt requests of this chiplet; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

HT1M_CntIRQ1: Register to mask pending counter interrupt requests; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in HT1MainIRQ register

Table 127. HT1CntIRQ1,HT1M_CntIRQ1 [0D3A H, 0D3B H]

Signal Name	Bit Pos.	Access	Default	Description
OV-ACBC	0	R/W	0	Overflow ACB cell counter
OV-IUC	1	R/W	0	Overflow idle/unassigned cell counter
OV-APSPE	2	R/W	0	Overflow APS parity error counter
TH-APSPE	3	R/W	0	Threshold equaled APS parity error counter
Reserved	7:4			Not used

ACH_Tx1 Configuration Registers

HT1Conf1:CELLTENABLE: register to control various modes of operation of this chiplet.

Table 128. HT1Conf1:CELLTENABLE [0D48 H]

Signal Name	Bit Pos.	Access	Default	Description
AutRst_Int	0	R/W	1	0: No action on read access 1: Auto-reset interrupt request registers upon read access. Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a 1 to that bit provided that the corresponding alarm condition is removed.
AutRst_Sta	1	R/W	1	0: No action on read access 1: Auto-reset all bits in the HT1Stat1 status register upon read access
ACBenable	2	R/W	1	0: ACB FIFO read disabled. The data that is transmitted depends on the setting of the IUCenable bit. If IUCenable is set to 0 then unequipped frames are transmitted. If IUCenable is set to 1 then idle/unassigned cells are transmitted in the SONET/SDH payload. 1: ACB FIFO read enabled
IUCenable	3	R/W	1	0: generation of IUC disabled. See the description of the ACBenable bit above for more information. 1: generation of IUC enabled
Reserved	7:4			Not used

HT1Conf2:ACBTXTHPAE: Threshold for Programmable Almost Empty flag (ACB_Tx1)

HT1Conf13:SDBTXTHPAF: Threshold for Programmable Almost Full flag (SDB_Tx1). This register setting should not be changed in Telecom Bus mode. In ATM or PPP modes, the PAF signal from the TX SDB FIFO is the signal to the APH block to stop writing data to it.

Table 129. HT1Conf2:ACBTXHPAE, HT1Conf13:SDBTXTHPAF [0D49 H, 0D54 H]

Signal Name	Bit Pos.	Access	Default	Description
ACBTXTHPAE(6:0)	6:0	R/W	0011011	Threshold for PAE flag (ACB_Tx1). This register should be set according to mode as follows: ATM: STM-4c/STS-12c (set all four chiplets the same) 07 H STM-1/STS-3c/STM-4/STS-12 (set only the chiplets enabled to process ATM to this value) 1B H PPP: For PPP mode these registers are not used. They can be left at their default values.
Reserved	7			Not used
SDBTXTHPAF(5:0)	5:0	R/W	010011	Threshold for PAF flag (SDB_Tx1). This threshold must be set to a value between the ThrNoW(5:0) and ThrHiW(5:0) thresholds in the OT1Conf9 and OT1Conf10 registers.
Reserved	7:6			Not used

HT1Conf3-7:HEADERBYTE1/2/3/4/5: Idle/Unassigned cell header bytes, default pattern according to [I.432].

HT1Conf8:PAYLOADBYTE: Idle/Unassigned cell payload byte.

Table 130. HT1Conf3-7:HEADERBYTE 1/2/3/4/5, HT1Conf8:PAYLOADBYTE [0D4A H, 0D4B H, 0D4C H, 0D4D H, 0D4E H, 0D4F H]

Signal Name	Bit Pos.	Access	Default	Description
HEADERBYTE1(7:0)	7:0	R/W	00000000	IU-cell header byte 1
HEADERBYTE2(7:0)	7:0	R/W	00000000	IU-cell header byte 2
HEADERBYTE3(7:0)	7:0	R/W	00000000	IU-cell header byte 3
HEADERBYTE4(7:0)	7:0	R/W	00000001	IU-cell header byte 4
HEADERBYTE5(7:0)	7:0	R/W	01010010	IU-cell header byte 5
PAYLOADBYTE(7:0)	7:0	R/W	01101010	IU-cell payload byte

HT1Conf9:HECENCTRL: HEC processing control configuration register.

Table 131. HT1Conf9:HECENCTRL [0D50 H]

Signal Name	Bit Pos.	Access	Default	Description
HECCntlUDF1(1:0)	1:0	R/W	00	Mode of final HEC manipulation by the UTOPIA UDF1 (UDF=User Defined) byte after HECOFFSET, HECMASKAND and HECMASKOR operations: 00: No manipulation 01: HEC XOR UDF1 10: HEC AND UDF1 11: HEC OR UDF1 This feature is available for both the 16-bit and 8-bit wide TX UTOPIA interfaces.
HECenable	2	R/W	1	0: HEC calculation/manipulation disabled. The UDF1 byte from the TX UTOPIA interface is transmitted. 1: HEC calculation/manipulation enabled. The HEC is calculated and inserted by the PHAST-12E based on the first four header bytes of the ATM Cell input on the TX UTOPIA interface.
SCRenable	3	R/W	1	0: ATM cell payload scrambling disabled 1: ATM cell payload scrambling enabled
CellType(2:0)	6:4	R/W	000	Payload byte control for Idle/Unassigned Cells: 000: Each PL byte is the same (default) 001: Increment PL byte for each ATM cell, start with default after reset. e.g., payload bytes of a cell are all set to M, the payloads bytes of the next cell are all set to M+1, etc., 010: Increment each PL byte of a cell, start each cell with default byte 011: Increment each PL byte of a cell, cross cell boundaries, start first cell after reset with default byte 1xx: Each PL byte is the same
Reserved	7			Not used

HT1Conf10:HECOFFSET: HEC offset pattern (also known as the coset) register for byte pattern used in ATM cell header HEC calculation as base offset according to [I.432].

HT1Conf11:HECMASKAND: HEC mask pattern register for the byte pattern used in the ATM cell header HEC calculation as dedicated (ANDing) HEC error corruption mask.

HT1Conf12:HECMASKOR: HEC mask pattern register for the byte pattern used in the ATM cell header HEC calculation as dedicated (ORing) HEC error corruption mask.

The HEC is calculated as follows with these registers:

- Intermediate HEC = (raw HEC XOR HECOFFSET) AND HECMASKAND OR HECMASKOR.
- Then the intermediate HEC is acted upon by the UDF1 input from the UTOPIA interface as dictated by the HECCntlUDF1(1:0) bits in the HT1Conf9:HECENCTRL register to produce the final HEC.

Table 132. HT1Conf10:HECOFFSET, HT1Conf11:HECMASKAND, HT1Conf12:HECMASKOR [0D51 H, 0D52 H, 0D53 H]

Signal Name	Bit Pos.	Access	Default	Description
HECOFFSET(7:0)	7:0	R/W	01010101	HEC offset/ coset pattern
HECMASKAND(7:0)	7:0	R/W	11111111	HEC error corruption mask (AND)
HECMASKOR(7:0)	7:0	R/W	00000000	HEC error corruption mask (OR)

HT1Conf14:APSSELECT: APS select matrix for transmit direction from internal APH blocks to external APS port and/or internal SFH blocks, or APS external input port towards internal SFH blocks. The flow of data is controlled by the SFH block via the TXAPSDARQ. The TXAPSDARQ signal is basically indicating that the TX SDB FIFO inside of the SFH block is almost empty and is requesting data. The TXAPSDAVA signal indicates that the data on the TXAPSDAT[7:0] bus is valid. Figure 63 below shows the direction of signal flow. Two sets of control bit settings are provided in the HT1Conf14 register: bridged and switched. The difference between these two sets of bits is the source of the TXAPSDARQ signal, otherwise the signals are routed the same way for either set of bits. When a bit setting from the bridged group is written, the TXAPSDARQ signal is comes from the working channel. When a bit setting from the switched group is written, the TXAPSDARQ signal is comes from the protection channel. **Note:** In multi-chip operation, with the TX SFH blocks of the different chips running off of different TX SFH clocks, it is necessary to enable pointer processing to account for the differences in those TX SFH clocks. Also note that the APS port signals are transferred by a common ACHCLK clock. A common ACHCLK signal is required when using the APS port in multi chip applications. The APS Port and APS functionality are only operational in 4xSTM-1/STS-3c mode.

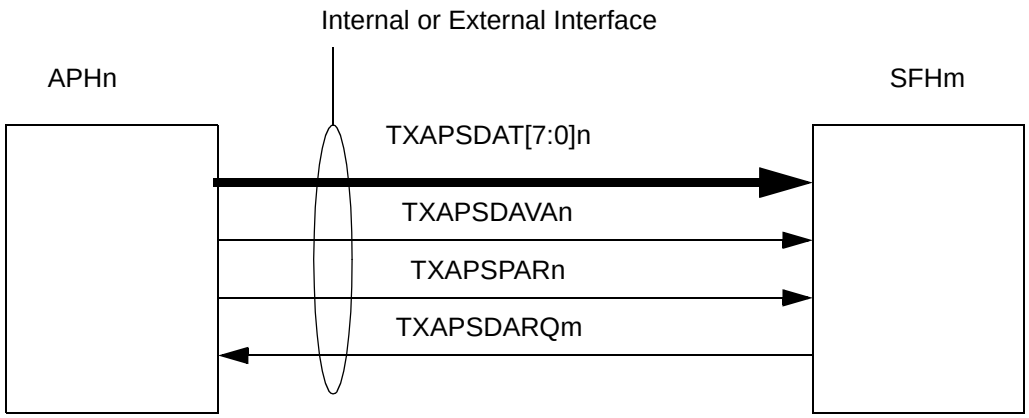


Figure 63. Direction of TX APS Flow Control

Table 133. HT1Conf14:APSSELECT [0D55 H]

Signal Name	Bit Pos.	Access	Default	Description
APSSELECT(5:0)	5:0	R/W	111111	APS bridged: The settings below describe the source of the bridge. Also, the control signals are from the SFH # that corresponds to the indicated source. e.g., 000000 causes the data from APH 2 to be bridged to SFH 1 and SFH 2. The control signals are from the SDB FIFO of SFH 2 to APH 2. These settings should be used if it is desired that the working channel control the flow of data. The TXAPSDARQ signal of the protection channel is disabled. 000000: SFH 1: Source is APH 2 000001: SFH 1: Source is APH 3 000010: SFH 1: Source is APH 4 000011: SFH 1: Source is APS external input port 000100: SFH 2: Source is APH 1 000101: SFH 2: Source is APH 3 000110: SFH 2: Source is APH 4 000111: SFH 2: Source is APS external input port 001000: SFH 3: Source is APH 1 001001: SFH 3: Source is APH 2 001010: SFH 3: Source is APH 4 001011: SFH 3: Source is APS external input port 001100: SFH 4: Source is APH 1 001101: SFH 4: Source is APH 2 001110: SFH 4: Source is APH 3 001111: SFH 4: Source is APS external input port 010000: APS out: Source is APH 1 010001: APS out: Source is APH 2 010010: APS out: Source is APH 3 010011: APS out: Source is APH 4

Table 133. HT1Conf14:APSSELECT [0D55 H] (Continued)

Signal Name	Bit Pos.	Access	Default	Description
APSSELECT(5:0) (cont.)	5:0	R/W	111111	APS switched: The settings below describe the source of the bridge. Also, the control signals are from the SFH # that corresponds to the protection channel. e.g., 010100 causes the data from APH 2 to be bridged to SFH 1 and SFH 2. The control signals are from the SDB FIFO of SFH 1 to APH 2. These settings should be used if it is desired that the protection channel control the flow of data. The TXAPSDARQ signal of the working channel is disabled. 010100: SFH 1: Source is APH 2 010101: SFH 1: Source is APH 3 010110: SFH 1: Source is APH 4 010111: SFH 1: Source is APS external input port 011000: SFH 2: Source is APH 1 011001: SFH 2: Source is APH 3 011010: SFH 2: Source is APH 4 011011: SFH 2: Source is APS external input port 011100: SFH 3: Source is APH 1 011101: SFH 3: Source is APH 2 011110: SFH 3: Source is APH 4 011111: SFH 3: Source is APS external input port 100000: SFH 4: Source is APH 1 100001: SFH 4: Source is APH 2 100010: SFH 4: Source is APH 3 100011: SFH 4: Source is APS external input port 100100: APS out: Source is APH 1 100101: APS out: Source is APH 2 100110: APS out: Source is APH 3 100111: APS out: Source is APH 4 101xxx: Do not use. 11xxxx: No APS activated, select blocks 1:1 (default)
Reserved	7:6			Not used

HT1Conf15:APSCONF: APS parity processing control register

Table 134. HT1Conf15:APSCONF [0D56 H]

Signal Name	Bit Pos.	Access	Default	Description
ApsOPaEn	0	R/W	0	APS external output parity control: 0: parity generation disabled 1: parity generation enabled
ApsOPaOdd	1	R/W	1	APS external output parity mode: 0: even parity 1: odd parity
ApsIPaEn	2	R/W	0	APS external input parity control: 0: parity checking disabled 1: parity checking enabled
ApsIPaOdd	3	R/W	1	APS external input parity mode: 0: even parity 1: odd parity
Reserved	7:4			Not used

ACH_TX2/3/4 CHIPLET ADDRESS MAPPING

Chiplet Base Address:

ACH_Tx2 0E00 H.

ACH_Tx3 0F00 H.

ACH_Tx4 1000 H.

The three ATM handlers in the transmit direction are grouped together in the following tables (# = 2,3,4).

Table 135. ACH_Tx2/3/4 Chiplet Address Mapping

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
HT#ROFmid	0	F 8	00000000	Read-on-the-fly register (Middle Significant Byte)	250
HT#ROFhi	1	F 8	00000000	Read-on-the-fly register (Most Significant Byte)	250
HT#CntEn1	2	X 2	00	COUNT ENABLE register	250
HT#Cnt1:ACBC	4/5	N 24	000000 H	LSByte of 24-bit ACB cell counter, no threshold	250
HT#Cnt2:IUC	6/7	N 24	000000 H	LSByte of 24-bit idle/unassigned cell counter, no threshold	250
HT#RESET	30	R 1	1	Default RESET register	251
HT#Stat1	33	S 6		Status register 1	251

Table 135. ACH_Tx2/3/4 Chiplet Address Mapping (Continued)

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
HT#Stat2	34	S 4		Status register 2	251
HT#MainIRQ	38	I 2		MAIN INTerrupt register	252
HT#M_MainIRQ	39	X 2	00	INT MASK register (for HT#MainIRQ)	252
HT#CntIRQ1	3A	I 2		COUNTER INTerrupt register	252
HT#M_CntIRQ1	3B	X 2	00	INT MASK register (for HT#CntIRQ1)	252
HT#Conf1: CELLTENABLE	48	C 4	1111	Chiplet configuration register	253
HT#Conf2: ACBTXTHPAE	49	C 7	0011011	Programmable almost empty threshold	253
HT#Conf3: HEADERBYTE1	4A	C 8	00000000	IU-cell header byte 1, defaults according to [I.432]	254
HT#Conf4: HEADERBYTE2	4B	C 8	00000000	IU-cell header byte 2, defaults according to [I.432]	254
HT#Conf5: HEADERBYTE3	4C	C 8	00000000	IU-cell header byte 3, defaults according to [I.432]	254
HT#Conf6: HEADERBYTE4	4D	C 8	00000001	IU-cell header byte 4, defaults according to [I.432]	254
HT#Conf7: HEADERBYTE5	4E	C 8	01010010	IU-cell header byte 5, defaults according to [I.432]	254
HT#Conf8: PAYLOADBYTE	4F	C 8	01101010	IU-cell payload byte	254
HT#Conf9: HECENCTRL	50	C 7	0001100	HEC processing control	254
HT#Conf10: HECOFFSET	51	C 8	01010101	HEC offset (i.e., coset) pattern register	255
HT#Conf11: HECMASKAND	52	C 8	11111111	HEC error corruption mask (AND)	255
HT#Conf12: HECMASKOR	53	C 8	00000000	HEC error corruption mask (OR)	255
HT#Conf13: SDBTXTHPAF	54	C 6	010100	Programmable almost full threshold	253

ACH_Tx (HT2/3/4) Counters

HT#ROFmid, HT#ROFhi: Read-on-the-fly registers.

Table 136. HT#ROFmid, HT#ROFhi [0E00 H, 0F00 H, 1000 H, 0E01 H, 0F01 H, 1001 H]

Signal Name	Bit Pos.	Access	Default	Description
HT#ROFmid(7:0)	7:0	R	00000000	Read-on-the-fly register (Middle Significant Byte)
HT#ROFhi(7:0)	7:0	R	00000000	Read-on-the-fly register (Most Significant Byte)

HT#Cnt1:ACBC: Number of cells transmitted from the ATM Cell Buffer (ACB_Tx2/3/4). Counter overflow leads to an interrupt request.

Table 137. HT#Cnt1:ACBC [0E04 H / 0E05 H, 0F04 H / 0F05 H, 1004 H / 1005 H]

Signal Name	Bit Pos.	Access	Default	Description
ACBC(7:0)	7:0	R	00000000	ACB cell counter, Least Significant Byte

HT#Cnt2:IUC: Number of transmitted Idle and Unassigned cells. Counter overflow leads to an interrupt request.

Table 138. HT#Cnt2:IUC [0E06 H / 0E07 H, 0F06 H / 0F07 H, 1006 H / 1007 H]

Signal Name	Bit Pos.	Access	Default	Description
IUC(7:0)	7:0	R	00000000	Idle/unassigned cell counter, Least Significant Byte

HT#CntEn1: Counter On/Off control register for ACH_Tx2/3/4 and ACB_Tx2/3/4.

For each bit position:

0: Counter is disabled

1: Counter is enabled

Table 139. HT#CntEn1 [0E02 H, 0F02 H, 1002 H]

Signal Name	Bit Pos.	Access	Default	Description
EN-ACBC	0	R/W	0	ACB cell counter enable
EN-IUC	1	R/W	0	Idle/unassigned cell counter enable
Reserved	7:2			Not used

ACH_Tx (HT2/3/4) Reset Registers

HT#RESET: Reset chiplet control registers. These registers are automatically preset to the default value by the reset signals ResHT2/3/4 from the GPPINT.

For each bit position:

0: Reset not active

1: Reset active

Table 140. HT#RESET [0E30 H, 0F30 H, 1030H]

Signal Name	Bit Pos.	Access	Default	Description
Reset	0	R/W	1	Reset (disable) ACH_Tx2/3/4 chiplet
Reserved	7:1			Not used

ACH_Tx (HT2/3/4) Status Registers

HT#Stat1: Status register 1 of this chiplet. The bits of this register are event latches.

Table 141. HT#Stat1 [0E33 H, 0F33 H, 1033 H]

Signal Name	Bit Pos.	Access	Default	Description
SocMiss	0	R/W		Missed start of cell event
sdbtxFF	1	R/W		FIFO full flag from SDB_Tx#
TxLpB1Fe	2	R/W		Transmit Loopback 1 configuration mismatch
TxLpB2Fe	3	R/W		Transmit Loopback 2 configuration mismatch
RxLpB2Fe	4	R/W		Receive Loopback 2 configuration mismatch
IUCFErr	5	R/W		Unexpected state transition in FSM
Reserved	7:6			Not used

HT#Stat2: Status register 2 of this chiplet. The bits of this register immediately follow the driving signal.

Table 142. HT#Stat2 [0E34 H, 0F34 H, 1034 H]

Signal Name	Bit Pos.	Access	Default	Description
acbtxEF	0	R		FIFO empty flag from ACB_Tx#
acbtxPAE	1	R		Programmable almost empty flag from ACB_Tx#
sdbtxPAF	2	R		Programmable almost full flag from SDB_Tx#
cellgenstatus	3	R		0: Idle/unassigned cell is transmitted 1: ACB cell is transmitted
Reserved	7:4			Not used

ACH_Tx (HT2/3/4) Interrupt Request and Mask Registers

HT#MainIRQ: Register to indicate fatal interrupt events and to point to user IRQ registers with active requests; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

HT#M_MainIRQ: Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates signal IRQHT2/3/4 toGPPINT

Table 143. HT#MainIRQ, HT#M_MainIRQ [0E38 H, 0F38 H, 1038 H, 0E39 H, 0F39 H, 1039 H]

Signal Name	Bit Pos.	Access	Default	Description
Fatal	0	R/W	0	Fatal event occurred
CntIRQ1	1	R/W	0	Active request in HT#CntIRQ1 register
Reserved	7:2			Not used

HT#CntIRQ1: Register to indicate active counter interrupt requests of this chiplet; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

HT#M_CntIRQ1: Register to mask pending counter interrupt requests; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in HT#MainIRQ register

Table 144. HT#CntIRQ1, HT#M_CntIRQ1 [0E3A H, 0F3A H, 103A H, 0E3B H, 0F3B H, 103B H]

Signal Name	Bit Pos.	Access	Default	Description
OV-ACBC	0	R/W	0	Overflow ACB cell counter
OV-IUC	1	R/W	0	Overflow idle/unassigned cell counter
Reserved	7:2			Not used

ACH_Tx (HT2/3/4) Configuration Registers

HT#Conf1:CELLTENABLE: register to control various modes of operation of this chiplet.

Table 145. HT#Conf1:CELLTENABLE [0E48 H, 0F48 H, 1048 H]

Signal Name	Bit Pos.	Access	Default	Description
AutRst_Int	0	R/W	1	0: No action on read access 1: Auto-reset interrupt request registers upon read access. Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a 1 to that bit provided that the corresponding alarm condition is removed.
AutRst_Sta	1	R/W	1	0: No action on read access 1: Auto-reset all bits in the HT#Stat1 status register upon read access
ACBenable	2	R/W	1	0: ACB FIFO read disabled 1: ACB FIFO read enabled
IUCenable	3	R/W	1	0: generation of IUC disabled 1: generation of IUC enabled
Reserved	7:4			Not used

HT#Conf2:ACBTXTHPAE: Threshold for Programmable Almost Empty flag (ACB_Tx2/3/4)

HT#Conf13:SDBTXTHPAF: Threshold for Programmable Almost Full flag (SDB_Tx2/3/4)

Table 146. HT#Conf2:ACBTXHPAE, HT#Conf13:SDBTXHPAF [0E49 H, 0F49 H, 1049 H, 0E54 H, 0F54 H, 1054 H]

Signal Name	Bit Pos.	Access	Default	Description
ACBTXTHPAE(6:0)	6:0	R/W	0011011	Threshold for PAE flag (ACB_Tx2/3/4). These registers should all be set according to mode as follows: ATM: STM-4c/STS-12c (set all four chiplets the same) 07 H STM-1/STS-3c/STM-4/STS-12 (set only the chiplets enabled to process ATM to this value) 1B H PPP: For PPP mode these registers are not used. They can be left at their default values.
Reserved	7			Not used
SDBTXTHPAF(5:0)	5:0	R/W	010100	Threshold for PAF flag (SDB_Tx2/3/4). This threshold must be set to a value between the ThrNoW(5:0) and ThrHiW(5:0) thresholds in the OT#Conf9 and OT#Conf10 registers.
Reserved	7:6			Not used

HT#Conf3-7:HEADERBYTE1/2/3/4/5: Idle/Unassigned cell header bytes, default pattern according to [I.432].

HT#Conf8:PAYLOADBYTE: Idle/Unassigned (IU) cell payload byte.

Table 147. HT#Conf3-7:HEADERBYTE1/2/3/4/5, HT#Conf8:PAYLOADBYTE [0E4A H, 0F4A H, 104A H, 0E4B H, 0F4B H, 104B H, 0E4C H, 0F4C H, 104C H, 0E4D H, 0F4D H, 104D H, 0E4E H, 0F4E H, 104E H, 0E4F H, 0F4F H, 104F H]

Signal Name	Bit Pos.	Access	Default	Description
HEADERBYTE1(7:0)	7:0	R/W	00000000	IU-cell header byte 1
HEADERBYTE2(7:0)	7:0	R/W	00000000	IU-cell header byte 2
HEADERBYTE3(7:0)	7:0	R/W	00000000	IU-cell header byte 3
HEADERBYTE4(7:0)	7:0	R/W	00000001	IU-cell header byte 4
HEADERBYTE5(7:0)	7:0	R/W	01010010	IU-cell header byte 5
PAYLOADBYTE(7:0)	7:0	R/W	01101010	IU-cell payload byte

HT#Conf9:HECENCTRL: HEC processing control configuration register.

Table 148. HT#Conf9:HECENCTRL [0E50 H, 0F50 H, 1050 H]

Signal Name	Bit Pos.	Access	Default	Description
HECCntlUDF1 1:0)	1:0	R/W	00	Mode of final HEC manipulation by the UTOPIA UDF1 byte after HECOFFSET, HECMASKAND and HECMASKOR operations: 00: No manipulation 01: HEC XOR UDF1 10: HEC AND UDF1 11: HEC OR UDF1 This feature is available for both the 16-bit and 8-bit wide UTOPIA interfaces.
HECenable	2	R/W	1	0: HEC calculation/manipulation disabled. The UDF1 byte from the TX UTOPIA interface is transmitted. 1: HEC calculation/manipulation enabled. The HEC is calculated and inserted by the PHAST-12E based on the first four header bytes of the ATM cell input on the TX UTOPIA interface.
SCRenable	3	R/W	1	0: ATM cell payload scrambling disabled 1: ATM cell payload scrambling enabled
CellType(2:0)	6:4	R/W	000	Payload byte control for Idle/Unassigned Cells: 000: Each PL byte is the same (default) 001: Increment PL byte for each ATM cell, start with default after reset 010: Increment each PL byte of a cell, start each cell with default byte 011: Increment each PL byte of a cell, cross cell boundaries, start first cell after reset with default byte 1xx: Each PL byte is the same
Reserved	7			Not used

HT#Conf10:HECOFFSET: HEC offset pattern (i.e., coset) register for the byte pattern used in the ATM cell header HEC calculation as base offset according to [I.432].

HT#Conf11:HECMASKAND: HEC mask pattern register for the byte pattern used in the ATM cell header HEC calculation as dedicated (ANDing) HEC error corruption mask.

HT#Conf12:HECMASKOR: HEC mask pattern register for the byte pattern used in the ATM cell header HEC calculation as dedicated (ORing) HEC error corruption mask.

The HEC is calculated as follows with these registers:

- Intermediate HEC = (raw HEC XOR HECOFFSET) AND HECMASKAND OR HECMASKOR.
- Then the intermediate HEC is acted upon by the UDF1 input from the UTOPIA interface as dictated by the HECCntlUDF1(1:0) bits in the HT#Conf9:HECENCTRL registers to produce the final HEC.

Table 149. HT#Conf10:HECOFFSET, HT#Conf11:HECMASKAND, HT#Conf12:HECMASKOR [0E51 H, 0F51 H, 1051 H, 0E52 H, 0F52 H, 1052 H, 0E53 H, 0F53 H, 1053 H

Signal Name	Bit Pos.	Access	Default	Description
HECOFFSET(7:0)	7:0	R/W	01010101	HEC offset (i.e., coset) pattern. Setting this register to 00 H has the effect of disabling the coset operation in the transmit direction.
HECMASKAND(7:0)	7:0	R/W	11111111	HEC error corruption mask (AND)
HECMASKOR(7:0)	7:0	R/W	00000000	HEC error corruption mask (OR)

ACH_RX1 CHIPLET ADDRESS MAPPING

Chiplet Base Address:

1100 H.

Table 150. ACH_Rx1 Chiplet Address Mapping

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
HR1ROFmid	0	F 8	00000000	Read-on-the-fly register (Middle Significant Byte)	257
HR1ROFhi	1	F 8	00000000	Read-on-the-fly register (Most Significant Byte)	257
HR1CntEn1	2	X 5	00000	COUNT ENABLE register	259
HR1Cnt1:FHR	4/5	N 24	000000 H	LSByte of 24-bit counter, ATM cells or HDLC-like Frames received from SFH, no threshold	257

Table 150. ACH_Rx1 Chiplet Address Mapping (Continued)

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
HR1Cnt2:IHR	6/7	N 24	000000 H	LSByte of 24-bit counter, received Idle cells from SFH1, no threshold	257
HR1Cnt3:EHR1	8/9	N 16	0000 H	LSByte of 16-bit counter, uncor-rected HEC errors with threshold	258
HR1Th32:EHR1T2	A	X 8	00000001	Threshold register Byte 2 (Least Significant Byte) for counter EHR1	258
HR1Th31:EHR1T1	B	X 8	10000000	Threshold register Byte 1 for counter EHR1	258
HR1Cnt4:EHR2	C/D	N 16	0000 H	LSByte of 16-bit counter, corrected HEC errors with threshold	258
HR1Th42:EHR2T2	E	X 8	00000001	Threshold register Byte 2 (Least Significant Byte) for counter EHR2	258
HR1Th41:EHR2T1	F	X 8	10000000	Threshold register Byte 1 for counter EHR2	258
HR1Cnt5:BHR	10/11	N 16	0000 H	LSByte of 16-bit counter, discarded cells: (TxLpB11=0) with threshold	259
HR1Th52:BHRTh2	12	X 8	00000001	Threshold register Byte 2 (Least Significant Byte) for counter BHR	259
HR1Th51:BHRTh1	13	X 8	10000000	Threshold register Byte 1 for counter BHR	259
HR1RESET	30	R 1	1	Default RESET register	260
HR1Stat1	33	S 3		Status register 1 (event latch)	260
HR1Stat2	34	S 5		Status register 2 (static)	260
HR1MainIRQ	38	I 3		MAIN INTerrupt register	261
HR1M_MainIRQ	39	X 3	0xxxxx00	INT MASK register (for HR1MainIRQ)	261
HR1CntIRQ1	3A	I 8		COUNTER INTerrupt register	261
HR1M_CntIRQ1	3B	X 8	00000000	INT MASK register (for HRCntIRQ1)	261
HR1Conf1	48	C 2	11	Chiplet configuration register 1	262
HR1Conf2	49	C 8	00000000	Chiplet configuration register 2	262
HR1Conf3	4A	C 8	01110110	Chiplet configuration register (Alpha/Delta)	263
HR1Conf4:ICU1	4B	C 8	00000000	Configuration bytes to identify idle or unassigned cells	263
HR1Conf5:ICU2	4C	C 8	00000000	Configuration bytes to identify idle or unassigned cells	263

Table 150. ACH_Rx1 Chiplet Address Mapping (Continued)

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
HR1Conf6:ICU3	4D	C 8	00000000	Configuration bytes to identify idle or unassigned cells	263
HR1Conf7:ICU4	4E	C 8	00000001	Configuration bytes to identify idle or unassigned cells	263
HR1Conf8:MODU	4F	C 8	01010101	HEC modulo pattern	263
HR1Conf9:PL	50	C 8	11010000	Dummy byte to align Payload in ACB_Rx1 (i.e., UDF2)	263
HR1Conf10:PAFT	51	C 7	1100000	ACB buffer Almost Full Threshold	264
HR1Conf11	52	C 5	11111	APS select matrix (receive direction)	265
HR1Conf12	53	C 4	0000	APS parity handling (receive direction)	266

ACH_Rx1 (HR1) Counters

HR1ROFmid, HR1ROFhi: Read-on-the-fly registers.

Table 151. HR1ROFmid, HR1ROFhi [1100 H, 1101 H]

Signal Name	Bit Pos.	Access	Default	Description
HR1ROFmid(7:0)	7:0	R	00000000	Read-on-the-fly register (Middle Significant Byte)
HR1ROFhi(7:0)	7:0	R	00000000	Read-on-the-fly register (Most Significant Byte)

HR1Cnt1:FHR: ATM Mode: Number of ATM cells received from RX SFH1 when the ACH chiplet's cell delineation logic is in the Sync state. Counter overflow leads to an interrupt request. PPP Mode: Number of HDLC-like Frames received from RX SFH1; a received EOF (End of Frame) causes the counter to increment. Counter overflow leads to an interrupt request.

Table 152. HR1Cnt1:FHR [1104 H / 1105 H]

Signal Name	Bit Pos.	Access	Default	Description
FHR(7:0)	7:0	R	00000000	ATM cell or HDLC-like Frame counter, Least Significant Byte

HR1Cnt2:IHR: Number of Idle cells received from RX SFH1. Counter overflow leads to an interrupt request.

Table 153: HR1Cnt2:IHR [1106 H / 1107 H]

Signal Name	Bit Pos.	Access	Default	Description
IHR(7:0)	7:0	R	00000000	Idle cell counter, Least Significant Byte

HR1Cnt3:EHR1: Number of uncorrected HEC errors. Counter overflow leads to an interrupt request.

HR1Th31:EHR1T1: Threshold for number of uncorrected HEC errors (Most Significant Byte).

HR1Th32:EHR1T2: Threshold for number of uncorrected HEC errors (Least Significant Byte).

Threshold equaled leads to an interrupt request.

Table 154: HR1Cnt3:EHR1, HR1Th31:EHR1T1, HR1Th32:EHR1T2 [1108 H / 1109 H, 110B H, 110A H]

Signal Name	Bit Pos.	Access	Default	Description
EHR1(7:0)	7:0	R	00000000	Uncorrected HEC error counter, Least Significant Byte
EHR1T1(7:0)	7:0	R/W	10000000	Threshold for uncorrected HEC error counter (Most Significant Byte)
EHR1T2(7:0)	7:0	R/W	00000001	Threshold for uncorrected HEC error count (Least Significant Byte)

HR1Cnt4:EHR2: Number of corrected HEC errors. Counter overflow leads to an interrupt request.

HR1Th41:EHR2T1: Threshold for number of corrected HEC errors (Most Significant Byte).

HR1Th42:EHR2T2: Threshold for number of corrected HEC errors (Least Significant Byte).

Threshold equaled leads to an interrupt request.

Table 155: HR1Cnt4:EHR2, HR1Th41:EHR2T1, HR1Th42:EHR2T2 [110C H / 110D H, 110F H, 110E H]

Signal Name	Bit Pos.	Access	Default	Description
EHR2(7:0)	7:0	R	00000000	Corrected HEC error counter, Least Significant Byte
EHR2T1(7:0)	7:0	R/W	10000000	Threshold for corrected HEC error count (Most Significant Byte)
EHR2T2(7:0)	7:0	R/W	00000001	Threshold for corrected HEC error count (Least Significant Byte)

HR1Cnt5:BHR: Number of discarded cells/chunks because of the ACB FIFO not being able to accept another complete cell/chunk due to the PAF threshold being exceeded. Counter overflow leads to an interrupt request.

HR1Th51:BHRTh1: Threshold for number of discarded cells (Most Significant Byte).

HR1Th52:BHRTh2: Threshold for number of discarded cells (Least Significant Byte). Threshold equaled leads to an interrupt request.

Table 156: HR1Cnt5:BHR, HR1Th51:BHRTh1, HR1Th52:BHRTh2 [1110 H / 1111 H, 1113 H, 1112 H]

Signal Name	Bit Pos.	Access	Default	Description
BHR(7:0)	7:0	R	00000000	Discarded cell counter, Least Significant Byte
BHRTh1(7:0)	7:0	R/W	10000000	Threshold for discarded cell counter (Most Significant Byte)
BHRTh2(7:0)	7:0	R/W	00000001	Threshold for discarded cell counter (Least Significant Byte)

HR1CntEn1: Counter On/Off control register for ACH_Rx1/ACB_Rx1.

For each bit position:

0: Counter is disabled

1: Counter is enabled

Table 157. HR1CntEn1 [1102 H]

Signal Name	Bit Pos.	Access	Default	Description
EN-FHR	0	R/W	0	ATM cell/HDLC-like Frame counter enable
EN-IHR	1	R/W	0	Idle cell counter enable
EN-EHR1	2	R/W	0	Uncorrected HEC error counter enable
EN-EHR2	3	R/W	0	Corrected HEC error counter enable
EN-BHR	4	R/W	0	Discarded cell counter enable
Reserved	7:5			Not used

ACH_Rx1 (HR1) Reset Register

HR1RESET: Reset chiplet control register. This register is automatically preset to the default value by the reset signal ResHR1 from the GPPINT.

For each bit position:

0: Reset not active

1: Reset active

Table 158. HR1RESET [1130 H]

Signal Name	Bit Pos.	Access	Default	Description
Reset	0	R/W	1	Reset (disable) ACH_Rx1 chiplet
Reserved	7:1			Not used

ACH_Rx1 Status Registers

HR1Stat1: Status register 1 of this chiplet. The bits of this register are event latches.

Table 159. HR1Stat1 [1133 H]

Signal Name	Bit Pos.	Access	Default	Description
APSParEr	0	R/W		0: no APS parity error was detected 1: at least one parity error was detected
SyncHunt	1	R/W		0: FSM still in Sync state 1: FSM returned from Sync to Hunt state (this bit is set only by the transition from Sync to Hunt state).
WrFlagFF	2	R/W		0: ACB FIFO did not raise the Full Flag 1: ACB FIFO did raise the Full Flag
Reserved	7:3			Not used

HR1Stat2: Status register 2 of this chiplet. The bits of this register are static latches that follow the driving signal immediately.

Table 160: HR1Stat2 [1134 H]

Signal Name	Bit Pos.	Access	Default	Description
CellDel(2:0)	2:0	R		State of the cell delineation process: 000: Reset state 001: Hunt state 010: Presync state 100: Sync state
WrFlagPAF	3	R		0: ACB FIFO is currently not almost full 1: ACB FIFO is currently almost full

Table 160: HR1Stat2 [1134 H] (Continued)

Signal Name	Bit Pos.	Access	Default	Description
RdFlagEF	4	R		0: SDB FIFO is currently not empty 1: SDB FIFO is currently empty
Reserved	7:5			Not used

ACH_Rx1 Interrupt Request and Mask Registers

HR1MainIRQ: Register to indicate fatal interrupt events and to point to user IRQ registers with active requests; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

HR1M_MainIRQ: Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates signal IRQHR1 to GPPINT

Table 161. HR1MainIRQ, HR1M_MainIRQ [1138 H, 1139 H]

Signal Name	Bit Pos.	Access	Default	Description
Fatal	0	R/W	0	Fatal event occurred
CntIRQ1	1	R/W	0	Active request in HR1CntIRQ1 register
LCD_defect	2	R/W	0	LCD defect. This bit becomes active when an Out of Cell Delineation (OCD) defect persists for 4 ms. The LCD defect terminates when the internal cell delineation state machine enters the Sync state for 4 continuous milliseconds.
Reserved	7:3			Not used

HR1CntIRQ1: Register to indicate active counter interrupt requests of this chiplet; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

HR1M_CntIRQ1: Register to mask pending counter interrupt requests; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in HR1MainIRQ register

Table 162. HR1CntIRQ1, HR1M_CntIRQ1 [113A H, 113B H]

Signal Name	Bit Pos.	Access	Default	Description
OV-FHR	0	R/W	0	Overflow ATM cell/HDLC-like Frame counter

Table 162. HR1CntIRQ1, HR1M_CntIRQ1 [113A H, 113B H] (Continued)

Signal Name	Bit Pos.	Access	Default	Description
OV-IHR	1	R/W	0	Overflow idle cell counter
OV-EHR1	2	R/W	0	Overflow Uncorrected HEC error counter
TH-EHR1	3	R/W	0	Threshold equaled Uncorrected HEC error counter
OV-EHR2	4	R/W	0	Overflow Corrected HEC error counter
TH-EHR2	5	R/W	0	Threshold equaled Corrected HEC error counter
OV-BHR	6	R/W	0	Overflow discarded cell counter
TH-BHR	7	R/W	0	Threshold equaled discarded cell counter

ACH_Rx1 Configuration Registers

HR1Conf1: register to control auto-resetting of bits upon read access.

Table 163. HR1Conf1 [1148 H]

Signal Name	Bit Pos.	Access	Default	Description
AutRst_Int	0	R/W	1	0: No action on read access 1: Auto-reset interrupt request registers upon read access. Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a 1 to that bit provided that the corresponding alarm condition is removed.
AutRst_Sta	1	R/W	1	0: No action on read access 1: Auto-reset all bits in the HR1Stat1 status register upon read access
Reserved	7:2			Not used

HR1Conf2: register to control the HEC correction modes of this chiplet.

Table 164. HR1Conf2 [1149 H]

Signal Name	Bit Pos.	Access	Default	Description
CorModeHi	0	R/W	0	0: FSM returns into detection mode after HEC error correction 1: FSM stays in correction mode until the Sync state is left
NCorHECEr	1	R/W	0	0: Single-bit HEC errors are corrected 1: Single-bit HEC errors are not corrected and the cell is not written into the ACB FIFO.
WrIdleC	2	R/W	0	0: Do not write Idle cell into ACB FIFO 1: write Idle cell into ACB FIFO

Table 164. HR1Conf2 [1149 H] (Continued)

Signal Name	Bit Pos.	Access	Default	Description
Ndescramb	3	R/W	0	0: Descramble ATM cell payload 1: do not descramble ATM cell payload
Reserved	4	R/W	0	Not Used.
Reserved	5	R/W	0	Not Used.
NWrToFifo	6	R/W	0	0: Write into ACB FIFO 1: Do not write into ACB FIFO; all received cells are discarded
DetStartOC	7	R/W	0	0: When TX Loopback stage 2 is enabled cell delineation is based on the looped back HEC. 1: When TX Loopback stage 2 is enabled cell delineation is based on the looped Start Of Cell Marker instead of the HEC. This mode is not valid for STM-4c/STS-12c modes.

HR1Conf3: register to control ATM cell synchronization in this chiplet.

Table 165. HR1Conf3 [114A H]

Signal Name	Bit Pos.	Access	Default	Description
Delta(3:0)	3:0	R/W	0110	Required number of consecutive good HECs detected to jump from PRESYNC to SYNC state
Alpha(3:0)	7:4	R/W	0111	Required number of consecutive false HECs detected to return from SYNC to HUNT state

HR1Conf4-7:ICU1/2/3/4: Header pattern to identify Idle/Unassigned cells. The PHAST-12E checks the first four header bytes of the RX cells and compares them to the values written to these registers. If a match is found and the WrIdleC bit in HR#Conf2 is set to a 0, then the cell is discarded.

HR1Conf8:MODU: Pattern to do last modulo operation in HEC (i.e., coset)

HR1Conf9:PL: Dummy byte to align the Payload in the ACB_Rx1 buffer (i.e., this is the UDF2 byte that is output on the RX 16-bit UTOPIA level 2 interface for ATM applications).

Table 166. HR1Conf4-7:ICU1/2/3/4, HR1Conf8:MODU, HR1Conf9:PL [114B H, 114C H, 114D H, 114E H, 114F H, 1150 H]

Signal Name	Bit Pos.	Access	Default	Description
ICU1(7:0)	7:0	R/W	00000000	Header byte 1
ICU2(7:0)	7:0	R/W	00000000	Header byte 2
ICU3(7:0)	7:0	R/W	00000000	Header byte 3
ICU4(7:0)	7:0	R/W	00000001	Header byte 4
MODU(7:0)	7:0	R/W	01010101	HEC modulo pattern (i.e., coset)
PL(7:0)	7:0	R/W	11010000	Payload alignment byte. This byte is the UDF2 byte that is output on the receive UTOPIA interface when a 16-bit wide data path is used.

HR1Conf10:PAFT: Threshold for Programmable Almost Full flag (ACB_Rx1)

Table 167. HR1Conf10:PAFT [1151 H]

Signal Name	Bit Pos.	Access	Default	Description
PAFT(6:0)	6:0	R/W	1100000	Threshold for PAF flag (ACB_Rx1). This register should be set according to mode as follows: ATM: STM-4c/STS-12c (set all four chiplets the same) 74 H STM-1/STS-3c/STM-4/STS-12 (set only the chiplets enabled to process ATM to this value) 60 H PPP: (set only the chiplets enabled to process PPP to this value; for STM-4c/STS-12c modes set all chiplets to the same value) 7B H
Reserved	7			Not used

HR1Conf11: APS select matrix for receive direction from SFH blocks or APS external input port towards an APH block. When any of the 0xxxx or 101xx bit settings are written, the signal from the indicated SFH block is bridged to the corresponding APH block or external APS interface. The 101xx settings are for 2 x 1+1 APS applications. However, the TX side of the PHAST-12E only supports 1 x 1+1 and 1:n APS.

Table 168: HR1Conf11 [1152 H]

Signal Name	Bit Pos.	Access	Default	Description
ApsSource(4:0)	4:0	R/W	11111	00000: APH 1: Source is SFH block 2 00001: APH 1: Source is SFH block 3 00010: APH 1: Source is SFH block 4 00011: APH 1: Source is APS external input port 00100: APH 2: Source is SFH block 1 00101: APH 2: Source is SFH block 3 00110: APH 2: Source is SFH block 4 00111: APH 2: Source is APS external input port 01000: APH 3: Source is SFH block 1 01001: APH 3: Source is SFH block 2 01010: APH 3: Source is SFH block 4 01011: APH 3: Source is APS external input port 01100: APH 4: Source is SFH block 1 01101: APH 4: Source is SFH block 2 01110: APH 4: Source is SFH block 3 01111: APH 4: Source is APS external input port 10000: APS out: Source is SFH block 1 10001: APS out: Source is SFH block 2 10010: APS out: Source is SFH block 3 10011: APS out: Source is SFH block 4 10100: APH 1: Source is SFH block 2 APH 2: not bridged, not used APH 3: Source is SFH block 4 APH 4: not bridged, not used 10101: APH 1: not bridged, not used APH 2: Source is SFH block 1 APH 3: Source is SFH block 4 APH 4: not bridged, not used 10110: APH 1: Source is SFH block 2 APH 2: not bridged, not used APH 3: not bridged, not used APH 4: Source is SFH block 3 10111: APH 1: not bridged, not used APH 2: Source is SFH block 1 APH 3: not bridged, not used APH 4: Source is SFH block 3 11xxx: No APS is activated, select blocks 1:1 (transparent) Note: Not bridged means that the APH# is still getting data from its corresponding SFH#. Not used refers to the fact that this particular block is not used.
Reserved	7:5			Not used

HR1Conf12: Controls APS parity handling (receive direction).

Table 169. HR1Conf12 [1153 H]

Signal Name	Bit Pos.	Access	Default	Description
ApsOPaEn	0	R/W	0	APS external output parity control: 0: Parity generation disabled 1: Parity generation enabled
ApsOPaOdd	1	R/W	0	APS external output parity: 0: Even parity 1: Odd parity
ApsIPaEn	2	R/W	0	APS external input parity control: 0: Parity checking disabled 1: Parity checking enabled
ApsIPaOdd	3	R/W	0	APS external input parity: 0: Even parity 1: Odd parity
Reserved	7:4	R/W		Not used

ACH_RX2/3/4 CHIPLET ADDRESS MAPPING

Chiplet Base Address:

ACH_Rx2 1200 H.

ACH_Rx3 1300 H.

ACH_Rx4 1400 H.

The other three ATM handlers in the receive direction are grouped together in the following tables (# = 2,3,4).

Table 170. ACH_Rx2/3/4 Chiplet Address Mapping

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
HR#ROFmid	0	F 8	00000000	Read-on-the-fly register (Middle Significant Byte)	268
HR#ROFhi	1	F 8	00000000	Read-on-the-fly register (Most Significant Byte)	268
HR#CntEn1	2	X 5	00000	COUNT ENABLE register	270
HR#Cnt1:FHR	4/5	N 24	000000 H	LSByte of 24-bit counter, ATM cells or HDLC-like Frames received from RX SFH#, no threshold	268
HR#Cnt2:IHR	6/7	N 24	000000 H	LSByte of 24-bit counter, received Idle cells from RX SFH#, no threshold	268
HR#Cnt3:EHR1	8/9	N 16	0000 H	LSByte of 16-bit counter, uncorrected HEC errors with threshold	269

Table 170. ACH_Rx2/3/4 Chiplet Address Mapping (Continued)

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
HR#Th32:EHR1T2	A	X 8	00000001	Threshold register Byte2 (Least Significant Byte) for counter EHR1	269
HR#Th31:EHR1T1	B	X 8	10000000	Threshold register Byte1 for counter EHR1	269
HR#Cnt4:EHR2	C/D	N 16	0000 H	LSByte of 16-bit counter, corrected HEC errors with threshold	269
HR#Th42:EHR2T2	E	X 8	00000001	Threshold register Byte2 (Least Significant Byte) for counter EHR2	269
HR#Th41:EHR2T1	F	X 8	10000000	Threshold register Byte1 for counter EHR2	269
HR#Cnt5:BHR	10/11	N 16	0000 H	LSByte of 16-bit counter, discarded cells: (TxLpB11=0) with threshold	270
HR#Th52:BHRTh2	12	X 8	00000001	Threshold register Byte2 (Least Significant Byte) for counter BHR	270
HR#Th51:BHRTh1	13	X 8	10000000	Threshold register Byte1 for counter BHR	270
HR#RESET	30	R 1	1	Default RESET register	271
HR#Stat1	33	S 2		Status register 1 (event latch)	271
HR#Stat2	34	S 5		Status register 2 (static)	271
HR#MainIRQ	38	I 3		MAIN INTerrupt register	272
HR#M_MainIRQ	39	X 3	0xxxxx00	INT MASK register (for MainIRQ)	272
HR#CntIRQ1	3A	I 8		COUNTER INTerrupt register	272
HR#M_CntIRQ1	3B	X 8	00000000	INT MASK register (for HR#CntIRQ1)	272
HR#Conf1	48	C 2	11	Chiplet configuration register 1	273
HR#Conf2	49	C 8	00000000	Chiplet configuration register 2	273
HR#Conf3	4A	C 8	01110110	Chiplet configuration register (Alpha/Delta)	274
HR#Conf4:ICU1	4B	C 8	00000000	Configuration bytes to identify idle or unassigned cells	274
HR#Conf5:ICU2	4C	C 8	00000000	Configuration bytes to identify idle or unassigned cells	274
HR#Conf6:ICU3	4D	C 8	00000000	Configuration bytes to identify idle or unassigned cells	274
HR#Conf7:ICU4	4E	C 8	00000001	Configuration bytes to identify idle or unassigned cells	274
HR#Conf8:MODU	4F	C 8	01010101	HEC modulo pattern (i.e., coset)	274
HR#Conf9:PL	50	C 8	11010000	Dummy byte to align Payload in ACB_Rx2/3/4 (i.e., UDF2)	274
HR#Conf10:PAFT	51	C 7	1100000	ACB buffer Almost Full Threshold	275

ACH_Rx2/3/4 (HR2/3/4) Counters

HR#ROFmid, HR#ROFhi: Read-on-the-fly registers.

Table 171. HR#ROFmid, HR#ROFhi [1200 H, 1300 H, 1400 H, 1201 H, 1301 H, 1401 H]

Signal Name	Bit Pos.	Access	Default	Description
HR#ROFmid(7:0)	7:0	R	00000000	Read-on-the-fly register (Middle Significant Byte)
HR#ROFhi(7:0)	7:0	R	00000000	Read-on-the-fly register (Most Significant Byte)

HR#Cnt1:FHR: ATM Mode: Number of ATM cells received from RX SFH# when the ACH chiplet's cell delineation logic is in the Sync state. Counter overflow leads to an interrupt request. PPP Mode: Number of HDLC-like Frames received from RX SFH#; a received EOF (End of Frame) causes the counter to increment. Counter overflow leads to an interrupt request.

Table 172. HR#Cnt1:FHR [1204 H / 1205 H, 1304 H / 1305 H, 1404 H / 1405 H]

Signal Name	Bit Pos.	Access	Default	Description
FHR(7:0)	7:0	R	00000000	ATM cell counter or HDLC-like Frame counter, Least Significant Byte

HR#Cnt2:IHR: Number of Idle cells received from RX SFH#. Counter overflow leads to an interrupt request.

Table 173. HR#Cnt2:IHR [1206 H / 1207 H, 1306 H / 1307 H, 1406 H / 1407 H]

Signal Name	Bit Pos.	Access	Default	Description
IHR(7:0)	7:0	R	00000000	Idle cell counter, Least Significant Byte

HR#Cnt3:EHR1: Number of uncorrected HEC errors. Counter overflow leads to an interrupt request.

HR#Th31:EHR1T1: Threshold for number of uncorrected HEC errors (Most Significant Byte).

HR#Th32:EHR1T2: Threshold for number of uncorrected HEC errors (Least Significant Byte).

Threshold equaled leads to an interrupt request.

Table 174. HR#Cnt3:EHR1, HR#Th31:EHR1T1, HR#Th32:EHR1T2 [1208 H / 1209 H, 1308 H / 1309 H, 1408 H / 1409 H, 120B H, 130B H, 140B H, 120A H, 130A H, 140A H]

Signal Name	Bit Pos.	Access	Default	Description
EHR1(7:0)	7:0	R	00000000	Uncorrected HEC error counter, Least Significant Byte
EHR1T1(7:0)	7:0	R/W	10000000	Threshold for uncorrected HEC error counter (Most Significant Byte)
EHR1T2(7:0)	7:0	R/W	00000001	Threshold for uncorrected HEC error counter (Least Significant Byte)

HR#Cnt4:EHR2: Number of corrected HEC errors. Counter overflow leads to an interrupt request.

HR#Th41:EHR2T1: Threshold for number of corrected HEC errors (Most Significant Byte).

HR#Th42:EHR2T2: Threshold for number of corrected HEC errors (Least Significant Byte).

Threshold equaled leads to an interrupt request.

Table 175. HR#Cnt4:EHR2, HR#Th41:EHR2T1, HR#Th42:EHR2T2 [120C H / 120D H, 130C H / 130D H, 140C H / 140D H, 120F H, 130F H, 140F H, 120E H, 130E H, 140E H]

Signal Name	Bit Pos.	Access	Default	Description
EHR2(7:0)	7:0	R	00000000	Corrected HEC error counter, Least Significant Byte
EHR2T1(7:0)	7:0	R/W	10000000	Threshold for corrected HEC error counter (Most Significant Byte)
EHR2T2(7:0)	7:0	R/W	00000001	Threshold for corrected HEC error counter (Least Significant Byte)

HR#Cnt5:BHR: Number of discarded cells/chunks because of the ACB FIFO not being able to accept another complete cell/chunk due to the PAF threshold being exceeded. Counter overflow leads to an interrupt request.

HR#Th51:BHRTh1: Threshold for number of discarded cells (Most Significant Byte).

HR#Th52:BHRTh2: Threshold for number of discarded cells (Least Significant Byte).

Threshold equaled leads to an interrupt request.

Table 176. HR#Cnt5:BHR, HR#Th51:BHRTh1, HR#Th52:BHRTh2 [1210 H / 1211 H, 1310 H / 1311 H, 1410 H / 1411 H, 1213 H, 1313 H, 1413 H, 1212 H, 1312 H, 1412 H]

Signal Name	Bit Pos.	Access	Default	Description
BHR(7:0)	7:0	R	00000000	Discarded cell counter, Least Significant Byte
BHRTh1(7:0)	7:0	R/W	10000000	Threshold for discarded cell count (Most Significant Byte)
BHRTh2(7:0)	7:0	R/W	00000001	Threshold for discarded cell counter (Least Significant Byte)

HR#CntEn1: Counter On/Off control register for ACH_Rx2/3/4 and ACB_Rx2/3/4.

For each bit position:

0: Counter is disabled

1: Counter is enabled

Table 177. HR#CntEn1 [1202 H, 1302 H, 1402 H]

Signal Name	Bit Pos.	Access	Default	Description
EN-FHR	0	R/W	0	ATM cell/HDLC-like Frame counter enable
EN-IHR	1	R/W	0	Idle cell counter enable
EN-EHR1	2	R/W	0	Uncorrected HEC error counter enable
EN-EHR2	3	R/W	0	Corrected HEC error counter enable
EN-BHR	4	R/W	0	Discarded cell counter enable
Reserved	7:5			Not used

ACH_Rx2/3/4 (HR2/3/4) Reset Registers

HR#RESET: Reset chiplet control registers. These registers are automatically preset to the default value by the reset signals ResHR2/3/4 from the GPPINT.

For each bit position:

0: Reset not active

1: Reset active

Table 178. HR#RESET [1230 H, 1330 H, 1430 H]

Signal Name	Bit Pos.	Access	Default	Description
Reset	0	R/W	1	Reset (disable) ACH_Rx2/3/4 chiplet
Reserved	7:1			Not used

ACH_Rx2/3/4 Status Registers

HR#Stat1: Status register 1 of this chiplet. The bits of this register are event latches.

Table 179. HR#Stat1 [1233 H, 1333 H, 1433 H]

Signal Name	Bit Pos.	Access	Default	Description
SyncHunt	0	R/W		0: FSM still in Sync state 1: FSM returned from Sync to Hunt state (this bit is set only by the transition from Sync to Hunt state).
WrFlagFF	1	R/W		0: ACB FIFO did not raise the Full Flag 1: ACB FIFO did raise the Full Flag
Reserved	7:2			Not used

HR#Stat2: Status register 2 of this chiplet. The bits of this register are static latches that follow the driving signal immediately.

Table 180. HR#Stat2 [1234 H, 1334 H, 1434 H]

Signal Name	Bit Pos.	Access	Default	Description
CellDel(2:0)	2:0	R		State of the cell delineation process: 000: Reset state 001: Hunt state 010: Presync state 100: Sync state.
WrFlagPAF	3	R		0: ACB FIFO is currently not almost full 1: ACB FIFO is currently almost full
RdFlagEF	4	R		0: SDB FIFO is currently not empty 1: SDB FIFO is currently empty
Reserved	7:5			Not used

ACH_Rx2/3/4 Interrupt Request and Mask Registers

HR#MainIRQ: Register to indicate fatal interrupt events and to point to user IRQ registers with active requests; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

HR#M_MainIRQ: Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates signal IRQHR2/3/4 to GPPINT

Table 181. HR#MainIRQ, HR#M_MainIRQ [1238 H, 1338 H, 1438 H, 1239 H, 1339 H, 1439 H]

Signal Name	Bit Pos.	Access	Default	Description
Fatal	0	R/W	0	Fatal event occurred
CntIRQ1	1	R/W	0	Active request in HR#CntIRQ1 register
LCD_defect	2	R/W	0	LCD defect. This bit becomes active when an Out of Cell Delineation (OCD) defect persists for 4 ms. The LCD defect terminates when the internal cell delineation state machine enters the Sync state for 4 continuous milliseconds.
Reserved	7:3			Not used

HR#CntIRQ1: Register to indicate active counter interrupt requests of this chiplet; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

HR#M_CntIRQ1: Register to mask pending counter interrupt requests; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in HR#MainIRQ register.

Table 182. HR#CntIRQ1, HR#M_CntIRQ1 [123A H, 133A H, 143A H, 123B H, 133B H, 143B H]

Signal Name	Bit Pos.	Access	Default	Description
OV-FHR	0	R/W	0	Overflow ATM cell/HDLC-like Frame counter
OV-IHR	1	R/W	0	Overflow idle cell counter
OV-EHR1	2	R/W	0	Overflow Uncorrected HEC error counter
TH-EHR1	3	R/W	0	Threshold equaled Uncorrected HEC error counter
OV-EHR2	4	R/W	0	Overflow Corrected HEC error counter
TH-EHR2	5	R/W	0	Threshold Corrected HEC error counter
OV-BHR	6	R/W	0	Overflow discarded cell counter
TH-BHR	7	R/W	0	Threshold equaled discarded cell counter

ACH_Rx2/3/4 Configuration Registers

HR#Conf1: register to control auto-resetting of bits upon read access.

Table 183. HR#Conf1 [1248 H, 1348 H, 1448 H]

Signal Name	Bit Pos.	Access	Default	Description
AutRst_Int	0	R/W	1	0: No action on read access 1: Auto-reset interrupt request registers upon read access. Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a 1 to that bit provided that the corresponding alarm condition is removed.
AutRst_Sta	1	R/W	1	0: No action on read access 1: Auto-reset all bits in the HR#Stat1 status register upon read access
Reserved	7:2			Not used

HR#Conf2: register to control the HEC correction modes of this chiplet.

Table 184. HR#Conf2 [1249 H, 1349 H, 1449 H]

Signal Name	Bit Pos.	Access	Default	Description
CorModeHi	0	R/W	0	0: FSM returns into detection mode after HEC error correction 1: FSM stays in correction mode until the Sync state is left
NCorHECEr	1	R/W	0	0: Single-bit HEC errors are corrected 1: Single-bit HEC errors are not corrected
WrIdleC	2	R/W	0	0: Do not write Idle cell into ACB FIFO 1: Write Idle cell into ACB FIFO
Ndescramb	3	R/W	0	0: Descramble ATM cell payload 1: Do not descramble ATM cell payload
Reserved	4	R/W	0	Not Used.
Reserved	5	R/W	0	Not Used.
NWrToFifo	6	R/W	0	0: Write into ACB FIFO 1: Do not write into ACB FIFO; all received cells are discarded
DetStartOC	7	R/W	0	0: When TX Loopback stage 2 is enabled cell delineation is based on the looped back HEC. 1: When TX Loopback stage 2 is enabled cell delineation is based on the looped Start Of Cell Marker instead of the HEC. This mode is not valid for STM-4c/STS-12c modes.

HR#Conf3: register to control ATM cell synchronization in this chiplet.

Table 185. HR#Conf3 [124A H, 134A H, 144A H]

Signal Name	Bit Pos.	Access	Default	Description
Delta(3:0)	3:0	R/W	0110	Required number of consecutive good HECs detected to jump from PRESYNC to SYNC state
Alpha(3:0)	7:4	R/W	0111	Required number of consecutive false HECs detected to return from SYNC to HUNT state

HR#Conf4-7:ICU1/2/3/4: Header pattern to identify Idle/Unassigned cells. The PHAST-12E checks the first four header bytes of the RX cells and compares them to the values written to these registers. If a match is found and the WrIdleC bit in HR#Conf2 is set to a 0, then the cell is discarded.

HR#Conf8:MODU: Pattern to do last modulo operation in HEC (i.e., coset)

HR#Conf9:PL: Dummy byte to align the Payload in the ACB_Rx2/3/4 buffer. (i.e., this is the UDF2 byte that is output on the RX 16-bit UTOPIA level 2 interface for ATM applications)

Table 186. HR#Conf4-7:ICU1/2/3/4, HR#Conf8:MODU, HR#Conf9:PL [124B H, 134B H, 144B H, 124C H, 134C H, 144C H, 124D H, 134D H, 144D H, 124E H, 134E H, 144E H, 124F H, 134F H, 144F H, 1250 H, 1350 H, 1450 H]

Signal Name	Bit Pos.	Access	Default	Description
ICU1(7:0)	7:0	R/W	00000000	Header byte 1
ICU2(7:0)	7:0	R/W	00000000	Header byte 2
ICU3(7:0)	7:0	R/W	00000000	Header byte 3
ICU4(7:0)	7:0	R/W	00000001	Header byte 4
MODU(7:0)	7:0	R/W	01010101	HEC modulo pattern. This is also known as the coset pattern. Setting this register to 00 H disables the coset operation in the receive direction.
PL(7:0)	7:0	R/W	11010000	Payload alignment byte

HR#Conf10:PAFT: Threshold for Programmable Almost Full flag (ACB_Rx2/3/4)

Table 187. HR#Conf10:PAFT [1251 H, 1351 H, 1451 H]

Signal Name	Bit Pos.	Access	Default	Description
PAFT(6:0)	6:0	R/W	1100000	Threshold for PAF flag, ACB_Rx2/3/4. These registers should be set according to mode as follows: ATM: STM-4c/STS-12c (set all four chiplets the same) 74 H STM-1/STS-3c/STM-4/STS-12 (set only the chiplets enabled to process ATM to this value) 60 H PPP: (set only the chiplets enabled to process PPP to this value; for STM-4c/STS-12c modes set all chiplets to the same value) 7B H.
Reserved	7			Not used

PPP CHIPLET ADDRESS MAPPING

Chiplet Base Address:

PPP 1500 H.

Table 188. PPP Chiplet Address Mapping

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
PPPCntEn1	2	X 6	000000	COUNT ENABLE register 1	278
PPPCntEn2	3	X 6	000000	COUNT ENABLE register 2	278
PPPCnt1:FCSE1	4/5	N 8	00000000	FCS (Frame Check Sequence) error/ABORT counter PPP chiplet 1, no threshold	277
PPPCnt2:MFLE1	6/7	N 8	00000000	MFLE (Maximum Frame Length Exceeded) event counter PPP chiplet 1, no threshold	277
PPPCnt3:BMFL1	8/9	N 8	00000000	BMFL (Below Minimum Frame Length) event counter PPP chiplet 1, no threshold	277
PPPCnt4:FCSE2	A/B	N 8	00000000	FCS error/ABORT counter PPP chiplet 2, no threshold	277
PPPCnt5:MFLE2	C/D	N 8	00000000	MFLE event counter PPP chiplet 2, no threshold	277

Table 188. PPP Chiplet Address Mapping (Continued)

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
PPPCnt6:BMFL2	E/F	N 8	00000000	BMFL event counter PPP chiplet 2, no threshold	277
PPPCnt7:FCSE3	10/11	N 8	00000000	FCS error/ABORT counter PPP chiplet 3, no threshold	277
PPPCnt8:MFLE3	12/13	N 8	00000000	MFLE event counter PPP chiplet 3, no threshold	277
PPPCnt9:BMFL3	14/15	N 8	00000000	BMFL event counter PPP chiplet 3, no threshold	277
PPPCnt10:FCSE4	16/17	N 8	00000000	FCS error/ABORT counter PPP chiplet 4, no threshold	277
PPPCnt11:MFLE4	18/19	N 8	00000000	MFLE event counter PPP chiplet 4, no threshold	277
PPPCnt12:BMFL4	1A/1B	N 8	00000000	BMFL event counter PPP chiplet 4, no threshold	277
PPPRESET	30	R 1	1	Default RESET register (PPP_Tx and PPP_Rx)	279
PPPMainIRQ	38	I 5		MAIN INTerrupt register	279
PPPM_MainIRQ	39	X 5	00000	INT MASK register (for PPPMainIRQ)	279
PPPCntIRQ1	3A	I 6		COUNTER INTerrupt register 1	280
PPPM_CntIRQ1	3B	X 6	000000	INT MASK register (for PPPCntIRQ1)	280
PPPCntIRQ2	3C	I 6		COUNTER INTerrupt register 2	280
PPPM_CntIRQ2	3D	X 6	000000	INT MASK register (for PPPCntIRQ2)	280
PPPIRQ1	3E	I 8		USER INTerrupt register 1	281
PPPM_IRQ1	3F	X 8	00000000	INT MASK register (for IRQ1)	281
PPPIRQ2	40	I 8		USER INTerrupt register 2	282
PPPM_IRQ2	41	X 8	00000000	INT MASK register (for IRQ2)	282
PPPConf1	48	C 2	11	Chiplet configuration register 1 (general A)	283
PPPConf2	49	C 4	0000	Configuration register 2 (general B)	283
PPPConf3	4A	C 8	00000000	Configuration register 3 (minimum frame length)	284
PPPConf4	4B	C 8	11111111	Configuration register 4 (maximum frame length, LSByte)	284
PPPConf5	4C	C 8	11111111	Configuration register 5 (maximum frame length, MSByte)	284
PPPConf6	4D	C 8	00000000	Configuration register 6 (PPP control)	285
PPPConf7	4E	C 8	00000000	Configuration register 7 (PPP control)	286
PPPConf8	4F	C 8	00000000	Configuration register 8 (PPP control)	

PPP Counters

In addition to the counters listed below, the HR#Cnt1:FHR counters in the ACH chiplets will count the number of HDLC-like Frames that have been received. The FCS error/Abort counters only count errored FCS blocks and the number of times that a 7D7E H has been received.

PPPCnt1..3:FCSE1/MFLE1/BMFL1: Counters for PPP chiplet 1. Counter overflow leads to an interrupt request.

Table 189. PPPCnt1..3:FCSE1/MFLE1/BMFL1 [1504 H / 1505 H, 1506 H / 1507 H, 1508 H / 1509 H]

Signal Name	Bit Pos.	Access	Default	Description
FCSE1(7:0)	7:0	R	00000000	FCS error/Abort counter, PPP chiplet 1
MFLE1(7:0)	7:0	R	00000000	MFLE event counter, PPP chiplet 1
BMFL1(7:0)	7:0	R	00000000	BMFL event counter, PPP chiplet 1

PPPCnt4..6:FCSE2/MFLE2/BMFL2: Counters for PPP chiplet 2. Counter overflow leads to an interrupt request.

Table 190. PPPCnt4..6:FCSE2/MFLE2/BMFL2 [150A H / 150B H, 150C H / 150D H, 150E H / 150F H]

Signal Name	Bit Pos.	Access	Default	Description
FCSE2(7:0)	7:0	R	00000000	FCS error/Abort counter, PPP chiplet 2
MFLE2(7:0)	7:0	R	00000000	MFLE event counter, PPP chiplet 2
BMFL2(7:0)	7:0	R	00000000	BMFL event counter, PPP chiplet 2

PPPCnt7..9:FCSE3/MFLE3/BMFL3: Counters for PPP chiplet 3. Counter overflow leads to an interrupt request.

Table 191: PPPCnt7..9:FCS3/MFLE3/BMFL3 [1510 H / 1511 H, 1512 H / 1513 H, 1514 H / 1515 H]

Signal Name	Bit Pos.	Access	Default	Description
FCSE3(7:0)	7:0	R	00000000	FCS error/Abort counter, PPP chiplet 3
MFLE3(7:0)	7:0	R	00000000	MFLE event counter, PPP chiplet 3
BMFL3(7:0)	7:0	R	00000000	BMFL event counter, PPP chiplet 3

PPPCnt10..12:FCSE4/MFLE4/BMFL4: Counters for PPP chiplet 4. Counter overflow leads to an interrupt request.

Table 192. PPPCnt10..12:FCSE4/MFLE4/BMFL4 [1516 H / 1517 H, 1518 H / 1519 H, 151A H / 151B H]

Signal Name	Bit Pos.	Access	Default	Description
FCSE4(7:0)	7:0	R	00000000	FCS error/Abort counter, PPP chiplet 4
MFLE4(7:0)	7:0	R	00000000	MFLE event counter, PPP chiplet 4
BMFL4(7:0)	7:0	R	00000000	BMFL event counter, PPP chiplet 4

PPPCntEn1: Counter On/Off control register 1 for PPP.

For each bit position:

0: Counter is disabled

1: Counter is enabled

Table 193. PPPCntEn1 [1502 H]

Signal Name	Bit Pos.	Access	Default	Description
EN-BMFL2	0	R/W	0	BMFL event counter PPP chiplet 2 enable
EN-MFLE2	1	R/W	0	MFLE event counter PPP chiplet 2 enable
EN-FCSE2	2	R/W	0	FCS error/Abort counter PPP chiplet 2 enable
EN-BMFL1	3	R/W	0	BMFL event counter PPP chiplet 1 enable
EN-MFLE1	4	R/W	0	MFLE event counter PPP chiplet 1 enable
EN-FCSE1	5	R/W	0	FCS error/Abort counter PPP chiplet 1 enable
Reserved	7:6			Not used

PPPCntEn2: Counter On/Off control register 2 for PPP.

For each bit position:

0: Counter is disabled

1: Counter is enabled

Table 194. PPPCntEn2 [1503 H]

Signal Name	Bit Pos.	Access	Default	Description
EN-BMFL4	0	R/W	0	BMFL event counter PPP chiplet 4 enable
EN-MFLE4	1	R/W	0	MFLE event counter PPP chiplet 4 enable
EN-FCSE4	2	R/W	0	FCS error/Abort counter PPP chiplet 4 enable
EN-BMFL3	3	R/W	0	BMFL event counter PPP chiplet 3 enable
EN-MFLE3	4	R/W	0	MFLE event counter PPP chiplet 3 enable
EN-FCSE3	5	R/W	0	FCS error/Abort counter PPP chiplet 3 enable
Reserved	7:6			Not used

PPP Reset Register

PPPRESET: Reset chiplet control register. This register is automatically preset to the default value by the reset signal ResPPP from the GPPINT.

For each bit position:

0: Reset not active

1: Reset active

Table 195. PPPRESET [1530 H]

Signal Name	Bit Pos.	Access	Default	Description
Reset	0	R/W	1	Reset (disable) PPP_Tx and PPP_Rx chiplets. 1: Disables the receive and transmit PPP chiplets. Flags (7E H) are transmitted in the transmit direction if transparent mode is turned off in the transmit direction else all 1s are transmitted. 0: Enables the receive and transmit PPP chiplets. If transparent mode is not enabled then the PHAST-12E looks for a flag followed by a non-flag before writing data into the receive ACB FIFO. Also it waits for a TXSOFI indication before it starts transmitting data; until then flag characters (7E H) are transmitted. If transparent mode is enabled, receive and transmit data are transferred immediately.
Reserved	7:1			Not used

PPP Interrupt Request and Mask Registers

PPPMainIRQ: Register to indicate fatal interrupt events and to point to user IRQ registers with active requests; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

PPPM_MainIRQ: Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates signal IRQPPP to GPPINT

Table 196. PPPMainIRQ, PPPM_MainIRQ [1538 H, 1539 H]

Signal Name	Bit Pos.	Access	Default	Description
Fatal	0	R/W	0	Fatal event occurred
CntIRQ1	1	R/W	0	Active request in PPPCntIRQ1 register
CntIRQ2	2	R/W	0	Active request in PPPCntIRQ2 register
IRQ1	3	R/W	0	Active request in IRQ1 register
IRQ2	4	R/W	0	Active request in IRQ2 register
Reserved	7:5			Not used

PPPCntIRQ1: Register 1 to indicate active counter interrupt requests of this chiplet; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

PPPM_CntIRQ1: Register 1 to mask pending counter interrupt requests; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in PPPMainIRQ register

Table 197. PPPCntIRQ1, PPPM_CntIRQ1 [153A H, 153B H]

Signal Name	Bit Pos.	Access	Default	Description
OV-BMFL2	0	R/W	0	Overflow BMFL event counter PPP chiplet 2
OV-MFLE2	1	R/W	0	Overflow MFLE event counter PPP chiplet 2
OV-FCSE2	2	R/W	0	Overflow FCS error/Abort counter PPP chiplet 2
OV-BMFL1	3	R/W	0	Overflow BMFL event counter PPP chiplet 1
OV-MFLE1	4	R/W	0	Overflow MFLE event counter PPP chiplet 1
OV-FCSE1	5	R/W	0	Overflow FCS error/Abort counter PPP chiplet 1
Reserved	7:6			Not used

PPPCntIRQ2: Register 2 to indicate active counter interrupt requests of this chiplet; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

PPPM_CntIRQ2: Register 2 to mask pending counter interrupt requests; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in PPPMainIRQ register

Table 198. PPPCntIRQ2, PPPM_CntIRQ2 [153C H, 153D H]

Signal Name	Bit Pos.	Access	Default	Description
OV-BMFL4	0	R/W	0	Overflow BMFL event counter PPP chiplet 4
OV-MFLE4	1	R/W	0	Overflow MFLE event counter PPP chiplet 4
OV-FCSE4	2	R/W	0	Overflow FCS error/Abort counter PPP chiplet 4
OV-BMFL3	3	R/W	0	Overflow BMFL event counter PPP chiplet 3
OV-MFLE3	4	R/W	0	Overflow MFLE event counter PPP chiplet 3
OV-FCSE3	5	R/W	0	Overflow FCS error/Abort counter PPP chiplet 3
Reserved	7:6			Not used

PPPIRQ1: Register 1 to indicate active user interrupt requests of this chiplet; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

PPPM_IRQ1: Register 1 to mask pending user interrupt requests; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in PPPMainIRQ register

Table 199. PPPIRQ1, PPPM_IRQ1 [153E H, 153F H]

Signal Name	Bit Pos.	Access	Default	Description
ABT2	0	R/W	0	Abort character (7D7E H) detected in RX PPP chiplet 2
BMFL2	1	R/W	0	Below minimum frame length, RX PPP chiplet 2. This bit is set when a packet is received that is shorter than the size set in MINFL(6:0).
MFLE2	2	R/W	0	Maximum frame length exceeded in RX PPP chiplet 2. This bit is set when a packet is received that is longer than or equal to the size set in the MAXFL(15:0) bits.
FCS2	3	R/W	0	Received bad frame in RX PPP chiplet 2. This bit is set when an FCS error is detected in the received packet.
ABT1	4	R/W	0	Abort character (7D7E H) detected in RX PPP chiplet 1
BMFL1	5	R/W	0	Below minimum frame length, RX PPP chiplet 1. This bit is set when a packet is received that is shorter than the size set in MINFL(6:0).
MFLE1	6	R/W	0	Maximum frame length exceeded in RX PPP chiplet 1. This bit is set when a packet is received that is longer than or equal to the size set in the MAXFL(15:0) bits.
FCS1	7	R/W	0	Received bad frame in RX PPP chiplet 1. This bit is set when an FCS error is detected in the received packet.

PPPIRQ2: Register 2 to indicate active user interrupt requests of this chiplet; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

PPPM_IRQ2: Register 2 to mask pending user interrupt requests; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in PPPMainIRQ register

Table 200. PPPIRQ2, PPPM_IRQ2 [1540 H, 1541 H]

Signal Name	Bit Pos.	Access	Default	Description
ABT4	0	R/W	0	Abort character (7D7E H) detected in RX PPP chiplet 4
BMFL4	1	R/W	0	Below minimum frame length, RX PPP chiplet 4. This bit is set when a packet is received that is shorter than the size set in MINFL(6:0).
MFLE4	2	R/W	0	Maximum frame length exceeded in RX PPP chiplet 4. This bit is set when a packet is received that is longer than or equal to the size set in the MAXFL(15:0) bits.
FCS4	3	R/W	0	Received bad frame in RX PPP chiplet 4. This bit is set when an FCS error is detected in the received packet.
ABT3	4	R/W	0	Abort character (7D7E H) detected in RX PPP chiplet 3
BMFL3	5	R/W	0	Below minimum frame length, RX PPP chiplet 3. This bit is set when a packet is received that is shorter than the size set in MINFL(6:0).
MFLE3	6	R/W	0	Maximum frame length exceeded in RX PPP chiplet 3. This bit is set when a packet is received that is longer than or equal to the size set in the MAXFL(15:0) bits.
FCS3	7	R/W	0	Received bad frame in RX PPP chiplet 3. This bit is set when an FCS error is detected in the received packet.

PPP Configuration Registers

PPPConf1: Configuration register 1. General PPP configuration signals A.

Table 201. PPPConf1 [1548 H]

Signal Name	Bit Pos.	Access	Default	Description
AutRst_Int	0	R/W	1	0: No action on read access 1: Auto-reset interrupt request registers upon read access. Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a 1 to that bit provided that the corresponding alarm condition is removed.
Reserved	1	R/W	1	Reserved
Reserved	7:2			Not used

PPPConf2: Configuration register 2. General PPP configuration signals B.

Table 202. PPPConf2 [1549 H]

Signal Name	Bit Pos.	Access	Default	Description
MFLAG	0	R/W	0	Multiple Flag: 0: At least one 7E H flag will be inserted between transmitted frames 1: At least two 7E H flags will be inserted between transmitted frames
SCRAM	1	R/W	0	Scrambler Enable: 0: Scrambler/descrambler is bypassed 1: The PPP Scrambler/descrambler is active. The scrambler operates over all of the C-n/SPE-payload bytes inserted into the SONET/SDH frame. The scrambler/descrambler polynomial is $X^{43}+1$.
FCSABT	2	R/W	0	FCS Abort: use of RXFCSEO lead 0: Only active if FCS error detected 1: Active if FCS or ABORT error detected, RXABTO lead remains at '0'
DMINF	3	R/W	0	Discard Minimum Frame: 0: All received frames that are less than MAXFL(15:0) bytes after destuffing are output. 1: Received frames that are less than the minimum size as indicated by the MINFL(6:0) bits are aborted
Reserved	7:4	R/W		Reserved

PPPConf3: Configuration register 3. Minimum frame length, in bytes used to monitor the received frames.

Table 203. PPPConf3 [154A H]

Signal Name	Bit Pos.	Access	Default	Description
MINFL(6:0)	6:0	R/W	0000000	Minimum Frame Length: minimum frame size to monitor received frames. Received frames that are less than the length indicated by MINFL(6:0) are discarded if the DMINF bit is set to a 1.
Reserved	7	R/W	0	Reserved

PPPConf4-5: Configuration registers 4 - 5. Maximum frame length, in bytes used to monitor the received frames.

Table 204. PPPConf4-5 [154B H, 154C H]

Signal Name	Bit Pos.	Access	Default	Description
MAXFL(7:0)	7:0	R/W	11111111	PPPConf4: Least significant byte of maximum frame length used to monitor received frames. Received frames that are equal to or greater than the length indicated by MAXFL(15:0) are always discarded.
MAXFL(15:8)	7:0	R/W	11111111	PPPConf5: Most significant byte of maximum frame length used to monitor received frames. Received frames that are equal to or greater than the length indicated by MAXFL(15:0) are always discarded.

PPPConf6: Configuration register 6. PPP control signals.

For all TXEN# bits, if transparent mode is disabled and a TXEN# bit is set to 0 while in the middle of a frame transfer for that PHY, an illegal sequence (7D7E H) is transmitted, followed by flags. The TXABTO lead will also be asserted when that PHY is selected. Otherwise flags (7E H) are transmitted. If transparent mode is enabled, and a TXEN# bit is set to 0, an all 1s pattern is inserted into the transmit data stream. When transparent mode is disabled, and a TXEN# bit is set to 1, flags (7E H) are transmitted until the start of a new frame is read out of the transmit ACB FIFO. If transparent mode is enabled and a TXEN# bit is set to 1, then data is just read out of the transmit ACB FIFO at the point where it left off.

For all RXEN# bits, if transparent mode is enabled or if transparent mode is disabled and the PHAST-12E is in the middle of a frame transfer, and a RXEN# bit is set to 0, operation will continue normally until the end of the current chunk, then the RXABTO (or RXFCSEO lead if enabled by the FCSABT bit), RXMSO, and RXEOFO signals will be asserted when that PHY is selected. If transparent mode is enabled, and RXEN# is set to a 1, data received for the receive PPP chiplet # is immediately written into the receive ACB, otherwise the PHAST-12E looks for a flag (7E H) followed by a non-flag character before writing data into the receive ACB FIFO.

Table 205. PPPConf6 [154D H]

Signal Name	Bit Pos.	Access	Default	Description
TXEN4	0	R/W	0	Transmit Enable: 0: Transmit PPP chiplet 4 is held in reset after completion of current chunk. 1: Transmit PPP chiplet 4 is enabled
TXEN3	1	R/W	0	Transmit Enable: 0: Transmit PPP chiplet 3 is held in reset after completion of current chunk 1: Transmit PPP chiplet 3 is enabled
TXEN2	2	R/W	0	Transmit Enable: 0: Transmit PPP chiplet 2 is held in reset after completion of current chunk 1: Transmit PPP chiplet 2 is enabled
TXEN1	3	R/W	0	Transmit Enable: 0: Transmit PPP chiplet 1 is held in reset after completion of current chunk 1: Transmit PPP chiplet 1 is enabled
RXEN4	4	R/W	0	Receive Enable: 0: Receive PPP chiplet 4 is held in reset after completion of current chunk 1: Receive PPP chiplet 4 is enabled
RXEN3	5	R/W	0	Receive Enable: 0: Receive PPP chiplet 3 is held in reset after completion of current chunk 1: Receive PPP chiplet 3 is enabled
RXEN2	6	R/W	0	Receive Enable: 0: Receive PPP chiplet 2 is held in reset after completion of current chunk 1: Receive PPP chiplet 2 is enabled
RXEN1	7	R/W	0	Receive Enable: 0: Receive PPP chiplet 1 is held in reset after completion of current chunk 1: Receive PPP chiplet 1 is enabled

PPPConf7: Configuration register 7. TX FCS generation.

Table 206. PPPConf7 [154E H]

Signal Name	Bit Pos.	Access	Default	Description
TFCS4(1:0)	1:0	R/W	00	Calculation of FCS in PPP_Tx chiplet 4: 00: Transparent mode 01: No FCS is calculated 10: 16-bit FCS is calculated 11: 32-bit FCS is calculated
TFCS3(1:0)	3:2	R/W	00	Calculation of FCS in PPP_Tx chiplet 3: 00: Transparent mode 01: No FCS is calculated 10: 16-bit FCS is calculated 11: 32-bit FCS is calculated
TFCS2(1:0)	5:4	R/W	00	Calculation of FCS in PPP_Tx chiplet 2: 00: Transparent mode 01: No FCS is calculated 10: 16-bit FCS is calculated 11: 32-bit FCS is calculated
TFCS1(1:0)	7:6	R/W	00	Calculation of FCS in PPP_Tx chiplet 1: 00: Transparent mode 01: No FCS is calculated 10: 16-bit FCS is calculated 11: 32-bit FCS is calculated

PPPConf8: Configuration register 8. RX FCS Calculation.

Table 207. PPPConf8 [154F H]

Signal Name	Bit Pos.	Access	Default	Description
RFCS4(1:0)	1:0	R/W	00	Calculation of FCS in PPP_Rx chiplet 4: 00: Transparent mode 01: No FCS is checked 10: 16-bit FCS is checked 11: 32-bit FCS is checked
RFCS3(1:0)	3:2	R/W	00	Calculation of FCS in PPP_Rx chiplet 3: 00: Transparent mode 01: No FCS is checked 10: 16-bit FCS is checked 11: 32-bit FCS is checked
RFCS2(1:0)	5:4	R/W	00	Calculation of FCS in PPP_Rx chiplet 2: 00: Transparent mode 01: No FCS is checked 10: 16-bit FCS is checked 11: 32-bit FCS is checked
RFCS1(1:0)	7:6	R/W	00	Calculation of FCS in PPP_Rx chiplet 1: 00: Transparent mode 01: No FCS is checked 10: 16-bit FCS is checked 11: 32-bit FCS is checked

OFP_TX1/2/3/4 CHIPLET ADDRESS MAPPING

Chiplet Base Address:

OFP_Tx1 1800 H.

OFP_Tx2 1C00 H.

OFP_Tx3 2000 H.

OFP_Tx4 2400 H.

The four Overhead Frame Processor chiplets in the transmit direction are grouped together in the following tables (# = 1,2,3,4).

Note: In 1xSTM-4c/STS-12c and 1xSTM-4/STS-12 modes each SFH block processes its own AU-n, but only SFH block 1 processes the actual Regenerator Section and Multiplex Section Overheads. The exceptions to this is are 1) RX B2 Error Processing which is performed separately in each SFH block, with SFH block 3 acting as the accumulator for the B2 Errors received in the other SFH blocks and 2) TX M1 processing and RX M1 counting, which are handled in TX SFH3 and RX SFH3 respectively. Therefore, when configured for one of these modes, controls, counters, and interrupt request bits associated with an AU-n need to be set and monitored in each SFH block; controls, counters, and interrupt request bits associated with the Regenerator Section and Multiplex Section Overheads, except B2 and M1, need to be set and monitored just for SFH block 1; controls, counters, and interrupt request bits related to the B2 and M1 bytes need to be set and monitored for SFH block 3.

Table 208. OFP_Tx1/2/3/4 Chiplet Address Mapping

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
OT#CntEn1	2	X 4	0000	COUNT ENABLE register	290
OT#Cnt1:PTRINC	4/5	N 8	00000000	Pointer increment event counter, no threshold	289
OT#Cnt2:PTRDEC	6/7	N 8	00000000	Pointer decrement event counter, no threshold	289
OT#Cnt3:ND_EVC	8/9	N 8	00000000	New data event counter, no threshold	289
OT#Cnt4:JUSC	A/B	N 8	00000000	Justification error counter with threshold	289
OT#Th4:JUSCTh	C	X 8	10000000	Threshold register for counter JUSC	289
OT#RESET	30	R 1	1	Default RESET register	290
OT#CMD1	31	O 3	000	Njus, Pjus, NDF	290
OT#Stat1	33	S 5		Init, HUG, Mode(2:0) (event)	291
OT#Stat2	34	S 3		Njus, Pjus, NDF (event)	291
OT#Stat3	35	S 8		K1 byte (static)	292
OT#Stat4	36	S 8		K2 byte (static)	292
OT#Stat5	37	S 8		K3 byte (static)	292
OT#MainIRQ	38	I 4		MAIN INTerrupt register	293
OT#M_MainIRQ	39	X 4	0000	INT MASK register (for OT#MainIRQ)	293

Table 208. OFP_Tx1/2/3/4 Chiplet Address Mapping (Continued)

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
OT#CntIRQ1	3A	I 5		COUNTER INTerrupt register	293
OT#M_CntIRQ1	3B	X 5	00000	INT MASK register (for OT#CntIRQ1)	293
OT#IRQ1	3C	I 7		USER INTerrupt register 1	294
OT#M_IRQ1	3D	X 7	0000000	INT MASK register (for IRQ1)	294
OT#IRQ2	3E	I 6		USER INTerrupt register 2	295
OT#M_IRQ2	3F	X 6	000000	INT MASK register (for IRQ2)	295
OT#Conf1	48	C 8	00000011	Chiplet configuration register 1 (general A)	296
OT#Conf2	49	C 8	00000000	Configuration register 2 (general B)	297
OT#Conf3	4A	C 8	See register description	Configuration register 3 (fscr reload pattern)	298
OT#Conf4	4B	C 8	00000000	Configuration register 4 (errmask)	298
OT#Conf5	4C	C 8	00000000	Configuration register 5 (erraddress)	298
OT#Conf6	4D	C 8	00000001	Configuration register 6 (fscr control)	298
OT#Conf7	4E	C 4	0000	Configuration register 7 (DCC control)	299
OT#Conf8	4F	C 6	000011	Configuration register 8 (ThrLoW)	299
OT#Conf9	50	C 6	010001	Configuration register 9 (ThrNoW)	299
OT#Conf10	51	C 6	100000	Configuration register 10 (ThrHiW)	299
OT#Conf11	52	C 5	00000	Configuration register 11 (Telecom Bus)	300
GRA	100-3FF			Growable Register Array (TOH)	301

OFP_Tx1/2/3/4 (OT1/2/3/4) Counters

OT#Cnt1:PTRINC: Number of pointer increment events. Counter overflow leads to an interrupt request.

Table 209. OT#Cnt1:PTRINC [1804 H / 1805 H, 1C04 H / 1C05 H, 2004 H / 2005 H, 2404 H / 2405 H]

Signal Name	Bit Pos.	Access	Default	Description
PTRINC(7:0)	7:0	R	00000000	Pointer increment counter

OT#Cnt2:PTRDEC: Number of pointer decrement events. Counter overflow leads to an interrupt request.

Table 210. OT#Cnt2:PTRDEC [1806 H / 1807 H, 1C06 H / 1C07 H, 2006 H / 2007 H, 2406 H / 2407 H]

Signal Name	Bit Pos.	Access	Default	Description
PTRDEC(7:0)	7:0	R	00000000	Pointer decrement counter

OT#Cnt3:ND_EVC: Number of new data events. Counter overflow leads to an interrupt request. A new data event occurs and an NDF enabled (1001) is transmitted the first time that the SDB FIFO normal fill level is exceeded after it has gone empty. This also causes the SFH block to start reading from its SDB FIFO (this is to allow the SDB FIFO to fill up to between its low and high water thresholds before data is read from it after recovering from an underflow condition). When the Telecom Bus mode is used and TX retiming is turned on, a new data event is triggered by the illegal movement of the J1 pulse on the TXTB#J0J1 lead. An illegal movement of the J1 byte is a repositioning of the J1 byte not in accordance with normal pointer adjustment activity.

Table 211. OT#Cnt3:ND_EVC [1808 H / 1809 H, 1C08 H / 1C09 H, 2008 H / 2009 H, 2408 H / 2409 H]

Signal Name	Bit Pos.	Access	Default	Description
ND_EVC(7:0)	7:0	R	00000000	New data event counter

OT#Cnt4:JUSC: Number of justification errors detected. Counter overflow leads to an interrupt request. A justification error is the occurrence of two pointer adjustments that are spaced less than 4 frames apart while the JusFrm bit is set to 1.

OT#Th4:JUSCTh: Threshold for number of justification errors. Threshold equaled leads to an interrupt request.

Table 212. OT#Cnt4:JUSC, OT#Th4:JUSCTh [180A H / 180B H, 1C0A H / 1C0B H, 200A H / 200B H, 240A H / 240B H, 180C H, 1C0C H, 200C H, 240C H]

Signal Name	Bit Pos.	Access	Default	Description
JUSC(7:0)	7:0	R	00000000	Justification error counter
JUSCTh(7:0)	7:0	R/W	10000000	Threshold for justification error counter

OT#CntEn1: Counter On/Off control register for OFP_Tx1/2/3/4

For each bit position:

0: Counter is disabled

1: Counter is enabled

Table 213. OT#CntEn1 [1802 H, 1C02 H, 2002 H, 2402 H]

Signal Name	Bit Pos.	Access	Default	Description
EN-PTRINC	0	R/W	0	Pointer increment counter enable
EN-PTRDEC		R/W	0	Pointer decrement counter enable
EN-ND_EVCNT	2	R/W	0	New data event counter enable
EN-JUSCNT	3	R/W	0	Justification error counter enable
Reserved	7:4			Not used

OFP_Tx1/2/3/4 (OT1/2/3/4) Reset Registers

OT#RESET: Reset chiplet control registers. These registers are automatically preset to the default value by the reset signals ResOT1/2/3/4 from the GPPINT.

For each bit position:

0: Reset not active

1: Reset active

Table 214. OT#RESET [1830 H, 1C30 H, 2030 H, 2430 H]

Signal Name	Bit Pos.	Access	Default	Description
Reset	0	R/W	1	Reset (disable) OFP_Tx1/2/3/4 chiplet
Reserved	7:1			Not used

OFP_Tx1/2/3/4 (OT1/2/3/4) Command Registers

OT#CMD1: Command register for the chiplet. Single-cycle active if 1 is written into bit position.

Table 215. OT#CMD1 [1831 H, 1C31 H, 2031 H, 2431 H]

Signal Name	Bit Pos.	Access	Default	Description
Njus	0	R/W	0	Perform a negative frequency justification
Pjus	1	R/W	0	Perform a positive frequency justification
NDF	2	R/W	0	Force a start-of-new-VC-n event. n=4 in 4xSTM-1/STS-3c and 1xSTM-4/STS-12 modes, and n=4-4c in STM-4c/STS-12c mode. This feature is not available in Telecom Bus mode and hence this bit should not be used in that mode.
Reserved	7:3			Not used

OFP_Tx1/2/3/4 Status Registers

OT#Stat1: Status register 1 of the chiplet. This is an event latch register.

Table 216. OT#Stat1 [1833 H, 1C33 H, 2033 H, 2433 H]

Signal Name	Bit Pos.	Access	Default	Description
Init (see Note)	0	R/W		0: Default GRA initialization not completed 1: Default GRA initialization completed
HUG	1	R/W		0: Higher-order unequipped generator inactive 1: Higher-order unequipped generator active. C2 byte =00 H, C-n/SPE payload is filled with all 0s. All other TX POH bytes are normal,
Mode(2:0)	4:2	R/W		Mode: XXB: 0=All macros are independent. 1= multi-macros act together but are non-concatenated (e.g., STM-4/STS-12). XBX: 0= Non-concatenation mode. 1= concatenation mode. BXX: 0= single-chip operation. 1= multi-chip operation. X10 and 1X0 are not allowed.
Reserved	7:5			Not used

Note: The Init bit must be polled during initialization. The TX ACH, TX PH, and TX ACI blocks must not be taken out of reset until this bit becomes set to 1.

OT#Stat2: Status register 2 of the chiplet. This is an event latch register.

Table 217. OT#Stat2 [1834 H, 1C34 H, 2034 H, 2434 H]

Signal Name	Bit Pos.	Access	Default	Description
Njus	0	R/W		0: NO negative frequency justification transmitted 1: Negative frequency justification transmitted
Pjus	1	R/W		0: NO positive frequency justification transmitted 1: Positive frequency justification transmitted
NDF	2	R/W		0: NO NDF transmitted 1: NDF transmitted
Reserved	7:3			Not used

OT#Stat3: Status register 3 of the chiplet. This is a static latch register; the bit values follow the driving signals immediately. This register is updated from local RX SFH# when LineRING=0. This register is updated from the Ring Port when LineRING=1.

Table 218. OT#Stat3 [1835 H, 1C35 H, 2035 H, 2435 H]

Signal Name	Bit Pos.	Access	Default	Description
K1byte(7:0)	7:0	R		This is the debounced K1 byte received from the Ring Port when the LineRING control bit is set to 1, otherwise it is the debounced K1 byte from RX SFH #.

OT#Stat4: Status register 4 of the chiplet. This is a static latch register; the bit values follow the driving signals immediately. This register is updated from local RX SFH# when LineRING=0. This register is updated from the Ring Port when LineRING=1. All of the K1 byte and the first 5 MSBits of the K2 byte are used in the debouncing process for the K1byte and K2byte registers. The K1 and K2 bytes are considered to be debounced if three consecutive and equal new K1 and the first 5 bits of K2 are received.

Table 219. OT#Stat4 [1836 H, 1C36 H, 2036 H, 2436 H]

Signal Name	Bit Pos.	Access	Default	Description
K2byte(7:0)	7:0	R		This is the debounced K2 byte received from the Ring Port when the LineRING control bit is set to 1, otherwise it is the debounced K2 byte from RX SFH#.

OT#Stat5: Status register 5 of the chiplet. This is a static latch register; the bit values follow the driving signals immediately. This register is updated from local RX SFH# when PathRING=0. This register is updated from the Ring Port when PathRING=1.

Table 220. OT#Stat5 [1837 H, 1C37 H, 2037 H, 2437 H]

Signal Name	Bit Pos.	Access	Default	Description
K3byte(7:0)	7:0	R		This is the debounced K3 byte received from the Ring Port when the PathRING control bit is set to 1, otherwise it is set to 0s.

OFP_Tx1/2/3/4 Interrupt Request and Mask Registers

OT#MainIRQ: Register to indicate fatal interrupt events and to point to user IRQ registers with active requests; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

Bit 0 in this register is “one shot”, i.e., set by a pulse, or by a condition which is unlikely to be persistent.

Bits 1-3 in this register persist as long as the triggering condition persists. i.e., If an interrupt request bit is read, the bit will clear and become set again in one SFH block clock cycle, if the corresponding condition persists.

OT#M_MainIRQ: Register to mask pending interrupt requests. A masked request will not generate an outgoing

IRQ to the GPPINT; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates signal IRQOT1/2/3/4 to GPPINT

Table 221. OT#MainIRQ, OT#M_MainIRQ
[1838 H, 1C38 H, 2038 H, 2438 H, 1839 H, 1C39 H, 2039 H, 2439 H]

Signal Name	Bit Pos.	Access	Default	Description
Fatal	0	R/W	0	Fatal event occurred
CntIRQ1	1	R/W	0	Active request in OT#CntIRQ1 register
IRQ1	2	R/W	0	Active request in IRQ1 register
IRQ2	3	R/W	0	Active request in IRQ2 register
Reserved	7:4			Not used

OT#CntIRQ1: Register to indicate active counter interrupt requests of this chiplet; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

Bits 0-4 in this register are “one shot”, i.e., set by a pulse, or by a condition which is unlikely to be persistent.

OT#M_CntIRQ1: Register to mask pending counter interrupt requests; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in OT#MainIRQ register

Table 222. OT#CntIRQ1, OT#M_CntIRQ1
[183A H, 1C3A H, 203A H, 243A H, 183B H, 1C3B H, 203B H, 243B H]

Signal Name	Bit Pos.	Access	Default	Description
OV-PTRINC	0	R/W	0	Overflow pointer increment counter
OV-PTRDEC	1	R/W	0	Overflow pointer decrement counter
OV-ND_EVCNT	2	R/W	0	Overflow new data event counter
OV-JUSCNT	3	R/W	0	Overflow justification error counter
TH-JUSCNT	4	R/W	0	Threshold equaled justification error counter
Reserved	7:5			Not used

OT#IRQ1: Register to indicate active user interrupt requests of this chiplet; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

Bits 1-6 in this register are “one shot”, i.e., set by a pulse, or by a condition which is unlikely to be persistent.

Bit 0 in this register persists as long as the triggering condition persists. i.e., If bit 0 is read, the bit will clear and become set again in one SFH block clock cycle, if the corresponding condition persists.

OT#M_IRQ1: Register to mask pending user interrupt requests; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in OT#MainIRQ register

Table 223. OT#IRQ1, OT#M_IRQ1
[183C H, 1C3C H, 203C H, 243C H, 183D H, 1C3D H, 203D H, 243D H]

Signal Name	Bit Pos.	Access	Default	Description
TxLPow	0	R/W	0	Low Power indication from O/E module. This interrupt request bit is activated via the TXLPOW# input lead.
SPCIR	1	R/W	0	SPC FSM interrupt request. See SPCI (3:0) in OT#Conf1 Table 225.
FrmErr	2	R/W	0	Framing error detected. This bit is set when the external TX frame reference (TXFRMIN) does not occur in the expected location.
FHigh	3	R/W	0	FIFO high threshold overstep. This interrupt request bit generally indicates that a pointer adjustment has occurred.
FLow	4	R/W	0	FIFO low threshold understep. This interrupt request bit generally indicates that a pointer adjustment has occurred.
DLoss	5	R/W	0	Data loss = Data FIFO empty. This condition generally occurs when the TX APH or Telecom Bus is switched off, in which case an unequipped frame is transmitted.
FPwarn	6	R/W	0	Frame pulse out of sync
Reserved	7			Not used

OT#IRQ2: Register to indicate active user interrupt requests of this chiplet; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

Bits 0, 1 and 5 in this register are “one shot”, i.e., set by a pulse, or by a condition which is unlikely to be persistent.

Bits 2-3 in this register persist as long as the triggering condition persists. i.e., If an interrupt request bit is read, the bit will clear and become set again in one SFH Block clock cycle, if the corresponding condition persists.

Bit 4 is set by a “one shot” pulse, but if the inconsistent K1 condition persists, this bit will become set again.

OT#M_IRQ2: Register to mask pending user interrupt requests; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in OT#MainIRQ register

Table 224. OT#IRQ2, OT#M_IRQ2
[183E H, 1C3E H, 203E H, 243E H, 183F H, 1C3F H, 203F H, 243F H]

Signal Name	Bit Pos.	Access	Default	Description
NewAPS	0	R/W	0	New debounced K1/K2 APS bytes. When the TX Ring Port is enabled to accept line overhead data structures (LineRING=1), this bit is set to indicate that a New APS indication was received from the Ring Port. When the TX Ring Port is disabled from accepting line overhead data structures (LineRING=0), this bit indicates that new debounced K1/K2 APS bytes have been received from the receive line. The K1 and K2 bytes are considered debounced when the K1 byte and first five bits of the K2 byte are new and consistent for three consecutive frames.
NewK3	1	R/W	0	New debounced K3 byte. When the PathRing bit is set to a 1, this bit is set to indicate that a New K3 indication was received from the Ring Port. When the PathRING is set to 0, this bit is disabled.
MS_LRDI	2	R/W	0	MS/Line RDI in corresponding receive section. This bit is set to indicate that a MS RDI indication was received from the Ring Port. This bit is active only when operating in RING Mode (LineRING=1). When LineRING=0, the line RDI indication is provided by bit 6 of register OR#IRQ3.
AIP_DLoss	3	R/W	0	Loss of Transmit Ring Port Data. This bit will become set if the start sequence is not detected for 1 to 2 transmit frame times, when either or both of the LineRING and PathRING control bits are set to 1. Only the interrupt and interrupt mask bits in OT1IRQ2 and OT1M_IRQ2 are used for this alarm. The corresponding mask bits in OT2M_IRQ2, OT3M_IRQ2 and OT4_IRQ2 should always be set to 0 to avoid multiple requests.
APS_Incon	4	R/W	0	Inconsistent K1 Byte. In order for this alarm to work properly, the corresponding control bit Pchan (ORCONF#2, bit 5) must be set to 1. When the TX Ring Port is disabled from accepting line overhead data structures (LineRING=0), this bit will become set when no 3 consecutive received K1 bytes of the last 12 successive frames are identical, starting with the last frame containing a previously consistent byte. This APS byte defect terminates when 3 consecutive received K1 bytes are identical. When the TX Ring Port is enabled to accept line overhead data structures (LineRING=1), this bit is set when the Inconsistent K1 Byte indication bit position in the TX Ring Port data stream is set to a 1.

Table 224. OT#IRQ2, OT#M_IRQ2 [183E H, 1C3E H, 203E H, 243E H, 183F H, 1C3F H, 203F H, 243F H] (Continued)

Signal Name	Bit Pos.	Access	Default	Description
PAR_ERR	5	R/W	0	A Telecom Bus parity error was detected.
Reserved	7:6			Not used

OFP_Tx1/2/3/4 Configuration Registers

OT#Conf1: Configuration register 1. General OFP_Tx configuration register.

Table 225. OT#Conf1 [1848 H, 1C48 H, 2048 H, 2448 H]

Signal Name	Bit Pos.	Access	Default	Description
AutRst_Int	0	R/W	1	0: No action on read access. 1: Auto-reset interrupt request registers upon read access. Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a 1 to that bit provided that the corresponding alarm condition is removed.
AutRst_Sta	2	R/W	1	0: No action on read access 1: Auto-reset all bits in the OT#Stat1 and OT#Stat2 status registers upon read access
JusFrm	2	R/W	0	This bit affects all modes in which pointer processing or retiming (VC-n Telecom Bus mode) is enabled. 0: Allow pointer modification to be performed on frame-to-frame basis 1: Enforces three frames being interleaved between two pointer modification operations
J1Mode	3	R/W	0	0: Transmit 16-byte J1 path trace 1: Transmit 64-byte J1 path trace
SPCI(3:0)	7:4	R/W	0000	Specifies STM-N/STS-M row number in which an interrupt request will be issued via the SPCIR interrupt request bit. e.g., 0000 means no interrupt will be generated; 0011 means that at the beginning of row three the SPCIR interrupt request bit will be asserted.

OT#Conf2: Configuration register 2. General OFP_Tx configuration register. When in STM-4c or STS-12c modes, it is only necessary to set the bit in chiplet 1 to transmit TOH-related alarm conditions; to transmit Path-related alarms, the corresponding command bits in each chiplet have to be set. Also, path-related alarms cannot be transmitted in Telecom Bus mode, as either the VC-4 or AU-4 is provided externally via the TX Telecom Bus Interfaces.

Table 226. OT#Conf2 [1849 H, 1C49 H, 2049 H, 2449 H]

Signal Name	Bit Pos.	Access	Default	Description
MsAIS	0	R/W	0	0: NO multiplex section AIS 1: Enforce multiplex section AIS. The MSOH and AU-n are set to all 1s.
HUG	1	R/W	0	0: NO unequipped VC-n signal 1: Enforce unequipped VC-n signal. An unequipped signal is generated by setting the C-n and C2 POH bytes to all 0s. The other POH bytes are processed normally. The C2 value in the GRA has no effect.
TxSDown	2	R/W	0	Directly connected to output lead: 0: The corresponding TXSDOWN# lead is set to 0. 1: The corresponding TXSDOWN# lead is set to 1.
P_AIS	3	R/W	0	0: NO Path AIS 1: Enforce Path AIS from microprocessor
P_RDI(1:0)	5:4	R/W	00	00: NO Path RDI XX: Path RDI pattern, microprocessor-enforced insertion in G1 byte. When set to 00 the TX Path RDI is sent as 001, when set to 01 the TX Path RDI is sent as 010, when set to 10 the TX Path RDI is sent as 101, and when set to 11 the TX Path RDI is sent as 110.
MS_RDI	6	R/W	0	0: No MS RDI 1: Enforce MS RDI from microprocessor This bit can still be used to force MS-RDI while LineRING=1.
ExtSync	7	R/W	0	Leave this bit set to 0.

OT#Conf3-5: Configuration registers 3 - 5.

Table 227. OT#Conf3-5 [184A H, 1C4A H, 204A H, 244A H, 184B H, 1C4B H, 204B H, 244B H, 184C H, 1C4C H, 204C H, 244C H]

Signal Name	Bit Pos.	Access	Default	Description
FSCR(7:0)	7:0	R/W	Default is as described to the right.	OT#Conf3: Reload pattern for frame scrambler; setting this register to all-zeros results in an unmodified data stream. Setting this register to its default values enables the scrambler. The following values are automatically written into the OT#Conf3 registers as the default values, based on the setting of the ADDR(2:0) leads and the GCascTx(3:0) bits as indicated; this allows the correct reload patterns for the TX scrambler to be initialized into the OT#Conf3 registers for the various modes of operation. GCascTx(3:0) = 0001,0010, 0111, 1000, ADDR(2:0) = 000: TX OFP chiplets 1-4 FE H GCascTx(3:0) = 11xx, 101x, 1001, 0011, ADDR(2:0) = 000: TX OFP chiplet 1 FE H TX OFP chiplet 2 04 H TX OFP chiplet 3 18 H TX OFP chiplet 4 51 H
ErrMask(7:0)	7:0	R/W	00000000	OT#Conf4: Mask register forcing bit error insertion; XOR-ed with retrieved SOH/POH
ErrAddr(7:0)	7:0	R/W	00000000	OT#Conf5: Error mask address register; indicates address of SOH/POH byte to be corrupted. See Address Offset column in Table 232 for the addresses to use.

OT#Conf6: Configuration register 6. Frame scrambling control register.

Table 228. OT#Conf6 [184D H, 1C4D H, 204D H, 244D H]

Signal Name	Bit Pos.	Access	Default	Description
Reserved	0	R/W	1	Data Select test bit. Do not modify. 0: Scrambler generator pattern is output to the line 1: Data from scrambler is output to line
Test	7:1	R/W	0000000	Test bits. Do not modify.

OT#Conf7: Configuration register 7. DCC control register.

Table 229. OT#Conf7 [184E H, 1C4E H, 204E H, 244E H]

Signal Name	Bit Pos.	Access	Default	Description
Enable	0	R/W	0	0: Disable DCC processing 1: Enable DCC processing
OpMode	1	R/W	0	0: DCC1 channel (D1 - D3) input on TDATA# 1: DCC2 channel (D4 - D12) input on TDATA# Before changing this bit, Enable (bit 0 of this register) should be set to a 0.
Reserved	2	R/W	0	Reserved
EdgeMode	3	R/W	0	0: TDATA# sampled on the falling edge of TDCLK#. 1: TDATA# sampled on the rising edge of TDCLK#.
Reserved	7:4			Not used

OT#Conf8-10: Configuration registers 8 - 10. TX 64-byte deep SDB FIFO threshold registers. The ThrLoW and the ThrHiW thresholds are used to trigger pointer adjustments. The ThrLoW and the ThrHiW thresholds should each be spaced at least D H away from the ThrNoW threshold. The values written to these threshold registers should be kept between the values of 6 H and 39 H.

Table 230. OT#Conf8-10 [184F H, 1C4F H, 204F H, 244F H, 1850 H, 1C50 H, 2050 H, 2450 H, 1851 H, 1C51 H, 2051 H, 2451 H]

Signal Name	Bit Pos.	Access	Default	Description
ThrLoW(5:0)	5:0	R/W	000011	OT#Conf8: Low Water FIFO threshold, default = 3 H. The recommended setting for this register is A H.
Reserved	7:6			Not used
ThrNoW(5:0)	5:0	R/W	010001	OT#Conf9: Normal Water FIFO threshold, default = 11 H. The recommended setting for this register is 18 H.
Reserved	7:6			Not used
ThrHiW(5:0)	5:0	R/W	100000	OT#Conf10: High Water FIFO threshold, default = 20 H. The recommended setting for this register is 27 H.
Reserved	7:6			Not used

OT#Conf11: Configuration register 11. Telecom Bus control signals.

Table 231. OT#Conf11 [1852 H, 1C52 H, 2052 H, 2452 H]

Signal Name	Bit Pos.	Access	Default	Description
FRM_SLT_SEL (1:0)	1:0	R/W	00	Slot selection for J0 pulse: These bits are used in Telecom Bus mode when transmit retiming is turned off (AU-n mode is enabled), and indicate which slot the J0 pulse (which is used as a slot identification pulse when in AU-n mode and not as a J0 byte identification pulse) is in. When in AU-n mode the J0 pulse in the TXTB#J0J1 signal does not have to line up with the J0 byte. However, the J0 byte has to be referenced to the TXCFRM output signal and the accompanying TXCCLK or TXCCLK clocks. 00: Do not use J0 (no delay compensation). 01: J0 pulse on slot 1 10: J0 pulse on slot 2 11: J0 pulse on slot 3 There are three slots (1-3) in a SONET/SDH frame. The 1st, 4th, 7th,... etc., column of the SONET/SDH frame is slot 1. The 2nd, 5th, 8th,... etc., column of the SONET/SDH frame is slot 2. The 3rd, 6th, 9th,... etc., column of the SONET/SDH frame is slot 3. When transmit retiming is turned off, the slot identification pulse on TXTB#J0J1 can be in any slot (1-3) provided that the FRM_SLT_SEL(1:0) bits are set accordingly and the TXTB#SPE signal is also low coincident with the slot identification pulse, where # = 1-4. The slot identification pulse needs to repeat once every 125 microseconds.
PAR_FULL	2	R/W	0	0: TX Telecom Bus Parity checked over data only 1: TX Telecom Bus Parity checked over data, J0J1, SPE, and FAIL signals
PAR_EN	3	R/W	0	0: No TX Telecom Bus Parity checking 1: TX Telecom Bus Parity checking enabled
PAR_EVEN	4	R/W	0	0: Odd TX Telecom Bus Parity 1: Even TX Telecom Bus Parity
Reserved	7:5			Not used

OFP_Tx1/2/3/4 Growable Register Array (GRA) Address Mapping

NOTE: Bytes marked as “X” are reserved for national use. The “*” character indicates national use bytes that are not included in frame scrambling. Therefore, care should be taken with their content as this can affect jitter generation. If these bytes are not used, it is recommended that an incrementing pattern (01 H - 0C H) be written to those bytes, so that they reflect the number of their respective "STS-1". Bytes marked as “$” are media dependent bytes. All unmarked bytes are reserved for future international standardization.

Regardless of mode, the B1, B2, 3-LSBs of K2, and M1 are always written by a state machine. The table below shows the bytes that are written by an internal state machine depending on the macro’s corresponding mode of operation.

Macro Mode	Byte	Source of Byte	Notes
4xSTM-1/STS-3c ATM or PPP, 1xSTM-4/STS-12 ATM or PPP, or 1xSTM-4c/STS-12c ATM or PPP	B3	State Machine	
4xSTM-1/STS-3c ATM or PPP, 1xSTM-4/STS-12 ATM or PPP, or 1xSTM-4c/STS-12c ATM or PPP	G1	State Machine	
4xSTM-1/STS-3c ATM or PPP, 1xSTM-4/STS-12 ATM or PPP, or 1xSTM-4c/STS-12c ATM or PPP	H1H2	State Machine	Just the first H1H2 bytes for the AU-3/AU-4/AU-4-4c that is generated by the macro.
Telecom Bus Mode	B3	Telecom Bus	All POH comes from the TX Telecom Bus.
Telecom Bus Mode	G1	Telecom Bus	All POH comes from the TX Telecom Bus.
Telecom Bus Mode, AU-n mode enabled	H1,H2, and H3	Telecom Bus	The AU-n for that macro comes from the Telecom Bus.
Telecom Bus Mode, VC-n mode enabled	H1,H2	State Machine	Just the first H1H2 bytes for the AU-n that is generated by the macro.

All GRA TOH locations that are not written by state machines can be written by an external microprocessor, except the POH bytes when in Telecom Bus mode.

Table 232. OFP_Tx1/2/3/4 Growable Register Array (GRA) Address Mapping [1900 H - 19BF H, 1D00 H - 1DBF H, 2100 H - 21BF H, 2500 H - 25BF H]

Address Offset (Hex)	Byte Name	Default (Hex)	Description
00	A1	F6	First A1 (In 1xSTM-4/STS-12 and 1xSTM-4c/STS-12c modes, 1st A1 is in TX OFP 1, the 2nd A1 is in TX OFP 2, 3rd A1 is in TX OFP 3, and 4th A1 is in TX OFP 4)
01	A1	F6	Second A1
02	A1	F6	Third A1
03	A2	28	First A2
04	A2	28	Second A2
05	A2	28	Third A2

Table 232. OFP_Tx1/2/3/4 Growable Register Array (GRA) Address Mapping [1900 H - 19BF H, 1D00 H - 1DBF H, 2100 H - 21BF H, 2500 H - 25BF H] (Continued)

Address Offset (Hex)	Byte Name	Default (Hex)	Description
06	J0*	55	(C11)
07	X*	55	(C12)
08	X*	55	(C13)
09	B1	55	
0A	$	55	
0B	$	55	
0C	E1	55	
0D	$	55	
0E		55	
0F	F1	55	
10	X	55	
11	X	55	
12	D1	55	
13	$	55	
14	$	55	
15	D2	55	
16	$	55	
17		55	
18	D3	55	
19		55	
1A		55	
1B	H11	68	
1C	Y (H12)	9F	
1D	Y (H13)	9F	
1E	H21	00	
1F	1s (H22)	FF	
20	1s (H23)	FF	
21	H31	55	These bytes should be programmed to 00 H
22	H32	55	These bytes should be programmed to 00 H
23	H33	55	These bytes should be programmed to 00 H
24	B2	55	
25	B2	55	
26	B2	55	
27	K1	00	
28		55	
29		55	

Table 232. OFP_Tx1/2/3/4 Growable Register Array (GRA) Address Mapping [1900 H - 19BF H, 1D00 H - 1DBF H, 2100 H - 21BF H, 2500 H - 25BF H] (Continued)

Address Offset (Hex)	Byte Name	Default (Hex)	Description
2A	K2	00	
2B		55	
2C		55	
2D	D4	55	
2E		55	
2F		55	
30	D5	55	
31		55	
32		55	
33	D6	55	
34		55	
35		55	
36	D7	55	
37		55	
38		55	
39	D8	55	
3A		55	
3B		55	
3C	D9	55	
3D		55	
3E		55	
3F	D10	55	
40		55	
41		55	
42	D11	55	
43		55	
44		55	
45	D12	55	
46		55	
47		55	
48	S1	00	
49		55	
4A		55	
4B	M1	00	M1 (TX OFP chiplet 3) for STM-4, STM-4c, STS-12, STS-12c.
4C		55	

Table 232. OFP_Tx1/2/3/4 Growable Register Array (GRA) Address Mapping [1900 H - 19BF H, 1D00 H - 1DBF H, 2100 H - 21BF H, 2500 H - 25BF H] (Continued)

Address Offset (Hex)	Byte Name	Default (Hex)	Description
4D	M1	00	M1 for STS-3c/STM-1
4E	E2	55	
4F		55	
50		55	
51		55	Reserved
52		55	
53		55	
54	J1	55	Reserved
55	B3	55	
56	C2	13	
57	G1	00	
58	F2	00	
59	H4	00	
5A	F3	00	
5B	K3	00	
5C	N1	00	
5D	Reserved	55	Reserved
5E	Reserved	55	Reserved
5F	Reserved	55	Reserved
60	J0	55	TX J0 section trace bytes.
...	..	..	
6F	J0	55	
70-7F	..	..	Reserved
80	J1	55	J1 path trace in 16-byte format
...	..	..	
8F	J1	55	
90	J1	55	Extra registers for 64-byte free format. Registers 80H-BFH are used for 64-byte free format.
...	..	..	
BF	J1	55	
C0 - 2FF	..	..	Reserved

OFP_RX1/2/3/4 CHIPLET ADDRESS MAPPING

Chiplet Base Address:

OFP_Rx1 2800 H.

OFP_Rx2 2C00 H.

OFP_Rx3 3000 H.

OFP_Rx4 3400 H.

The four Overhead Frame Processor chiplets in the receive direction are grouped together in the following tables (# = 1,2,3,4).

Note: In 1xSTM-4c/STS-12c and 1xSTM-4/STS-12 modes each SFH block processes its own AU-n, but only SFH block 1 processes the actual Regenerator Section and Multiplex Section Overheads. The exceptions to this is are 1) RX B2 Error Processing which is performed separately in each SFH block, with SFH block 3 acting as the accumulator for the B2 Errors received in the other SFH blocks and 2) TX M1 processing and RX M1 counting, which are handled in TX SFH3 and RX SFH3 respectively. Therefore, when configured for one of these modes, controls, counters, and interrupt request bits associated with an AU-n need to be set and monitored in each SFH block; controls, counters, and interrupt request bits associated with the Regenerator Section and Multiplex Section Overheads, except B2 and M1, need to be set and monitored just for SFH block 1; controls, counters, and interrupt request bits related to the B2 and M1 bytes need to be set and monitored for SFH block 3.

Table 233. OFP_Rx1/2/3/4 Chiplet Address Mapping

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
OR#ROFmid	0	F 8	00000000	Read-on-the-fly register	309
OR#CntEn1	2	X 8	00000000	COUNT ENABLE register 1	313
OR#CntEn2	3	X 3	000	COUNT ENABLE register 2	314
OR#Cnt1:B1BITC	4/5	N 16	0000 H	LSByte of 16-bit BIP-8 B1 bit error counter	309
OR#Th12:B1BITCTh2	6	X 8	00000000	Threshold register Byte 2 (LSByte) for B1BITC	309
OR#Th11:B1BITCTh1	7	X 8	01111101	Threshold register Byte 1 for counter B1BITC	309
OR#Cnt2:B1BLKC	8/9	N 16	0000 H	LSByte of 16-bit BIP-8 B1 block error counter	309
OR#Th22:B1BLKCTh2	A	X 8	00000000	Threshold register Byte 2 (LSByte) for B1BLKC	309
OR#Th21:B1BLKCTh1	B	X 8	01111101	Threshold register Byte 1 for counter B1BLKC	309
OR#Cnt3:B2BITC	C/D	N 16	0000 H	LSByte of 16-bit BIP-24 B2 bit error counter, 2 threshold	310

Table 233. OFP_Rx1/2/3/4 Chiplet Address Mapping (Continued)

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
OR#Th32d:B2BITCTh2d	E	X 8	00100000	Degradation threshold Byte 2 (LSByte) for B2BITC	310
OR#Th31d:B2BITCTh1d	F	X 8	01001110	Degradation threshold Byte 1 for B2BITC	310
OR#Th32f:B2BITCTh2f	10	X 8	00000000	Failure threshold Byte 2 (LSByte) for B2BITC	310
OR#Th31f:B2BITCTh1f	11	X 8	01111101	Failure threshold Byte 1 for B2BITC	310
OR#Cnt4:B2BLKC	12/13	N 16	0000 H	LSByte of 16-bit BIP-24 B2 block error counter, 2 threshold	310
OR#Th42d:B2BLKCTh2d	14	X 8	00100000	Degradation threshold Byte 2 (LSByte) for B2BLKC	310
OR#Th41d:B2BLKCTh1d	15	X 8	01001110	Degradation threshold Byte 1 for B2BLKC	310
OR#Th42f:B2BLKCTh2f	16	X 8	00000000	Failure threshold Byte 2 (LSByte) for B2BLKC	310
OR#Th41f:B2BLKCTh1f	17	X 8	01111101	Failure threshold Byte 1 for B2BLKC	310
OR#Cnt5:B3BITC	18/19	N 16	0000 H	LSByte of 16-bit BIP-8 B3 bit error counter	311
OR#Th52:B3BITCTh2	1A	X 8	00000000	Threshold register Byte 2 (LSByte) for B3BITC	311
OR#Th51:B3BITCTh1	1B	X 8	01111101	Threshold register Byte 1 for counter B3BITC	311
OR#Cnt6:B3BLKC	1C/1D	N 16	0000 H	LSByte of 16-bit BIP-8 B3 block error counter	311
OR#Th62:B3BLKCTh2	1E	X 8	00000000	Threshold register Byte 2 (LSByte) for B3BLKC	311
OR#Th61:B3BLKCTh1	1F	X 8	01111101	Threshold register Byte 1 for counter B3BLKC	311
OR#Cnt7:MSREIC	20/21	N 16	0000 H	LSByte of 16-bit multiplex section remote error indication counter	312
OR#Th72:MSREICTh2	22	X 8	00000000	Threshold register Byte 2 (LSByte) for MSREIC	312
OR#Th71:MSREICTh1	23	X 8	01111101	Threshold register Byte 1 for counter MSREIC	312

Table 233. OFP_Rx1/2/3/4 Chiplet Address Mapping (Continued)

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
OR#Cnt8:HPREIC	24/25	N 16	0000 H	LSByte of 16-bit higher-order path remote error indication counter	312
OR#Th82:HPREICTh2	26	X 8	00000000	Threshold register Byte 2 (LSByte) for HPREIC	312
OR#Th81:HPREICTh1	27	X 8	01111101	Threshold register Byte 1 for counter HPREIC	312
OR#Cnt9:PJ_EVCNT	28/29	N 8	00000000	Positive justification counter, no threshold	313
OR#Cnt10:NJ_EVCNT	2A/2B	N 8	00000000	Negative justification counter, no threshold	313
OR#Cnt11:ND_EVCNT	2C/2D	N 8	00000000	New data event counter, no threshold	313
OR#RESET	30	R 1	1	Default RESET register	314
OR#Stat1	33	S 3		Status register 1 (Mode; event)	314
OR#Stat2	34	S 8		Status register 2 (AU pointer; event)	315
OR#MainIRQ	38	I 7		MAIN INTerrupt register	316
OR#M_MainIRQ	39	X 7	0000000	INT MASK register (for OR#MainIRQ)	316
OR#CntIRQ1	3A	I 8		COUNTER INTerrupt register	316
OR#M_CntIRQ1	3B	X 8	00000000	INT MASK register (for OR#CntIRQ1)	316
OR#CntIRQ2	3C	I 8		COUNTER INTerrupt register	317
OR#M_CntIRQ2	3D	X 8	00000000	INT MASK register (for OR#CntIRQ2)	317
OR#CntIRQ3	3E	I 5		COUNTER INTerrupt register	317
OR#M_CntIRQ3	3F	X 5	00000	INT MASK register (for OR#CntIRQ3)	317
OR#IRQ1	40	I 5		USER INTerrupt register	318
OR#M_IRQ1	41	X 5	00000	INT MASK register (for OR#IRQ1)	318
OR#IRQ2	42	I 8		USER INTerrupt register	319
OR#M_IRQ2	43	X 8	00000000	INT MASK register (for OR#IRQ2)	319
OR#IRQ3	44	I 8		USER INTerrupt register	321

Table 233. OFP_Rx1/2/3/4 Chiplet Address Mapping (Continued)

Register Name	Address Offset (Hex)	Type/ Width	Initial Value (binary)	Description	See Page
OR#M_IRQ3	45	X 8	00000000	INT MASK register (for OR#IRQ3)	321
OR#Conf1	48	C 8	00111111	Configuration register 1 (general)	322
OR#Conf2	49	C 8	10000000	Configuration register 2 (SOH processing)	323
OR#Conf3	4A	C 8	00100000	Configuration register 3 (POH byte processing)	325
OR#Conf4	4B	C 8	00000000	Configuration register 4 (APS processing)	325
OR#Conf5	4C	C 8	00000000	Configuration register 5 (K1 shadow)	326
OR#Conf6	4D	C 8	00000000	Configuration register 6 (K2 shadow)	326
OR#Conf7	4E	C 8	00000100	Configuration register 7 (miscellaneous)	327
OR#Conf8	4F	C 8	See register description	Configuration register 8 (FSCR)	328
OR#Conf9	50	C 8	00010011	Configuration register 9 (SL)	328
OR#Conf10	51	C 8	00000000	Configuration register 10 (SM)	328
OR#Conf11	52	C 8	00000000	Configuration register 11 (H4)	328
OR#Conf12	53	C 7	0010101	Configuration register 12 (RDI control)	329
OR#Conf13	54	C 3	000	Configuration register 13 (Telecom Bus control)	330
GRA	100-3FF			Growable Register Array (TOH)	330

OFP_Rx1/2/3/4 (OR1/2/3/4) Counters

OR#ROFmid: Read-on-the-fly register.

Table 234. OR#ROFmid [2800 H, 2C00 H, 3000 H, 3400 H]

Signal Name	Bit Pos.	Access	Default	Description
OR#ROFmid(7:0)	7:0	R	00000000	Read-on-the-fly register

OR#Cnt1:B1BITC: Number of BIP-8 B1 bit errors counted since last counter reset. Counter overflow leads to an interrupt request.

OR#Th11:B1BITCTh1: Threshold for number of BIP-8 B1 bit errors (MSByte).

OR#Th12:B1BITCTh2: Threshold for number of BIP-8 B1 bit errors (LSByte).

Threshold equaled leads to an interrupt request.

Table 235. OR#Cnt1:B1BITC, OR#Th11:B1BITCTh1, OR#Th12:B1BITCTh2 [2804 H / 2805 H, 2C04 H / 2C05 H, 3004 H / 3005 H, 3404 H / 3405 H, 2807 H, 2C07 H, 3007 H, 3407 H, 2806 H, 2C06 H, 3006 H, 3406 H]

Signal Name	Bit Pos.	Access	Default	Description
B1BITC(7:0)	7:0	R	00000000	BIP-8 B1 bit error counter (LSByte)
B1BITCTh11(7:0)	7:0	R/W	01111101	Threshold for BIP-8 B1 bit error counter (MSByte)
B1BITCTh12(7:0)	7:0	R/W	00000000	Threshold for BIP-8 B1 bit error counter (LSByte)

OR#Cnt2:B1BLKC: Number of BIP-8 B1 block errors counted since last counter reset. Counter overflow leads to an interrupt request.

OR#Th21:B1BLKCTh1: Threshold for number of BIP-8 B1 block errors (MSByte).

OR#Th22:B1BLKCTh2: Threshold for number of BIP-8 B1 block errors (LSByte).

Threshold equaled leads to an interrupt request.

Table 236. OR#Cnt2:B1BLKC, OR#Th21:B1BLKCTh1, OR#Th22:B1BLKCTh2 [2808 H / 2809 H, 2C08 H / 2C09 H, 3008 H / 3009 H, 3408 H / 3409 H, 280B H, 2C0B H, 300B H, 340B H, 280A H, 2C0A H, 300A H, 340A H]

Signal Name	Bit Pos.	Access	Default	Description
B1BLKC(7:0)	7:0	R	00000000	BIP-8 B1 block error counter (LSByte)
B1BLKCTh1(7:0)	7:0	R/W	01111101	Threshold for BIP-8 B1 block error counter (MSByte)
B1BLKCTh2(7:0)	7:0	R/W	00000000	Threshold for BIP-8 B1 block error counter (LSByte)

OR#Cnt3:B2BITC: Number of BIP-24 B2 bit errors counted since last counter reset. Counter overflow leads to an interrupt request. In STS-12, STS-12c, STM-4, and STM-4c modes of operation, only OR3Cnt3:B2BITC is active.

OR#Th31d:B2BITCTh1d: Degradation threshold for number of BIP-24 B2 bit errors (MSByte).

OR#Th32d:B2BITCTh2d: Degradation threshold for number of BIP-24 B2 bit errors (LSByte).

Threshold equaled leads to an interrupt request.

OR#Th31f:B2BITCTh1f: Failure threshold for number of BIP-24 B2 bit errors (MSByte).

OR#Th32f:B2BITCTh2f: Failure threshold for number of BIP-24 B2 bit errors (LSByte).

Threshold equaled leads to an interrupt request.

Table 237. OR#Cnt3:B2BITC, OR#Th31d:B2BITCTh1d, OR#Th32d:B2BITCTh2d, OR#Th31f:B2BITCTh1f, OR#Th32f:B2BITCTh2f [280C H / 280D H, 2C0C H / 2C0D H, 300C H / 300D H, 340C H / 340D H, 280F H, 2C0F H, 300F H, 340F H, 280E H, 2C0E H, 300E H, 340E H, 2811 H, 2C11 H, 3011 H, 3411 H, 2810 H, 2C10 H, 3010 H, 3410 H]

Signal Name	Bit Pos.	Access	Default	Description
B2BITC(7:0)	7:0	R	00000000	BIP-24 B2 bit error counter (LSByte)
B2BITCTh1d(7:0)	7:0	R/W	01001110	Degradation threshold for BIP-24 B2 bit error counter (MSByte)
B2BITCTh2d(7:0)	7:0	R/W	00100000	Degradation threshold for BIP-24 B2 bit error counter (LSByte)
B2BITCTh1f(7:0)	7:0	R/W	01111101	Failure threshold for BIP-24 B2 bit error counter (MSByte)
B2BITCTh2f(7:0)	7:0	R/W	00000000	Failure threshold for BIP-24 B2 bit error counter (LSByte)

OR#Cnt4:B2BLKC: Number of BIP-24 B2 block errors counted since last counter reset. Counter overflow leads to an interrupt request. In STS-12, STS-12c, STM-4, and STM-4c modes of operation, only OR3Cnt4:B2BLKC is active.

OR#Th41d:B2BLKCTh1d: Degradation threshold for number of BIP-24 B2 block errors (MSByte).

OR#Th42d:B2BLKCTh2d: Degradation threshold for number of BIP-24 B2 block errors (LSByte).

Threshold equaled leads to an interrupt request.

OR#Th41f:B2BLKCTh1f: Failure threshold for number of BIP-24 B2 block errors (MSByte).

OR#Th42f:B2BLKCTh2f: Failure threshold for number of BIP-24 B2 block errors (LSByte).

Threshold equaled leads to an interrupt request.

Table 238. OR#Cnt4:B2BLKC, OR#Th41d:B2BLKCTh1d, OR#Th42d:B2BLKCTh2d, OR#Th41f:B2BLKCTh1f, OR#Th42f:B2BLKCTh2f [2812 H / 2813 H, 2C12 H / 2C13 H, 3012 H / 3013 H, 3412 H / 3413 H, 2815 H, 2C15 H, 3015 H, 3415 H, 2814 H, 2C14 H, 3014 H, 3414 H, 2817 H, 2C17 H, 3017 H, 3417 H, 2816 H, 2C16 H, 3016 H, 3416 H]

Signal Name	Bit Pos.	Access	Default	Description
B2BLKC(7:0)	7:0	R	00000000	BIP-24 B2 block error counter (LSByte)

Table 238. OR#Cnt4:B2BLKC, OR#Th41d:B2BLKCTh1d, OR#Th42d:B2BLKCTh2d, OR#Th41f:B2BLKCTh1f, OR#Th42f:B2BLKCTh2f [2812 H / 2813 H, 2C12 H / 2C13 H, 3012 H / 3013 H, 3412 H / 3413 H, 2815 H, 2C15 H, 3015 H, 3415 H, 2814 H, 2C14 H, 3014 H, 3414 H, 2817 H, 2C17 H, 3017 H, 3417 H, 2816 H, 2C16 H, 3016 H, 3416 H] (Continued)

Signal Name	Bit Pos.	Access	Default	Description
B2BLKCTh1d(7:0)	7:0	R/W	01001110	Degradation threshold for BIP-24 B2 block error counter (MSByte)
B2BLKCTh2d(7:0)	7:0	R/W	00100000	Degradation threshold for BIP-24 B2 block error counter (LSByte)
B2BLKCTh1f(7:0)	7:0	R/W	01111101	Failure threshold for BIP-24 B2 block error counter (MSByte)
B2BLKCTh2f(7:0)	7:0	R/W	00000000	Failure threshold for BIP-24 B2 block error counter (LSByte)

OR#Cnt5:B3BITC: Number of BIP-8 B3 bit errors counted since last counter reset. Counter overflow leads to an interrupt request.

OR#Th51:B3BITCTh1: Threshold for number of BIP-8 B3 bit errors (MSByte).

OR#Th52:B3BITCTh2: Threshold for number of BIP-8 B3 bit errors (LSByte).

Threshold equaled leads to an interrupt request.

Table 239. OR#Cnt5:B3BITC, OR#Th51:B3BITCTh1, OR#Th52:B3BITCTh2 [2818 H / 2819 H, 2C18 H / 2C19 H, 3018 H / 3019 H, 3418 H / 3419 H, 281B H, 2C1B H, 301B H, 341B H, 281A H, 2C1A H, 301A H, 341A H]

Signal Name	Bit Pos.	Access	Default	Description
B3BITC(7:0)	7:0	R	00000000	BIP-8 B3 bit error counter (LSByte)
B3BITCTh1(7:0)	7:0	R/W	01111101	Threshold for BIP-8 B3 bit error counter (MSByte)
B3BITCTh2(7:0)	7:0	R/W	00000000	Threshold for BIP-8 B3 bit error counter (LSByte)

OR#Cnt6:B3BLKC: Number of BIP-8 B3 block errors counted since last counter reset. Counter overflow leads to an interrupt request.

OR#Th61:B3BLKCTh1: Threshold for number of BIP-8 B3 block errors (MSByte).

OR#Th62:B3BLKCTh2: Threshold for number of BIP-8 B3 block errors (LSByte).

Threshold equaled leads to an interrupt request.

Table 240. OR#Cnt6:B3BLKC, OR#Th61:B3BLKCTh1, OR#Th62:B3BLKCTh2 [281C H / 281D H, 2C1C H / 2C1D H, 301C H / 301D H, 341C H / 341D H, 281F H, 2C1F H, 301F H, 341F H, 281E H, 2C1E H, 301E H, 341E H]

Signal Name	Bit Pos.	Access	Default	Description
B3BLKC(7:0)	7:0	R	00000000	BIP-8 B3 block error counter (LSByte)
B3BLKCTh1(7:0)	7:0	R/W	01111101	Threshold for BIP-8 B3 block error counter (MSByte)
B3BLKCTh2(7:0)	7:0	R/W	00000000	Threshold for BIP-8 B3 block error counter (LSByte)

OR#Cnt7:MSREIC: Multiplex Section Remote Error Indication counter. Counter overflow leads to an interrupt request. In STS-12, STS-12c, STM-4, and STM-4c modes of operation only OR3Cnt7:MSREIC should be enabled via the EN-MSREICNT control bit in the OR3Cnten1 control register.

OR#Th71:MSREICTh1: Threshold for number of Multiplex Section Remote Errors (MSByte).

OR#Th72:MSREICTh2: Threshold for number of Multiplex Section Remote Errors (LSByte).

Threshold equaled leads to an interrupt request.

Table 241. OR#Cnt7:MSREIC, OR#Th71:MSREICTh1, OR#Th72:MSREICTh2 [2820 H / 2821 H, 2C20 H / 2C21 H, 3020 H / 3021 H, 3420 H / 3421 H, 2823 H, 2C23 H, 3023 H, 34123 H, 2822 H, 2C22 H, 3022 H, 3422 H]

Signal Name	Bit Pos.	Access	Default	Description
MSREIC(7:0)	7:0	R	00000000	Multiplex Section Remote Error Indication counter (LSByte)
MSREICTh1(7:0)	7:0	R/W	01111101	Threshold for Multiplex Section Remote Error Indication counter (MSByte)
MSREICTh2(7:0)	7:0	R/W	00000000	Threshold for Multiplex Section Remote Error Indication counter (LSByte)

OR#Cnt8:HPREIC: Higher-order Path Remote Error Indication counter. Counter overflow leads to an interrupt request.

OR#Th81:HPREICTh1: Threshold for number of Higher-order Path Remote Errors (MSByte).

OR#Th82:HPREICTh2: Threshold for number of Higher-order Path Remote Errors (LSByte).

Threshold equaled leads to an interrupt request.

Table 242. OR#Cnt8:HPREIC, OR#Th81:HPREICTh1, OR#Th82:HPREICTh2 [2824 H / 2825 H, 2C24 H / 2C25 H, 3024 H / 3025 H, 3424 H / 3425 H, 2827 H, 2C27 H, 3027 H, 3427 H, 2826 H, 2C26 H, 3026 H, 3426 H]

Signal Name	Bit Pos.	Access	Default	Description
HPREIC(7:0)	7:0	R	00000000	Higher-order Path Remote Error Indication counter (LSByte)
HPREICTh1(7:0)	7:0	R/W	01111101	Threshold for Higher-order Path Remote Error Ind. counter (MSByte)
HPREICTh2(7:0)	7:0	R/W	00000000	Threshold for Higher-order Path Remote Error Ind. counter (LSByte)

OR#Cnt9:PJ_EVCNT: Positive Justification Event counter. Counter overflow leads to an interrupt request.

Table 243. OR#Cnt9:PJ_EVCNT [2828 H / 2829 H, 2C28 H / 2C29 H, 3028 H / 3029 H, 3428 H / 3429 H]

Signal Name	Bit Pos.	Access	Default	Description
PJ_EVCNT(7:0)	7:0	R	00000000	Positive Justification Event counter

OR#Cnt10:NJ_EVCNT: Negative Justification Event counter. Counter overflow leads to an interrupt request.

Table 244. OR#Cnt10:NJ_EVCNT [282A H / 282B H, 2C2A H / 2C2B H, 302A H / 302B H, 342A H / 342B H]

Signal Name	Bit Pos.	Access	Default	Description
NJ_EVCNT(7:0)	7:0	R	00000000	Negative Justification Event counter

OR#Cnt11:ND_EVCNT: New Data Event counter. Counter overflow leads to an interrupt request.

Table 245. OR#Cnt11:ND_EVCNT [282C H / 282D H, 2C2C H / 2C2D H, 302C H / 302D H, 342C H / 342D H]

Signal Name	Bit Pos.	Access	Default	Description
ND_EVCNT(7:0)	7:0	R	00000000	New Data Event counter

OR#CntEn1: Counter On/Off control register 1 for OFP_Rx1/2/3/4

For each bit position:

0: Counter is disabled

1: Counter is enabled

Table 246. OR#Cnten1 [2802 H, 2C02 H, 3002 H, 3402 H]

Signal Name	Bit Pos.	Access	Default	Description
EN-B1BITCNT	0	R/W	0	BIP-8 B1 bit error counter enable
EN-B1BLKCNT	1	R/W	0	BIP-8 B1 block error counter enable
EN-B2BITCNT	2	R/W	0	BIP-24 B2 bit error counter enable
EN-B2BLKCNT	3	R/W	0	BIP-24 B2 block error counter enable
EN-B3BITCNT	4	R/W	0	BIP-8 B3 bit error counter enable
EN-B3BLKCNT	5	R/W	0	BIP-8 B3 block error counter enable
EN-MSREICNT	6	R/W	0	Multiplex Section Remote Error Indication counter enable
EN-HPREICNT	7	R/W	0	Higher-order Path Remote Error Indication counter enable

OR#CntEn2: Counter On/Off control register 2 for OFP_Rx1/2/3/4

For each bit position:

0: Counter is disabled

1: Counter is enabled

Table 247. OR#CntEn2 [2803 H, 2C03 H, 3003 H, 3403 H]

Signal Name	Bit Pos.	Access	Default	Description
EN-PJ_EVCNT	0	R/W	0	Positive Justification Event counter enable
EN-NJ_EVCNT	1	R/W	0	Negative Justification Event counter enable
EN-ND_EVCNT	2	R/W	0	New Data Event counter enable
Reserved	7:3			Not used

OFP_Rx1/2/3/4 (OR1/2/3/4) Reset Registers

OR#RESET: Reset chiplet control registers. These registers are automatically preset to the default value by the reset signals ResOR1/2/3/4 from the GPPINT.

For each bit position:

0: Reset not active

1: Reset active

Table 248. OR#RESET [2830 H, 2C30 H, 3030 H, 3430 H]

Signal Name	Bit Pos.	Access	Default	Description
Reset	0	R/W	1	Reset (disable) OFP_Rx1/2/3/4 chiplet.
Reserved	7:1			Not used

OFP_Rx1/2/3/4 Status Registers

OR#Stat1: Status register 1 of the chiplet. OFP_Rx Mode status information. This is an event latch register.

Table 249. OR#Stat1 [2833 H, 2C33 H, 3033 H, 3433 H]

Signal Name	Bit Pos.	Access	Default	Description
Mode(2:0)	2:0	R/W		Mode: XXB: 0=All macros are independent. 1= multi-macros act together but are non-concatenated (e.g., STM-4/STS-12). XBX: 0= Non-concatenation mode. 1= concatenation mode. BXX: 0= single-chip operation. 1= multi-chip operation. X10 and 1X0 are not allowed.
Reserved	7:3			Not used

OR#Stat2: Status register 2 of the chiplet. AU pointer status information of OFP_Rx. This is an event latch register.

Table 250. OR#Stat2 [2834 H, 2C34 H, 3034 H, 3434 H]

Signal Name	Bit Pos.	Access	Default	Description
Njus	0	R/W		Negative frequency justification received
Pjus	1	R/W		Positive frequency justification received
NDF	2	R/W		NDF received. An NDF is detected when a 1001, 0001, 1101, 1011, or a 1000 are detected in the NDF field of the received pointer.
InvPtr	3	R/W		Invalid Pointer received
NewPtr	4	R/W		Valid New Pointer received
CONCrx	5	R/W		Concatenation indication received. This bit indicates that a concatenation indication was received for this chiplet. This bit is valid only for RX OFP chiplets 2-4 and should be ignored in the OR1Stat2 register.
LOP	6	R/W		Loss of pointer event for this specific chiplet. When an STM-4c/STS-12c is being processed, this bit indicates a LOPC [annex C of G.783] in RX OFP chiplets 2-4 or LOP in RX OFP chiplet 1. Otherwise, for 1xSTM-4/STS-12 or for 4 x STM-1/STS-3c, this bit indicates LOP for its respective AU-n (n=4).
PtrAIS	7	R/W		Pointer AIS event for this specific chiplet. When an STM-4c/STS-12c is being processed, this bit indicates that the AISC state has been entered [annex C of G.783] in RX OFP chiplets 2-4 or the AIS state in RX OFP chiplet 1 has been entered. Otherwise, for 1xSTM-4/STS-12 or for 4 x STM-1/STS-3c, this bit indicates that the AIS state for its respective AU-n (n=4) has been entered.

OFP_Rx1/2/3/4 Interrupt Request and Mask Registers

OR#MainIRQ: Register to indicate fatal interrupt events and to point to user IRQ registers with active requests; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

Bits 0 in this register is “one shot”, i.e., set by a pulse, or by a condition which is unlikely to be persistent.

Bits 1-7 in this register persist as long as the triggering condition persists. i.e., If an interrupt request bit is read, the bit will clear and become set again in one RX SFH byte clock cycle, if the corresponding condition persists.

OR#M_MainIRQ: Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates signal IRQOR1/2/3/4 to GPPINT

Table 251. OR#MainIRQ, OR#M_MainIRQ
[2838 H, 2C38 H, 3038 H, 3438 H, 2839 H, 2C39 H, 3039 H, 3439 H]

Signal Name	Bit Pos.	Access	Default	Description
Fatal	0	R/W	0	Fatal event occurred
CntIRQ1	1	R/W	0	Active request in OR#CntIRQ1 register
CntIRQ2	2	R/W	0	Active request in OR#CntIRQ2 register
CntIRQ3	3	R/W	0	Active request in OR#CntIRQ3 register
IRQ1	4	R/W	0	Active request in IRQ1 register
IRQ2	5	R/W	0	Active request in IRQ2 register
IRQ3	6	R/W	0	Active request in IRQ3 register
Reserved	7			Not used

OR#CntIRQ1: Register 1 to indicate active counter interrupt requests of this chiplet; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

All bits in this register are “one shot”, i.e., set by a pulse, or by a condition which is unlikely to be persistent.

OR#M_CntIRQ1: Register to mask pending counter interrupt requests; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in OR#MainIRQ register

Table 252. OR#CntIRQ1, OR#M_CntIRQ1
[283A H, 2C3A H, 303A H, 343A H, 283B H, 2C3B H, 303B H, 343B H]

Signal Name	Bit Pos.	Access	Default	Description
OV-B1BITCNT	0	R/W	0	Overflow BIP-8 B1 bit error counter
TH-B1BITCNT	1	R/W	0	Threshold equaled BIP-8 B1 bit error counter
OV-B1BLKCNT	2	R/W	0	Overflow BIP-8 B1 block error counter
TH-B1BLKCNT	3	R/W	0	Threshold equaled BIP-8 B1 block error counter
OV-B2BITCNT	4	R/W	0	Overflow BIP-24 B2 bit error counter
TH-B2BITCNT	5	R/W	0	Signal Degradation threshold equaled BIP-24 B2 bit error counter
T2-B2BITCNT	6	R/W	0	Signal Failure threshold equaled BIP-24 B2 bit error counter
OV-B2BLKCNT	7	R/W	0	Overflow BIP-24 B2 block error counter

OR#CntIRQ2: Register 2 to indicate active counter interrupt requests of this chiplet; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

All bits in this register are “one shot”, i.e., set by a pulse, or by a condition which is unlikely to be persistent.

OR#M_CntIRQ2: Register to mask pending counter interrupt requests; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in OR#MainIRQ register

Table 253. OR#CntIRQ2, OR#M_CntIRQ2
[283C H, 2C3C H, 303C H, 343C H, 283D H, 2C3D H, 303D H, 343D H]

Signal Name	Bit Pos.	Access	Default	Description
TH-B2BLKCNT	0	R/W	0	Signal Degradation threshold equaled p BIP-24 B2 block error counter
T2-B2BLKCNT	1	R/W	0	Failure threshold equaled BIP-24 B2 block error counter
OV-B3BITCNT	2	R/W	0	Overflow BIP-8 B3 bit error counter
TH-B3BITCNT	3	R/W	0	Threshold equaled BIP-8 B3 bit error counter
OV-B3BLKCNT	4	R/W	0	Overflow BIP-8 B3 block error counter
TH-B3BLKCNT	5	R/W	0	Threshold equaled BIP-8 B3 block error counter
OV-MSREICNT	6	R/W	0	Overflow MS Remote Error Indication counter
TH-MSREICNT	7	R/W	0	Threshold equaled MS Remote Error Indication counter

OR#CntIRQ3: Register 3 to indicate active counter interrupt requests of this chiplet; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

All implemented bits in this register are “one shot”, i.e., set by a pulse, or by a condition which is unlikely to be persistent.

OR#M_CntIRQ3: Register to mask pending counter interrupt requests; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in OR#MainIRQ register

Table 254. OR#CntIRQ3, OR#M_CntIRQ3
[283E H, 2C3E H, 303E H, 343E H, 283F H, 2C3F H, 303F H, 343F H]

Signal Name	Bit Pos.	Access	Default	Description
OV-HPREICNT	0	R/W	0	Overflow HPREI error indication counter
TH-HPREICNT	1	R/W	0	Threshold equaled Higher-order Path Remote Error Indication counter
OV-PJ_EVCNT	2	R/W	0	Overflow Positive Justification event counter
OV-NJ_EVCNT	3	R/W	0	Overflow Negative Justification event counter
OV-ND_EVCNT	4	R/W	0	Overflow New Data event counter
Reserved	7:5			Not used

OR#IRQ1: Register to indicate active user interrupt requests of this chiplet; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

All bits in this register are “one shot”, i.e., set by a pulse, or by a condition which is unlikely to be persistent.

OR#M_IRQ1: Register to mask pending user interrupt requests; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in OR#MainIRQ register

Table 255. OR#IRQ1, OR#M_IRQ1 [2840 H, 2C40 H, 3040 H, 3440 H, 2841 H, 2C41 H, 3041 H, 3441 H]

Signal Name	Bit Pos.	Access	Default	Description
HPREI	0	R/W	0	Higher-order Path Remote Error Indication. Received HP-REI values larger than 8 do not cause this bit to become set.
S1chg	1	R/W	0	Synchronization Status changed. If the received S1 byte differs from the expected S1 byte in OR#Conf10 for five consecutive frames then this interrupt bit becomes set. When the received S1 byte matches the expected S1 byte in OR#Conf10 for five consecutive frames then the interrupt signal to set this bit is removed. Please note that all 8 bits of the receive S1 byte and all 8 bits of the SMexpct(7:0) register are used in the comparison.
FrmErr	2	R/W	0	Framing error detected. This bit is set when the internally generated start of frame pulses become misaligned such as could happen when the OOF state is entered and exited again.
SDBfull	3	R/W	0	SDB_Rx FIFO full. This bit should never become set under normal operating conditions. This bit becomes set when the RX APH block is running with a clock whose frequency is less than that of the corresponding RX SFH block. This bit has no meaning in Telecom Bus mode and is disabled, and thus it should be masked off in that case. When this bit becomes set, the recovery process is automatic, provided that the condition that caused this bit to become set is removed. Should recovery not occur automatically, then a global reset of the ACH_Rx# chiplet may need to be performed.
H4chg	4	R/W	0	Unexpected H4 byte received. If the received H4 byte differs from the expected H4 byte in OR#Conf11 for five consecutive frames then this interrupt bit becomes set. When the received H4 byte matches the expected H4 byte in OR#Conf11 for five consecutive frames then the interrupt signal to set this bit is removed.
Reserved	7:5			Not used

OR#IRQ2: Register to indicate active user interrupt requests of this chiplet; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

All interrupt request bits in this register persist as long as the triggering condition persists. i.e., If an interrupt request bit is read, the bit will clear and become set again in one RX SFH byte clock cycle, if the corresponding condition persists.

OR#M_IRQ2: Register to mask pending user interrupt requests; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in OR#MainIRQ register

Table 256. OR#IRQ2, OR#M_IRQ2 [2842 H, 2C42 H, 3042 H, 3442 H, 2843 H, 2C43 H, 3043 H, 3443 H]

Signal Name	Bit Pos.	Access	Default	Description
SLM	0	R/W	0	Signal label mismatch alarm. When the received C2 byte does not match the expected C2 value in the OR#Conf9 register or 01 H for five consecutive frames, then this bit is asserted. When the received C2 byte equals the expected C2 value in OR#Conf9 or 01H for five consecutive frames, then the signal label mismatch condition is terminated. 00 H is not regarded as a signal label mismatch regardless of the setting of the OR#Conf9 register.
UNEQ	1	R/W	0	Unequipped signal. When the received C2 byte equals 00 H for five consecutive frames, then this bit is asserted. When the received C2 byte equals any non-zero value for five consecutive frames, then the unequipped signal condition is terminated. When UNEQ is declared in ATM/PPP mode, C-y data is not forwarded to the SDB FIFOs. y=4 for 4xSTM-1/STS-3c and 1xSTM-4/STS-12 modes, and y=4-4c for 1xSTM-4c/STS-12 modes.
HPRDI	2	R/W	0	Higher-order path RDI: This bit is set when either 1XX or 010 is received in the RDI bit positions for five consecutive frames. The HPRDI condition is terminated when an 00X or 011 is detected in the RDI bits for five consecutive frames. The HPRDI condition is not checked for when an PtrAIS or LOP condition is received.
PtrAIS	3	R/W	0	Pointer AIS. When an STM-4c/STS-12c is being processed, and RX OFP1 enters the AIS state or RX OFP2, 3, or 4, enters the AIS state, then the PtrAIS bit in RX OFP1 will be set to a 1. Also, the chiplet(s) where the alarm occurred will also have their PtrAIS bit(s) set to a 1. Therefore, if this bit is set to 1 in RX OFP 1, the OR#Stat2 register should be read to determine in which RX OFP chiplets that the alarm(s) actually occurred in. For 1xSTM-4/STS-12 or for 4 x STM-1/STS-3c modes, this bit indicates PtrAIS for its respective AU-y in its respective RX OFP chiplet. y=4 for 4xSTM-1/STS-3c and 1xSTM-4/STS-12 mode.

Table 256. OR#IRQ2, OR#M_IRQ2 [2842 H, 2C42 H, 3042 H, 3442 H, 2843 H, 2C43 H, 3043 H, 3443 H]

Signal Name	Bit Pos.	Access	Default	Description
LOP	4	R/W	0	Loss of pointer alarm. When an STM-4c/STS-12c is being processed, and an LOP is detected in RX OFP1 or an LOPC [annex C of G.783] is detected in RX OFP2, 3, or 4, then the LOP bit in RX OFP1 will bet set to a 1. Also, the chiplet(s) where the alarm occurred will also have their LOP bit(s) set to a 1. Therefore, if this bit is set to 1 in RX OFP 1, the OR#Stat2 register should be read to determine in which RX OFP chiplets that the alarm(s) actually occurred in. For 1xSTM-4/STS-12 or for 4 x STM-1/STS-3c modes, this bit indicates LOP for its respective AU-y in its respective RX OFP chiplet. y=4 for 4xSTM-1/STS-3c and 1xSTM-4/STS-12 mode.
LOF	5	R/W	0	Loss of frame alarm. This bit becomes set when the OOF condition exists for x milliseconds, where x is determined by the OUTnum(1:0) register setting.
LOS	6	R/W	0	Loss of signal alarm. This bit is set when the corresponding LOSSSIG# lead is asserted. The internal LOS condition (that sets this bit and causes RX Line AIS and TX Line RDI to be generated), will terminate when the LOSSSIG# lead goes inactive and two valid framing patterns are detected, provided that the LOSSSIG# lead does not go active between those two frame patterns. The polarity of the LOSSSIG# leads are determined by the Invert_LOS bit in the PIMRConf1 register.
OOF	7	R/W	0	Out of frame alarm. The Algo#(1:0) bits indicate how this alarm is declared. The internal OOF condition is terminated when two good framing patterns are detected.

OR#IRQ3: Register to indicate active user interrupt requests of this chiplet; for each bit position:

0: No interrupt request pending

1: Interrupt request pending

Bits 0 and 3-5 in this register are “one shot”, i.e., set by a pulse, or by a condition which is unlikely to be persistent.

Bits 1, 2, 6, and 7 in this register persist as long as the triggering condition persists. i.e., If an interrupt request bit is read, the bit will clear and become set again in one RX SFH byte clock cycle, if the corresponding condition persists.

OR#M_IRQ3: Register to mask pending user interrupt requests; for each bit position:

0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in MainIRQ register

Table 257. OR#IRQ3, OR#M_IRQ3 [2844 H, 2C44 H, 3044 H, 3444 H, 2845 H, 2C45 H, 3045 H, 3445 H]

Signal Name	Bit Pos.	Access	Default	Description
PtrErr	0	R/W	0	Pointer processing error
HPTIM	1	R/W	0	Higher-order path trace identifier mismatch. HPTIM detection is enabled regardless of the Bellcore bit setting. This bit is also set if the TIM_uP bit in OR#Conf12 is set.
STIM	2	R/W	0	Section trace identifier mismatch.
MSPRR	3	R/W	0	Multiplex Section protection release request. This bit signals a request to the external microprocessor interface to release the switch. i.e., the data stream is no longer received on the protection channel. This bit is set when the channel indicated by the received K2 byte does not match the channel indicated by the shadow K1 byte (K1shdrx(7:0)). Once this interrupt request is cleared by reading this bit or writing a 1 to it, it will not become set if the original condition that caused the interrupt is still present.
MSPSR	4	R/W	0	Multiplex Section protection switch request. This bit signals a request to the external microprocessor to read the K2 byte to find the working channel (number) which must be switched to protection. This bit is set when the channel number in the corresponding K1 shadow register (K1shdrx(7:0)) matches the channel number in the received K2 byte and bit 3 of the transmitted K2 byte matches bit 3 of the received K2 byte, and the channel in the received K2 byte is not 0 and the protection channel is fail free (i.e., no signal degrade or signal fail detected). Once this interrupt request is cleared by reading this bit or writing a 1 to it, it will not become set if the original condition that caused the interrupt is still present.

Table 257. OR#IRQ3, OR#M_IRQ3 [2844 H, 2C44 H, 3044 H, 3444 H, 2845 H, 2C45 H, 3045 H, 3445 H]

Signal Name	Bit Pos.	Access	Default	Description
MSPBR	5	R/W	0	Multiplex Section protection bridge request. This bit signals a request to the external microprocessor to read the K1 byte to find the working channel (number) which must be bridged to protection. This interrupt is set when the received K1 request is of a higher or equal priority than that in the corresponding shadow register (K1shdrx(7:0) in register OR#Conf5). Since this bit becomes set when a bridge request is received, of an equal priority to that of the current request, the software must ignore this situation. Once this interrupt request is cleared by reading this bit or writing a 1 to it, it will not become set if the original condition that caused the interrupt is still present.
MSRDI	6	R/W	0	Multiplex Section RDI. Bellcore=0: MSRDI is declared/terminated upon receiving/not receiving three consecutive K2 bytes where bits 6, 7 and 8 equal 110. Bellcore=1: MSRDI is declared/terminated upon receiving/not receiving five consecutive K2 bytes where bits 6, 7 and 8 equal 110.
MSAIS	7	R/W	0	Multiplex Section AIS. Bellcore=0: MSAIS is declared/terminated upon receiving/not receiving three consecutive K2 bytes where bits 6, 7 and 8 equal 111. Bellcore=1: MSAIS is declared/terminated upon receiving/not receiving five consecutive K2 bytes where bits 6, 7 and 8 equal 111. When MSAIS is declared in ATM/PPP mode, C-y data is not forwarded to the SDB FIFOs when the All1En control bit is set to a 1. y=4 for 4xSTM-1/STS-3c and 1xSTM-4/STS-12 modes, and y=4-4c for 1xSTM-4c/STS-12c modes.

OFP_Rx1/2/3/4 Configuration Registers

OR#Conf1: Configuration register 1. General OFP_Rx configuration signals.

Table 258. OR#Conf1 [2848 H, 2C48 H, 3048 H, 3448 H]

Signal Name	Bit Pos.	Access	Default	Description
AutRst_Int	0	R/W	1	0: No action on read access. 1: Auto-reset interrupt request registers upon read access. Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a 1 to that bit provided that the corresponding alarm condition is removed.
AutRst_Sta	1	R/W	1	0: No action on read access 1: Auto-reset all bits in the OR#Stat1 and OR#Stat2 status registers upon read access
GRAen	2	R/W	1	0: Do not write SOH/POH to GRA 1: Write received SOH/POH to GRA

Table 258. OR#Conf1 [2848 H, 2C48 H, 3048 H, 3448 H] (Continued)

Signal Name	Bit Pos.	Access	Default	Description
FIFOen	3	R/W	1	0: Do not write C-y payload to RX SDB FIFO 1: Write C-y payload to RX SDB FIFO y=4 for 4xSTM-1/STS-3c and 1xSTM-4/STS-12 modes, and y=4-4c for 1xSTM-4c/STS-12c modes.
J0GRA	4	R/W	1	0: Do not write J0 section trace to GRA 1: Write J0 section trace to GRA
J1GRA	5	R/W	1	0: Do not write J1 section trace to GRA 1: Write J1 section trace to GRA
Bellcore	6	R/W	0	0: Operate according to ITU-T standard 1: Operate according to Bellcore specs
ResHunt	7	R/W	0	0: Hunt free running. 1: Reset Hunt to PIM. This setting forces a re synchronization to the framing pattern (i.e., A1/A2 bytes). This bit must be returned to 0.

OR#Conf2: Configuration register 2. SOH processing configuration signals.

Table 259. OR#Conf2 [2849 H, 2C49 H, 3049 H, 3449 H]

Signal Name	Bit Pos.	Access	Default	Description
J0proc	0	R/W	0	0: Disable J0 section trace processing. The STIM interrupt request bit is forced to 0. 1: Enable J0 section trace processing The operation of this bit is independent of the Bellcore bit setting.
M1en	1	R/W	0	0: Disable M1 REI processing. The transmitted M1 byte is always forced to 00H. Automatic TX Line RDI generation is disabled. The line REI and RDI fields on the RX Ring Port output are forced to all 0s. 1: Enable M1 REI processing and automatic TX Line RDI generation. In 1xSTM-4/STM-4c/STS-12/STS-12c modes this bit only needs to be set in SFH 3.
S1en	2	R/W	0	0: Disable S1 synchronization status processing. The S1chg interrupt request bit is forced to 0. 1: Enable S1 synchronization status processing
K2en	3	R/W	0	0: Disable K2 AIS/RDI processing. MSAIS and MSRDI bits are not active. Also, generation of all 1s AIS downstream is inhibited. Generation of line RDI in the transmit direction due to the detection of MSAIS is also inhibited. The MSPRR and MSPSR interrupt request bits are forced to 0. 1: Enable K2 AIS/RDI processing. The setting of this bit does not affect the transfer of the K1 or K2 bytes across the Ring Port.

Table 259. OR#Conf2 [2849 H, 2C49 H, 3049 H, 3449 H] (Continued)

Signal Name	Bit Pos.	Access	Default	Description
K1en	4	R/W	0	0: Disable K1 and first 5 msbs of K2 APS processing. The debounced K1/K2 bytes are forced to 0. The new APS Indication on the RX Ring Port output is forced to 0. The NewAPS bit in OT#IRQ2 is forced to 0. 1: Enable K1 APS processing
Pchan	5	R/W	0	This bit is used to indicate which channel is the protection channel as follows: 0: RX SFH# is working channel (#=1...4) 1: RX SFH# is protection channel (#=1...4) The K1 bytes of the working channels are ignored, inconsistent K1 detection (APS_Incon, bit 4 of OT#IRQ2) is active only if this bit is set to 1.
All1En	6	R/W	0	0: Disable all 1s data path forwarding. When a RX PtrAIS is received or all 1s AIS is to be generated downstream, the received SONET/SDH frame data is passed to the RX SDB FIFOs and the RX Telecom Bus interfaces in place of the all 1s AIS signal. The corresponding RXTB#FAIL outputs will also go active. If an STS-3 frame is being received while in 4xSTS-3c/STM-1 mode, which contains three STS-1 SPEs, then the All1En bit should be set to 0 to allow the STS-1 SPEs along with their pointers to be passed through to the Telecom Bus so that they may be processed by an external device. In ATM/PPP mode, when a RX PtrAIS is received or all 1s AIS is to be generated downstream, the received SONET/SDH frame data is passed to the RX SDB FIFOs. The data will be processed by the APH block, possibly resulting in errors or alarm conditions being detected at the APH blocks. This bit is not recommended to be set to a 0 for ATM/PPP mode. 1: Enable all 1s data path forwarding. When terminating ATM/PPP payloads and one of the conditions shown in Figure 57 on page 156 occurs, then no C-y data is forwarded to the RX SDB FIFOs. y=4 for 4xSTM-1/STS-3c and 1xSTM-4/STS-12 modes, and y=4-4c for 1xSTM-4c/STS-12 modes. In Telecom Bus mode, when a condition shown in Figure 58 on page 157 occurs, the all 1s AIS signal is passed to the RX Telecom Bus interface and the corresponding RXTB#FAIL outputs will go active.
M1BitBlk	7	R/W	1	0: MS-REI bit error counting 1: MS-REI block error counting. This bit affects the M1 counters (OR#Cnt7:MSREIC), the transmitted M1, and the M1 that goes out over the RX RING Port.

OR#Conf3: Configuration register 3. POH byte processing configuration signals.

Table 260. OR#Conf3 [284A H, 2C4A H, 304A H, 344A H]

Signal Name	Bit Pos.	Access	Default	Description
J1proc	0	R/W	0	0: Disable J1 path trace processing 1: Enable J1 path trace processing The operation of this bit is independent of the Bellcore bit setting.
J1mode64	1	R/W	0	0: 16-byte J1 trace 1: 64-byte J1 trace The operation of this bit is independent of the Bellcore bit setting.
G1en	2	R/W	0	0: Disable G1 path status processing. The HPRDI and HPREI interrupt request bits are forced to 0. 1: Enable G1 path status processing This bit must be set to a 1 to enable path RDI to be transmitted in the TX G1 byte and to enable the “no alarm” RDI code of 001 to be generated when no alarms are detected.
C2en	3	R/W	0	0: Disable C2 signal label processing 1: Enable C2 signal label processing
G1BitBlk	4	R/W	0	0: P-REI bit error counting 1: P-REI block error counting. This bit affects the Path FEBE counters (OR#Cnt8:HPREIC), the transmitted path FEBE and the path FEBE that goes out over the RX RING Port.
JusITU	5	R/W	1	Perform Increment/Decrement decoding based on: 0: 8-of-10 majority vote 1: ITU-T G.707
H4en	6	R/W	0	0: Disable H4 byte processing 1: Enable H4 byte processing
K3en	7	R/W	0	0: Disable K3 byte processing 1: Enable K3 byte processing

OR#Conf4: Configuration register 4. APS processing configuration signals.

Table 261. OR#Conf4 [284B H, 2C4B H, 304B H, 344B H]

Signal Name	Bit Pos.	Access	Default	Description
ChNum(3:0)	3:0	R/W	0000	Channel Number. These bits are not used by the PHAST-12E. They are provided to allow the software to indicate a channel number.

Table 261. OR#Conf4 [284B H, 2C4B H, 304B H, 344B H] (Continued)

Signal Name	Bit Pos.	Access	Default	Description
Prior	4	R/W	0	Priority level. 0: Low priority 1: High Priority This bit is not used by the device. This bit is provided to allow the software to indicate if this channel has a high or a low priority.
Reserved	6:5	R/W	00	Reserved
SFen	7	R/W	0	0: Disable Signal Fail K2 MS_RDI processing. 1: Enable Signal Fail K2 MS_RDI processing. When the B2 bit or block error count fail threshold is equaled an excessive error defect (EED) condition is declared. The EED condition is generated for at least 20 frames. If after the 20 frames the EED condition no longer exists the EED condition is cleared. The EED condition will persist for as long as the B2 bit or block error count fail threshold is equaled or exceeded, or for 20 frames, whichever is longer.

OR#Conf5-6: Configuration registers 5/6. Shadow registers.

Table 262. OR#Conf5-6 [284C H, 2C4C H, 304C H, 344C H, 284D H, 2C4D H, 304D H, 344D H]

Signal Name	Bit Pos.	Access	Default	Description
K1shdrx(7:0)	7:0	R/W	00000000	OR#Conf5: Shadows the K1 byte of the protection channel. This register is updated by the microprocessor to reflect the transmit K1 byte of the protection channel (i.e., after the microprocessor updates the transmit K1 byte, a copy of that K1 byte is written to this register).
K2shdrx(7:0)	7:0	R/W	00000000	OR#Conf6: Shadows the K2 byte of the protection channel. This register is updated by the microprocessor to reflect the transmit K2 byte of the protection channel after a bridge operation (i.e., after the microprocessor updates the transmit K2 byte, a copy of that K2 byte is written to this register).

OR#Conf7: Configuration register 7. Miscellaneous OFP_Rx configuration signals.

Table 263. OR#Conf7 [284E H, 2C4E H, 304E H, 344E H]

Signal Name	Bit Pos.	Access	Default	Description
INnum(1:0)	1:0	R/W	00	Number of OOF-free ms to cause loss-of-frame to in-frame transition. 00 = 0 ms Note: Do not use. 01 = 1 ms 10 = 2 ms 11 = 3 ms
OUTnum(1:0)	3:2	R/W	01	Number of ms for OOF to cause in-frame to loss-of-frame transition. 00 = 0 ms Note: Do not use. 01 = 1 ms 10 = 2 ms 11 = 3 ms
DCCen	4	R/W	0	0: Disable DCC processing 1: Enable DCC processing
OpMode	5	R/W	0	0: DCC1 channel (D1-D3) are output on RDATA# 1: DCC2 channel (D4-D12) are output on RDATA# Before changing this bit, DCCen (bit 4 of this register) should be set to a 0.
ClkMode	6	R/W	0	0: Continuous clock mode 1: Strobed clock mode (do not use this mode)
EdgeMode	7	R/W	0	0: RDATA# is launched on the falling edge of RDCLK# 1: RDATA# is launched on the rising edge of RDCLK#

OR#Conf8-11: Configuration registers 8 - 11. Pattern registers.

Table 264. OR#Conf8-11 [284F H, 2C4F H, 304F H, 344F H, 2850 H, 2C50 H, 3050 H, 3450 H, 2851 H, 2C51 H, 3051 H, 3451 H, 2852 H, 2C52 H, 3052 H, 3452 H]

Signal Name	Bit Pos.	Access	Default	Description
FSCRrx(7:0)	7:0	R/W	Default is as described to the right.	Or#Conf8: Reload pattern for frame scrambler; setting this register to all-zeros turns off the descrambler. Setting this register to its default values enables the descrambler. The following values are automatically written into the OR#Conf8 registers as the default values, based on the setting of the ADDR(2:0) leads and the GCascRx(3:0) bits as indicated; this allows the correct reload patterns for the RX descrambler to be initialized into the OR#Conf8 registers for the various modes of operation. GCascRx(3:0) = 0001,0010, 0111, 1000, ADDR(2:0) = 000: RX OFP chiplets 1-4 FE H GCascRx(3:0) = 11xx, 101x, 1001, 0011, ADDR(2:0) = 000: RX OFP chiplet 1 FE H RX OFP chiplet 2 04 H RX OFP chiplet 3 18 H RX OFP chiplet 4 51 H
SLexpct(7:0)	7:0	R/W	00010011	OR#Conf9: Expected signal label. The received C2 byte is compared to the value in this register and an internal value of 01 H to determine if a SLM alarm has occurred.
SMexpct(7:0)	7:0	R/W	00000000	OR#Conf10: Expected synchronization message. The received S1 byte is compared to the value in this register in determining if a S1chg alarm has occurred. Please note that all 8 bits of the receive S1 byte and all 8 bits of this register are used in the comparison.
H4expct(7:0)	7:0	R/W	00000000	OR#Conf11: Expected H4 byte. The received H4 byte is compared to the value in this register in determining if a H4chg alarm has occurred.

OR#Conf12: Configuration register 12. RDI control bits. The operation of the bits in this register is independent of the Bellcore bit setting.

Table 265. OR#Conf12 [2853 H, 2C53 H, 3053 H, 3453 H]

Signal Name	Bit Pos.	Access	Default	Description
SLM_RDI	0	R/W	1	0: Exclude SLM defect from TX P-RDI and RX all 1s AIS generation 1: Bellcore mode: Include SLM defect in TX P-RDI and RX all 1s AIS generation. ITU-T mode: Include SLM defect in RX all 1s AIS generation but not in TX P-RDI generation.
SLM_uP	1	R/W	0	0: NO microprocessor-enforced SLM defect 1: microprocessor-enforced SLM defect. In ITU-T mode, an RDI code of 100 is forced in the TX G1 byte to match old equipment and RX all 1s AIS is generated downstream. In Bellcore mode, an RDI code of 010 is forced in the TX G1 byte and RX all 1s AIS is generated downstream. This bit has priority over the SLM_RDI bit.
TIM_RDI	2	R/W	1	0: Exclude TIM defect from TX P-RDI and RX all 1s AIS generation 1: Include TIM defect in TX P-RDI and RX all 1s AIS generation
TIM_uP	3	R/W	0	0: NO microprocessor-enforced TIM defect 1: Microprocessor-enforced TIM defect This bit has priority over the TIM_RDI bit. The same alarm actions occur as if path TIM were detected and TIM_RDI=1. The HPTIM interrupt request bit in OR#IRQ3 also becomes set.
LCD_RDI	4	R/W	1	0: Exclude LCD defect from TX P-RDI generation. 1: Include LCD defect in TX P-RDI generation.
LCD_uP	5	R/W	0	0: NO microprocessor-enforced LCD defect 1: Microprocessor-enforced LCD defect This bit has priority over the LCD_RDI bit. The same alarm actions occur as if path LCD were detected and LCD_RDI=1.
EED_uP	6	R/W	0	0: NO microprocessor-enforced EED defect (excessive error defect) 1: Microprocessor-enforced EED defect. All 1s AIS is generated downstream.
Reserved	7			Not used

OR#Conf13: Configuration register 13. Telecom Bus control signals.

Table 266. OR#Conf13 [2854 H, 2C54 H, 3054 H, 3454 H]

Signal Name	Bit Pos.	Access	Default	Description
PAR_FULL	0	R/W	0	0: Parity over data only 1: Parity over data, J0J1, SPE, and FAIL signals
PAR_EVEN	1	R/W	0	0: Odd parity 1: Even parity
CPOS	2	R/W	0	0: RXTB#J0J1 lead indicates last A2 byte and no J1 1: RXTB#J0J1 lead indicates J0 and J1
Reserved	7:3			Not used

OFP_Rx1/2/3/4 Growable Register Array (GRA) Address Mapping

NOTE: Bytes marked as “X” are reserved for national use. The “*” character indicates bytes that are not included in frame scrambling. Therefore, care should be taken with their content. Bytes marked as “$” are media dependent bytes. All unmarked bytes are reserved for future international standardization. For STS-12/STS-12c/STM-4/STM-4c, the PHAST-12E does a demux of the bytes into the OFP_Rx# GRA.

Table 267. OFP_Rx1/2/3/4 Growable Register Array (GRA) Address Mapping [2900 H - 29BF H, 2D00 H - 2DBF H, 3100 H - 31BF H, 3500 H - 35BF H]

Address Offset (Hex)	Byte Name	Default (Hex)	Description
00	A1		First A1
01	A1		Second A1
02	A1		Third A1
03	A2		First A2
04	A2		Second A2
05	A2		Third A2
06	J0		(C11)
07	X*		(C12)
08	X*		(C13)
09	B1		
0A	$		
0B	$		
0C	E1		
0D	$		
0E			
0F	F1		
10	X		
11	X		

Table 267. OFP_Rx1/2/3/4 Growable Register Array (GRA) Address Mapping [2900 H - 29BF H, 2D00 H - 2DBF H, 3100 H - 31BF H, 3500 H - 35BF H] (Continued)

Address Offset (Hex)	Byte Name	Default (Hex)	Description
12	D1		
13	$		
14	$		
15	D2		
16	$		
17			
18	D3		
19			
1A			
1B	H11		
1C	Y (H12)		
1D	Y (H13)		
1E	H21		
1F	1s (H22)		
20	1s (H23)		
21	H31		
22	H32		
23	H33		
24	B2		
25	B2		
26	B2		
27	K1		
28			
29			
2A	K2		
2B			
2C			
2D	D4		
2E			
2F			
30	D5		
31			
32			
33	D6		
34			

Table 267. OFP_Rx1/2/3/4 Growable Register Array (GRA) Address Mapping [2900 H - 29BF H, 2D00 H - 2DBF H, 3100 H - 31BF H, 3500 H - 35BF H] (Continued)

Address Offset (Hex)	Byte Name	Default (Hex)	Description
35			
36	D7		
37			
38			
39	D8		
3A			
3B			
3C	D9		
3D			
3E			
3F	D10		
40			
41			
42	D11		
43			
44			
45	D12		
46			
47			
48	S1		
49			
4A			
4B	M1		M1 (TX OFP chiplet 3) for STM-4, STM-4c, STS-12, STS-12c.
4C			
4D	M1		M1 for STS-3c, STM-1
4E	E2		
4F			
50			
51			Reserved
52			
53			
54	J1		Reserved
55	B3		
56	C2		
57	G1		

Table 267. OFP_Rx1/2/3/4 Growable Register Array (GRA) Address Mapping [2900 H - 29BF H, 2D00 H - 2DBF H, 3100 H - 31BF H, 3500 H - 35BF H] (Continued)

Address Offset (Hex)	Byte Name	Default (Hex)	Description
58	F2		
59	H4		
5A	F3		
5B	K3		
5C	N1		
5D	Reserved		Reserved
5E	Reserved		Reserved
5F	Reserved		Reserved
60	J0		Expected 16-byte J0 section trace.
...	..		
6F	J0		
70	J0		Received 16-byte J0 section trace. If the RX J0 message does not match the expected 16-byte J0 section trace in offsets 60H-6FH, then only offset 70H is updated on a per frame basis. If the RX J0 message matches the expected 16-byte J0 section trace then offsets 70H-7FH are updated with the RX J0 message.
...	..		
7F	J0		
80	J1		Expected J1 path trace in 16-byte format
...	..		
8F	J1		
90	J1		Received J1 path trace in 16-byte format
...	..		
9F	J1		
80	J1		Received J1 path trace in 64-byte free format
...	..		
BF	J1		
C0-2FF	--		Reserved.

PARALLEL INTERFACE MODULE (PIM)

The PIM module has no dynamic configuration nor interrupt request signals. It therefore has no handshaking interface with the GPPINT.

BOUNDARY SCAN

BOUNDARY SCAN INTRODUCTION

The IEEE 1149.1 Standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface leads of the device. The Test Access Port block, which implements the boundary scan functions, consists of a Test Access Port (TAP) controller, instruction and test data registers, and a boundary scan register path bordering the input and output leads, as illustrated in Figure 64. The boundary scan test bus interface consists of four input signals (i.e., the Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{\text{TRST}}$) input signals) and a Test Data Output (TDO) output signal. A brief description of boundary scan operation is provided below; further information is available in the IEEE Standard document.

The TAP controller receives external control information via a Test Clock (TCK) signal, a Test Mode Select (TMS) signal, and a Test Reset (TRST) signal, and it sends control signals to the internal scan paths. The scan path architecture consists of a two-bit serial instruction register, a one-bit bypass register and a boundary scan register. The instruction and data registers are connected in parallel between the serial Test Data Input (TDI) and Test Data Output (TDO) signals. The TDI signal is routed to the instruction, bypass and boundary scan registers and is used to transfer serial data into a register during a scan operation. The data to the TDO signal is selected from either register during a scan operation. When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output signals at the device leads to pass to and from the PHAST-12E device's internal logic, as illustrated in Figure 64. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. A timing diagram for the boundary scan feature is provided in Figure 34.

Boundary Scan Support

The maximum frequency the PHAST-12E device will support for boundary scan is 20 MHz. The PHAST-12E device performs the following boundary scan test instructions:

- EXTEST (00)
- SAMPLE/PRELOAD (01)
- BYPASS (11)
- IDCODE (10)

EXTEST Test Instruction:

One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the PHAST-12E device is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external PHAST-12E input and output leads.

SAMPLE/PRELOAD Test Instruction:

When the SAMPLE/PRELOAD instruction is shifted in, the PHAST-12E device remains fully operational. While in this test mode, PHAST-12E input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.

BYPASS Test Instruction:

When the BYPASS instruction is shifted in, the PHAST-12E device remains fully operational. While in this test mode, a scan operation will transfer serial data from the TDI input, through an internal scan cell, to the TDO

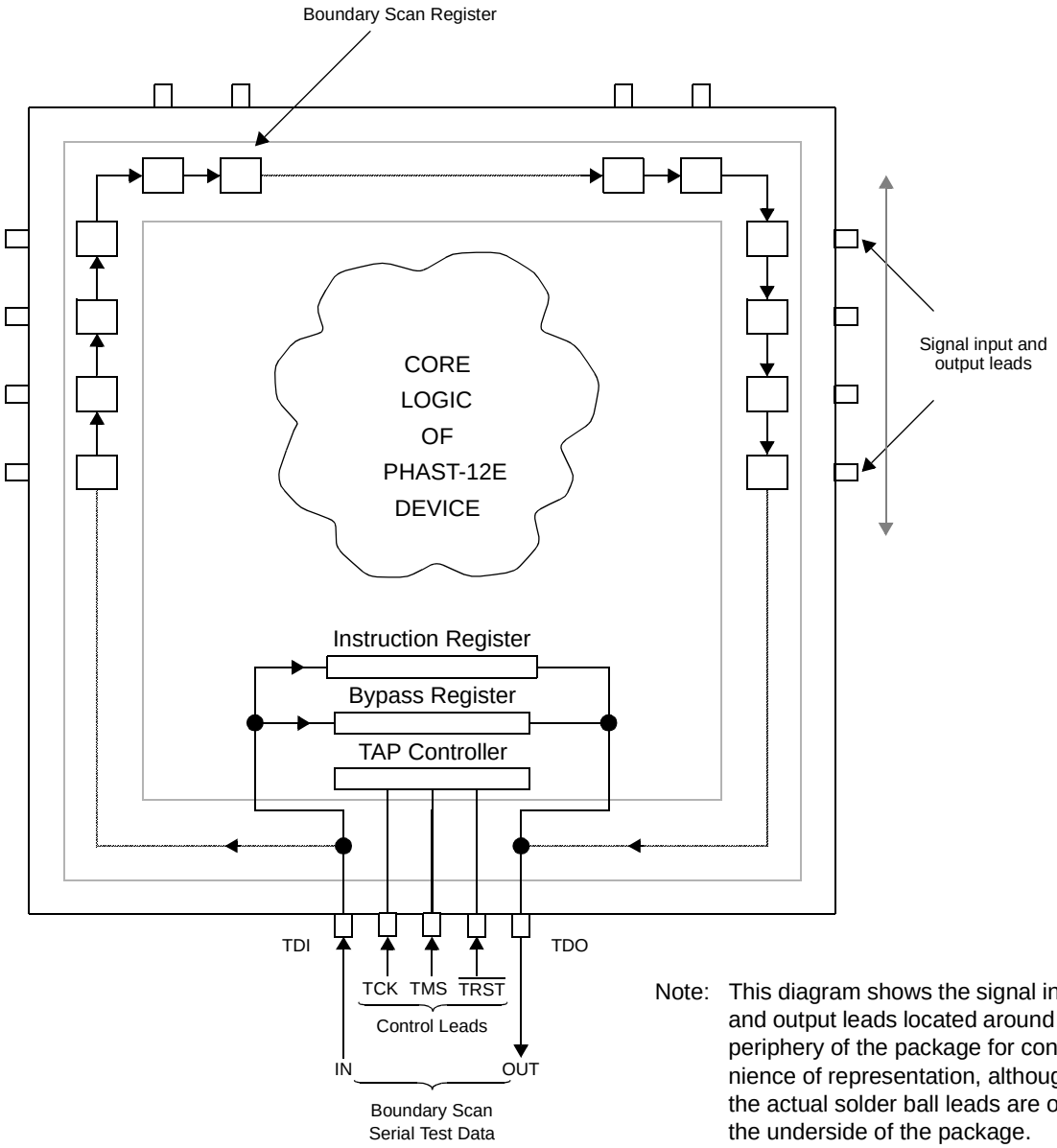
lead. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay.

IDCODE Test Instruction:

When the IDCODE instruction is shifted in, the contents of the IDCODE register can be read.

Boundary Scan Reset:

Specific control of the $\overline{\text{TRST}}$ lead is required in order to ensure that the boundary scan logic does not interfere with normal device operation. This lead should be held low whenever boundary scan operations are not being performed and also during power up.



Note: This diagram shows the signal input and output leads located around the periphery of the package for convenience of representation, although the actual solder ball leads are on the underside of the package.

Figure 64. Boundary Scan Schematic

BOUNDARY SCAN CHAIN

Bidirectional device leads have combined input/output scan cells. Additional scan cells are used for direction control as needed.

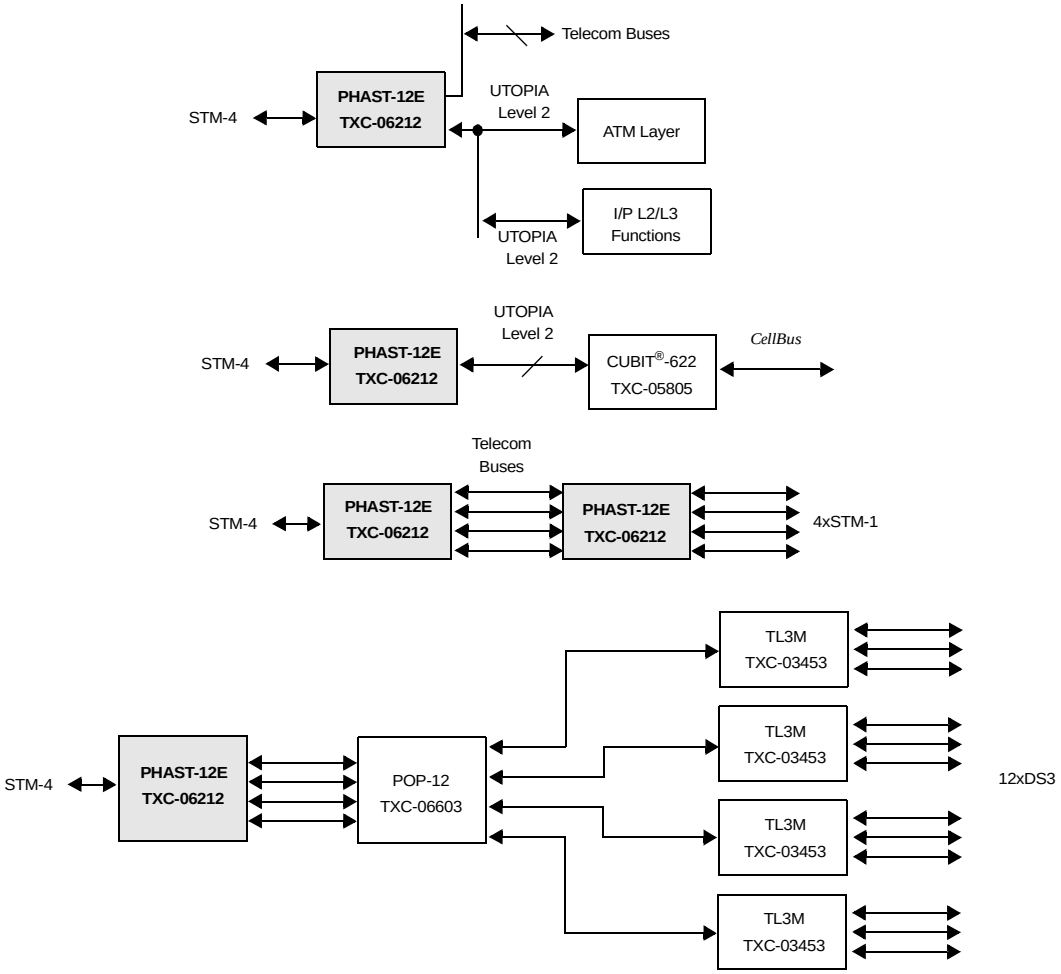
BSDL FILE

A BSDL file for use with the PHAST-12E will be available from the TranSwitch Internet Web Site at www.transwitch.com.

APPLICATION EXAMPLES

MULTISERVICE APPLICATION

Some example ATM cell, “PPP in HDLC-like Frame”, and transmission applications are shown in Figure 65.



Note: Instead of connecting to the 2.488 Gbit/s PHY device, the serial interfaces of each PHAST-12E device can be connected to a 622 Mbit/s fiber optic transceiver for STS-12/STS-12c/STM-4/STM-4c operation. Alternatively, four 155 Mbit/s fiber optic transceivers can be connected to the line interfaces of each PHAST-12E device for quad STS-3c/STM-1 applications.

Figure 65. Example PHAST-12E TXC-06212 Applications

STS-12/STM-4 MULTISERVICE APPLICATION

One of many possible examples is shown in Figure 66 below. In this example, the PHAST-12E is terminating a channelized STS-12/STM-4 signal which contains three individual VC-4/STS-3c-SPE and a fourth channel which contains 3 STS-1-SPEs[1]. The first two STS-3c-SPE/VC-4 contain ATM data while the third STS-3c-SPE/VC-4 contains PPP data. These payloads are terminated into the UTOPIA Level 2/2P interface into PHYs 1 through 3 respectively. When PHY 1 or 2 is selected, the UTOPIA Level 2/2P interface of the PHAST-12E uses the UTOPIA Level 2 handshaking protocol to transfer ATM cells. When PHY 3 is selected, the UTOPIA Level 2/2P interface of the PHAST-12E uses the UTOPIA Level 2P handshaking protocol to transfer PPP packets. The fourth channel (STS-3-SPE) contains TDM data which consists of DS1s mapped into VT1.5s. The RX Telecom Bus of the PHAST-12E is connected in wired-OR fashion to create a mux which can be tristated through control bits in the PHAST-12E to create a 4 to 1 mux. This allows the STS-3 that contains TDM data to be interfaced to the POP-12 device. The POP-12 is also transmitting data to the TX Telecom Bus. This allows the channel that is not configured for ATM or PPP mode to transmit the TDM data. The POP-12 device performs STS-1 POH and pointer processing up to four independent telecom buses, while the TEMx28® and T1Fx8 devices allow 2016 DS0 channels to be inserted/extracted from the 3 STS-1-SPEs via a TDM Bus. Multiservice applications can also be achieved for 4xSTS-3c/STM-1 mode.

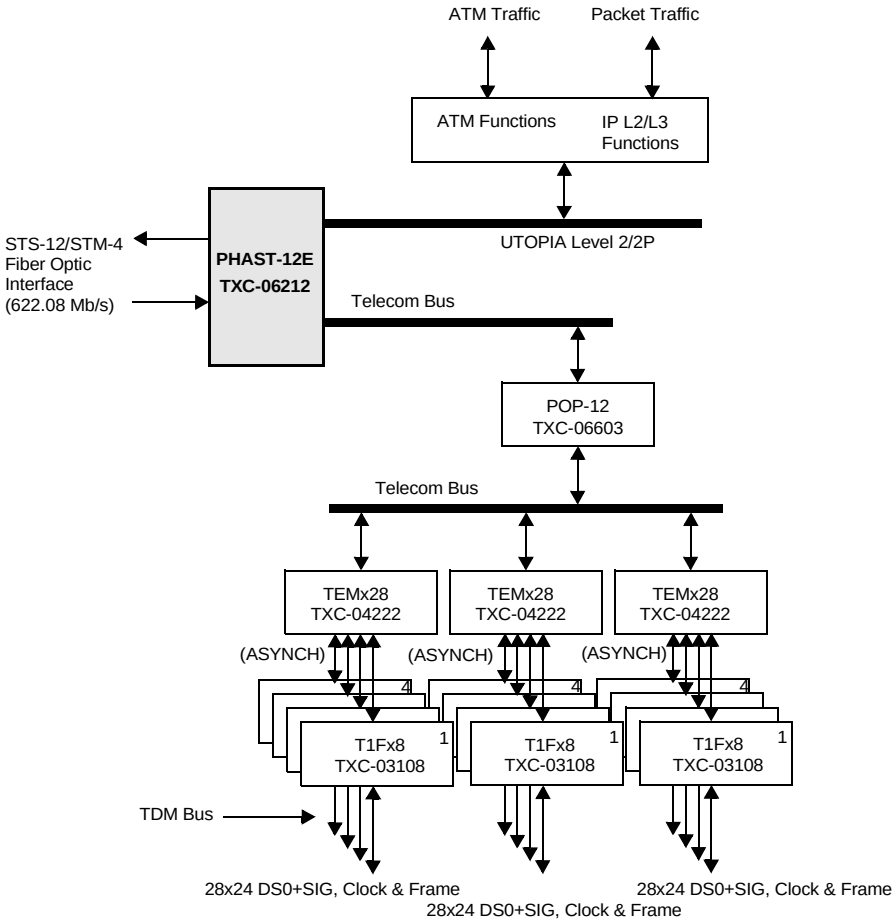


Figure 66. Multi-Service Access Mux

1. The PHAST-12E is set up to process STS-12/STM-4 and can only process signal components down to the STS-3c-SPE/VC-4 level. If STS-1 SPEs are contained in the frame, then they can be accessed by using TranSwitch POP-12 or similar devices for further processing of the STS-3 component.

APPENDIX 1: TXC PHAST-12E CONFIGURATION PSEUDO-CODE EXAMPLE

Please refer to the section "PHAST-12E Power Up, Reset and Autotrim Sequence, on Page 131'.

Please contact the TranSwitch Applications Engineering Department for the complete sample configuration files.

Description: TranSwitch PHAST-12E Configuration Pseudo-Code example.

```
/*****************************************************************************/
        /* ASSERT HARDWARE RESETS          */
/*****************************************************************************/
        /* A pulse is applied to FRESET pin, as shown on Figure 42 of the Data Sheet*/
/*****************************************************************************/
        /* ASSERT GLOBAL RESETS            */
/*****************************************************************************/
        (TXC_REG*)0x 3800=0xFF;   /* Reset GP1 */
        (TXC_REG*)0x 3801=0xFF;
        (TXC_REG*)0x 3802=0xFF;
        (TXC_REG*)0x 3803=0xFF;
        (TXC_REG*)0x 3804=0xFF;
        (TXC_REG*)0x 3805=0xC0;

/*****************************************************************************/
        /*  CONFIGURE SIM CHIPLET          */
/*****************************************************************************/
        /* the SIM configuration registers are configured according to the user's application  */
        /* in this example they are configured in 4* STM-1 mode    */

        (TXC_REG*)0x 3909=0x23;  /* in SIM #1 only, bit 4 is set to 0  */
        (TXC_REG*)0x 3949=0x33;
        (TXC_REG*)0x 3989=0x33;
        (TXC_REG*)0x 39C9=0x33;

        (TXC_REG*)0x 390B=0x00;   /*All Channels in 155 Mbps */
        (TXC_REG*)0x 394B=0x00;
        (TXC_REG*)0x 398B=0x00;
        (TXC_REG*)0x 39CB=0x00;

        (TXC_REG*)0x 3908=0x00;   /* Set refclk freq to 19.44 MHz */

        TXC_SleepTask(10);  /* 10 ms delay */
```

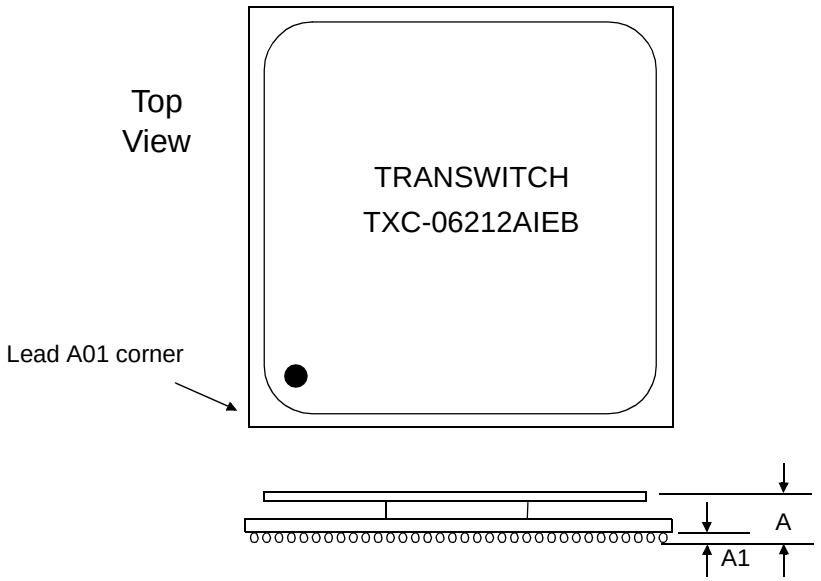
```
/*****************************************************************************/
        /*  AUTOTRIM  value 7 not allowed */
/*****************************************************************************/

        for (dd=0;dd<1000;dd++)
        {
                (TXC_REG*)0x 3902=0x00;
                (TXC_REG*)0x 3903=0x00;
                (TXC_REG*)0x 3904=0x00;

                (TXC_REG*)0x 3900=0x07;
                (TXC_REG*)0x 3900=0x06;
                (TXC_REG*)0x 3900=0x07;  /* transition of bit 1 triggers the autotrim */

                /* the cc loop is repeated until bit 3 and 4 of 3921 are set to 1 */

                for (cc=0;cc<1000;cc++)
                {
                        TXC_SleepTask(1);
                        tempReg = PHAST12E_ReadReg((TXC_REG*)0x 3921);
                        tempReg &= 0x18;

                        if (tempReg == 0x18)
                                break;
                }

                /* the dd loop ensures that the autotrim is repeated until the computed trim value is not 7 */

                tempReg = PHAST12E_ReadReg((TXC_REG*)0x 3921);
                tempReg &= 0x07;

                if (tempReg != 0x07 and tempReg != 0x06 and tempReg != 0x02 and temReg != 0x01 and
                tempReg != 0x00)
                        break;
        }

        (TXC_REG*)0x 3902=0x02;
        (TXC_REG*)0x 3908=0x00;

        TXC_SleepTask(10);  /* 10 ms delay */

/*****************************************************************************/
        /*  CONFIGURE GLOBAL REGISTERS   */
/*****************************************************************************/
        /* the global configuration registers (in the GPPINT) are configured according to the user's application
```

```
/*****************************************************************************/
        /* DEASSERT GLBOAL RESETS          */
/*****************************************************************************/
        (TXC_REG*)0x 3805=0x00;   /*  This sequence is required 5,4,0,1,2.3 */
        (TXC_REG*)0x 3804=0x00;
        (TXC_REG*)0x 3800=0x50;
        (TXC_REG*)0x 3801=0x00;
        (TXC_REG*)0x 3802=0x00;
        (TXC_REG*)0x 3803=0x0C;

/*****************************************************************************/
        /* CONFIGURE LOCAL CHIPLETS        */
/*****************************************************************************/

        /* Transmit and Receive ACI, PH, ACH, OFP configuration registers are configured according to the
user's application

/*****************************************************************************/
        /* LOCAL CHIPLETS ENABLE SEQUENCE */
/*****************************************************************************/

        /* Tx ACI */

        (TXC_REG*)0x 0130=0x00;

        /* Tx PH */

        (TXC_REG*)0x 0530=0x00;
        (TXC_REG*)0x 0630=0x00;
        (TXC_REG*)0x 0730=0x00;
        (TXC_REG*)0x 0830=0x00;

        /* Tx ACH */

        (TXC_REG*)0x 1030=0x00;
        (TXC_REG*)0x 0F30=0x00;
        (TXC_REG*)0x 0E30=0x00;
        (TXC_REG*)0x 0D30=0x00;

        /* TxOFP */

        /* note the init bit is polled after each OFP is enabled */

        (TXC_REG*)0x 2430=0x00;
        for(cc=0;cc<1000;cc++)
        {
                tempReg = PHAST12E_ReadReg((TXC_REG*)0x 2433);
                tempReg &= 0x01;
                if(tempReg)
                        break;
        }

        (TXC_REG*)0x 2030=0x00;

        for(cc=0;cc<1000;cc++)
```

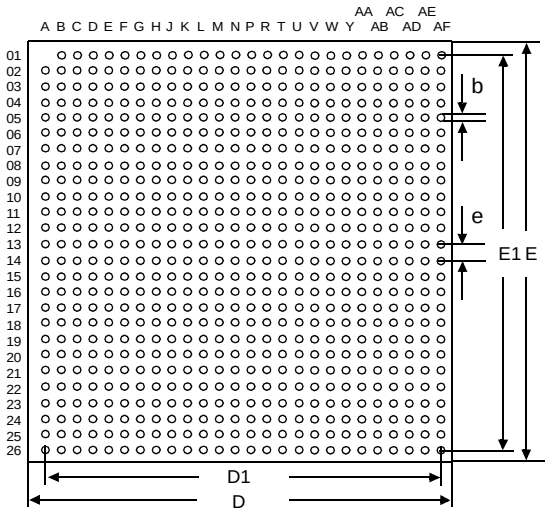
```
{
                tempReg = PHAST12E_ReadReg((TXC_REG*)0x 2033);
                tempReg &= 0x01;
                if(tempReg)
                        break;
}

(TXC_REG*)0x 1C30=0x00;

for(cc=0;cc<1000;cc++)
{
                tempReg = PHAST12E_ReadReg((TXC_REG*)0x 1c33);
                tempReg &= 0x01;
                if(tempReg)
                        break;
}

(TXC_REG*)0x 1830=0x00;

for(cc=0;cc<1000;cc++)
{
                tempReg = PHAST12E_ReadReg((TXC_REG*)0x 1833);
                tempReg &= 0x01;
                if(tempReg)
                        break;
}

/* Rx ACI */

(TXC_REG*)0x 0330=0x00;

/* Rx PH  */

(TXC_REG*)0x 0930=0x00;
(TXC_REG*)0x 0A30=0x00;
(TXC_REG*)0x 0B30=0x00;
(TXC_REG*)0x 0C30=0x00;

/* Rx ACH  */

(TXC_REG*)0x 1430=0x00;
(TXC_REG*)0x 1330=0x00;
(TXC_REG*)0x 1230=0x00;
(TXC_REG*)0x 1130=0x00;

/* Rx OFP */

(TXC_REG*)0x 3430=0x00;
(TXC_REG*)0x 3030=0x00;
(TXC_REG*)0x 2C30=0x00;
(TXC_REG*)0x 2830=0x00;

/* PPP */
/* not enabled if not in PPP mode */
(TXC_REG*)0x 1530=0x00;
```

PACKAGE INFORMATION

The PHAST-12E device is packaged in a 675-lead Enhanced Plastic Ball Grid Array package that is suitable for surface mounting, as illustrated in Figure 67 below.



Dimension (Note 1)	Min	Max
A (nom.)	3.35	
A1	0.40	0.60
b (nom.)	0.50	0.70
D	26.80	27.20
D1 (nom.)	25.00	
E	26.80	27.20
E1 (nom.)	25.00	
e (nom.)	1.0	



Bottom View

Notes:

1. All dimensions are in millimeters. Values shown are for reference only.
2. Size of array: 26 x 26. Package Outline Conforms to JEDEC MO-151-AAL-1**.**
3. Diagram is stylized and not to scale.

Figure 67. PHAST-12E TXC-06212 675-Lead Enhanced Plastic Ball Grid Array Package

ORDERING INFORMATION

Part Number: TXC-06212AIEB 675-lead Enhanced Plastic Ball Grid Array package

RELATED PRODUCTS

TXC-03452B, L3M VLSI Device (Level 3 Mapper/Desynchronizer) - L3M maps a DS3 or E3 signal into an SDH/SONET signal formatted for STM-n (VC-3 via TU-3) or STS-n (via STS-1 SPE).

TXC-03453, TL3M VLSI Device (Triple Level 3 Mapper). Maps three 44.736 Mbit/s DS3 to an STM-1, TUG-3 or STS-3 STS-1 SPE SDH/SONET signal. An 34.368 Mbit/s E3 signal is mapped in to an STM-1 TUG-3. The TL3M's SDH/SONET interface format is COMBUS, byte wide parallel. The TL3M supports drop bus and add bus SDH/SONET timing modes. Drop bus timing provides timing signals for the add side while timing for both busses is independent for the add bus timing mode.

TXC-03456, L4M VLSI Device (Level 4 Mapper/Desynchronizer) - L4M Maps a 139.264 Mbit/s asynchronous line signal into an AU-4 VC-4/STS-3c SPE signal. The SONET/SDH signal is transmitted via the add bus with timing derived from the drop bus, add bus or an external source. The L4M provides test features such as line loopback, SONET/SDH loopback and on-chip test pattern generator and analyzer. The L4M meets strict jitter requirements to transport broadcast grade video signals.

TXC-04222, TEMx28 VLSI Device (21/28 Channel Dual Bus High Density Mapper). An add/drop multiplexer, terminal multiplexer, and dual and single unidirectional ring applications. Up to 28 E1, DS1, or VT/TU payloads are mapped to and from VT1.5/TU-11s and VT2/TU-12s carried in an STM-1 VC-4 or STS-3 format.

TXC-04228, T1Mx28 VLSI Device (DS1 Mapper 28-CHannel Device). The DS1MX28 maps twenty eight DS1 signals into any seven selected asynchronous or byte-synchronous mode VT1.5 or TU-11 tributaries in a SONET/SDH synchronous payload envelope.

TXC-05804, CUBIT-3 is a single-chip solution for implementing low-cost ATM multiplexing and switching systems, based on the *CellBus* architecture. Such systems are constructed from a number of CUBIT-3 devices, all interconnected by a 37-line common bus, the *CellBus*. CUBIT-3 supports unicast, broadcast and spatial multicast transfers, and has all necessary functions for implementing a switch: cell address translation, cell routing and outlet cell queuing. The CUBIT-3 is a VLSI product designed to interface directly on the terminal side with UTOPIA Level 1/2 8/16-bit compliant devices.

TXC-05805, CUBIT-622 VLSI Device (Multi-PHY *CellBus* Switch Access Device). A single-chip solution for implementing low-cost ATM multiplexing and switching systems, based on the *CellBus* architecture. The CUBIT-622 device is an enhanced version of the CUBIT-3 (TXC-05804) device. The two major enhancements include a throughput increase to 622 Mbit/s and a port density increase to 64 ports. The rate decoupling FIFO have been increased from 4 to 32 cells on ingress to accommodate the higher bandwidth interface.

TXC-06101, PHAST-1 VLSI Device (SONET STS-1 Overhead Terminator). This device performs section, line and path overhead processing for STS-1 SONET signals. It has programmable STS-1 or STS-N modes. It operates from a 3.3 volt supply and consumes less power than the SOT-1E TXC-03011 device with similar capability.

TXC-06103, PHAST-3N Device (STM-1/STS-3/STS-3c SDH/SONET Overhead Terminator). This device performs STM-1/STS-3/STS-3c termination into a Telecom Bus interface. Section, line, and path overhead byte processing is performed. A serial and byte parallel line interface is provided. TX and RX retiming and clock synthesis/recovery at 155.52 Mb/s is provided on chip. Alarm and error processing is provided along with STS-1 loopback capability.

TXC-06112, PHAST-12 VLSI Device (Programmable, High-Performance ATM/Packet/Transmission SONET/SDH Terminator for Level 12). A highly integrated SONET/SDH terminator device designed for ATM cell, frame, higher-order multiplexing, and transmission applications. This PHAST-12 VLSI device provides a Telecom Bus interface for downstream devices and operates from a power supply of 3.3 volts. The PHAST-12 is a predecessor of the PHAST-12E device.

TXC-06203, PHAST-3P Device (STM-1/STS-3c SDH/SONET Overhead Terminator with CDB/PPP UTOPIA Interface). This device performs STM-1/STS-3c termination into a UTOPIA Level 2 for ATM cell data, or a UTOPIA Level 2P interface for PPP data. Single-PHY or Multi-PHY operation is supported. A serial and byte parallel line interface is provided. Section, line, and path overhead byte processing is performed. Clock synthesis/recovery at 155.52 Mb/s, alarm and error processing, as well as TX and RX retiming is provided.

TXC-06603, POP-12 Device (OC-12 SONET/SDH Path Overhead Processor, Retimer, and Cross Connect). The POP-12 integrates VC-3/VC-4 POH processing, AU-3/AU-4 pointer processing/retiming, and VC-3/VC-4 cross connect for four Telecom Bus interfaces into one package. It provides an interface to high density mapper applications when used with the TranSwitch PHAST-12E (TXC-06212), and mapper and framer devices. The POP-12 device is designed to provide a seamless interface with the PHAST-12E device.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
25 West 43rd Street
New York, New York 10036

Tel: (212) 642-4900
Fax: (212) 398-0023
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

404 Balboa Street
San Francisco, CA 94118

Tel: (415) 561-6275
Fax: (415) 561-6120
Web: www.atmforum.com

ATM Forum Europe Office

Kingsland House - 5th Floor
361-373 City Road
London EC1 1PQ, England

Tel: 20 7837 7882
Fax: 20 7417 7500

ATM Forum Asia-Pacific Office

Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3438 3694
Fax: 3 3438 3698

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112

Tel: (800) 854-7179 (within U.S.A.)
Tel: (303) 397-7956 (outside U.S.A.)
Fax: (303) 397-2740
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia-Antipolis Cedex, France

Tel: 4 92 94 42 00
Fax: 4 93 65 47 16
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007

Tel: (800) 669-6857 (within U.S.A.)
Tel: (903) 769-3717 (outside U.S.A.)
Fax: (903) 769-3818
Web: www.mvip.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5852
Fax: 22 730 5853
Web: www.itu.int

JEDEC (International):

Joint Electron Device Engineering Council
2500 Wilson Boulevard
Arlington, VA 22201-3834

Tel: (703) 907-7559
Fax: (703) 907-7583
Web: www.jedec.org

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: (215) 697-2179
Fax: (215) 697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
5440 SW Westgate Dr., #217
Portland, OR 97221

Tel: (800) 433-5177 (within U.S.A.)
Tel: (503) 291-2569 (outside U.S.A.)
Fax: (503) 297-1090
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place Rm 3A184
Piscataway, NJ 08854-4157

Tel: (800) 521-2673 (within U.S.A.)
Tel: (732) 699-2000 (outside U.S.A.)
Fax: (732) 336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunication Technology Committee
Hamamatsu-cho Suzuki Building
1-2-11, Hamamatsu-cho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated PHAST-12E Data Sheet that have significant differences relative to the previous and now superseded PHAST-12E Ed. 5 Data Sheet:

Updated PHAST-12E Data Sheet: Ed. 6, July 2003

Previous PHAST-12E Data Sheet: *PRELIMINARY* Ed. 5, August 2002

The page numbers indicated below of this updated Data Sheet include changes relative to the previous Data Sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date. Removed *PRELIMINARY* markings (and explanatory text on pages 1 and 347).
1	Changed Copyright information in bottom of left margin.
54	Modified “Lead Description” column for Lead Name “ACHCLK”.
132	Modified wave form in Figure 42 for “xxx-CLK”.
133	Modified sentence for #8.
163	Changed last column for “c/ Multiplexed Status Indication with 1 Status Line”.
339	Modified the line begin with “if (tempReg != 0x07 and tempReg != . . . . “.
345	Updated “Standards Documentation Sources" section.
347	Updated "List of Data Sheet Changes" section.

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