CICADA SEMICONDUCTOR

CIS8201

SimpliPHY™ Gigabit Ethernet PHY Series

Single Port, Low Power, 10 / 100 / 1000BASE-T PHYwith GMII / MII, RGMII, TBI and RTBI MAC Interfaces

1 General Description

Enabling widespread, low-cost, Gigabit-to-the-Desktop deployment, Cicada's low-power, single chip CIS8201 integrates a complete triple speed (10BASE-T, 100BASE-TX, and 1000BASE-T) Ethernet physical layer transceiver in two small footprint package options. RJ-45 footprint compatible options are a 128-pin Plastic Low-Profile Quad Flat Pack (LQFP) package, and a 11x11mm footprint 100-ball LBGA package.

The 1000BASE-T transceiver features the industry standard GMII/MII, plus the pin-saving RGMII / RTBI system interfaces. Unlike competitors' products, the CIS8201 integrates self-calibrating series termination resistors on MAC interface pins, simplifying system design significantly by eliminating more than a dozen external components. These innovative terminations also reduce PCB layout complexity, increase system timing margins, and minimize EMI engineering challenges. In addition, the CIS8201 includes innovative on-chip RGMII timing compensation circuits on the MAC interface pins to simplify PCB design.

The twisted pair interface includes an innovative internal hybrid and a very low EMI line driver with robust Cable Sourced ESD (CESD) performance, allowing the use of the lowest-cost 1:1 magnetic modules, minimum external components, and less complex PCB traces. To further reduce system complexity and cost, the CIS8201 can optionally be powered from a single 3.3V power supply when utilizing the device's on-chip regulator control circuit to produce the 1.5V core power supply voltage.

The CIS8201 leverages Cicada's proprietary **2nd generation SimpliPHY™ DSP Technology**, key to enabling an extremely low-power Gigabit PHY on a single chip. Cicada's mixed signal and DSP architecture yields robust performance, supporting both full- and half-duplex 10BASE-T, 100BASE-TX, and 1000BASE-T Ethernet over unshielded twisted pair (UTP) cable, with more than 5dB of design margin with respect to all worst-case impairments (NEXT, FEXT, Echo, and system noise). The industry's highest-performance, low-power DSP-based transceiver utilizes an optimum trellis decoding algorithm in concert with all digital gain control and timing recovery.

To enable maximum network management feedback to the host system and the user, Cicada-provided software routines, referred to as the VeriPHY™ Link Management Suite, allow extensive network and cable plant operating and status information, such as the cable length and the effective Bit Error Rate (BER), to be easily integrated with NIC or switch software, greatly simplifying Gigabit Ethernet network deployment and management.

2 System Diagram

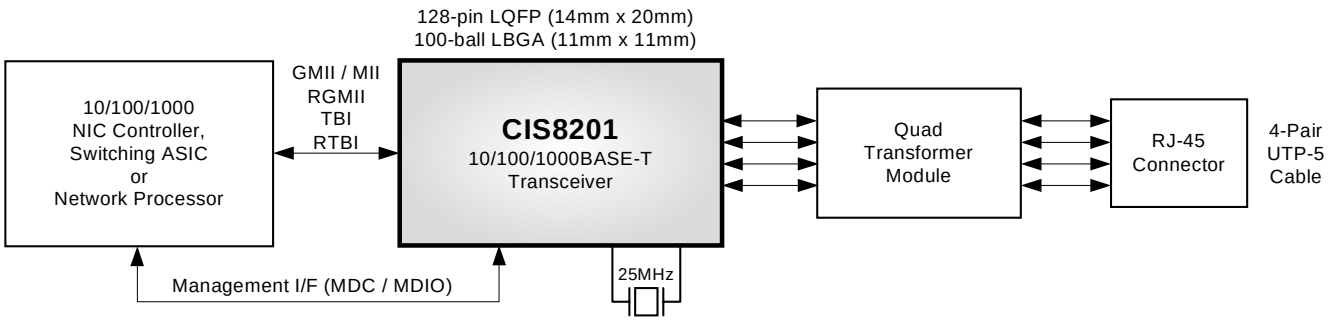


Figure 2-1. CIS8201 System Diagram

3 Features

Features	Benefits
• <1.0W power consumption	• Eliminates expensive regulators, heat sinks & fans
• Optional on-chip regulator control circuit	• Enables a single 3.3V supply design for lowest cost
• Advanced Power Management complies with PC99/ PC2000, Wake on LAN™, & PCI 2.2 power requirements	• Enables widespread, low-cost, 1000BASE-T deployment in desktop LOM, NICs, & switches
• Fully IEEE 802.3, 802.3u (10BASE-T, 100BASE-TX), & 802.3ab (1000BASE-T) compliant	• Ensures full specification compliance & seamless deployment throughout Category-5 networks with the industry's highest performance & noise immunity
• Automatic detection & correction of cable pair swaps, pair skew, & pair polarity, along with an Auto MDI/MDI-X crossover function	• Compatible with first generation 1000BASE-T PHYs, allowing trouble-free migration to 1000BASE-T by minimizing common interoperability problems
• Choice of standard GMII/MII or TBI, or pin-saving RGMII/RTBI interfaces	• Connects to existing GMII and TBI-based MACs, or significantly reduces pin-count requirements on MAC & switching ASICs from 24 (GMII) to 12 (RGMII).
• Self-calibrating, series termination resistors on MAC interface pins	• Eases board designs & EMI challenges, improves MAC I/F signal integrity, lowers power consumption, & eliminates >12 external components on a system board
• Unique on-chip RGMII timing compensation supports both 2.5V and 3.3V RGMII operation	• Decreases board design efforts, increases PCB timing margins & yields, & shortens time to market
• Optional integrated oscillator circuit	• Supports single low-cost 25MHz crystal, or either a 25MHz or 125MHz standard reference clock input
• >10KB jumbo frame support with programmable synchronization FIFOs	• Provides for maximum jumbo frame sizes in custom SAN & LAN systems
• Six direct drive LED pins	• LED flexibility with minimum external components
• Low EMI line drivers with robust CESD performance	• Reduces EMI & qualification engineering risks & efforts
• Manufactured in mainstream, 3.3V/1.5V digital CMOS process	• Minimizes costs & enables highest PHY integration levels & process portability
• Choice of two small footprint packages: - 14x20mm LQFP - 11x11mm LBGA	• Low cost plastic packaging compatible with compact PC LAN-on-Motherboards

4 Applications

- Desktop and Server NICs
- LAN-on-Motherboard and Mobile PC NICs
- Workgroup and Desktop Switches/Routers
- SAN Switches and NAS Appliances

5 Device Block Diagram

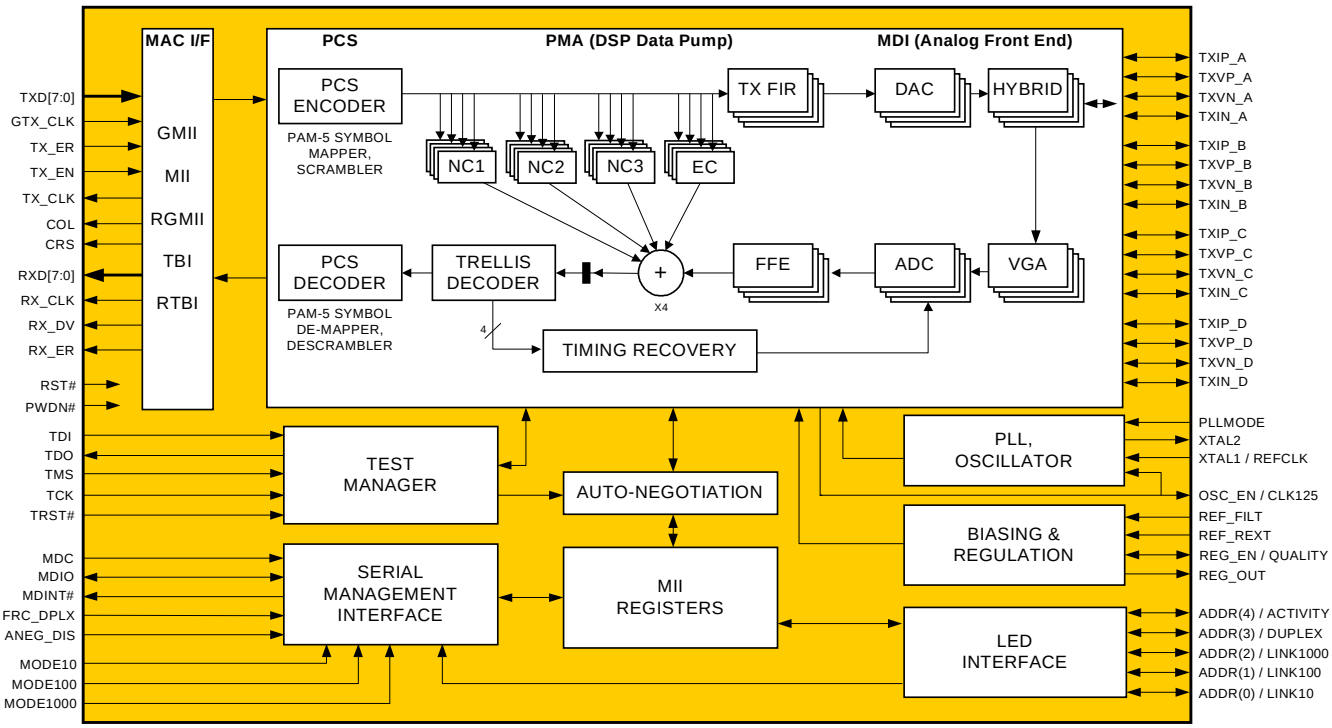


Figure 5-1. CIS8201 Block Diagram

Table of Contents

List of Figures

List of Tables

6 Relevant Specifications & Documentation

The CIS8201 conforms to the following specifications. Please refer to these documents for additional information.

Table 6-1. CIS8201 Relevant Specifications

Specification - Revision	Description
IEEE 802.3-2000	Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications. IEEE 802.3-2000 consolidates and supersedes the following specifications: 802.3ab (1000BASE-T), 802.3z (1000BASE-X), 802.3u (Fast Ethernet), with references to ANSI X3T12 TP-PMD standard (ANSI X3.263 TP-PMD).
IEEE 1149.1-1990	Test Access Port and Boundary Scan Architecture[1]. Includes IEEE Standard 1149.1a-1993 and IEEE Standard 1149.1b-1994.
JEDEC EIA/JESD8-5	2.5V±0.2V (Normal Range), and 1.8V to 2.7V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits.
JEDEC JESD22-A114-B	Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM). Revision of JESD22-A114-A.
JEDEC JESD22-A115-A	Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM). Revision of EIA/JESD22-A115.
JEDEC EIA/JESD78	IC Latch-Up Test Standard.
MIL-STD-883E	Miltary Test Method Standard for Microcircuits.
RGMII Specification[2] - v1.3, v2.0	Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Devices (per Hewlett Packard). Includes both RGMII and RTBI standards.
PICMG 2.16	IP Backplane for CompactPCI.

[1] Often referred to as the “JTAG” test standard.

[2] The CIS8201 RGMII interface is timing and electrically compatible with the RGMII v1.3 specification. The CIS8201 RGMII interface is timing only and not electrically compatible with the RGMII v2.0 specification.

7 Data Sheet Conventions

Conventions used throughout this data sheet are specified in the following table.

Table 7-1. Data Sheet Conventions

Convention	Syntax	Examples	Description
Register number	RegisterNumber.Bit or RegisterNumber.BitRange	23.10 23.12:10	Register 23 (address 17h), bit 10. Register 23 (address 17h), bits 12, 11, and 10.
Signal name (active high)	SIGNALNAME[1]	PLLMODE	Signal name for PLLMODE.
Signal name (active low)	SIGNALNAME#[1]	RST#	Active low reset signal.
Signal bus name	BUSNAME[MSB:LSB][1]	PHYADD[4:2]	PHY Address bus, bits 4, 3, and 2.

[1] All signal names are in all CAPITAL LETTERS.

8 Functional Overview

Cicada's single chip CIS8201 is a complete triple speed (10BASE-T, 100BASE-TX, and 1000BASE-T) low-power Ethernet physical layer transceiver. The CIS8201 transceiver is based on a highly robust DSP Data Pump architecture with a triple speed capable Analog Front End (AFE).

A number of innovative features have been engineered into the device with the primary goal of simplifying overall systems design and reducing power consumption, leading to reduced system complexity and cost.

At the systems level, the following components are required to interface to the CIS8201:

- A MAC device supporting any of the following interfaces: a GMII, MII, RGMII, TBI, or RTBI interface
- An optional Station Manager
- A single reference clock (either 25MHz or 125MHz), or an optional single 25MHz crystal
- One to three fixed power supplies, depending on the MAC I/F mode and the use of the optional on-chip regulator control circuit:
  - GMII mode: 3.3V and 1.5V (or only 3.3V with use of regulator)
  - RGMII[1] and RTBI modes: 3.3V, 2.5V, and 1.5V (or only 3.3V and 2.5V with use of regulator)
- A simple, external series pass type MOSFET transistor for supply regulation (optional)
- A 1:1 quad transformer module[2]
- Line termination resistors (on MAC TX and Media side only)
- Reference capacitor and resistor
- Power supply decoupling capacitors

The configurable PHY includes all the required physical layer functionality to support 1000BASE-T, 100BASE-TX, and 10BASE-T, in either half-duplex or full-duplex operation at each speed. The PHY port can be configured to connect with virtually any triple speed Ethernet MAC or Network Processor by individually selecting one of four available MAC interfaces: GMII (including MII for 10M/100Mb modes), RGMII, RTBI, or TBI.

8.1 MAC Interface (GMII / RGMII / MII, or TBI / RTBI)

- Connects the CIS8201 PHY port to the appropriate layer 2 function, such as a triple speed Ethernet MAC.
- Supports both the IEEE standard Gigabit Media Independent Interface (GMII), or the more pin-efficient Reduced Gigabit Media Independent Interface (RGMII), without requiring a SERDES type interface to a MAC.
- All MAC interface output pins feature integrated, adaptively calibrated, 50 ohm series termination resistors to simplify PC board design, resulting in improved signal quality, elimination of all external series termination resistors, and lower on-chip power consumption.
- Supports operation in 10BASE-T and 100BASE-TX modes via the IEEE standard MII.
- Supports operation in 1000BASE-T via the IEEE Standard TBI or more pin-efficient RTBI interface.

8.2 Twisted Pair Interface (TPI)

- Connects the CIS8201 PHY port's four dual-duplex channels to an external 1:1 magnetic module.
- Implements an internal hybrid, which minimizes the number of external passive components and easily interfaces to several, readily available, quad transformer modules to support all three operating modes.

The CIS8201 also includes four shared interfaces, used for chip and board testing, in addition to configuring the PHY port's operating modes, or monitoring the status of the port.

[1]The RGMII interface is timing compatible with the v1.3 and v2.0 specifications. The RGMII interface is not electrically compatible with the v2.0 specifications as this requires HSTL voltage levels which the CIS8201 does not support.

[2]For PICMG 2.16 applications, the transformer can be removed. See *PICMG 2.16 Applications Note* for more information.

8.3 Serial Management Interface (SMI)

- Enables communication- and standards-specified configuration of the CIS8201 PHY port via a system controller, such as an external CPU or ASIC.
- Fully compliant with the IEEE 802.3 MII Management Interface specifications.
- Supports Management Data Clock (MDC) operating speeds from 0MHz to approximately 12.5MHz
- Provides a shared, open drain, interrupt pin (MDINT#) to signal the Station Manager of any change in the operating conditions of the PHY port.
- Optional configuration pins, MODE (10, 100, and 1000), FRC_DPLX, and ANEG_DIS, provide an alternative, direct method for presetting the operating mode (speed and duplex) of the PHY port without the need for a dedicated station manager.

8.4 Parallel LED Interface (PLI)

- Enables the PHY port to communicate its operating conditions (e.g., duplex, link, speed, activity, collision, and quality) by directly driven status LEDs.

8.5 System Clock Interface (SCI)

- Generates all internal and external clocks from the internal PLL, maintaining clock synchronization throughout the device with very low jitter.
- Allows either a single 25MHz or 125MHz reference clock (or an optional reference crystal, used with the on-chip oscillator) to be used as the reference clock for the PHY.

8.6 Test Mode Interface (TMI)

- Enables IC manufacturing test and standard board-level testing through an industry standard JTAG 1149.1 Boundary Scan controller
- Facilitates the operation of several innovative analog and digital Built-in-Self-Test functions, which simplify and improve manufacturing test coverage, leading to reduced component and systems costs

The three major sub-functions for the CIS8201 PHY port are described in the following sections.

8.7 Analog Front End (AFE)

The CIS8201 employs an advanced, low-power, hybrid “PHY” architecture, utilizing a high speed AFE and an extremely gate- and power-efficient, compact DSP core.

The analog front end, or “AFE”, performs the following functions in each operating mode:

- Receive and transmit signal separation (via on-chip hybrid circuitry)
- Transmit wave filtering and shaping (PMA Transmit Filter and AFE TX DAC)
- Automatic gain control (VGA)
- Receive signal quantization (ADC)
- Digital timing recovery (ADC and VGA, in concert with DSP Data Pump Core)
- Link pulse detection

In the receive data path, digital words quantized by the PHY port’s four ADCs are supplied to the PMA (Physical Media Attachment) for further processing by the various DSP Data Pump elements (Adaptive equalization, Echo cancellation, NEXT and FEXT cancellation, trellis decoder, and the digital timing recovery loop).

On the transmit data path, the digital transmit filters in the PMA provide digital transmit words in 3-bit PAM5 (1000BASE-T), 2-level MLT-3 (100BASE-TX), or Manchester-encoded format to the triple speed, pulse-shaping transmit DACs.

The AFE also includes an analog PLL, which generates all internal and externally-sourced clocks from either a 25MHz or 125MHz reference clock (or a reference crystal, used with the on-chip oscillator). The PLL also provides an optional, free-running 125MHz output clock for use as a highly accurate, low-jitter clock for use by other ICs in the system.

8.8 DSP Data Pump Core

Due to its robust, low-power DSP architecture, the CIS8201 eases interoperability concerns by maintaining error-free operation in the presense of extreme noise and interference and in substandard cabling environments. It aslo supports link partner frequency offset tolerances well outside the Ethernet specifications (typically ±450ppm of local and link partner frequency offset tolerances).

The primary Receive functions performed within the DSP Data Pump include:

- Echo cancellation
- Crosstalk cancellation (near and far end)
- Baseline wander correction and cancellation
- Adaptive receive equalization
- Receive signal slicing
- Digital timing recovery
- Cable pair skew compensation
- Trellis decoding (or forward error correction)

Other functions performed by the DSP core include:

- Automatic pair swap detection and correction
- Automatic cable pair polarity compensation
- Automatic MDI crossover for all three speeds

The primary transmit function implemented by the DSP core is:

- Transmit pulse shaping

8.9 Physical Coding Sublayer (PCS)

The PCS is responsible for controlling all transmit and receive data interchanges with external MACs. Depending on which MAC interface is enabled on the PHY port, the PCS transfers data to and from the MAC at various word widths, in conjunction with several MAC interface-specific control signals.

For example, in 1000BASE-T mode, the PCS receive path includes three primary functions:

- Trellis decoding
- Symbol descrambling
- 4D-PAM5 symbol demapping

These elements serve together to:

- Convert PAM-5 symbols from the DSP core into 8-bit receive data symbols for transmission to the MAC on the RXD[7:0] output pins (GMII mode)
- Generate the associated receive data control and status signals (RX_DV, RX_ER) for use by the MAC

In 1000BASE-T mode, the PCS transmit path includes the following functions:

- Trellis encoding
- Symbol scrambling
- 4D-PAM5 symbol encoding

From a functional perspective, these elements serve together to:

- Convert transmit data words from the MAC on the TXD[7:0] pins (GMII mode) to PAM-5 symbols, which are sent to the transmit filters and DACs in the DSP core and AFE, respectively

8.10 Synchronization FIFOs

The PCS is also ultimately responsible for managing clock domain synchronization between the various clocks within, and delivered to, the CIS8201. For this purpose, the PHY port of the 8201 contains a synchronizing transmit FIFO to absorb frequency differences between the local PHY clock and transmit clocks delivered by a MAC in TBI, GMII, and RGMII/RTBI modes. In TBI/RTBI modes, the device also includes a receive synchronization FIFO. The following table summarizes available synchronization FIFOs for the various MAC interface operating modes. See MII Register 24 (Extended PHY Control Register #2) for more information.

Table 8-1. Synchronization FIFOs

MAC I/F Mode	RX FIFO	TX FIFO
GMII	N/A	Yes
MII	N/A	N/A
RGMII	N/A	Yes
TBI	Yes	Yes
RTBI	Yes	Yes

8.11 Optional Fixed Power Supply Regulator

The CIS8201 can optionally be powered from a single 3.3V power supply when utilizing the device's on-chip regulator control circuit to produce the 1.5V core power supply voltage. The optional on-chip regulator control circuit drives a simple, external series pass type MOSFET transistor for supply regulation, enabling a single 3.3V supply design for lowest cost. See Section 10: "System Schematics" for more information.

9 Package Pin Assignments & Signal Descriptions

9.1 128 Pin LQFP Package Pinout Diagram

For complete specifications, refer to Figure 23-1: “128 LQFP Mechanical Specification”.

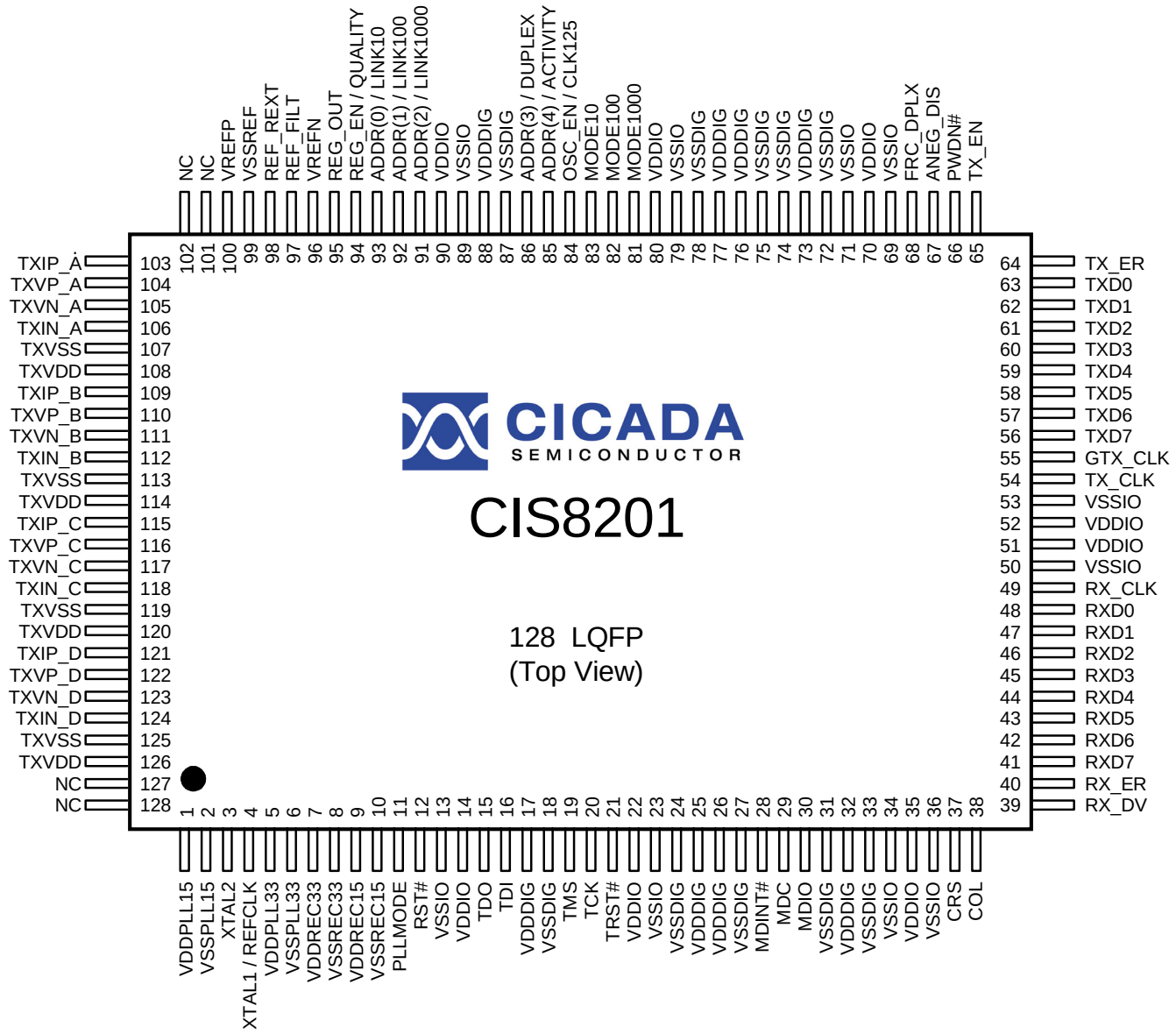


Figure 9-1. CIS8201 Package Pinout

9.2 11 x 11mm 100 Ball LBGA Package Ballout Diagram.

	1	2	3	4	5	6	7	8	9	10	
A	TXIP_A	TXVP_A	REG_EN or QUALITY	REF_FILT	REG_OUT	ADDR4 or ACTIVITY	OSC_EN or CLK125	TX_EN	TX_ER	TXD0	A
B	TXIN_A	TXVN_A	VREFP	REF_REXT	ADDR2 or LINK1000	ADDR3 or DUPLEX	MODE10	MODE1000	TXD1	TXD2	B
C	TXIP_B	TXVP_B	NC	ADDR0 or LINK10	ADDR1 or LINK100	VDDDIG	MODE100	ANEG_DIS	TXD3	TXD4	C
D	TXIN_B	TXVN_B	NC	VSS	VSS	VSS	VDDDIG	PWDN#	TXD5	TXD6	D
E	TXIP_C	TXVP_C	TXVDD	VSS	VSS	VSS	VSSIO	VDDIO	TXD7	TX_CLK	E
F	TXIN_C	TXVN_C	TXVDD	VSS	VSS	VSS	VSSIO	VDDIO	GTX_CLK	RX_CLK	F
G	TXIP_D	TXVP_D	VDDA33	VSS	VSS	VSS	VSSIO	VDDIO	RXD0	RXD1	G
H	TXIN_D	TXVN_D	VDDA33	VDDA15	VDDA15	VDDDIG	VDDDIG	VDDIO	RXD2	RXD3	H
J	PLLMODE	RESET#	TDI	TCK	MDINT#	MDIO	COL	RX_DV	RXD4	RXD5	J
K	XTAL2	XTAL1 or REFCLK	TDO	TMS	TRST#	MDC	CRS	RX_ER	RXD6	RXD7	K
	1	2	3	4	5	6	7	8	9	10	

9.3 Pin Descriptions

Where applicable, all electrical specifications will adhere to the GMII/MII, RGMII/RTBI, and TBI specifications found in their respective standards documents (IEEE 802.3-2000 and RGMII Specification version 1.2a), unless otherwise noted.

9.4 Signal Type Descriptions

Table 9-1. Signal Type Descriptions

Symbol	Signal Type	Description
I	Digital Input	Standard digital input signal. No internal pull-up or pull-down.
I_{PU}	Digital Input with Pull-up	Standard digital input. Includes on-chip 100kΩ pull-up to VDDIO.
$I_{PU(5V)}$	5V-Tolerant Digital Input with Pull-Up	5V-tolerant digital input. Includes on-chip 100kΩ pull-up to VDDIO.
I_{PD}	Digital Input with Pull-down	Standard digital input. Includes on-chip 100kΩ pull-down to VSSIO.
O_{ZC}	Impedance Controlled Output	50Ω integrated (on-chip) source series terminated, digital output signal. Used primarily for timing-sensitive MAC I/F and 125MHz clock output pins, in addition to high speed manufacturing test mode pins.
I/O	Digital Bidirectional	Tristate-able, digital input and output signal.
I_{PU}/O	Digital Bidirectional	Tristate-able, digital input and output signal. Includes on-chip 100kΩ pull-up to VDDIO.
I_{PD}/O	Digital Bidirectional	Tristate-able, digital input and output signal. Includes on-chip 100kΩ pull-down to VSSIO.
OD	Digital Open Drain Output	Open drain digital output signal. Must be pulled to VDDIO through an external pull-up resistor.
A_{DIFF}	Analog Differential	Analog differential signal pair for twisted pair interface.
A_{BIAS}	Analog Bias	Analog bias or reference signal. Must be tied to external resistor and/or capacitor bias network, as shown in System Schematic.
NC	No Connect	No connect signal. Must be left floating.

9.5 MAC Transmit Interface Pins (MAC TX)

Table 9-2. MAC TX Signal Descriptions (Sheet 1 of 2)

LQFP Pin #	LBGA Ball #	Signal Name MAC Interface Mode					Type	Description
		TBI	RTBI	GMII	MII	RGMII		
60 61 62 63	C9 B10 B9 A10	TX[3:0]	TD[8:5] and TD[3:0]	TXD[3:0]	TXD[3:0]	TD[7:4] and TD[3:0]	I_{PD}	**Transmit Data Inputs (All modes).** Transmit code-group data is input on these pins synchronously to GTX_CLK in GMII mode, TXC in RTBI/RGMII modes, or PMA_TX_CLK in TBI mode. **Multiplexed Transmit Data Nibbles (RTBI mode).** Bits [3:0] are synchronously input on the rising edge of TXC, and bits [8:5] on the falling edge of TXC. **Multiplexed Transmit Data Nibbles (RGMII mode).** Bits [3:0] are synchronously input on the rising edge of TXC, and bits [7:4] on the falling edge of TXC.
56 57 58 59	E9 D10 D9 C10	TX[7:4]	*Not used*	TXD[7:4]	*Not used*	*Not used*	I_{PD}	**Transmit Data Inputs (TBI mode).** Transmit data is input on these pins synchronously to PMA_TX_CLK in TBI mode. **Transmit Data Inputs (GMII mode).** Transmit data is input on these pins synchronously to GTX_CLK in GMII mode.
65	A8	TX[8]	*Not used*	TX_EN	TX_EN	*Not used*	I_{PD}	**Transmit Data Code Group, bit [8] (TBI mode).** **Transmit Enable Input (GMII, MII modes).** Synchronized to the rising edge of GTX_CLK (1000Mb mode) or TX_CLK (100Mb mode), this input indicates valid data is present on the TXD bus.
64	A9	TX[9]	TD[9] and TD[4]	TX_ER	TX_ER	TX_CTL	I_{PD}	**Transmit Data Code Group, bit [9] (TBI mode).** **Multiplexed Transmit Data (RTBI mode).** Bit [4] is synchronously input on the rising edge of TXC, and bit [9] on the falling edge of TXC. **Transmit Error Input (GMII, MII modes).** When asserted, this synchronous input causes error symbols to be transmitted from the PHY when operating in 1000Mb or 100Mb modes. **Transmit Enable, Transmit Error Multiplexed Input (RGMII mode).** This input is sampled by the PHY on opposite edges of TXC to indicate two transmit conditions of the MAC: 1) On the rising edge of TXC, this input serves as TXEN, indicating valid data is available on the TD input data bus. 2) On the falling edge of TXC, this input signals a transmit error from the MAC based on a logical derivative of TXEN and TXERR, per RGMII Specification v1.2a (section 3.4).

Table 9-2. MAC TX Signal Descriptions (Sheet 2 of 2)

LQFP Pin #	LBGA Ball #	Signal Name MAC Interface Mode					Type	Description
		TBI	RTBI	GMII	MII	RGMII		
55	F9	PMA_TX_CLK	TXC	GTX_CLK	*Not used*[1]	TXC	I	**PMA Transmit Code-Group Clock Input (TBI mode).** 125MHz transmit code-group clock. This code-group clock is used to latch data into the PMA (in this case, the PHY) for transmission. PMA_TX_CLK is also used by the transmitter clock multiplier unit to generate the 1250MHz bit rate clock. PMA_TX_CLK has a ±100ppm tolerance and is derived from GMII GTX_CLK. **Transmit Clock Input (RTBI mode).** The transmit clock is 125MHz with a ±50ppm tolerance. **Transmit Clock Input (GMII mode).** The transmit clock GTX_CLK is a 125MHz ±100ppm reference clock used to synchronize the TXD data code group, TXD[7:0], into the PCS. **Transmit Clock Input (RGMII mode).** The transmit clock is either 125MHz (1000Mb) or 25MHz (100Mb/10Mb) with a ±50ppm tolerance.

[1] See TX_CLK pin description in following section.

9.6 MAC Receive Interface Pins (MAC RX)

All output pins for the MAC interface include impedance-calibrated, tristate-able output drive capability.

Table 9-3. MAC RX Signal Descriptions (Sheet 1 of 3)

LQFP Pin #	LBGA Ball #	Signal Name MAC Interface Mode					Type	Description
		TBI	RTBI	GMII	MII	RGMII		
45 46 47 48	H10 H9 G10 G9	RX[3:0]	RD[8:5] and RD[3:0]	RXD[3:0]	RXD[3:0]	RD[7:4] and RD[3:0]	O_{ZC}	**Receive Data Code Group (TBI mode).** Part of 10-bit parallel receive code-group data. When code groups are properly aligned, any received code group containing a comma is clocked by PMA_RX_CLK1. **Multiplexed Receive Data Nibbles (RTBI mode).** Bits [3:0] are synchronously input on the rising edge of RXC, and bits [8:5] on the falling edge of RXC. **Receive Data Code Group (GMII, MII modes).** Receive data is driven out of the device synchronously to the rising edge of RX_CLK. RXD[3] is the MSB; RXD[0] is the LSB. **Multiplexed Receive Data Nibbles (RGMII mode).** Bits [3:0] are synchronously output on the rising edge of RXC, and bits [7:4] on the falling edge of RXC.
41 42 43 44	K10 K9 J10 J9	RX[7:4]	*Leave pins uncon-nected*	RXD[7:4]	*Not used*	*Leave pins uncon-nected*	O_{ZC}	**Receive Data Code Group (TBI mode).** Part of 10-bit parallel receive code-group data. When code groups are properly aligned, any received code group containing a comma is clocked by PMA_RX_CLK1. **Receive Data Code Group (GMII mode).** Receive data is driven out of the device synchronously to the rising edge of RX_CLK. RXD[7] is the MSB. *In MII, RGMII, and RTBI modes, these pins are not used.*
49	F10	PMA_RX_CLK0	RXC	RX_CLK	RX_CLK	RXC	O_{ZC}	**PMA Receiver Clock 0 Output (TBI mode).** The 62.5MHz receive clock that the protocol device (MAC) uses to latch odd-numbered code groups in the received PHY bit stream. This clock may be stretched during code-group alignment and is not shortened. **Receive Clock Output (GMII, MII, and RGMII/RTBI modes).** Receive data is sourced from the PHY synchronously on the rising edge of RX_CLK in GMII/MII modes, or RXC in RGMII/RTBI modes, and is the recovered clock from the media.

Table 9-3. MAC RX Signal Descriptions (Sheet 2 of 3)

LQFP Pin #	LBGA Ball #	Signal Name MAC Interface Mode					Type	Description
		TBI	RTBI	GMII	MII	RGMII		
54	E10	PMA_RX_CLK1	*Leave pins unconnected*	*unused*	TX_CLK	*Leave pins unconnected*	O_{ZC}	**PMA Receiver Clock 1 Output (TBI mode).** The 62.5MHz receive clock that the protocol device (MAC) uses to latch even-numbered code groups in the received PHY bit stream. PMA_RX_CLK1 is 180° out of phase with PMA_RX_CLK0. This clock may be stretched during code-group alignment and is not shortened. **Transmit Clock (MII mode).** 25MHz MII clock output used to synchronize TXD data in 100Mb mode, or 2.5MHz MII output clock to synchronize TXD data in 10Mb mode. *In GMII, RGMII, and RTBI modes, these pins should be left unconnected since they are not used.*
39	J8	RX[8]	*Leave pins unconnected*	RX_DV	RX_DV	*Leave pins unconnected*	O_{ZC}	**Receive Data Code Group, bit [8] (TBI mode).** **Receive Data Valid Output (GMII, MII modes).** RX_DV is asserted by the PHY to indicate that the PHY is presenting recovered and decoded data on the RXD[7:0] pins. RX_DV is synchronous with respect to RX_CLK. *In RGMII and RTBI modes, these output pins should be left unconnected since they are not used.*
40	K8	RX[9]	RD[9] and RD[4]	RX_ER	RX_ER	RX_CTL	O_{ZC}	**Receive Data Code Group, bit [9] (TBI mode).** **Multiplexed Receive Data (RTBI mode).** Bit [4] is synchronously input on the rising edge of RXC, and bit [9] on the falling edge of RXC. **Receiver Error Output (GMII, MII modes).** This active high output is synchronous to the received data clock (RX_CLK). For 1000Mb mode, this signal is asserted when error symbols or carrier extension symbols are received; in 100Mb mode, it is asserted when error symbols are received. **Multiplexed Receive Data Valid / Receive Error Output (RGMII mode).** In RGMII mode, this output is sampled by the MAC on opposite edges of RXC to indicate two receive conditions from the PHY: 1) on the rising edge of RXC, this output serves as RXDV, signaling valid data is available on the RD input data bus. 2) on the falling edge of RXC, this output signals a receive error from the PHY based on a logical derivative of RXDV and RXERR, per RGMII Specification v1.2a (section 3.4).

Table 9-3. MAC RX Signal Descriptions (Sheet 3 of 3)

LQFP Pin #	LBGA Ball #	Signal Name MAC Interface Mode					Type	Description
		TBI	RTBI	GMII	MII	RGMII		
37	K7	COM_DET	*Leave pins uncon-nected*	CRS	CRS	*Leave pins uncon-nected*	O_{ZC}	**Comma Detect Output (TBI mode).** An indication that the code group associated with the current PMA_RX_CLK1 contains a valid comma. The TBI in the CIS8201 detects and code-group-aligns to the comma+ bit sequence. **Carrier Sense Output (GMII, MII modes).** CRS is asserted high when a valid carrier is detected on the media.
38	J7	RX_CLK125	*Leave pins uncon-nected*	COL	COL	*Leave pins uncon-nected*	O_{ZC}	**Receiver Clock 125MHz Output (TBI mode).** This signal behaves differently, depending on whether TBI loopback mode is enabled: 1) When no carrier is present on the media, this signal is the same as the device's free running output clock signal, CLK125. 2) When a valid carrier is detected on the media, this output signal is the recovered clock from the TBI's data stream. When switching from one of these three operating modes to another, RX_CLK125's low time will be extended, if necessary, to avoid clock glitching. **Collision Detect Output (GMII, MII modes).** This output is asserted high when a collision is detected on the media. For full-duplex modes, this output is driven low.

9.7 Twisted Pair Interface Pins (TPI)[1]

Table 9-4. TPI Signal Descriptions

LQFP Pin #	LBGA Ball #	Signal Name	Type	Description
103	A1	TXIP_A	A_{DIFF}	**TX/RX Channel "A" Positive Hybrid Pair.** Positive differential pair connected to external termination resistors and then to the positive primary side of the transformer. This pin pair forms the positive signal of the "A" data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1. See Figure 9-2.
104	A2	TXVP_A		
105	B2	TXVN_A	A_{DIFF}	**TX/RX Channel "A" Negative Hybrid Pair.** Negative differential pair connected to external termination resistors and then to the negative primary side of the transformer. This pin pair forms the negative signal of the "A" data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2. See Figure 9-2.
106	B1	TXIN_A		
109	C1	TXIP_B	A_{DIFF}	**TX/RX Channel "B" Positive Hybrid Pair.** Positive differential pair connected to external termination resistors and then to the positive primary side of the transformer. This pin pair forms the positive signal of the "B" data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3. See Figure 9-2.
110	C2	TXVP_B		
111	D2	TXVN_B	A_{DIFF}	**TX/RX Channel "B" Negative Hybrid Pair.** Negative differential pair connected to external termination resistors and then to the negative primary side of the transformer. This pin pair forms the negative signal of the "B" data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6. See Figure 9-2.
112	D1	TXIN_B		
115	E1	TXIP_C	A_{DIFF}	**TX/RX Channel "C" Positive Hybrid Pair.** Positive differential pair connected to external termination resistors and then to the positive primary side of the transformer. This pin pair forms the positive signal of the "C" data channel. In 1000Mb mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10M/100M modes). See Figure 9-2.
116	E2	TXVP_C		
117	F2	TXVN_C	A_{DIFF}	**TX/RX Channel "C" Negative Hybrid Pair.** Negative differential pair connected to external termination resistors and then to the negative primary side of the transformer. This pin pair forms the negative signal of the "C" data channel. In 1000Mb mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10M/100M modes). See Figure 9-2.
118	F1	TXIN_C		
121	G1	TXIP_D	A_{DIFF}	**TX/RX Channel "D" Positive Hybrid Pair.** Positive differential pair connected to external termination resistors and then to the positive primary side of the transformer. This pin pair forms the positive signal of the "D" data channel. In 1000Mb mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10M/100M modes). See Figure 9-2.
122	G2	TXVP_D		
123	H2	TXVN_D	A_{DIFF}	**TX/RX Channel "D" Negative Hybrid Pair.** Negative differential pair connected to external termination resistors and then to the negative primary side of the transformer. This pin pair forms the negative signal of the "D" data channel. In 1000Mb mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10M/100M modes). See Figure 9-2.
124	H1	TXIN_D		

[1]The 1000BASE-T output waveforms of some devices may not conform to the linearity requirements of the IEEE 802.3 standard (Section 40.6.1.2.1). Although devices have been measured to pass in typical operating environments, this parameter is not guaranteed over worst case operating conditions. This has no impact on performance or inter-operability of the PHY.

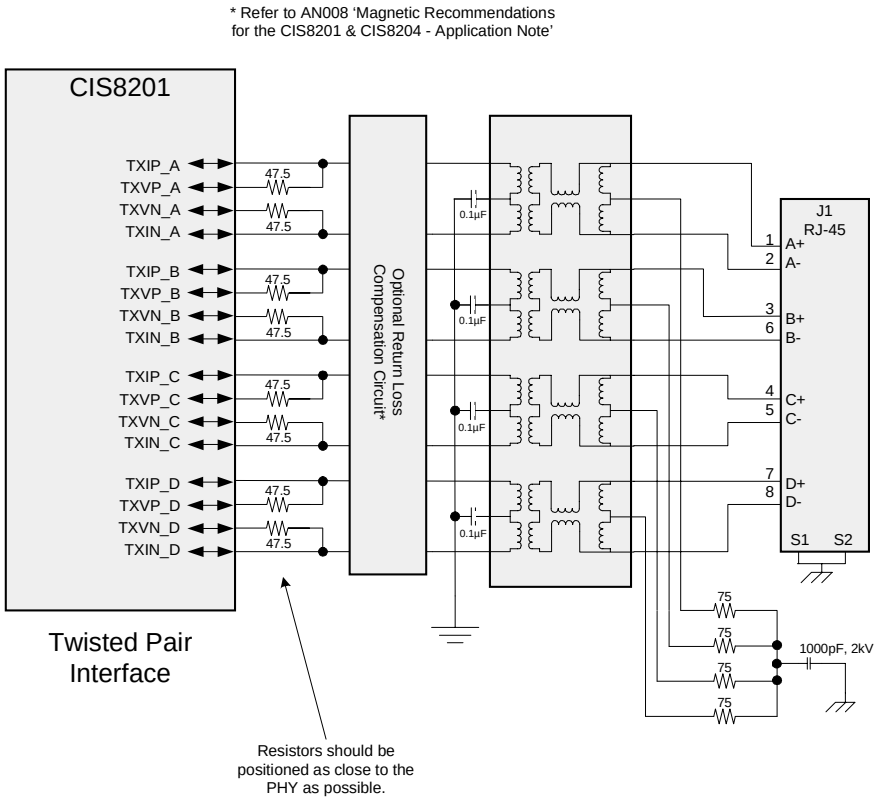


Figure 9-2. CIS8201 Twisted Pair Interface

9.8 Serial Management Interface Pins (SMI)

Table 9-5. SMI Signal Descriptions

LQFP Pin #	LBGA Ball #	Signal Name	Type	Description
29	K6	MDC	I	**Management Data Clock.** A 0 to 12.5MHz reference input used to clock serial MDIO data into and out of the CIS8201. The expected nominal frequency is 2.5MHz, as specified by the IEEE standard. This clock is typically asynchronous with respect to the PHY's transmit or receive clock.
30	J6	MDIO	I/O	**Management Data I/O.** MDIO configuration and status data is exchanged on this pin bidirectionally between the PHY and the Station Manager, synchronously to the rising edge of MDC. This pin normally requires a 1.5kΩ to 2kΩ external pull-up resistor at the Station Manager. The value of the pull-up resistor depends on the MDC clock frequency and the maximum capacitive load on the MDIO pin.
28	J5	MDINT#	OD	**Management Interrupt Output.** This open drain, active low output signal indicates a change in the PHY's link operating conditions for which a station manager must interrogate to determine further information. See MII Registers 25 (bit 15) and 26 (bit 15) for more information. This pin should be pulled up to VDDIO at the Station Manager or controller through an external 10KΩ pull-up resistor.
85 86 91 92 93	A6 B6 B5 C5 C4	ADDR(4)/ACTIVITY ADDR(3)/DUPLEX ADDR(2)/LINK1000 ADDR(1)/LINK100 ADDR(0)/LINK10	I_{PD}/O_{ZC}[1]	**PHY Address Bus (Input).** In input mode, these pins set the 5-bit IEEE-specified PHY address. The states of these pins are latched when a hardware reset is deasserted. On-chip, 100kΩ pull-down resistors provide a default PHY address of 0. **LED Status (Output).** In output mode, these pins serve as the five of the six available direct drive LED output pins (LINK1000, LINK100, LINK10, DUPLEX, and ACTIVITY). For more information, see Section 9.11: "Parallel LED Interface Pins (PLI)" and the diagrams in Section 10.4: "PLI Connections".

[1] In output mode during normal device operation, these pins are used as indicated above. However, for manufacturing test purposes, these pins are also used as digital output pins.

9.9 Configuration and Control Pins (Config)

Table 9-6. Config Signal Descriptions (Sheet 1 of 2)

LQFP Pin #	LBGA Ball #	Signal Name	Type	Description
12	J2	RST#	I	**Hardware Chip Reset.** Active low input, which resets the PHY's MII Management Register Set bits to their default reset states. See MII Register bit 0.15 for more information.
66	D8	PWDN#	I	**Chip Power-Down.** Active low input forces entire device into lowest power operating mode. The PHY is deactivated during power-down mode.

Table 9-6. Config Signal Descriptions (Sheet 2 of 2)

<table>
<tr><th>LQFP Pin #</th><th>LBGA Ball #</th><th>Signal Name</th><th>Type</th><th>Description</th></tr>
<tr><td>83
82
81</td><td>B7
C7
B8</td><td>MODE10
MODE100
MODE1000</td><td>I_{PU}/O_{ZC}</td><td>Force Advertised Operating Mode. The MODE inputs force or preset the PHY's advertised link capabilities (speed and duplex) in conjunction with the FRC_DPLX and ANEG_DIS pins below. The states of these pins force an operating mode when ANEG_DIS is high, and advertising operating mode(s) when ANEG_DIS is low. In output mode, the MODE pins are used for manufacturing test purposes only.

<table>
<tr><th>ANEG_DIS</th><th>FRC_DPLX</th><th>MODE10</th><th>MODE100</th><th>MODE1000</th><th>Effect</th></tr>
<tr><td>0</td><td>X</td><td>0</td><td>0</td><td>0</td><td>Auto-Negotiation active; do not advertise any operating modes</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Advertise 1000BASE-T, half duplex</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Advertise 100BASE-TX, half duplex</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Advertise 100BASE-TX, 1000BASE-T, half duplex</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Advertise 10BASE-T, half duplex</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Advertise 10BASE-T, 1000BASE-T, half duplex</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Advertise 10BASE-T, 100BASE-TX, half duplex</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>Advertise all link speeds, half duplex</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Advertise 1000BASE-T, full/half duplex</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Advertise 100BASE-TX, full/half duplex</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Advertise 100BASE-TX, 1000BASE-T, full/half duplex</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Advertise 10BASE-T, full/half duplex</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>Advertise 10BASE-T, 1000BASE-T, full/half duplex</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>Advertise 10BASE-T, 100BASE-TX, full/half duplex</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>Advertise all link speeds, full/half duplex</td></tr>
<tr><td>1</td><td>X</td><td>0</td><td>0</td><td>0</td><td>Auto-Negotiation disabled; no operating mode forced</td></tr>
<tr><td>1</td><td>0</td><td>X</td><td>1</td><td>0</td><td>Force 100BASE-TX, half duplex</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Force 10BASE-T, half duplex</td></tr>
<tr><td>1</td><td>1</td><td>X</td><td>1</td><td>0</td><td>Force 100BASE-TX, full duplex</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Force 10BASE-T, full duplex</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>Specified by MII register bits</td></tr>
</table>
Notes:
1) The priority of the MODE, FRC_DPLX, and ANEG_DIS pins versus the MII register settings may be changed by writing the Mode/Duplex Pin Priority Select bit (MII Register bit 28.2).
2) If the Auto-Negotiation or Parallel-Detect processes do not result in a link operating mode that matches that specified by the MODE, FRC_DPLX, and ANEG_DIS pins, the link will NOT be established. The PHY will enter the "link_fail" state.
3) Since these pins include on-chip pull-ups, these pins may be left unconnected for designs which do not require this functionality.
4) The states of these pins are not latched. Any change in the states of these pins will cause the PHY to restart the auto-negotiation sequence.
5) In output mode during normal device operation, these pins are used as indicated above. However, for manufacturing test purposes, these pins are also used as digital output pins.</td></tr>
<tr><td>68</td><td>NA</td><td>FRC_DPLX</td><td>I_{PU}</td><td>Force Duplex Mode. When high, this pin causes the Auto-Negotiation process to force the device into full-duplex mode of operation for any link speed. When low (normal operation), the Auto-Negotiation process forces the device into half-duplex mode. This pin's states are valid only when at least one MODE pin is high; it forces the duplex mode when ANEG_DIS is high, and advertises a duplex mode when ANEG_DIS is low.</td></tr>
<tr><td>67</td><td>C8</td><td>ANEG_DIS</td><td>I_{PD}</td><td>Auto-Negotiation Disable. When low (normal operation), this pin enables the Auto-Negotiation function to control all PHY operating characteristics. If at least one MODE pin is high, certain mode(s) will be advertised by the other configuration control pins (MODE10/100/1000 and FRC_DPLX, see above). When ANEG_DIS is high (for testing purposes, or when a station manager is not present), Auto-Negotiation is disabled, and the other configuration control pins become "force advertise" mode pins.</td></tr>
</table>

9.10 System Clock Interface Pins (SCI)

Table 9-7. SCI Signal Descriptions

LQFP Pin #	LBGA Ball #	Signal Name	Type	Description
4	K2	XTAL1/REFCLK	I	**PHY Reference Clock Input / Crystal Input.** The reference input clock can either be a 25MHz or 125MHz reference clock, with a ±50ppm frequency tolerance, or connected to a 25MHz, parallel resonant crystal with a ±50ppm frequency tolerance. When used with a crystal, a 33pF capacitor is connected from this pin to ground.
3	K1	XTAL2	O	**Crystal Output.** 25MHz parallel resonant crystal output. A 33pF capacitor is connected from this output to ground.
11	J1	PLLMODE	I_{PD}	**PLL Mode Select.** Pin is sampled during the device power-up sequence. When PLLMODE is high, indicates to PLL that a 125MHz clock input is used as the PHY's reference clock. When pulled low, indicates to the PLL that the reference clock is a 25MHz reference from either an external crystal or a clock reference input.
84	A7	OSC_EN / CLK125	I_{PD}/O_{ZC}	**Oscillator Enable / 125MHz Reference Clock Output.** In input mode, this pin is sampled on the rising edge of RST# to determine if the on-chip oscillator is enabled, allowing operation with an external 25MHz crystal. When low (the default, due to on-chip 100kΩ pull-down to GND), the oscillator is disabled and the device must be supplied with either a 25MHz or 125MHz clock on the XTAL1/REFCLK input pin, depending on the state of the PLLMODE pin. When crystal oscillator use is desired, OSC_EN should be tied to V+IO with an external pull-up resistor of approximately 10kΩ. In output mode, this pin serves as a general purpose, free-running, low jitter, 125MHz reference clock output, regenerated either from the 25MHz or 125MHz clock reference supplied on the REFCLK pin. The 125MHz clock output pin is enabled (toggling) by default. See MII Register bit 18.0 for more information.

9.11 Parallel LED Interface Pins (PLI)

Table 9-8. PLI Signal Descriptions

LQFP Pin #	LBGA Ball #	Signal Name	Type	Description
85 86 91 92 93 94	A6 B6 B5 C5 C4 A3	ADDR(4) / ACTIVITY ADDR(3) / DUPLEX ADDR(2) / LINK1000 ADDR(1) / LINK100 ADDR(0) / LINK10 REG_EN / QUALITY	I_{PD}/O_{ZC}	**LED Status Outputs**[1]**.** Output pins for directly driving status LEDs. The QUALITY LED status output is optional and alternately serves as the regulator control enable pin during input mode. The remaining five pins also serve as PHY address pins, ADDR(4:0), when a hardware reset is deasserted. The REG_EN and ADDR(4:0) pins are sampled at start-up to determine the polarity of the LED output signals. If the PHY address or REG_EN bit = 0, then the LED output is active high. If the PHY address or REG_EN bit = 1, then the LED output is active low. See Section 13: "Parallel LED Interface" and Section 10.4: "PLI Connections" for more information. When enabled by SMI Register bit 27.3, all LED outputs are pulsed at 5KHz with a 20% duty cycle for low-power operation.

[1] In output mode during normal device operation, these pins are used as indicated above. However, in manufacturing test mode, these pins are also used as digital output pins.

9.12 JTAG Test Access Port (TAP)

Table 9-9. JTAG TAP Signal Descriptions

LQFP Pin #	LBGA Ball #	Signal Name	Type	Description
16	J3	TDI	$I_{PU(5V)}$	**JTAG Test Data Serial Input Data.** Serial test pattern data is scanned into the device on this input pin, which is sampled with respect to the rising edge of TCK. This pin should be tied high during normal chip operation.
15	K3	TDO	O_{ZC}	**JTAG Test Data Serial Output Data.** Serial test data from the CIS8201 is driven out of the device on the falling edge of TCK. This pin should be left floating during normal chip operation.
19	K4	TMS	$I_{PU(5V)}$	**JTAG Test Mode Select.** This input pin, sampled on the rising edge of TCK, controls the TAP (Test Access Port) controller's 16-state, instruction state machine. This pin should be tied high during normal chip operation.
20	J4	TCK	$I_{PU(5V)}$	**JTAG Test Clock.** This input pin is the master clock source used to control all JTAG test logic in the device. This pin should be tied low during normal chip operation.
21	K5	TRST#	$I_{PU(5V)}$	**JTAG Reset.** This active low input pin serves as an asynchronous reset to the JTAG TAP controller's state machine. As required by the JTAG standard, this pin includes an integrated on-chip pull-up resistor. Alternatively, if the JTAG port of the CIS8201 is *not* used on the printed circuit board, then this pin should be tied to ground (VSSIO) with a pull-down resistor.

9.13 Regulator Control and Analog Bias Pins (AP)

Table 9-10. AP Signal Descriptions

LQFP Pin #	LBGA Ball #	Signal Name	Type	Description
98	B4	REF_REXT	A_{BIAS}	**Bias** pin to external 2.26kΩ (1%) resistor tied to analog ground.
97	A4	REF_FILT	A_{BIAS}	**Reference Generator Filter** pin to external 1µF (±10%) capacitor tied to analog ground.
95	A5	REG_OUT	A_{BIAS}	**Regulator Output** used to drive an external series pass regulator. See Power Supply Pins (next section).
94	A3	REG_EN/QUALITY	I_{PD}/O_{ZC}	**Regulator Control Enable.** Active high input enables on-chip regulator control loop to drive an optional external series pass regulator (MOSFET) in order to generate the 1.5V supply voltage. Includes on-chip 100kΩ pull-down to GND. During output mode, this pin alternately serves as an optional direct drive LED output pin (QUALITY). See Section 9.11: "Parallel LED Interface Pins (PLI)" for more information.
100	B3	VREFP[1]	A_{BIAS}	**Positive Reference Bias.** Analog reference generator positive supply input. VREFP should be tied to analog V+A33 supply with a short signal trace. A 1µF capacitor should be placed between VREFP and VREFN, as close to the device package as possible.
96	*NA*	VREFN[1]	A_{BIAS}	**Negative Reference Bias.** Reference filter ground. Must be tied with a short signal trace to the bottom of the REF_FILT capacitor, and then to GND.

[1] VREFP supplies the analog voltage reference circuitry. Careful attention to the PCB layout for this supply pin must be observed in order to avoid any bus drops, which would cause voltage inaccuracy in the voltage reference generator. Separate traces for VREFP and VREFN to the 3.3V power regulator output and ground, respectively, are recommended. VREFN is internally grounded in the LBGA package. See Applications Note "CIS8201 Design and Layout Guidelines" for more information.

9.14 No Connects (NC)

Table 9-11. NC Signal Descriptions

LQFP Pin #	LBGA Ball #	Signal Name	Type	Description
101 102 127 128	C3 D3	NC	NC	Do not connect these pins. They are used only in IC manufacturing test. Leave all pins floating during normal operation.

9.15 Digital Power Supply Pins for LQFP Package

Table 9-12. Digital Power Supply Signal Descriptions for LQFP Package

LQFP Pin #	LQFP Supply Name	Recommended PCB Power Plane Assignment	Type	Nominal Supply Voltage (V)	Description
Digital I/O Power Pins					
14, 22, 35 51, 52 70, 80, 90	VDDIO	V+IO	P	3.3 or 2.5	I/O power supply (3.3V for GMII or TBI modes, or 2.5V for RGMII or RTBI modes).
13, 23, 34, 36 50, 53 69, 71, 79, 89	VSSIO	GND	G	0	I/O ground (0V).
Digital Core Power Pins					
17, 25, 26, 32 73, 76, 77, 88	VDDDIG	V+DIG	P	1.5	Core power supply.
18, 24, 27, 31, 33 72, 74, 75, 78, 87	VSSDIG	GND	G	0	Core ground (0V).

9.16 Digital Power Supply Pins for LBGA Package

Table 9-13. Digital Power Supply Signal Descriptions for LBGA Package

LBGA Ball #	LBGA Supply Name	Recommended PCB Power Plane Assignment	Type	Nominal Supply Voltage (V)	Description
Digital I/O Power Pins					
E8, F8, G8, H8	VDDIO	V+IO	P	3.3 or 2.5	I/O power supply (3.3V for GMII or TBI modes, or 2.5V for RGMII or RTBI modes). RGMII operation with a 3.3V VDDIO supply is also supported.
E7, F7, G7	VSSIO	GND	G	0	I/O ground (0V).
Digital Core Power Pins					
C6, D7, H6, H7	VDDDIG	V+DIG	P	1.5	Core power supply.

9.17 Analog Power Supply Pins for LQFP Package

Table 9-14. Analog Power Supply Signal Descriptions for LQFP Package

LQFP Pin #	LQFP Supply Name	Recommended PCB Power Plane Assignment	Type	Nominal Supply Voltage (V)	Description
Analog I/O Power Pins					
108, 114, 120, 126	TXVDD	V+A33	P	3.3	Line driver 3.3V power supply.
107, 113, 119, 125	TXVSS	GND	G	0	Line driver ground (0V).
Analog Core Power Pins					
7	VDDREC33	V+A33	P	3.3	Analog receive 3.3V power supply.
8	VSSREC33	GND	G	0	Analog receive ground (0V).
9	VDDREC15	V+A15	P	1.5	Analog receive 1.5V power supply.
10	VSSREC15	GND	G	0	Analog receive ground (0V).
5	VDDPLL33	V+A33	P	3.3	PLL 3.3V supply.
6	VSSPLL33	GND	G	0	PLL ground.
1	VDDPLL15	V+A15	P	1.5	PLL 1.5V supply.
2	VSSPLL15	GND	G	0	PLL ground.
99	VSSREF	GND	G	0	Analog reference generator ground.

9.18 Analog Power Supply Pins for LBGA Package

Table 9-15. Analog Power Supply Signal Descriptions for LBGA Package

LBGA Ball #	LBGA Supply Name	Recommended PCB Power Plane Assignment	Type	Nominal Supply Voltage (V)	Description
Analog I/O Power Pins					
E3, F3	TXVDD	V+A33	P	3.3	Line driver 3.3V power supply.
Analog Core Power Pins					
G3, H3	VDDA33	V+A33	P	3.3	Analog receive 3.3V power supply.
H4, H5	VDDA15	V+A15	P	1.5	Analog receive 1.5V power supply.
Ground Pins					
D4, D5, D6, E4, E5, E6, F4, F5, F6, G4, G5, G6	VSS	GND	G	0	Power Supply Ground
E7, F7, G7	VSSIO	GND	G	0	IO Ground

10 System Schematics

10.1 General System Schematic (Separate 3.3V and 1.5V Supply Application with Regulator Disabled)

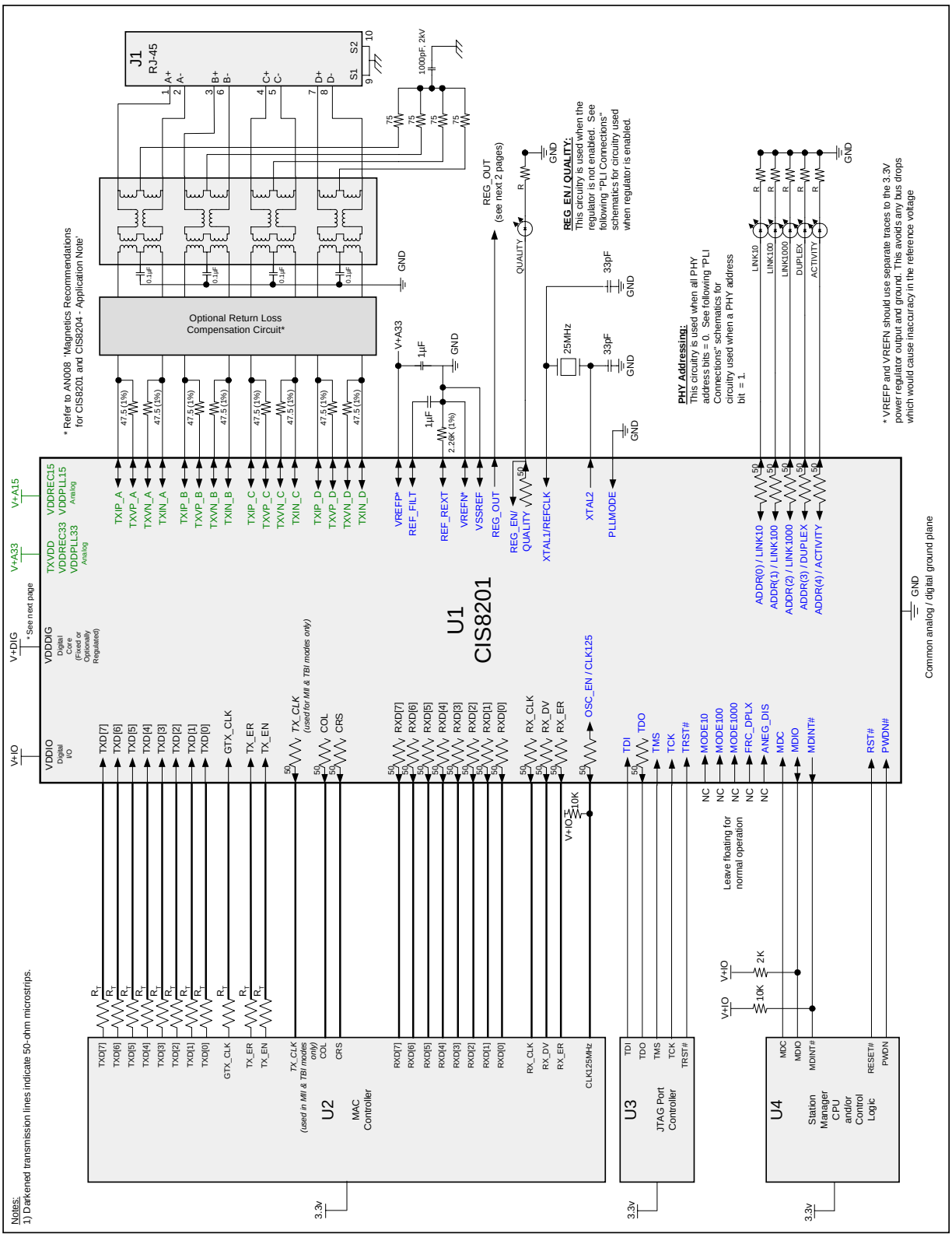


Figure 10-1. General System Schematic (shown with GMII and 3.3V I/O)

10.2 Separate 3.3V and 1.5V Power Supply Configuration

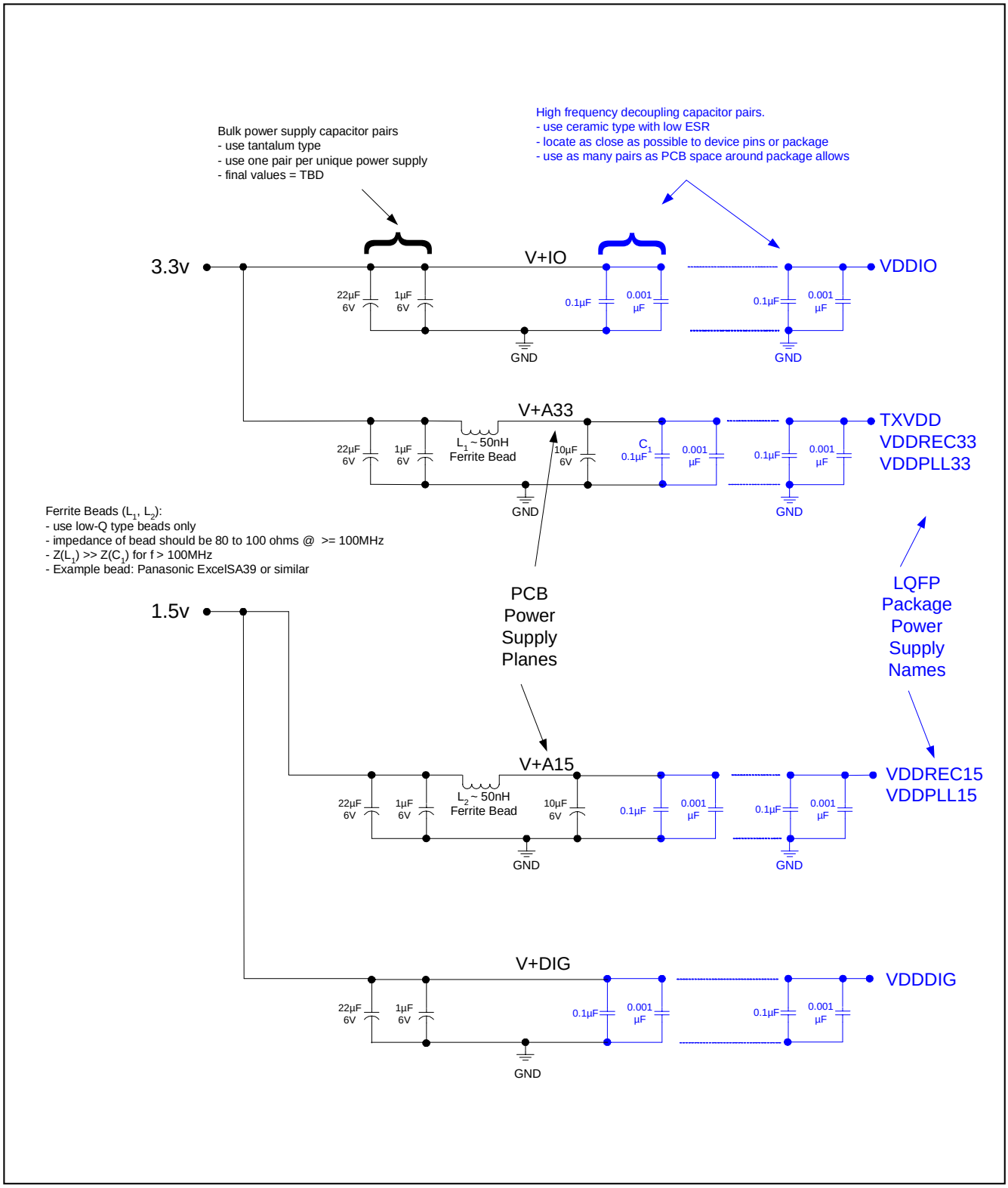


Figure 10-2. Power Supply and Regulator Connections for a 3.3V I/O Application with Separate 3.3V and 1.5V Power Supplies

10.3 3.3V Power Supply with Optional Fixed Regulator at 1.5V

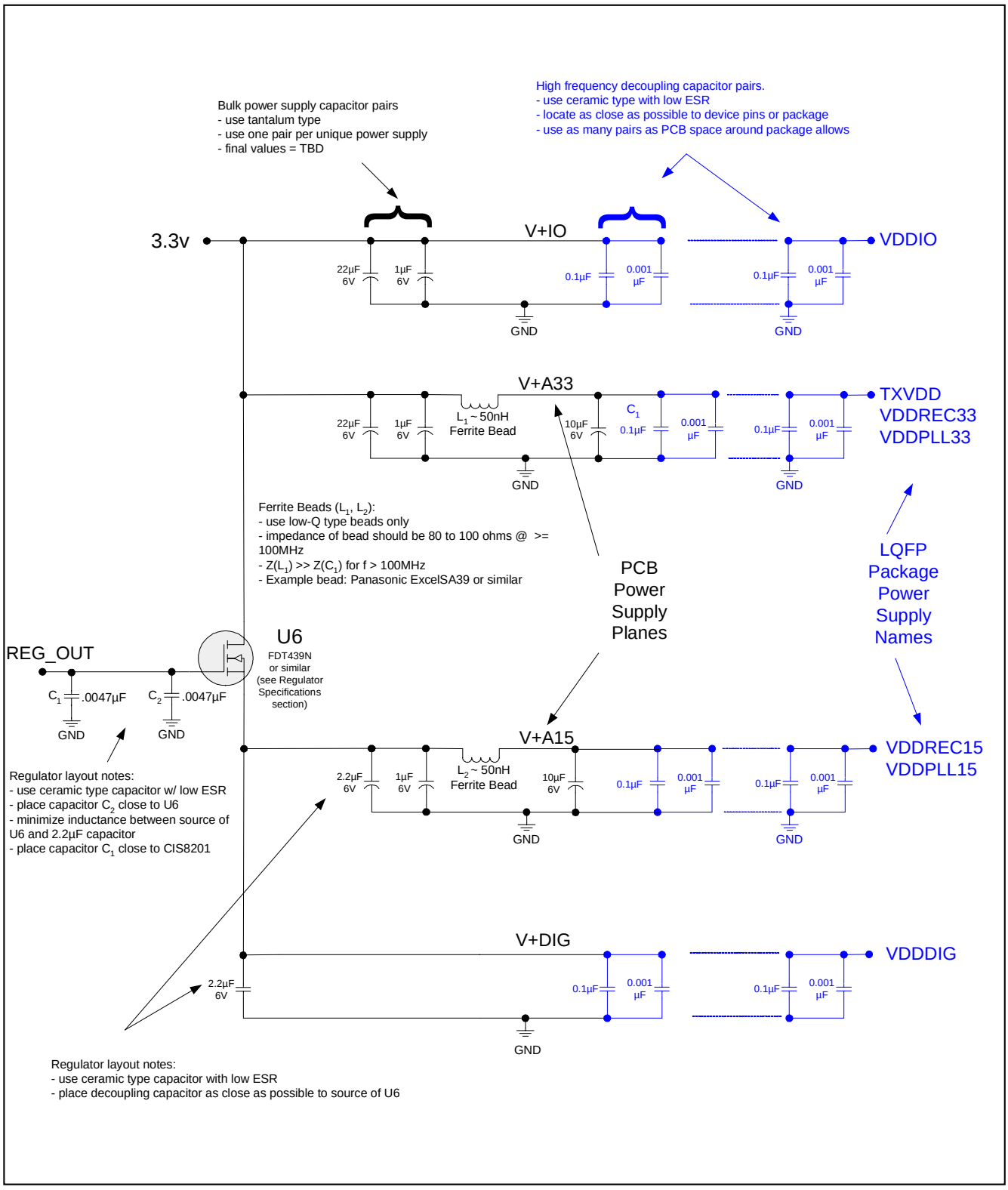


Figure 10-3. Power Supply Connections for a 3.3V I/O Application with a Single 3.3V Supply and Optional Fixed 1.5V Regulator

10.4 PLI Connections[1]

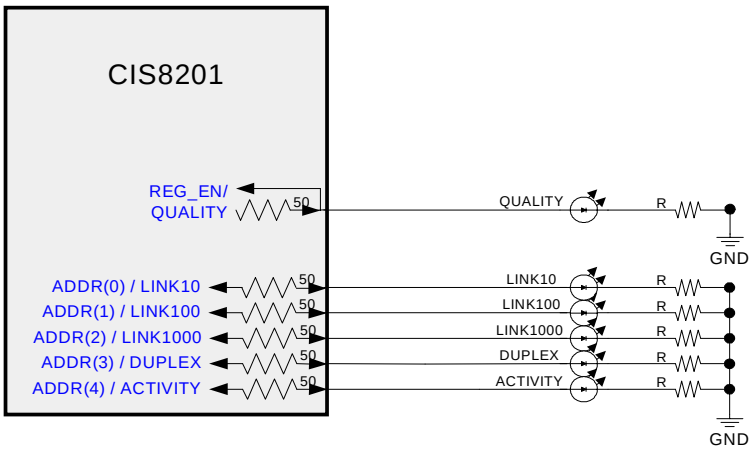


Figure 10-4. PLI Connections for All PHY Address and REG_EN Bits = 0

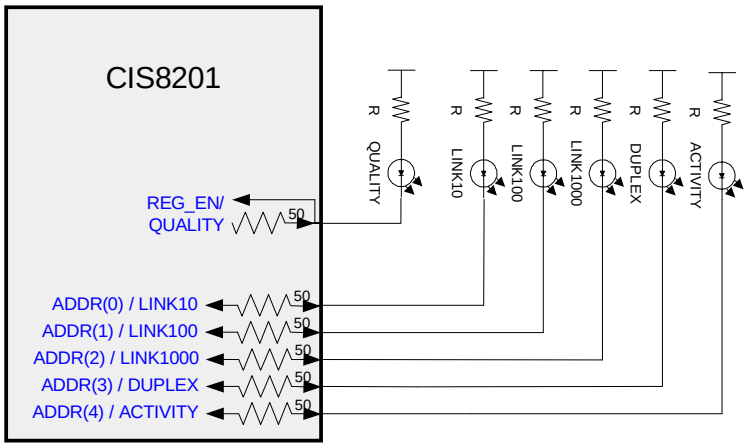


Figure 10-5. PLI Connections for All PHY Address and REG_EN Bits = 1

[1] "R" is typically 200Ω-300Ω. See *CIS8201 PCB Design and Layout Guidelines* for additional information.

11 MAC Interfaces

11.1 GMII MAC I/F

GMII MAC I/F mode, selected by setting the MAC I/F selection bits to GMII/MII mode (Register 23.15:12 = “0000”), clocks data at 125MHz in 1000Mb mode, 25MHz in 100Mb mode, or 2.5MHz in 10Mb mode. The I/O power supply should be set at 3.3V. See Section 15.5: “MAC I/F Configuration” for more information.

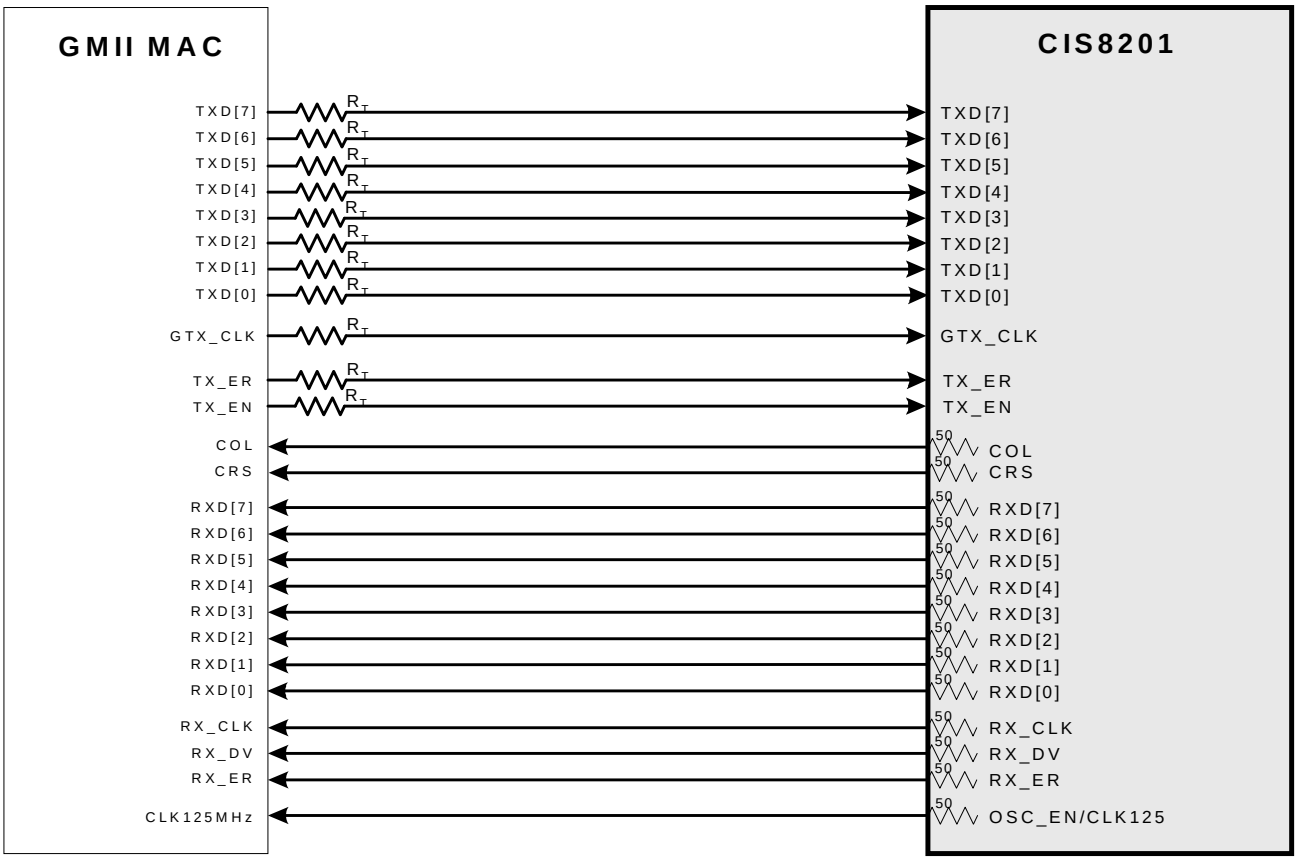


Figure 11-1. GMII MAC Interface

Note:

- MAC TX lines are usually terminated on the source side (at the MAC), with R_T typically ~22Ω.
- Since the CIS8201 includes on-chip, calibrated, series termination resistors, no external series termination resistors are required on the PCB.
- Darkened transmission lines indicate 50Ω controlled impedance traces.

11.2 MII MAC I/F

MII MAC I/F mode, selected by setting the MAC I/F selection bits to GMII/MII mode (Register 23.15:12 = “0000”), clocks data at 25MHz in 100Mb mode, or 2.5MHz in 10Mb mode. The I/O power supply should be set at 3.3V. See Section 15.5: “MAC I/F Configuration” for more information.

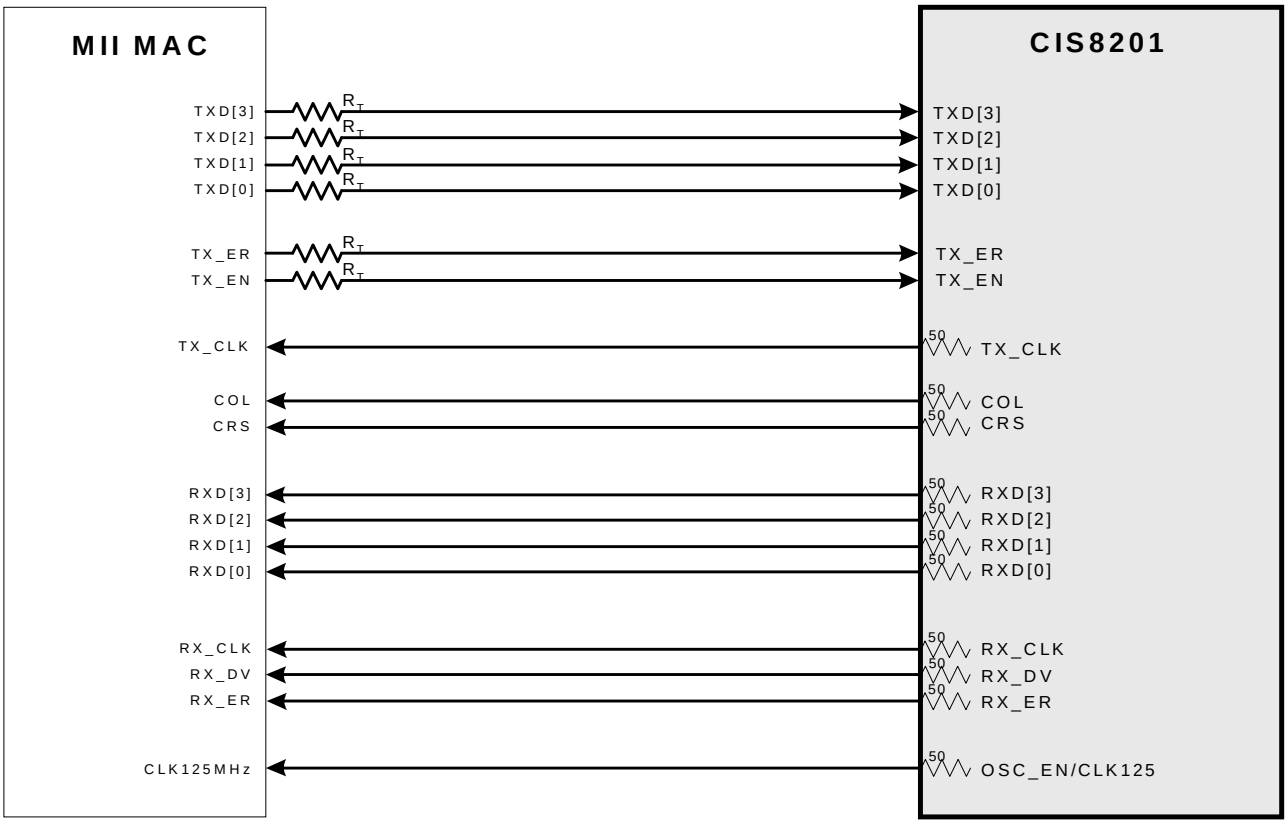


Figure 11-2. MII MAC Interface

Note:

- MAC TX lines are usually terminated on the source side (at the MAC), with R_T typically ~22Ω.
- Since the CIS8201 includes on-chip, calibrated, series termination resistors, no external series termination resistors are required on the PCB.
- Darkened transmission lines indicate 50Ω controlled impedance traces.

11.3 RGMII MAC I/F

RGMII MAC I/F mode, selected by setting the MAC I/F selection bits to RGMII mode (Register 23.15:12 = “0001”), clocks data at 125MHz in 1000Mb mode, 25MHz in 100Mb mode, or 2.5MHz in 10Mb mode. The I/O power supply should be set at 2.5V. See Section 15.5: “MAC I/F Configuration” for more information.

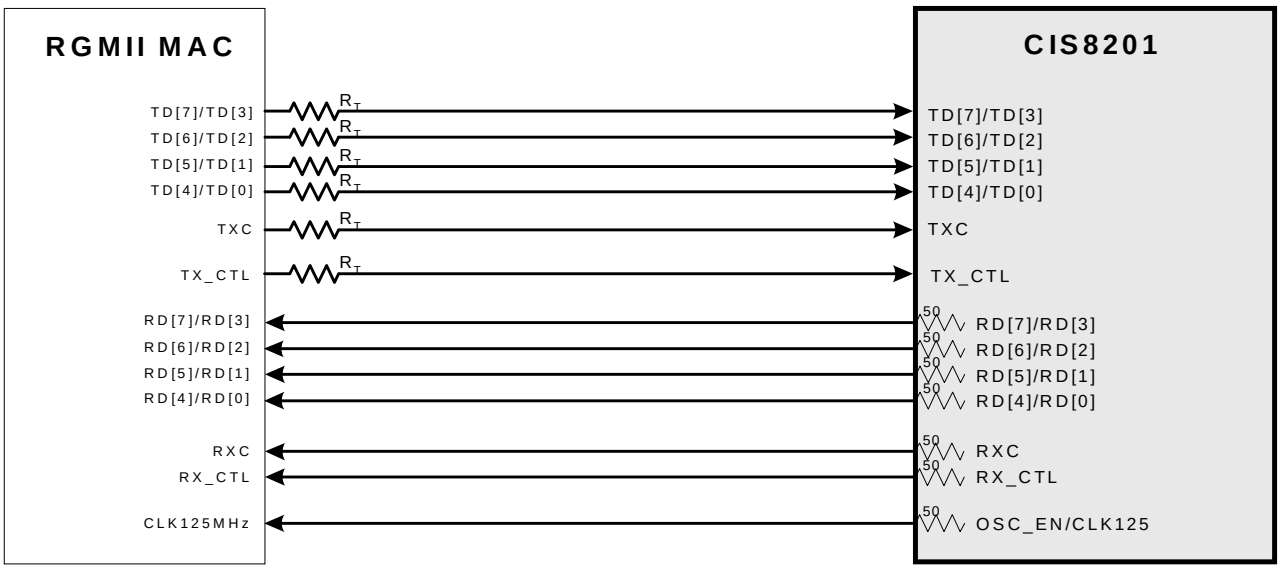


Figure 11-3. RGMII MAC Interface

Note:

- MAC TX lines are usually terminated on the source side (at the MAC), with R_T typically ~22Ω.
- Since the CIS8201 includes on-chip, calibrated, series termination resistors, no external series termination resistors are required on the PCB.
- Darkened transmission lines indicate 50Ω controlled impedance traces.

11.4 TBI MAC I/F

TBI MAC I/F mode, selected by setting the MAC I/F selection bits to TBI mode (Register 23.15:12 = “0010”), clocks data at 125MHz. The I/O power supply should be set at 3.3V. See Section 15.5: “MAC I/F Configuration” for more information.

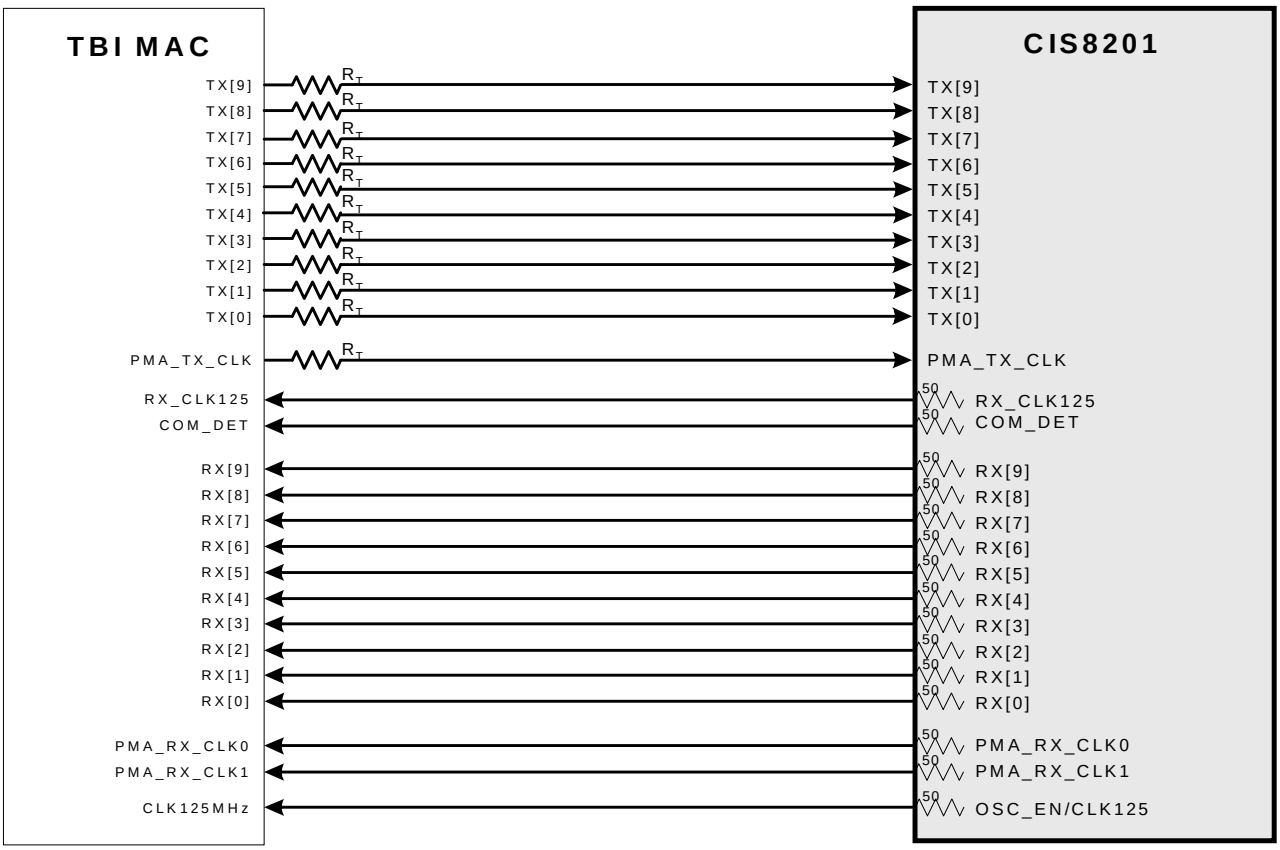


Figure 11-4. TBI MAC Interface

Note:

- MAC TX lines are usually terminated on the source side (at the MAC), with R_T typically ~22Ω.
- Since the CIS8201 includes on-chip, calibrated, series termination resistors, no external series termination resistors are required on the PCB.
- Darkened transmission lines indicate 50Ω controlled impedance traces.

11.5 RTBI MAC I/F

RTBI MAC I/F mode, selected by setting the MAC I/F selection bits to RTBI mode (Register 23.15:12 = “0011”), clocks data at 125MHz. The I/O power supply should be set at 2.5V. See Section 15.5: “MAC I/F Configuration” for more information.

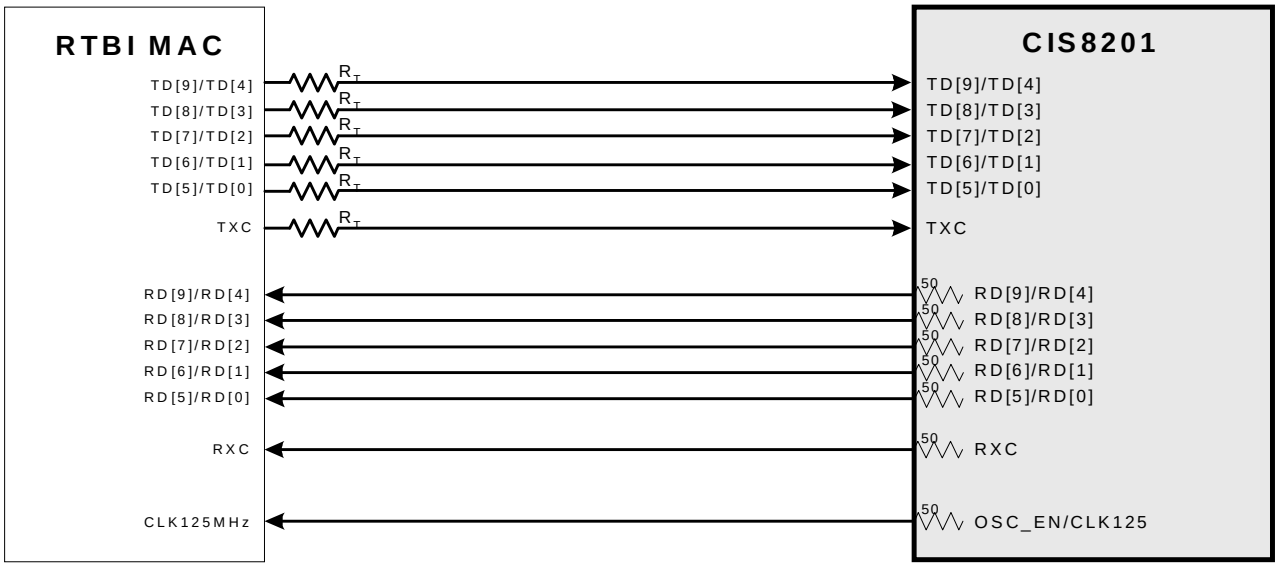


Figure 11-5. RTBI MAC Interface

Note:

- MAC TX lines are usually terminated on the source side (at the MAC), with R_T typically ~22Ω.
- Since the CIS8201 includes on-chip, calibrated, series termination resistors, no external series termination resistors are required on the PCB.
- Darkened transmission lines indicate 50Ω controlled impedance traces.

12 Serial Management Interface (SMI)

The CIS8201 includes a Serial Management Interface, or “SMI”, that is fully compliant with the IEEE 802.3-2000 specifications. The SMI interface provides access to various status and control registers within the CIS8201. This MII Register set is comprised of a block of thirty-two 16-bit registers. Registers 0 through 10, in addition to Register 15, are required for IEEE compliance. The CIS8201 implements all IEEE-required registers, in addition to several others, providing additional performance-monitoring capabilities. See MII Register Descriptions section section for more information.

The SMI is a two pin, synchronous serial interface, with bidirectional data on MDIO being clocked on the rising edge of MDC. The SMI can be clocked at a rate from 0 to 12.5MHz, depending on the total load on MDIO.

As many as thirty-two CIS8201s (thirty-two distinct PHY ports) can share a common SMI signal pair (MDC, MDIO). Thirty-two distinct PHYs can be addressed via the ADDR(4:0) pins. An external pull-up is required on MDIO; it is typically 2kΩ, but depends on the total load on MDIO.

Data is transferred over the SMI using 32-bit frames with an optional and arbitrary length preamble. The SMI frame format is described in the following table.

Table 12-1. SMI Frame Format

	Direction from CIS8201	Preamble	Start of Frame	Op Code	PHY Address	Register Address	Turn-Around	Data	Idle
# of bits		0+	2	2	5	5	2	16	1+
Read	Output	Z’s	ZZ	ZZ	Z’s	Z’s	Z0	data	Z’s
	Input	1’s	01	10	addr	addr	ZZ	Z’s	Z’s
Write	Output	Z’s	ZZ	ZZ	Z’s	Z’s	ZZ	Z’s	Z’s
	Input	1’s	01	01	addr	addr	10	data	Z’s

- Idle: During idle, the MDIO node goes to a high-impedance state. This allows an external pull-up resistor to pull the MDIO node up to a logical “1” state. Since idle mode should not contain any transitions on MDIO, the number of bits is undefined during idle.
- Preamble: For the CIS8201, the preamble is optional. By default, preambles are not expected or required. The preamble is a string of “1”s. See MII Register 1.6 for more information.
- Start of frame: A “01” pattern indicates the start of frame. If these bits are anything other than “01”, all following bits are ignored until the next “preamble:0” pattern is detected.
- Operation code: A “10” pattern indicates a read. A “01” pattern indicates a write. If these bits are anything other than “01” or “10”, all following bits are ignored until the next “preamble:0” pattern is detected.
- PHY address: The next five bits are the PHY address. The CIS8201 responds to a message frame only when the received PHY address matches its physical address. The PHY’s address is indicated by the ADDR(4:0) pins.
- Register address: The next five bits are the register address.
- Turn-around: The next two bits are “turn-around” (TA) bits. They are used to avoid contention when a read operation is performed on the MDIO. During read operations, the CIS8201 will drive the second TA bit, which is a logical “0”.
- Data: The next sixteen bits are data bits. When data is being read from the PHY, data is valid at the output of the PHY from one rising edge of MDC to the next rising edge of MDC. When data is being written to the PHY, data must be valid around the rising edge of MDC.
- Idle: At least one idle bit is required between consecutive SMI frames.

The following two figures diagram SMI read and SMI write operations.

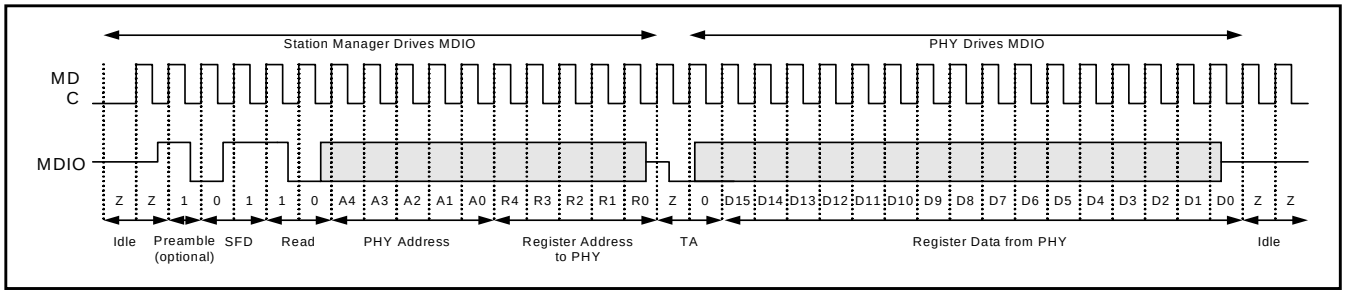


Figure 12-1. MDIO Read Frame

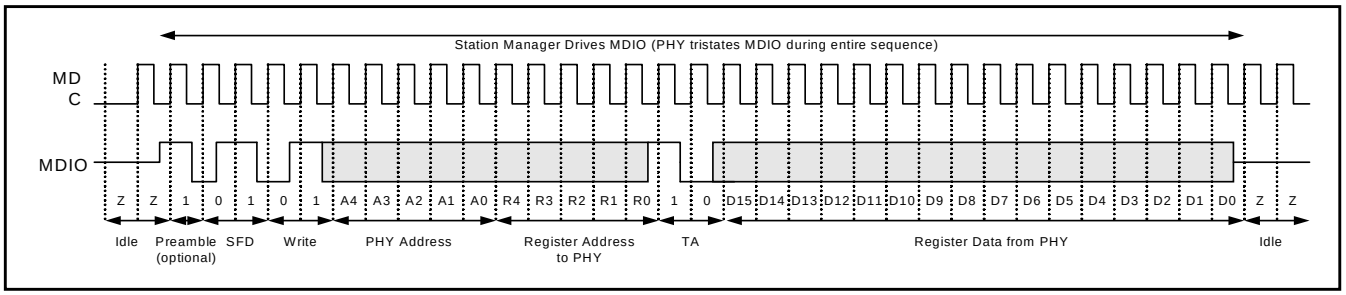


Figure 12-2. MDIO Write Frame

12.1 SMI Interrupt

The SMI includes an active low, open-drain output signal (MDINT#) for signalling the Station Manager when certain events occur in the PHY. When the CIS8201 PHY generates an interrupt, the open-drain MDINT# pin is pulled low, as long as the interrupt pin enable bit (MII Register bit 25.15) is enabled. MDINT# must be tied to VDDIO with a pull-up resistor at the Station Manager. See Figure 12-3.

Interrupts are disabled (masked off) in the CIS8201 PHY by default. All interrupt mask bits are located in MII Register 25. Interrupt status bits are in MII Register 26. An interrupt is automatically acknowledged (cleared) when status bits in Register 26 are read.

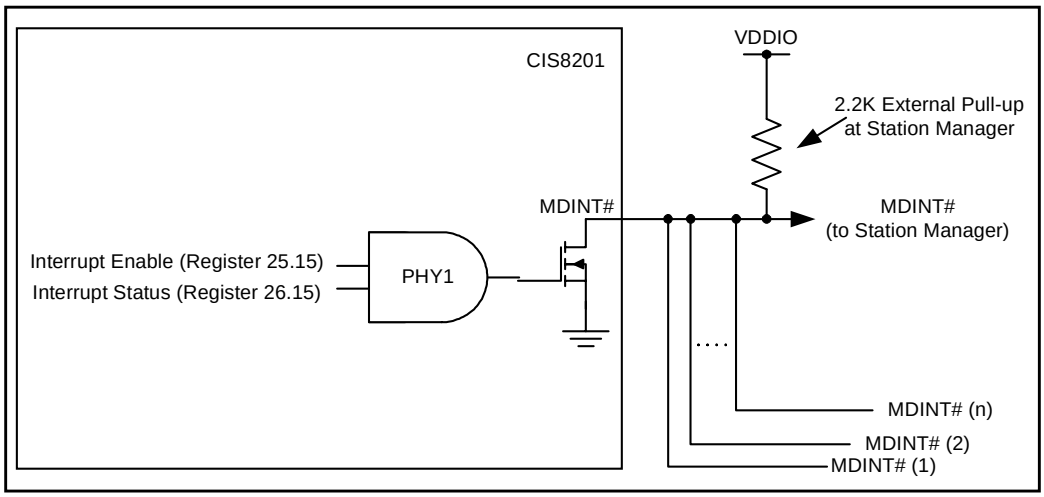


Figure 12-3. Logical Representation of MDINT# Pin

13 Parallel LED Interface

The CIS8201 includes LED output signals in parallel via directly driving LED status output pins. When enabled by SMI Register bit 27.3, all LED outputs are pulsed at 5KHz with a 20% duty cycle for low-power operation.

The ADDR(4:0) and REG_EN pins are sampled at start-up to determine the polarity of the LED output signals. If the PHY address or REG_EN bit is set to 0, then the LED output is active high, and the cathode of the LED is connected to the CIS8201 output pin through a current-limiting resistor. If the PHY address or REG_EN bit is set to 1, then the LED output is active low, and the anode of the LED is connected to the CIS8201 output pin through a current-limiting resistor. See the diagram of the LED output pin equivalent circuit below, or Section 10.4: “PLI Connections” for more information.

The Parallel LED Interface’s bit definitions are defined in the following table.

Table 13-1. PLI Bit Definitions

LED Status Bit	Active State (asserted high)	Inactive State (asserted low)
Duplex	Link is operating in full-duplex mode	Link is operating in half-duplex mode. Collision LED function is turned on, causing this LED to visibly blink at a 5Hz rate when collisions occur.
Link1000	Link established at 1Gbps	Link NOT established at 1Gbps
Link100	Link established at 100Mbps	Link NOT established at 100Mbps
Link10	Link established at 10Mbps	Link NOT established at 10Mbps
Link Quality	Link quality meets or is better than the IEEE-specified bit error rate, AND a valid link is established at either 1Gbps or 100Mbps speed	Link quality is worse than the IEEE-specified bit error rate, OR link is not established at 1Gpbs or 100Mbps speed
Activity[1]	Link is established and Transmit or Receive activity detected	Transmit or Receive activity NOT detected

[1] Activity can be programmed to be steady state or blinking.

The Parallel LED Control Register (MII Register 27) controls all operating characteristics of the Parallel LED Interface. The default states of the LED enable bits in MII Register 27 enable five of the above LEDs in a triple speed Ethernet application. The Link Quality LED status bit is optional, and is disabled by default.

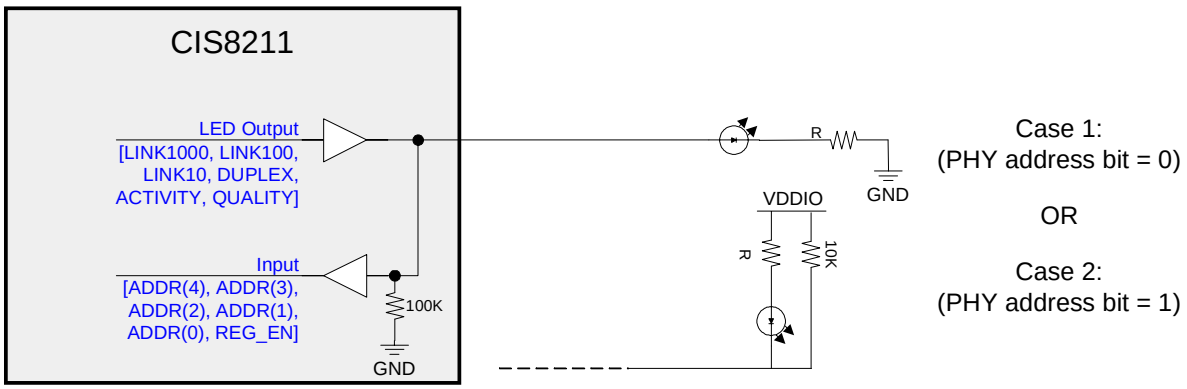


Figure 13-1. LED Output Pin Equivalent Circuit

14 Test Mode Interface (JTAG)

The CIS8201 supports the Test Access Port and Boundary Scan Architecture IEEE 1149.1 standards. The device includes an IEEE 1149.1 conformant test interface, often referred to as a “JTAG TAP Interface”. IEEE 1149.1 defines test logic to provide standardized test methodologies for:

- testing the interconnections between integrated circuits once they have been assembled onto a printed circuit board or other substrate,
- testing the integrated circuit itself during IC and systems manufacture, and
- observing or modifying circuit activity during the component’s normal operation.

The JTAG Test interface logic on the CIS8201, accessed through a Test Access Port (TAP) interface, consists of a boundary-scan register and other logic control blocks. The TAP controller includes all IEEE-required signals (TMS, TCK, TDI, and TDO), in addition to the optional asynchronous reset signal TRST#. Refer to the JTAG TAP Signal Descriptions and System Schematic sections for additional information about these pins.

The following figure diagrams the TAP and Boundary Scan Architecture.

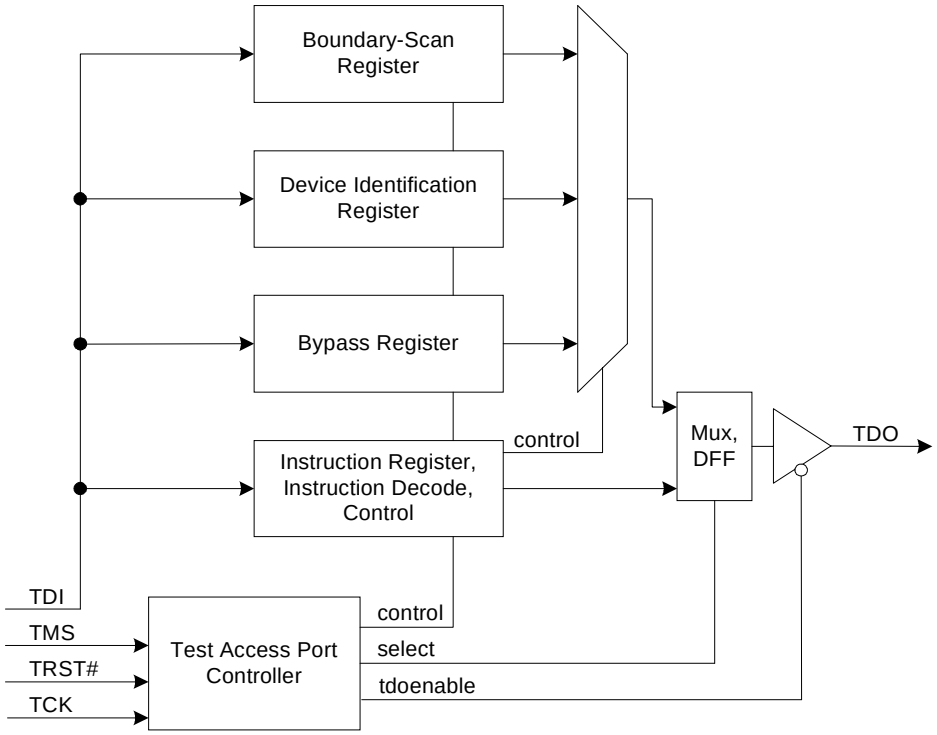


Figure 14-1. Test Access Port and Boundary Scan Architecture

The CIS8201 also includes the optional Device Identification Register, shown in the following table, which allows the manufacturer, part number, and version number of the device to be determined through the TAP Controller. See Chapter 11 of the IEEE 1149.1-1990 specifications for more details. Also, note that some of the information in the identification register is duplicated in the IEEE-specified bit fields in MII Register 3 (PHY Identifier Register #2).

Table 14-1. JTAG Device Identification Register Description

Description	Device Version Number (or Revision Code)	Part Number (or Model Number)	Cicada’s Manufacturer Identity	LSB
Bit Field	31 - 28	27 - 12	11 - 1	0
Binary Value	0001 = Silicon Revision A0 0010 = Silicon Revision A1 0011 = Silicon Revision A2	0000000000000001	00110011000	1

The JTAG TAP port's AC timing requirements can be found in Section 20: "AC Timing Specifications".

14.1 Supported Instructions and Instruction Codes

After a TAP reset, the Device Identification Register is serially connected between TDI and TDO by default. The TAP Instruction Register is loaded either from a shift register (when a new instruction is shifted in), or, if there is no new instruction in the shift register, a hard-wired default value of 0110 (IDCODE) is loaded. Using this method, there is always a valid code in the instruction register, and the problem of toggling instruction bits during a shift is avoided. Unused codes are mapped to the BYPASS instruction.

The CIS8201 supports the instruction codes listed in the following table and described below.

Table 14-2. JTAG Interface Instruction Codes

Instruction	Code	Selected Register	Register Width	Specification
EXTEST	000	Boundary-Scan Register	75	Mandatory IEEE 1149.1
SAMPLE/PRELOAD	001	Boundary-Scan Register	75	Mandatory IEEE 1149.1
IDCODE	110	Device Identification Register	32	Optional IEEE 1149.1
CLAMP	010	Bypass Register	1	Optional IEEE 1149.1
HIGHZ	011	Bypass Register	1	Optional IEEE 1149.1
BYPASS	111	Bypass Register	1	Mandatory IEEE 1149.1
NANDTEST	101	Bypass Register	1	Optional IEEE 1149.1
Reserved	100			

EXTEST
The mandatory EXTEST instruction allows testing of off-chip circuitry and board-level interconnections by sampling input pins and loading data onto output pins. Outputs are driven by the contents of the boundary-scan cells, which have to be updated with valid values (with the PRELOAD instruction) prior to the EXTEST instruction.[1]

SAMPLE/PRELOAD
The mandatory SAMPLE/PRELOAD instruction allows a snapshot of inputs and outputs during normal system operation to be taken and examined. It also allows data values to be loaded into the boundary-scan cells prior to the selection of other boundary-scan test instructions.

IDCODE
The optional IDCODE instruction provides the version number (bits 31:28), part number (bits 27:12), and Cicada's manufacturer identity (bits 11:1) to be serially read from the CIS8201. See Table 14-1: "JTAG Device Identification Register Description" for the CIS8201-specific values for this instruction.

CLAMP
The optional CLAMP instruction allows the state of the signals driven from the component pins to be determined from the Boundary-Scan Register while the Bypass Register is selected as the serial path between TDI and TDO. While the CLAMP instruction is selected, the signals driven from the component pins will not change.[2]

HIGHZ
The optional HIGHZ instruction places the component in a state in which *all* of its system logic outputs are placed in a high impedance state. In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring a risk of damage to the component. This makes it possible to use a board where not all of the components are compatible with the IEEE 1149.1 standard.[2]

[1] Following the use of this instruction, the on-chip system logic may be in an indeterminate state that will persist until a system reset is applied. Therefore, the on-chip system logic may need to be reset on return to normal (i.e., non-test) operation.

[2] Following the use of this instruction, the on-chip system logic may be in an indeterminate state that will persist until a system reset is applied. Therefore, the on-chip system logic may need to be reset on return to normal (i.e., non-test) operation.

BYPASS
The Bypass Register contains a single shift-register stage and is used to provide a minimum-length serial path (one TCK clock period) between TDI and TDO to bypass the device when no test operation is required.

NANDTEST
NANDTEST is an internal command used to activate the NAND Tree test mode. See Section 14.3: “NAND Tree Test Mode” for more information.

14.2 Boundary-Scan Register Cell Order

All inputs and outputs are observed in the Boundary-Scan Register cells. All outputs are additionally driven by the contents of Boundary-Scan Register cells. Bidirectional pins have all three related Boundary-Scan Register cells: the input, the output, and the control.

Port ordering from TDI to TDO is listed in the following table.

Table 14-3. JTAG Boundary-Scan Port Order

No.	Port	Type
1	PLLMODE (IN)	Observe
2	RST# (IN)	Observe
3	MDINT# (OUT)	Observe
4	MDC (IN)	Observe
5	MDIO (IN)	Observe
6	MDIO (OUT)	Control/Observe
7	MDIO (CTRL)	Control/Observe
8	CRS (OUT)	Control/Observe
9	CRS (CTRL)	Control/Observe
10	COL (OUT)	Control/Observe
11	COL (CTRL)	Control/Observe
12	RX_DV (OUT)	Control/Observe
13	RX_DV (CTRL)	Control/Observe
14	RX_ER (OUT)	Control/Observe
15	RX_ER (CTRL)	Control/Observe
16	RXD[7] (OUT)	Control/Observe
17	RXD[7] (CTRL)	Control/Observe
18	RXD[6] (OUT)	Control/Observe
19	RXD[6] (CTRL)	Control/Observe
20	RXD[5] (OUT)	Control/Observe
21	RXD[5] (CTRL)	Control/Observe
22	RXD[4] (OUT)	Control/Observe
23	RXD[4] (CTRL)	Control/Observe
24	RXD[3] (OUT)	Control/Observe
25	RXD[3] (CTRL)	Control/Observe
26	RXD[2] (OUT)	Control/Observe
27	RXD[2] (CTRL)	Control/Observe
28	RXD[1] (OUT)	Control/Observe
29	RXD[1] (CTRL)	Control/Observe
30	RXD[0] (OUT)	Control/Observe
31	RXD[0] (CTRL)	Control/Observe
32	RX_CLK (OUT)	Control/Observe
33	RX_CLK (CTRL)	Control/Observe
34	TX_CLK (OUT)	Control/Observe
35	TX_CLK (CTRL)	Control/Observe
36	GTX_CLK (IN)	Observe
37	TXD[7] (IN)	Observe
38	TXD[6] (IN)	Observe
39	TXD[5] (IN)	Observe
40	TXD[4] (IN)	Observe
41	TXD[3] (IN)	Observe
42	TXD[2] (IN)	Observe
43	TXD[1] (IN)	Observe
44	TXD[0] (IN)	Observe
45	TX_ER (IN)	Observe
46	TX_EN (IN)	Observe
47	PWDN# (IN)	Observe
48	ANEG_DIS (IN)	Observe
49	FRC_DPLX (IN)	Observe
50	MODE1000 (IN)	Observe
51	MODE1000 (OUT)	Control/Observe
52	MODE1000 (CTRL)	Control/Observe
53	MODE100 (IN)	Observe
54	MODE100 (OUT)	Control/Observe
55	MODE100 (CTRL)	Control/Observe
56	MODE10 (IN)	Observe
57	MODE10 (OUT)	Control/Observe
58	MODE10 (CTRL)	Control/Observe
59	CLK125 (OUT)	Control/Observe
60	CLK125 (CTRL)	Control/Observe
61	ACTIVITY (IN)	Observe
62	ACTIVITY (OUT)	Control/Observe
63	ACTIVITY (CTRL)	Control/Observe
64	DUPLEX (IN)	Observe
65	DUPLEX (OUT)	Control/Observe
66	DUPLEX (CTRL)	Control/Observe
67	LINK1000 (IN)	Observe
68	LINK1000 (OUT)	Control/Observe
69	LINK1000 (CTRL)	Control/Observe
70	LINK100 (IN)	Observe
71	LINK100 (OUT)	Control/Observe
72	LINK100 (CTRL)	Control/Observe
73	LINK10 (IN)	Observe
74	LINK10 (OUT)	Control/Observe
75	LINK10 (CTRL)	Control/Observe

14.3 NAND Tree Test Mode

The NAND Tree test mode is an asynchronous test mode that is especially useful due to its speed advantages. This command connects groups of input pins together into a NAND Tree scheme. A group's inputs are initially held to logic high while its corresponding group of output pins are driven low. If any one of the input pins within a group is toggled from logic high to logic low, all the outputs in that group will toggle to the logic high state. This mode is entered by using the NANDTEST instruction code "101" within the JTAG Interface.

There are two NAND Tree pin groups, each with its separate assigned group of outputs, as listed in the following table and logic diagrams.

Table 14-4. NAND Tree Chains

Inputs	Outputs
GTX_CLK, TX_ER, TX_EN, TXD[7:0]	RX_CLK, TX_CLK, RX_ER, RX_DV, RXD[7:0], COL, CRS
PLLMODE, MODE10, MODE100, MODE1000, FRC_DPLX, ANEG_DIS, MDIO, MDC	LINK10, LINK100, LINK1000, ACTIVITY, DUPLEX, CLK125

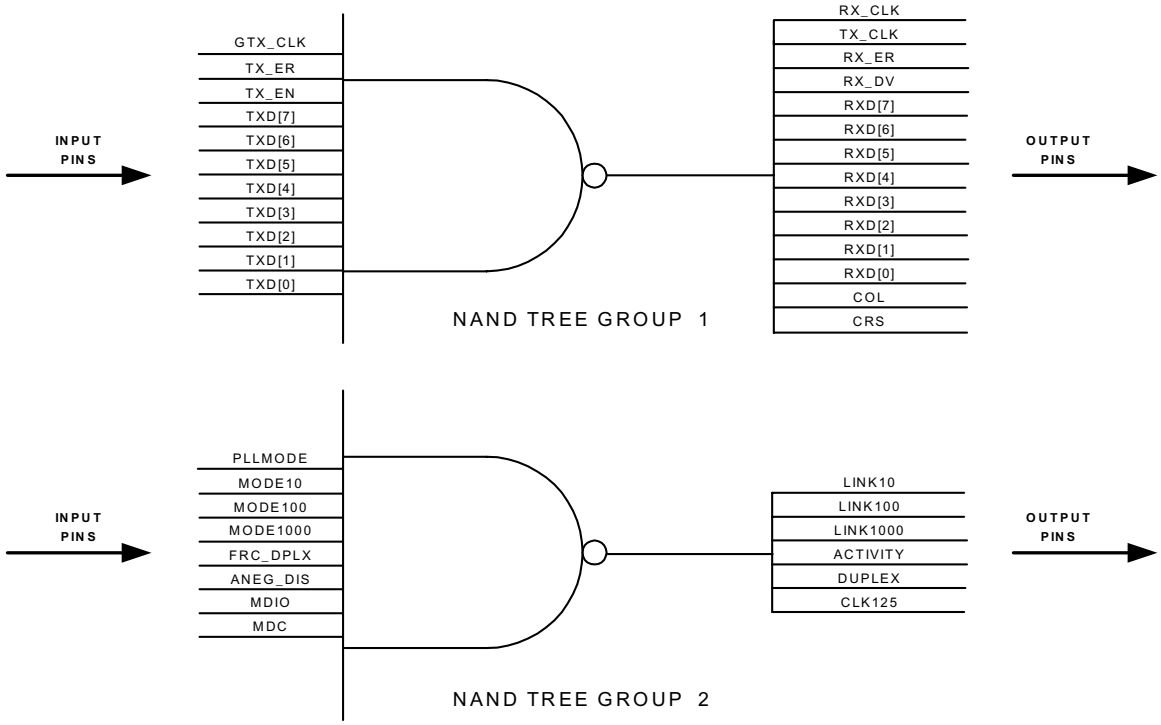


Figure 14-2. NAND Tree Logic Diagrams

15 Initialization & Configuration

15.1 Resets

A hardware reset is asynchronous (not related to MDC or any other input clock) and is activated by asserting the RST# signal (pulling to logical “0”).

A software reset is synchronous with MDC. The table below summarizes the differences between the various initialization types.

Table 15-1. Initialization Types

Initialization Type	Activated by	MII Register States	TX_CLK and RX_CLK Active?
Power-Up	1) Power supplies stable 2) Drive PWDN# = 1 3) Drive RST# = 1	Undefined	No
Hardware Reset	Drive RST# = 0	Default	No
Software Reset	Write MII Register 0.15 = 1	Default	Yes
Power-Down	Drive PWDN# = 0	Values are retained	No

The CIS8201 supports four power management modes:

1) IEEE-Compliant Mode (Register bit 0.11 = 1; RST# and PWDN# are driven high; CLK125 and MDC/MDIO remain active; analog reference voltages and currents, including the PLL, remain powered up; a “software power-down”),
2) “Hardware Power-Down” (RST# is held high while PWDN# is driven low; CLK125 and MDC/MDIO remain active; analog reference voltages and currents, including the PLL, remain powered up),
3) “Sleep” Mode (RST# is driven low while PWDN# is low; CLK125 and MDC/MDIO are disabled; all analog circuits are powered down), and
4) ActiPHY™ Power Management Mode (see Section 15.9: “ActiPHYTM Power Management” for more information).

15.2 Power-Up Sequence

The power-up sequence for the CIS8201 is as follows. Note that device power-up cannot occur unless the PWDN# pin is de-asserted (pulled high) at least 10ms before RST# goes high. For more information, see Section 20.16: “Power-Down and Reset Timing”.

1) Analog Initialization: After all the power supplies are stable and within their specified limits, the analog circuitry (except for the PLL) establishes proper bias currents and voltages within 10ms.

2) PLL Lock: Once the RST# pin goes inactive (to a logical “1”), the PLL completes lock for the next 50µs. All state machines, logic, and registers are set to their default states during this time.

3) Auto-Negotiation / Parallel-Detect Sequence: If Auto-Negotiation is enabled (see MII Register bit 0.12), and the MODE10/100/1000, FRC_DPLX, and ANEG_DIS pins do not force the device into a manual configuration (see below), the Auto-Negotiation and Parallel-Detect state machines are automatically activated by the PHY. After the Auto-Negotiation or Parallel-Detect processes are completed, the device attempts to establish link.

15.3 Manual Configuration

The MODE10/100/1000 and FRC_DPLX pins are intended for use in designs where a station manager is not available, or when manual PHY characterization testing or system diagnostics must be performed. The states of these pins will force the PHY's advertised link capabilities only when the ANEG_DIS pin is set high. This situation implies that the MII registers will not generally be extensively manipulated to control a PHY's operation (when the MODE10/100/1000, FRC_DPLX, and ANEG_DIS pins are used to set the operating mode). The states of these pins are not latched; any change in the states of these pins will cause the PHY to restart the auto-negotiation sequence.

In order to force the PHY's speed and duplex operating modes, the recommended sequence of events is as follows:

1) During a power-up or hardware reset sequence, force the MODE10/100/1000 and FRC_DPLX pins to their desired states (e.g., VDDIO or GND). ANEG_DIS must also be set high in order to preset link capabilities. See Register bit 28.2 for more information.

2) Subsequent Auto-Negotiation and Parallel-Detect processes will now use the values specified by the MODE10/100/1000 and FRC_DPLX pins.

The effect of values forced on the MODE10/100/1000 and FRC_DPLX pins when Auto-Negotiation or Parallel-Detect processes are completed will now only be visible in the Auxiliary Control and Status Register (28, bits 5:3).

15.4 Auto-Negotiation

The CIS8201 supports Auto-Negotiation, a standards-defined (IEEE 802.3-2000, Clause 28) process for determining the operating attributes of the local PHY and its link partner. Auto-Negotiation evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode.

In particular, Auto-Negotiation can determine speed, duplex, and MASTER/SLAVE modes for 1000BASE-T. Auto-Negotiation also allows the local MAC to communicate with the Link Partner MAC (via optional "Next-Pages") to set attributes that may not be defined in the standard.

The operating mode of the local PHY of the CIS8201 can be set by any one of three methods:

- Configuration control pins (MODE10/100/1000, FRC_DPLX, and ANEG_DIS), as described in the previous section,
- SMI configuration control bits, or
- Auto-Negotiation.

Auto-Negotiation is used by default. Indeed, a station manager (connected via the SMI to the CIS8201) is optional; in the absence of a station manager, the CIS8201 will auto-negotiate upon exiting reset.

By default, the configuration control pins take precedence over the SMI configuration control bits unless ANEG_DIS is low, which is the default operating mode for enabling Auto-Negotiation. See Section 9.9: "Configuration and Control Pins (Config)" for more information.

If Auto-Negotiation is enabled, Auto-Negotiation will start upon any of the following conditions:

- Release of hardware reset,
- Release of software reset,
- Restart Auto-Negotiation (Register bit 0.9),
- Release of Power-Down (Register bit 0.11), or
- Entering the "link_fail" state.

Once Auto-Negotiation starts, the CIS8201 will first determine if the Link Partner is Auto-Negotiation capable. If the Link Partner is Auto-Negotiation capable, the CIS8201 will, by default, determine the highest-performance operating mode that is common between the local PHY and the Link Partner's PHY. If the Link Partner is not Auto-Negotiation capable, the CIS8201 will use Parallel-Detect to set the operating mode.

Note: IEEE 802.3z (Clause 37) TBI Auto-Negotiation was conceived to support two PHYs on opposite sides of a fiber optic cable, not to support MAC to PHY Auto-Negotiation. Therefore, when connecting the CIS8201 to a TBI-based MAC, IEEE 802.3z Auto-Negotiation is partially supported. The MAC will automatically receive an 802.3z Auto-Negotiation handshake from the CIS8201. This handshake will, by default, always send bits to indicate: full-duplex mode, no explicit pause control (though the link will still be able to receive any valid flow control frames), and no remote fault support. This default mode can only be disabled by using an unused bit combination ("111") of the TX FIFO Latency Register (24.9:7).

15.5 MAC I/F Configuration

The MAC interface supports five different modes of operation: GMII, MII, RGMII, TBI, and RTBI. By default, the device operates in GMII MAC I/F mode with 3.3V I/O. Alternate MAC I/F operating modes, as well as I/O voltage supply levels, are selected by writing the appropriate MII Register 23 (Extended PHY Control Register #1) as shown in the following table.

Table 15-2. MAC I/F Mode Descriptions

MAC I/F Mode	Standard (Clause)	Supported Speed (Mbps)	Data Path Width x Freq.	I/O Voltage (Spec.)	Mode Selected by	Notes
GMII	802.3 (Clause 35)	1000	8b x 125MHz	3.3V	Hardware Reset or Software Reset or MII Register Write: 23.15:12 = 0000 23.11:9 = 000	Default operating mode
MII	802.3 (Clause 22)	100	4b x 25MHz			MII is default operating mode when link Auto-Negotiates (or is forced) to operate at 10Mb or 100Mb speeds
		10	4b x 2.5MHz			
RGMII[1]	RGMII v1.3	1000	4b x 125MHz DDR	2.5V (JEDEC EIA/JESD8-5)	MII Register Write: 23.15:12 = 0001 23.11:9 = 001 23.8 = 0/1 (uncompensated/ compensated mode)	RGMII vs. 802.3 differences: 1) TXC is always generated by the MAC 2) RXC is always generated by the PHY
	RGMII v1.3 + MII (802.3 Clause 22)	100	4b x 25MHz			
		10	4b x 2.5MHz			
TBI	802.3 (Clause 36)	1000	10b x 125MHz	3.3V	MII Register Write: 23.15:12 = 0010 23.11:9 = 000	-
RTBI	RGMII v1.3	1000	5b x 125MHz DDR	2.5V[1] (JEDEC EIA/JESD8-5)	MII Register Write: 23.15:12 = 0011 23.11:9 = 001 23.8 = 0/1 (uncompensated/ compensated mode)	-

[1] The RGMII interface is timing compatible with the v1.3 and v2.0 specifications. The RGMII interface is not electrically compatible with the v2.0 specifications as this requires HSTL voltage levels which the CIS8201 does not support. RGMII may also be used with a 3.3V supply.

Switching between the various MAC interface modes is not recommended during normal operation, unless as supported by the GMII and RGMII standards to allow switching between 1000Mb, 100Mb, and 10Mb speeds. In addition, although any of the MAC interfaces will function electrically with I/O power supplies set at 3.3V or 2.5V, correct logical operation of the MAC interfaces at I/O voltages other than those specified above is not implied or guaranteed.

15.6 System Clock Interface (SCI)

The SCI is a four-pin interface comprised of the following pins: PLLMODE, XTAL1/REFCLK, XTAL2, and OSC_EN/CLK125. See Section 9.10: “System Clock Interface Pins (SCI)” for more information.

PLLMODE is an input pin, sampled during power-up or reset sequences, which sets the reference clock frequency used by the PLL. When PLLMODE is low, the reference clock frequency of REFCLK is required to be 25MHz, with a ±50ppm frequency offset tolerance. When PLLMODE is high, REFCLK’s input frequency must be 125MHz (±50ppm).

The SCI also provides a free-running, general purpose, 125MHz output clock signal, CLK125, for use within the system. By default, the CLK125 output pin is normally enabled (toggling) by default (but driven low when not enabled). OSC_EN is sampled on the rising edge of RST# to determine if the on-chip oscillator is enabled, allowing operation with an external 25MHz crystal. See Register 18.0 and Section 9.10: “System Clock Interface Pins (SCI)” for more information on OSC_EN/CLK125.

15.7 Auto MDI / MDI-X Function

For trouble-free configuration and management of Ethernet links, the CIS8201 includes robust Automatic Crossover Detection functionality for all three speeds (10BASE-T, 100BASE-TX, and 1000BASE-T) – fully compliant with the IEEE standard. In addition, the CIS8201 detects and corrects polarity errors on *all* MDI pairs, which is not required by the standard. Both the Automatic MDI/MDI-X and Polarity Correction functions are enabled by default.[1] However, complete user control of these two features is contained in MII Registers 18.5 (Automatic MDI/MDI-X Correction) and 18.4 (Automatic Polarity Correction). Status bits for each of these functions are indicated in MII Registers 26.6 and 26.5. For all three speeds of operation, any of the following MDI pair (A, B, C, D) connection combinations may be supplied to the device, with complete automatic detection and correction by the CIS8201.

The CIS8201's Automatic MDI/MDI-X algorithm will successfully detect, correct, and operate with any of the MDI wiring pair combinations listed in the following table.

Table 15-3. Accepted MDI Pair Connection Combinations

	RJ-45 Connections				Comments
	1,2	3,6	4,5	7,8	
MDI Pair Connection Combinations Accepted by CIS8201	A	B	C	D	Normal MDI mode Normal DTE/NIC mode No crossovers
	B	A	C	D	MDI-X mode Normal for switches & repeaters Crossover on A and B pairs only
	A	B	D	C	Normal MDI mode Normal for DTEs (NICs) No crossovers Pair swap on C and D pairs
	B	A	D	C	Normal MDI-X mode Normal switch/repeater mode Crossovers assumed Crossover on A and B pairs Pair swap on C and D pairs

[1] Consistent with 10/100/1000BASE-T PHYs on the market today, Auto MDI/MDI-X functionality is automatically disabled when Auto-Negotiation is disabled.

The diagram below depicts the last combination in the table above, showing the CIS8201 operating with a link partner with crossovers on all four MDI pairs.

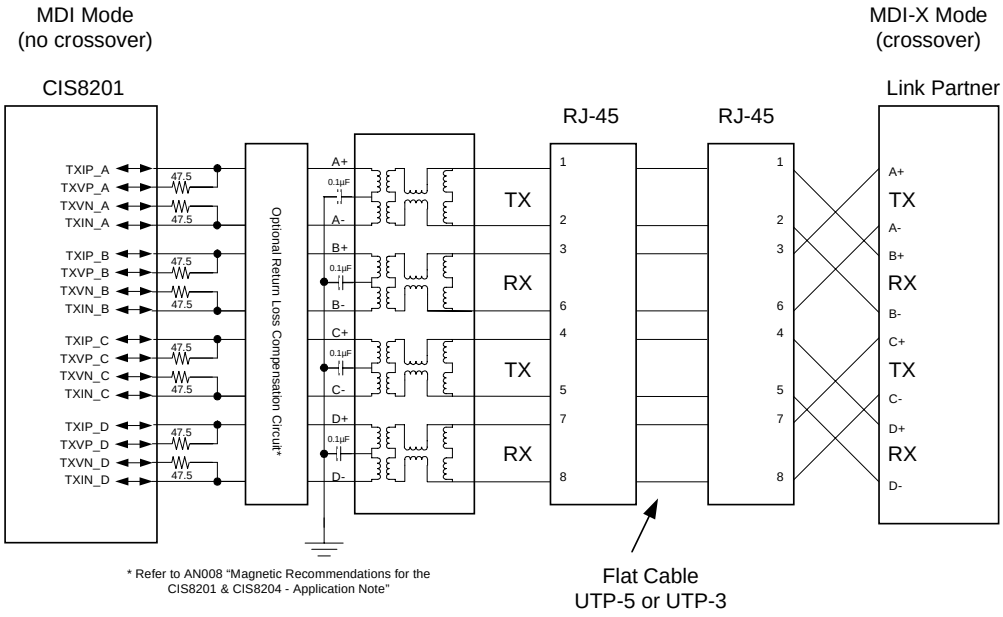


Figure 15-1. MDI / MDI-X Crossover Example

15.8 Parallel LED I/F

See Section 13: "Parallel LED Interface" for more information.

15.9 ActiPHY™ Power Management

In addition to the IEEE-specified (i.e., Register bit 0.11 = 1) and "sleep" power management modes, the CIS8201's ActiPHY™ power management mode enables support for power-sensitive applications such as laptop computers with Wake-on-LAN™ capability by utilizing a signal-detect function[1].

When the Station Manager detects that the PHY has not established a link for an arbitrary amount of time (determined by the Station Manager), it can put the PHY in a low-power energy-detect state by setting the ActiPHY™ Enable bit (MII Register bit 23.5). In response, the PHY powers down all unused blocks, stops auto-negotiating, and enables the logic block that generates an interrupt when valid energy levels are detected on the media interface. The Station Manager also sets the Link State-Change/ActiPHY™ interrupt mask bit (25.13) so that the PHY can generate an interrupt in response to a signal-detect event. With bits 23.5, 25.15, and 25.13 all set to "1", the Interrupt Status Register (MII Register 26) must be read in order to automatically clear any pending interrupts. The PHY will only respond to the presence of valid network energy levels (listed in MII Register 22.11:10) when in this mode; it does not attempt to establish a link.

When the PHY does detect energy on the media interface, it sends an interrupt to the Station Manager if bits 25.15 and 25.13 are set to "1". In response, the Station Manager must clear bit 23.5, which automatically brings the CIS8201 out of the ActiPHY™ low-power mode and allows it to establish a link.

There are two ActiPHY™ power management modes. If bit 18.0 (125MHz clock output enable bit) is set to "1", then the PLL will remain on. If bit 18.0 is set to "0", then the PLL will be turned off, further reducing power consumption. In either ActiPHY™ low-power mode, the CIS8201 will consume less than 100mW. See Section 18.4: "Thermal Specifications" for the typical power consumption values in each ActiPHY™ mode.

15.10 Power Supply Decoupling and Board Layout Guidelines

Please refer to the System Schematics in this document and the Applications Note: "Design and Layout Guidelines for the CIS8201".

[1]See Wake-on-LAN Design Considerations Application note for further details.

16 MII Register Set Conventions

The MII registers' bit modes are defined in the following table.

Table 16-1. MII Register Bit Modes

Register Bit Type	Description
R/W	Read and Write
RO	Read Only
LH	Latched High
LL	Latched Low
SC	Self-Cleared
RS	Reset-Sticky

Register conventions are as follows:

- Shaded registers indicate standard MII registers.
- All unshaded registers are optional registers, per the IEEE 802.3 standard.
- "Reset value" refers to the state of register bit(s) after *either* a hardware *or* a software reset. The only difference between a hardware and software reset is that all internal analog reference voltages and currents, including the PLL, are powered down while a hardware reset is asserted, but are not powered down while a software reset is asserted.
- "Reset-Sticky" refers to register bit(s) that may not be reset when a software reset is issued - See section 22.29 for a description of the Reset-Sticky bit function.

16.1 MII Register Names & Addresses

Table 16-2. MII Register Names & Addresses

Register Name	Register Number	Register Address (Hex)
Mode Control	0	00
Mode Status	1	01
PHY Identifier Register #1	2	02
PHY Identifier Register #2	3	03
Auto-Negotiation Advertisement	4	04
Auto-Negotiation Link Partner Ability	5	05
Auto-Negotiation Expansion	6	06
Auto-Negotiation Next-Page Transmit	7	07
Auto Negotiation Link Partner Next Page	8	08
1000BASE-T Control	9	09
1000BASE-T Status	10	0A
Reserved	11	0B
Reserved	12	0C
Reserved	13	0D
Reserved	14	0E
1000BASE-T Status Extension #1	15	0F
100BASE-TX Status Extension	16	10
1000BASE-T Status Extension #2	17	11
Bypass Control	18	12
Receive Error Counter	19	13
False Carrier Sense Counter	20	14
Disconnect Counter	21	15
10BASE-T Control & Status	22	16
Extended PHY Control #1	23	17
Extended PHY Control #2	24	18
Interrupt Mask	25	19
Interrupt Status	26	1A
Parallel LED Control	27	1B
Auxiliary Control & Status	28	1C
Delay Skew Status	29	1D
Reserved	30	1E
Reserved	31	1F

16.2 Reset-Sticky Bits

Table 16-3. Reset-Sticky Bits

Register	Bit	Name
18	Bypass Control Register	
	6	Bypass Non-compliant BCM5400 Detection
	3	Parallel-Detect Control
	1	Disable Automatic 1000BASE-T Next-Page Exchange
	0	125MHz Clock Output Enable
22	10BASE-T Control & Status Register	
	15	Link Disable
	14	Jabber Detect Disable
	13	Disable 10BASE-T/100BASE-TX Echo Mode
	12	SQE Disable Mode
	11:10	Squelch Control
	5:3	Current Reference Trim
23	Extended PHY Control Register #1	
	15:12	MAC Interface Mode Select
	11:9	MAC Interface and Digital I/O Power Supply Voltage Select
	8	RGMII Skew Timing Compensation Enable
	6	TBI Bit Order Reversal Enable
24	Extended PHY Control Register #2	
	15:13	100/1000BASE-T Edge Rate Control
	12:10	100/1000BASE-T Transmit Voltage Reference Trim
	9:7	TX FIFO Latency Control for GMII, RGMII, TBI, and RTBI
	6:4	RTX FIFO Latency Control (TBI Only)
25	Interrupt Mask Register	
	14	Speed State-Change Interrupt Mask
	13	Link State-Change/ActiPHY™ Interrupt Mask
	12	Duplex State-Change Interrupt Mask
	11	Auto-Negotiation Error Interrupt Mask
	10	Auto-Negotiation Done Interrupt Mask
	9	Page-Received Interrupt Mask
	8	Symbol Error Interrupt Mask
	7	Descrambler Lock-Lost Interrupt Mask
	6	MDI Crossover Interrupt Mask
	5	Polarity-Change Interrupt Mask
	4	Jabber-Detect Interrupt Mask
	3	False Carrier Interrupt Mask
	2	Parallel-Detect Interrupt Mask
	1	MASTER/SLAVE Interrupt Mask
	0	10BASE-T RX_ER Interrupt Mask
28	Auxiliary Control & Status Register	
	2	Mode/Duplex Pin Priority Select
27	Parallel LED Control Register	
	14	LINK10 LED Disable
	12	LINK100 LED Disable
	10	LINK1000 LED Disable
	8	Duplex LED Disable
	6	Activity LED Disable
	4	Quality LED Disable
	3	Pulse LED Enable
	2	Blink/Activity Blink Enable
	1	Blink/Activity Blink Rate

16.3 MII Register Map Quick Reference (Sheet 1 of 2)

Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register 0 (00h) Mode Control Register	Software Reset 0	Loopback 0	Forced Speed Select[0] 0	Auto-Neg Enable 1	Power-Down 0	Isolate 0	Restart Auto-Neg 0	Duplex Mode 0	Collision Test 0	Forced Speed Select[1] 1	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 1 (01h) Mode Status Register	100B-T4 0	100B-X FDX 1	100B-X HDX 1	10B-T FDX 1	10B-T HDX 1	100B-T2 FDX 0	100B-T2 HDX 0	Extended Status 1	Reserved 0	Preamble Suppression 1	Auto-Neg Complete 0	Remote Fault 0	Auto-Neg Capability 1	Link Status 0	Jabber Detect 0	Extended Capability 1
Register 2 (02h) PHY Identifier #1	OUI_MSB[3] 0	OUI_MSB[4] 0	OUI_MSB[5] 0	OUI_MSB[6] 0	OUI_MSB[7] 0	OUI_MSB[8] 0	OUI_MSB[9] 0	OUI_MSB[10] 0	OUI_MSB[11] 0	OUI_MSB[12] 0	OUI_MSB[13] 0	OUI_MSB[14] 0	OUI_MSB[15] 1	OUI_MSB[16] 1	OUI_MSB[17] 1	OUI_MSB[18] 1
Register 3 (03h) PHY Identifier #2	OUI_LSB[19] 1	OUI_LSB[20] 1	OUI_LSB[21] 0	OUI_LSB[22] 0	OUI_LSB[23] 0	OUI_LSB[24] 1	Vendor Model Number[5] 0	Vendor Model Number[4] 0	Vendor Model Number[3] 0	Vendor Model Number[2] 0	Vendor Model Number[1] 0	Vendor Model Number[0] 1	Vendor Rev Number[3] 0	Vendor Rev Number[2] 0	Vendor Rev Number[1] 0	Vendor Rev Number[0] 1
Register 4 (04h) Auto-Neg Advertisement Register	Next Page 0	Reserved 0	Remote Fault 0	Reserved 0	Asymmetric Pause 0	Symmetric Pause 0	100B-T4 0	100B-X FDX 1	100B-X HDX 1	10B-T FDX 1	10B-T HDX 1	Selector Field[4] 0	Selector Field[3] 0	Selector Field[2] 0	Selector Field[1] 0	Selector Field[0] 1
Register 5 (05h) Auto-Neg Link Partner Ability Register	Next Page 0	ACK 0	Remote Fault 0	Reserved 0	Asymmetric Pause 0	Symmetric Pause 0	100B-T4 0	100B-X FDX 0	100B-X HDX 0	10B-T FDX 0	10B-T HDX 0	Selector Field[4] 0	Selector Field[3] 0	Selector Field[2] 0	Selector Field[1] 0	Selector Field[0] 0
Register 6 (06h) Auto-Neg Expansion Register	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Parallel Detect Fault 0	LP NP Able 0	NP Able 1	Page Received 0	LP Auto-Neg Able 0
Register 7 (07h) Auto-Neg NP Transmit Register	Next Page 0	Reserved 0	Message Page 1	ACK2 0	Toggle 0	Message/ Unformatted[10] 0	Message/ Unformatted[9] 0	Message/ Unformatted[8] 0	Message/ Unformatted[7] 0	Message/ Unformatted[6] 0	Message/ Unformatted[5] 0	Message/ Unformatted[4] 0	Message/ Unformatted[3] 0	Message/ Unformatted[2] 0	Messag/ Unformatted[1] 0	Message/ Unformatted[0] 1
Register 8 (08h) Auto-Neg Link Partner NP Receive Register	LP Next Page 0	LP ACK 0	LP Message Page 0	LP ACK2 0	LP Toggle 0	LP Message/ Unformatted[10] 0	LP Message/ Unformatted[9] 0	LP Message/ Unformatted[8] 0	LP Message/ Unformatted[7] 0	LP Message/ Unformatted[6] 0	LP Message/ Unformatted[5] 0	LP Message/ Unformatted[4] 0	LP Message/ Unformatted[3] 0	LP Message/ Unformatted[2] 0	LP Message/ Unformatted[1] 0	LP Message/ Unformatted[0] 0
Register 9 (09h) 1000BASE-T Control Register	Transmit Test[1] 0	Transmit Test[2] 0	Transmit Test[3] 0	M/S Config Enable 0	M/S Config Value 0	Port Type 0	1000B-T FDX 1	1000B-T HDX 1	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 10 (0Ah) 1000BASE-T Status Register	M/S Config Fault 0	M/S Config Resolution 1	Local Receiver Status 0	Remote Receiver Status 0	LP 1000B-T FDX 0	LP 1000B-T HDX 0	Reserved 0	Reserved 0	Idle Error Count[7] 0	Idle Error Count[6] 0	Idle Error Count[5] 0	Idle Error Count[4] 0	Idle Error Count[3] 0	Idle Error Count[2] 0	Idle Error Count[1] 0	Idle Error Count[0] 0
Register 11 (0Bh) Reserved Register	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 12 (0Ch) Reserved Register	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 13 (0Dh) Reserved Register	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 14 (0Eh) Reserved Register	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 15 (0Fh) 1000BASE-T Status Extension Register	1000B-X FDX 0	1000B-X HDX 0	1000B-T FDX 1	1000B-T HDX 1	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0

Key: Bit Name (Read/Writable) Reset Value — Bit Name (Read Only) Reset Value

16.4 MII Register Map Quick Reference (Sheet 2 of 2)

Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register 16 (10h) 100BASE-TX Status Extension Register	100B-TX Descrambler Locked 0	100B-TX Lock Error Detected 0	100B-TX Disconnect State 0	100B-TX Current Link Status 0	100B-TX Receive Error Detected 0	100B-TX Transmit Error Detected 0	100B-TX SSD Error Detected 0	100B-TX ESD Error Detected 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 17 (11h) 1000BASE-T Status Extension Register #2	1000B-T Descrambler Locked 0	1000B-T Lock Error Detected 0	1000B-T Disconnect State 0	1000B-T Current Link Status	1000B-T Receive Error Detected 0	1000B-T Transmit Error Detected 0	1000B-T SSD Error Detected 0	1000B-T ESD Error Detected 0	1000B-T Carrier Extension Error Detected 0	Non-compliant BCM5400 Detected 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 18 (12h) Bypass Control Register	Transmit Disable 0	Bypass 4B5B Encoder/ Decoder 0	Bypass Scrambler 0	Bypass Descrambler 0	Bypass PCS Receive 0	Bypass PCS Transmit 0	Bypass LFI Timer 0	Transmitter Test Clock Enable 0	Non-compliant BCM5400 Detect 0	Bypass Non-compliant BCM5400 0	Disable Automatic Pair Swap Correction 0	Disable Polarity Correction 0	Parallel-Detect Control 0	Disable Pulse Shaping Filter 0	Disable Auto 1000B-T NP Exchange 0	125MHz Clock Output Enable 1
Register 19 (13h) Receive Error Counter Register	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Receive Error Counter[7] 0	Receive Error Counter[6] 0	Receive Error Counter[5] 0	Receive Error Counter[4] 0	Receive Error Counter[3] 0	Receive Error Counter[2] 0	Receive Error Counter[1] 0	Receive Error Counter[0] 0
Register 20 (14h) False Carrier Sense Counter Register	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	False Carrier Counter[7] 0	False Carrier Counter[6] 0	False Carrier Counter[5] 0	False Carrier Counter[4] 0	False Carrier Counter[3] 0	False Carrier Counter[2] 0	False Carrier Counter[1] 0	False Carrier Counter[0] 0
Register 21 (15h) Disconnect Counter Register	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Disconnect Counter[7] 0	Disconnect Counter[6] 0	Disconnect Counter[5] 0	Disconnect Counter[4] 0	Disconnect Counter[3] 0	Disconnect Counter[2] 0	Disconnect Counter[1] 0	Disconnect Counter[0] 0
Register 22 (16h) 10BASE-T Control & Status Register	Link Integrity Test Disable 0	Jabber Detect Disable 0	Echo Disable 0	SQE Disable 0	Squelch[1] 0	Squelch[0] 0	Reserved 0	EOF Error Detected 0	10B-T Disconnect 0	10B-T Link Status 0	Current Ref Trim[2] 0	Current Ref Trim[1] 0	Current Ref Trim[0] 0	Reserved 0	Reserved 0	Reserved 0
Register 23 (17h) Extended PHY Control Register #1	MAC I/F Mode[3] 0	MAC I/F Mode[2] 0	MAC I/F Mode[1] 0	MAC I/F Mode[0] 0	MAC I/F Voltage[2] 0	MAC I/F Voltage[1] 0	MAC I/F Voltage[0] 0	RGMII Skew Compensation 0	EWRAP 0	TBI Bit Order Reversal 0	ActiPHY™ 0	Reserved 0	Reserved 0	Reserved 0	GMII Transmit Pin Reversal 0	Reserved 0
Register 24 (18h) Extended PHY Control Register #2	100/1000B-TX Edge Rate[2] 0	100/1000B-TX Edge Rate[1] 0	100/1000B-TX Edge Rate[0] 0	100/1000B-T TX VRef Trim[2] 0	100/1000B-T TX VRef Trim[1] 0	100/1000B-T TX VRef Trim[0] 0	TX FIFO Depth[2] (all modes) 1	TX FIFO Depth[1] (all modes) 0	TX FIFO Depth[0] (all modes) 0	RX FIFO Depth[2] (TBI) 1	RX FIFO Depth[1] (TBI) 0	RX FIFO Depth[0] (TBI) 0	Cable Quality Status 0	Cable Quality Status 0	Cable Quality Status 0	1000B-T Analog Loopback 0
Register 25 (19h) Interrupt Mask Register	Interrupt Pin Enable 0	Speed State-Change Interrupt Mask 0	Link State-Chg/ ActiPHY™ Interrupt Mask 0	Duplex State-Change Interrupt Mask 0	Auto-Neg Error Interrupt Mask 0	Auto-Neg-Done Interrupt Mask 0	Page-Received Interrupt Mask 0	Symbol Error Interrupt Mask 0	Descrambler Lock-Lost Interrupt Mask 0	MDI Crossover Interrupt Mask 0	Polarity-Change Interrupt Mask 0	Jabber-Detect Interrupt Mask 0	False Carrier Interrupt Mask 0	Parallel-Detect Interrupt Mask 0	MASTER/ SLAVE Interrupt Mask 0	10B-T RX_ER Interrupt Mask 0
Register 26 (1Ah) Interrupt Status Register	Interrupt Status 0	Speed State-Change Interrupt Status 0	Link State-Chg/ ActiPHY™ Interrupt Status 0	Duplex State-Change Interrupt Status 0	Auto-Neg Error Interrupt Status 0	Auto-Neg-Done Interrupt Status 0	Page-Received Intterupt Status 0	Symbol Error Interrupt Status 0	Descrambler Lock-Lost Interrupt Status 0	MDI Crossover Interrupt Status 0	Polarity-Change Interrupt Status 0	Jabber-Detect Interrupt Status 0	False Carrier Interrupt Status 0	Parallel-Detect Interrupt Mask 0	MASTER/ SLAVE Interrupt Status 0	RX_ER Interrupt Status 0
Register 27 (1Bh) Parallel LED Control Register	Link10 LED Force On 0	Link10 LED Disable 0	Link100 LED Force On 0	Link100 LED Disable 0	Link1000 LED Force On 0	Link1000 LED Disable 0	Duplex LED Force On 0	Duplex LED Disable 0	Activity LED Force On 0	Activity LED Disable 0	Quality LED Force On 0	Quality LED Disable 0	LED Pulse Enable 0	Link/Activity LED Blink Enable 0	Link/Activity Blink Rate 0	Reserved 0
Register 28 (1Ch) Auxiliary Control & Status Register	Auto-Neg Complete 0	Auto-Neg Disabled 0	MDI/MDI-X XOver Indication 0	CD Pair Swap 0	A Polarity Inversion 0	B Polarity Inversion 0	C Polarity Inversion 0	D Polarity Inversion 0	Reserved 0	Reserved 0	Duplex Status 0	Speed Status[1] 0	Speed Status[0] 0	Mode/Duplex Pin Priority 0	Reset Control 0	Reserved 0
Register 29 (1Dh) Delay Skew Status Register	Reserved 0	Pair A Delay Skew[2] 0	Pair A Delay Skew[1] 0	Pair A Delay Skew[0] 0	Reserved 0	Pair B Delay Skew[2] 0	Pair B Delay Skew[1] 0	Pair B Delay Skew[0] 0	Reserved 0	Pair C Delay Skew[2] 0	Pair C Delay Skew[1] 0	Pair C Delay Skew[0] 0	Reserved 0	Pair D Delay Skew[2] 0	Pair D Delay Skew[1] 0	Pair D Delay Skew[0] 0
Register 30 (1Eh) Reserved Register	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 31 (1Fh) Reserved Register	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0

Key: Bit Name (Read/Writable) Reset Value — Bit Name (Read Only) Reset Value

17 MII Register Descriptions

17.1 Register 0 (00h) – Mode Control Register

Register 0 (00h) – Mode Control Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	Software Reset	R/W SC	1 = Reset asserted 0 = Reset de-asserted	0
14	Loopback	R/W	1 = Loopback on 0 = Loopback off	0
6, 13	Forced Speed Selection	R/W	00 = 10Mbps 01 = 100Mbps 10 = 1000Mbps 11 = Reserved	10
12	Auto-Negotiation Enable	R/W	1 = Auto-Negotiation on 0 = Auto-Negotiation off	1
11	Power-Down	R/W	1 = Power-down 0 = Power-up	0
10	Isolate[1]	R/W	1 = Isolate PHY 0 = Connect PHY to MII	0
9	Restart Auto-Negotiation	R/W SC	1 = Restart MII 0 = Normal operation	0
8	Duplex Mode	R/W	1 = Full duplex 0 = Half duplex	0
7	Collision Test Enable	R/W	1 = Collision test enabled 0 = Collision test disabled	0
6	MSB for Speed Selection (see bit 13 above)	-	-	1
5:0	Reserved	-	-	000000

[1] Setting this bit does not isolate the GMII/MII inputs (i.e. when isolate bit is set the GMII/MII data on TX pins will be transmitted on the MDI interface if the link is up). This behavior does not comply with the IEEE 802.3 standard. To isolate the GMII/MII inputs, both MII Register bits 0.11 and 0.10 must be set. It should be noted that setting bits 0.11 and 0.10 will cause the link to drop.

0.15 – Software Reset

Software Reset (i.e., setting Software Reset to “1”) is self-clearing (i.e., automatically set to “0”). The only difference between a hardware and software reset is that a hardware reset also powers down all internal analog reference voltages and currents, including the PLL.

Once Software Reset is asserted, the PHY is returned to normal operating mode and is ready for the next SMI transaction, so Software Reset always reads back “0”. Software Reset restores all SMI registers to their default states unless the reset-sticky control bit 28.1 is set. When control bit 28.1 is set to “1”, the reset-sticky bits retain their values after a software reset, as specified in table 21-3. See section 22.24 for more details.

0.14 – Loopback

When Loopback is asserted, the Transmit Data (TXD) on the MAC interface is looped back as Receive Data (RXD). In loopback mode, no signal is transmitted over the network media. The loopback mechanism works in all (10/100/1000) modes of operation. The operating mode is determined by resister bits 0.13, 0.6 (Forced Speed Selection)

0.13, 0.6 – Forced Speed Selection

These bits determine the 10/100/1000 speed when Auto-Negotiation is disabled by clearing control bit 0.12. These bits are ignored if control bit 0.12 is set. Note that Auto-Negotiation is always required in 1000BASE-T mode in normal operating modes

unless the MODE, FRC_DPLX, and ANEG_DIS pins are used (see MII Register 28 for more information). These bits also set the operating mode when loopback (0.14) is set to “1”.

0.12 – Auto-Negotiation Enable

After a power-up, or reset, the PHY automatically activates the Auto-Negotiation state machine, setting bit 0.12 to a “1”. If bit 0.12 is written to a “0”, the Auto-Negotiation process is disabled, and the present contents of the PHY’s SMI register bits determine the operating characteristics. However, the values of the MODE10/100/1000, FRC_DPLX, and ANEG_DIS pins take precedence in setting the advertised operating capabilities determined by the PHY’s SMI register bits, unless MII Register bit 28.2 (Mode/Duplex Pin Priority Select bit) is set to “1”. Note that Auto-Negotiation is always required in 1000BASE-T mode.

0.11 – Power-Down

Power-Down functions the same as Software Reset, except that it is not self-clearing, and that R/W SMI bits are *not* restored to their default states by Power-Down. After Power-Down is deactivated (i.e., set to “1”), the PHY will be ready for normal operation before the next SMI transaction. If Auto-Negotiation is enabled, the PHY will begin Auto-Negotiation immediately upon exiting Power-Down.

0.10 – Isolate[1]

When Isolate is asserted (i.e., set to “1”), all MII and GMII outputs (except for MDIO) will be high impedance. Operation of the PHY is otherwise unaffected. For example, if Isolate is asserted while Auto-Negotiation is under way, Auto-Negotiation will continue unaffected.

0.9 – Restart Auto-Negotiation

When Restart Auto-Negotiation is asserted (i.e., set to “1”), the Auto-Negotiation state machine will restart the Auto-Negotiation process, even if it is in the middle of an Auto-Negotiation process. This control bit is self-clearing, meaning that it will always return a “0” when read.

0.8 – Duplex Mode

The CIS8201 operates in half-duplex by default when auto-negotiation is disabled. The CIS8201 can be reconfigured to operate in full-duplex by setting the Duplex Mode bit to a “1” while Auto-Negotiation is disabled by clearing bit 0.12. Changes to the state of Duplex Mode while Auto-Negotiation is enabled are ignored.

0.7 – Collision Test Enable

The collision test mode allows the COL pins to be tested during loopback mode. While the collision test mode is enabled (by setting Collision Test Enable to a “1”), asserting TX_EN will cause the COL output to go high within 512 bit times. De-asserting TX_EN will cause the COL output to go low within 4 bit times. The collision test mode should be enabled only when loopback is enabled.

05:0 – Reserved

[1]Setting this bit does not isolate the GMII/MII inputs (i.e. when isolate bit is set the GMII/MII data on TX pins will be transmitted on the MDI interface if the link is up). This behavior does not comply with the IEEE 802.3 standard. To isolate the GMII/MII inputs, both MII Register bits 0.11 and 0.10 must be set. It should be noted that this will cause the link to chop.

17.2 Register 1 (01h) – Mode Status Register

Register 1 (01h) – Mode Status Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	100BASE-T4 Capability	RO	1 = 100BASE-T4 capable	0
14	100BASE-X FDX Capability	RO	1 = 100BASE-X FDX capable	1
13	100BASE-X HDX Capability	RO	1 = 100BASE-X HDX capable	1
12	10BASE-T FDX Capability	RO	1 = 10BASE-T FDX capable	1
11	10BASE-T HDX Capability	RO	1 = 10BASE-T HDX capable	1
10	100BASE-T2 FDX Capability	RO	1 = 100BASE-T2 FDX capable	0
9	100BASE-T2 HDX Capability	RO	1 = 100BASE-T2 HDX capable	0
8	Extended Status Enable	RO	1 = Extended status information present in R15	1
7	Reserved	RO		0
6	Preamble Suppression Capability	RO	1 = MF preamble may be suppressed 0 = MF preamble always required	1
5	Auto-Negotiation Complete	RO	1 = Auto-Negotiation complete 0 = Auto-Negotiation not complete	0
4	Remote Fault	RO LH	1 = Far-end fault detected 0 = No fault detected	0
3	Auto-Negotiation Capability	RO	1 = Auto-Negotiation capable	1
2	Link Status	RO LL	1 = Link is up (Link pass) 0 = Link is down (Link fail)	0
1	Jabber Detect	RO LH	1 = Jabber condition detected 0 = No jabber condition detected	0
0	Extended Capability	RO	1 = Extended register capable	1

1.15 – 100BASE-T4 Capability

The CIS8201 is not 100BASE-T4 capable, so this bit is hard-wired to “0”.

1.14 – 100BASE-X FDX Capability

The CIS8201 is 100BASE-X FDX capable, so this bit is hard-wired to “1”.

1.13 – 100BASE-X HDX Capability

The CIS8201 is 100BASE-X HDX capable, so this bit is hard-wired to “1”.

1.12 – 10BASE-T FDX Capability

The CIS8201 is 10BASE-T FDX capable, so this bit is hard-wired to “1”.

1.11 – 10BASE-T HDX Capability

The CIS8201 is 10BASE-T HDX capable, so this bit is hard-wired to “1”.

1.10 – 100BASE-T2 FDX Capability

The CIS8201 is not 100BASE-T2 FDX capable, so this bit is hard-wired to “0”.

1.9 – 100BASE-T2 HDX Capability

The CIS8201 is not 100BASE-T2 HDX capable, so this bit is hard-wired to “0”.

1.8 – Extended Status Enable

The CIS8201 is extended status capable, so this bit is hard-wired to “1”.

1.7 – Reserved

1.6 – Preamble Suppression Capability

The CIS8201 accepts management frames on the SMI without preambles, so preamble suppression capability is hard-wired to “1”. The management frame preamble may be as short as 1 bit.

1.5 – Auto-Negotiation Complete

When this bit is a “1”, the contents of Registers 4, 5, 6, and 15 are valid.

1.4 – Remote Fault

Bit 1.4 will be set to “1” if the Link Partner signals a far-end fault. The bit is cleared automatically upon a read if the far-end fault condition has been removed.

1.3 – Auto-Negotiation Capability

The CIS8201 is Auto-Negotiation capable, so this bit is hard-wired to “1”. Note that this bit will read a “1” even if Auto-Negotiation is disabled via bit 0.12.

1.2 – Link Status

This bit will return a “1” when the CIS8201 link state machine has reached the “link pass” state, meaning that a valid link has been established. If the link is subsequently lost, the Link Status will revert to a “0” state. It will remain a “0” until Link Status is read while the link state machine is in the “link pass” state. In this case, Link Status will return a “0”, but it will return a “1” on subsequent reads as long as the “link pass” state is maintained.

1.1 – Jabber Detect

Note that Jabber Detect is required for 10BASE-T mode only. Jabber Detect will be set to “1” when the jabber condition is detected. Jabber Detect will be cleared automatically when this register is read.

1.0 – Extended Capability

The CIS8201 has extended register capability, so this bit is hard-wired to “1”.

17.3 Register 2 (02h) – PHY Identifier Register #1

	Register 2 (02h) – Mode Control Register			
15:0	Organizationally Unique Identifier	RO	OUI most significant bits (Cicada OUI bits 3:18)	0000000000001111 or (000Fh)

2.15:0 – PHY Identifier Register #1

Cicada has been assigned an OUI from the IEEE of 0003F1h. Per IEEE requirements, only OUI bits 3 to 18 are used in this register.

17.4 Register 3 (03h) – PHY Identifier Register #2

	Register 3 (03h) – PHY Identifier Register #2			
Bit	**Name**	**Access**	**States**	**Reset Value**
15:10	Organizationally Unique Identifier	RO	OUI least significant bits (Cicada OUI bits 19:24)	110001
9:4	Vendor Model Number	RO	Vendor's model number (IC)	000001 = CIS8201
3:0	Vendor Revision Number	RO	Vendor's revision number (IC)	0001 = Silicon Revision A0 0010 = Silicon Revision A1 0011 = Silicon Revision A2

3.15:0 – PHY Identifier Register #2

Cicada has been assigned an OUI from the IEEE of 0003F1h. Per IEEE requirements, only OUI bits 19 to 24 are used in this register.

17.5 Register 4 (04h) – Auto-Negotiation Advertisement Register

Register 4 (04h) – Auto-Negotiation Advertisement Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	Next-Page Transmission Request	R/W	1 = Next-Page transmission request	0
14	Reserved	RO		0
13	Transmit Remote Fault	R/W	1 = Transmit remote fault	0
12	Reserved technologies	R/W		0
11	Advertise Asymmetric Pause	R/W	1 = Advertise Asymmetric Pause capable	0
10	Advertise Symmetric Pause	R/W	1 = Advertise Symmetric Pause capable	0
9	Advertise 100BASE-T4 Capability	R/W	1 = 100BASE-T4 capable	0
8	Advertise 100BASE-X FDX	R/W	1 = 100BASE-X FDX capable	1
7	Advertise 100BASE-X HDX	R/W	1 = 100BASE-X HDX capable	1
6	Advertise 10BASE-T FDX	R/W	1 = 10BASE-T FDX capable	1
5	Advertise 10BASE-T HDX	R/W	1 = 10BASE-T HDX capable	1
4:0	Advertise Selector Field	R/W		00001

This register controls the advertised abilities of the local (not remote) PHY. The state of this register is latched when the Auto-Negotiation state machine enters the ABILITY_DETECT state. Thus, any writes to this register prior to completion of Auto-Negotiation as indicated by bit 1.5 should be followed by a re-negotiation for the new values to be properly used for Auto-Negotiation. Once Auto-Negotiation has completed, this register value may be read via the SMI to determine the highest common denominator technology.

4.15 – Auto-Negotiation Additional Next-Page Transmission Request

In 1000BASE-T, there are required Next-Pages transmitted per the standard. A user may optionally transmit additional Next-Pages. The CIS8201 supports additional Next-Page transmission. Bit 4.15 is set by the user to request additional Next-Page transmission. See description of register bit 18.1 for more details on Next-Page exchanges.

4.14, 4.12 – Reserved

4.13 – Transmit Remote Fault

The state of this bit is transmitted to the Link Partner during Auto-Negotiation. This bit does not have any effect on the local PHY operation. This bit is automatically cleared following a successful negotiation with the Link Partner.

4.11:10 – Advance Pause Capability

These bits are used by the local MAC to communicate pause capability to the Link Partner; this has no effect on PHY operation.

4.9:5 – Advertise Capability

Bits 4.9:5 allow the user to customize the ability information transmitted to the Link Partner. The default value for each bit reflects the abilities of the local PHY. By writing a “1” to any of the bits, the corresponding ability will be advertised to the Link Partner. Writing a “0” to any bit causes the corresponding ability to be suppressed from transmission. The state of these bits has no other effect on the operation of the local PHY. Resetting the chip restores the default bit values. Note that the default values of these bits indicate the true ability of the CIS8201.

4.4:0 – Advertise Selector Field

Since the CIS8201 is a member of the 802.3 class of PHYs, the Advertise Selector Field defaults to “00001”. These bits are R/W only because the Ethernet standard requires them to be R/W. However, these bits should not be changed because an 802.3 PHY uses them to verify that the Link Partner is also an 802.3 PHY before completing Auto-Negotiation.

17.6 Register 5 (05h) – Auto-Negotiation Link Partner Ability Register

Register 5 (05h) – Auto-Negotiation Link Partner Ability Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	LP Next-Page Transmit Request	RO	1 = LP NP transmit request	0
14	LP Acknowledge	RO	1 = LP acknowledge	0
13	LP Remote Fault	RO	1 = LP remote fault	0
12	Reserved technologies	RO		0
11	LP Asymmetric Pause Capability	RO	1 = Advertise Asymmetric Pause capable	0
10	LP Symmetric Pause Capability	RO	1 = Advertise Symmetric Pause capable	0
9	LP Advertise 100BASE-T4 Capability	RO	1 = LP Advertise 100BASE-T4 capable	0
8	LP Advertise 100BASE-X FDX	RO	1 = LP 100BASE-X FDX capable	0
7	LP Advertise 100BASE-X HDX	RO	1 = LP 100BASE-X HDX capable	0
6	LP Advertise 10BASE-T FDX	RO	1 = LP 10BASE-T FDX capable	0
5	LP Advertise 10BASE-T HDX	RO	1 = LP 10BASE-T HDX capable	0
4:0	LP Advertise Selector Field	RO	LP Advertise Selector Field	00000

5.15 – LP Next-Page Transmit Request

Bit 5.15 returns a “1” when the Link Partner implements the Next-Page function and has Next-Page information it wants to transmit. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) or the Page Received bit (6.1) is set.

5.14 – LP Acknowledge

Bit 5.14 returns a “1” when the Link Partner signals that it has received the Link Code Word from the local PHY. The local PHY uses this bit for proper Link Code Word exchange, as defined in Clause 28 of IEEE 802.3.

5.13 – LP Remote Fault

Bit 5.13 returns a “1” when the Link Partner signals that a remote fault (from its perspective) has occurred. The local PHY does not otherwise use this bit.

5.12 – Reserved

5.11 – LP Asymmetric Pause Capability

The LP Asymmetric Pause Capability bit indicates whether the Link Partner has asymmetric pause capability. This bit is used by the Link Partner’s MAC to communicate symmetric pause capability to the local MAC; it has no effect on PHY operation.

5.10 – LP Symmetric Pause Capability

The LP Symmetric Pause Capability bit indicates whether the Link Partner supports symmetric pause frame capability. This bit is used by the Link Partner’s MAC to communicate symmetric pause capability to the local MAC; it has no effect on PHY operation.

5.9:5 – Advertise Capability

Bits 9:5 reflect the abilities of the Link Partner. A “1” on any of these bits indicates that the Link Partner advertises capability of performing the corresponding mode of operation.

5.4:0 – LP Selector Field Status

Bits 5.4:0 indicate the state of the Link Partner’s Selector Field. The local PHY does not otherwise use these bits.

17.7 Register 6 (06h) – Auto-Negotiation Expansion Register

Register 6 (06h) – Auto-Negotiation Expansion Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15:5	Reserved	RO		00000000000
4	Parallel Detection Fault	RO LH	1 = Parallel detection fault	0
3	LP Next-Page Able	RO	1 = LP Next-Page capable	0
2	Local PHY Next-Page Able	RO	1 = Next-Page capable	1
1	Page Received	RO LH	1 = New page has been received	0
0	LP Auto-Negotiation Able	RO	1 = LP Auto-Negotiation capable	0

6.15:5 – Reserved

6.4 – Parallel Detection Fault

Parallel Detection Fault returns a “1” when a parallel detection fault occurs in the local Auto-Negotiation state machine. Once set, this bit is automatically cleared when (and only when) Register 6 is read.

6.3 – LP Next-Page Able

LP Next-Page Able returns a “1” when the Link Partner has Next-Page capabilities. This bit is used in the Auto-Negotiation state machines, as defined in Clause 28 of IEEE 802.3. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) or the Page Received bit (6.1) is set.

6.2 – Local PHY Next-Page Able

Since the CIS8201 is Next-Page able, this bit is hard-wired to “1”.

6.1 – Page Received

Page Received is set to “1” when a new Link Code Word is received from the Link Partner, validated, and acknowledged. Page Received is automatically cleared when (and only when) Register 6 is read via the SMI.

6.0 – LP Auto-Negotiation Able

LP Auto-Negotiation Capable is set to “1” if the Link Partner advertises Auto-Negotiation capability. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) or the Page Received bit (6.1) is set.

17.8 Register 7 (07h) – Auto-Negotiation Next-Page Transmit Register

Register 7 (07h) – Auto-Negotiation Next-Page Transmit Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	Next Page	R/W	1 = More pages follow 0 = Last page	0
14	Reserved	RO		0
13	Message Page	R/W	1 = Message page 0 = Unformatted page	1
12	Acknowledge2	R/W	1 = Will comply with request 0 = Cannot comply with request	0
11	Toggle	RO	1 = Previous transmitted LCW == 0 0 = Previous transmitted LCW == 1	0
10:0	Message/Unformatted Code	R/W		00000000001

7.15 – Next Page

The Next Page bit indicates whether this is the last Next-Page to be transmitted. By default, this bit is set to “0”, indicating that this is the last page.

7.14 – Reserved

7.13 – Message Page

The Message Page bit indicates whether this page is a message page or an unformatted page. This bit does not otherwise affect the operation of the local PHY. By default, this bit is set to “1”, indicating that this is a message page.

7.12 – Acknowledge2

The Acknowledge2 bit indicates if the local MAC reports that it is able to act on the information (or perform the task) indicated in the previous message. The local PHY does not interpret or act on changes in the state of this bit.

7.11 – Toggle

The Toggle bit is used by the arbitration function in the local PHY to ensure synchronization with the Link Partner during Next-Page exchanges. The Toggle bit is automatically set to the opposite state of the Toggle bit in the previously exchanged Link Code Word.

7.10:0 – Message/Unformatted Code

The Message/Unformatted Code bits indicate the message code being transmitted to the Link Partner. The local PHY passes the message code to the Link Partner without interpreting or reacting to it. By default, this code is set to “000 0000 0001”, indicating a null message.

17.9 Register 8 (08h) – Auto-Negotiation Link Partner Next-Page Receive Register

Register 8 (08h) – Auto-Negotiation Link Partner Next-Page Receive Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	LP Next Page	RO	1 = More pages follow 0 = Last page	0
14	LP Acknowledge	RO	1 = LP acknowledge	0
13	LP Message Page	RO	1 = Message page 0 = Unformatted page	0
12	LP Acknowledge2	RO	1 = LP will comply with request	0
11	LP Toggle	RO	1 = Previous transmitted LCW == 0 0 = Previous transmitted LCW == 1	0
10:0	LP Message/Unformatted Code	RO		00000000000

SMI Register 8 contains the Link Partner's Next-Page register contents. The contents of this register are valid only when the Page Received bit (6.1) is set.

8.15 – LP Next Page

This bit indicates if more pages follow from the Link Partner.

8.14 – LP Acknowledge

This bit returns a "1" when the Link Partner signals that it has received the Link Code Word from the local PHY. The local PHY uses this bit for proper Link Code Word exchange, as defined in Clause 28 of IEEE 802.3.

8.13 – LP Message Page

The Message Page bit indicates if the page received from the Link Partner is a message page or an unformatted page.

8.12 – LP Acknowledge2

The Acknowledge2 bit indicates whether the Link Partner reports that it is able to act on the information (or perform the task) indicated in the message. The local PHY does not interpret or act on changes in the state of this bit.

8.11 – LP Toggle

The Toggle bit is used by the arbitration function in the local PHY to ensure synchronization with the Link Partner during Next-Page exchanges. In the Link Partner, the Toggle bit is automatically set to the opposite state of the Toggle bit in the previously exchanged Link Code Word from the Link Partner.

8.10:0 – LP Message/Unformatted Code

The Message/Unformatted Code bits indicate the message code being transmitted to the Link Partner.

17.10 Register 9 (09h) – 1000BASE-T Control Register[1]

Register 9 (09h) – 1000BASE-T Control Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15:13	Transmitter Test Mode	R/W	Described below, per IEEE 802.3, 40.6.1.1.2	000
12	MASTER/SLAVE Manual Configuration Enable	R/W	1 = Enable MASTER/SLAVE Manual Configuration value 0 = Disable MASTER/SLAVE Manual Configuration value	0
11	MASTER/SLAVE Manual Configuration Value	R/W	1 = Configure PHY as MASTER during MASTER/ SLAVE negotiation, only when bit 9.12 is set to logical one. 0 = Configure PHY as SLAVE during MASTER/SLAVE negotiation, only when bit 9.12 is set to logical one.	0
10	Port Type	R/W	1 = Multi-port device 0 = Single-port device	0
9	1000BASE-T FDX Capability	R/W	1 = PHY is 1000BASE-T FDX capable	1
8	1000BASE-T HDX Capability	R/W	1 = PHY is 1000BASE-T HDX capable	1
7:0	Reserved	R/W		00000000

9.15:13 Transmitter/Receiver Test Mode[1]

This test is valid only in 1000BASE-T mode. Refer to IEEE 802.3-2000, section 40.6.1.1.2 for more information.

Table 17-1. 1000BASE-T Transmitter/Receiver Test Modes

Bit 1 (9.15)	Bit 2 (9.14)	Bit 3 (9.13)	Test Mode
0	0	0	Normal operation
0	0	1	Test Mode 1 – Transmit waveform test
0	1	0	Test Mode 2 – Transmit jitter test in MASTER mode
0	1	1	Test Mode 3 – Transmit jitter test in SLAVE mode
1	0	0	Test Mode 4 – Transmitter distortion test
1	0	1	Reserved; operation not defined
1	1	0	Reserved; operation not defined
1	1	1	Reserved; operation not defined

- **Test Mode 1:** The PHY repeatedly transmits the following sequence of data symbols from all four transmitters: {{"+2" followed by 127 "0" symbols}, {"-2" followed by 127 "0" symbols}, {"+1" followed by 127 "0" symbols}, {"-1" followed by 127 "0" symbols}, {128 "+2" symbols, 128 "-2" symbols, 128 "+2" symbols, 128 "-2" symbols}, {1024 "0" symbols}}. The transmitter should use a 125.00 MHz ± 0.01% clock and should operate in MASTER timing mode.
- **Test Mode 2:** The PHY transmits the data symbol sequence {+2, -2} repeatedly on all channels. The transmitter should use a 125.00 MHz ± 0.01% clock in the MASTER timing mode.
- **Test Mode 3:** The PHY transmits the data symbol sequence {+2, -2} repeatedly on all channels. The transmitter should use a 125.00 MHz ± 0.01% clock and should operate in SLAVE timing mode.
- **Test Mode 4:** The PHY transmits the sequence of symbols generated by the following scrambler generator polynomial, bit generation, and level mappings:

[1]The state of this register is internally latched when the Auto-Negotiation state machine enters the ABILITY_DETECT state. Changes to the states of these bits are recognized only at that time. This register is valid only in 1000BASE-T mode.

The maximum-length shift register used to generate the sequences defined by this polynomial is updated once per symbol interval (8ns). The bits stored in the shift register delay line at a particular time *n* are denoted by Scrn[10:0]. At each symbol period, the shift register is advanced by one bit, and one new bit represented by Scrn[0] is generated. Bits $Scr_n[8]$ and $Scr_n[10]$ are exclusive-OR'd together to generate the next $Scr_n[0]$ bit. The bit sequences, $x0_n$, $x1_n$, and $x2_n$, generated from combinations of the scrambler bits as shown in the following equations, shall be used to generate the quinary symbols, s_n, as shown in Table 17-2. The transmitter should use a 125.00 MHz ± 0.01% clock and should operate in MASTER timing mode.

Table 17-2. 1000BASE-T Transmitter/Receiver Test Mode 4 – Quinary Symbols

$x2_n$	$x1_n$	$x0_n$	Quinary Symbol, s_n
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	-1
1	0	0	0
1	0	1	1
1	1	0	-2
1	1	1	-1

9.12 – MASTER/SLAVE Manual Configuration Enable[1]

When this bit is set to “0” (default), the MASTER/SLAVE designation of the local PHY is determined using the arbitration protocol established in the IEEE Ethernet standard. When this bit is set to “1”, the MASTER/SLAVE designation of the local PHY is set by bit 9.11. Note that MASTER/SLAVE timing is valid only in 1000BASE-T mode.

9.11 – MASTER/SLAVE Configuration Value[1]

This bit is ignored when bit 9.12 is set to “0”. However, if bit 9.12 is set to “1”, bit 9.11 determines the MASTER/SLAVE designation of the local PHY. If bit 9.12 is set to “1” and bit 9.11 set to “0” (default), the local PHY is forced to be a SLAVE. If bit 9.12 is set to “1” and bit 9.11 set to “1”, the local PHY is forced to be a MASTER. Note that MASTER/SLAVE timing is valid only in 1000BASE-T mode.

9.10 – Port Type[1]

Since the CIS8201 is a single port physical layer transceiver, bit 9.10 is set to “0” by default. When set to “1”, this bit indicates a preference for operation as a MASTER. If the Link Partner does not indicate the same preference, the local PHY will operate as a MASTER, and the Link Partner will be a SLAVE. Otherwise, the normal MASTER/SLAVE assignment protocol is used.

9.9 – 1000BASE-T FDX[1]

Since the CIS8201 is 1000BASE-T FDX capable, this bit is “1” by default. If bit 9.9 is written to be “0”, the Auto-Negotiation state machine for the local PHY will be blocked from advertising 1000BASE-T FDX. Note that the Link Partner will be notified of the state of 9.9 during Auto-Negotiation. After Auto-Negotiation is complete, changing the state of this bit has no effect unless Auto-Negotiation is manually restarted.

9.8 – 1000BASE-T HDX[1]

Since the CIS8201 is 1000BASE-T HDX capable, this bit is “1” by default. If bit 9.8 is written to be “0”, the Auto-Negotiation state machine for the local PHY will be blocked from advertising 1000BASE-T HDX. Note that the Link Partner will be notified of the state of 9.8 during Auto-Negotiation. After Auto-Negotiation is complete, changing the state of this bit has no effect unless Auto-Negotiation is manually restarted.

9.7:0 – Reserved

[1]The state of this register is internally latched when the Auto-Negotiation state machine enters the ABILITY_DETECT state. Changes to the states of these bits are recognized only at that time. This register is valid only in 1000BASE-T mode.

17.11 Register 10 (0Ah) – 1000BASE-T Status Register[1]

Register 10 (0Ah) – 1000BASE-T Status Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	MASTER/SLAVE Configuration Fault	RO LH SC	1 = MASTER/SLAVE configuration fault detected 0 = No MASTER/SLAVE configuration fault detected	0
14	MASTER/SLAVE Configuration Resolution	RO	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE	1
13	Local Receiver Status	RO	1 = Local receiver OK (loc_rcvr_status == OK) 0 = Local receiver not OK (loc_rcvr_status == NOT_OK)	0
12	Remote Receiver Status	RO	1 = Remote receiver OK (rem_rcvr_status == OK) 0 = Remote receiver not OK (rem_rcvr_status == NOT_OK)	0
11	LP 1000BASE-T FDX Capability	RO	1 = LP 1000BASE-T FDX capable 0 = LP not 1000BASE-T FDX capable	0
10	LP 1000BASE-T HDX Capability	RO	1 = LP is 1000BASE-T HDX capable 0 = LP is not 1000BASE-T HDX capable	0
9:8	Reserved	RO		00
7:0	Idle Error Count	RO SC		00000000

10.15 – MASTER/SLAVE Configuration Fault[1]

This bit indicates whether a MASTER/SLAVE configuration fault has been detected by the local PHY. A configuration fault occurs if both the local and remote PHYs are forced to the same MASTER/SLAVE state, or if no resolution is reached after seven retries. When such a fault has been detected, this bit is set to “1”, but the PHY continues to renegotiate until the MASTER/SLAVE configuration is resolved. Once set, this bit is automatically cleared when (and only when) Register 10 is read via the SMI.

10.14 – MASTER/SLAVE Configuration Resolution[1]

By default, the MASTER/SLAVE configuration is determined as part of the Auto-Negotiation process. However, the MASTER/SLAVE status can optionally be manually forced via bits in MII Register 9. Bit 10.14 indicates the final MASTER/SLAVE configuration status for the local PHY. This bit can change state only as a result of the reset or subsequent restart of the Auto-Negotiation process. This bit is only valid when the Auto-Negotiation Complete bit (1.5) is set.

10.13 – Local Receiver Status[1]

Bit 10.13 indicates the state of the loc_rcvr_status flag within the PMA receive function within the local PHY.

10.12 – Remote Receiver Status[1]

Bit 10.12 indicates the state of the rem_rcvr_status flag within the PMA receive function within the local PHY.

10.11 – LP 1000BASE-T FDX Capability[1]

Bit 10.11 is set to “1” if the Link Partner PHY advertises 1000BASE-T FDX capability; otherwise, this bit is set to “0”.

10.10 – LP 1000BASE-T HDX Capability[1]

Bit 10.10 is set to “1” if the Link Partner PHY advertises 1000BASE-T HDX capability; otherwise, this bit is set to “0”.

[1]The bits in this register apply only when the Page Received bit (6.1) is set..

10.9:8 – Reserved

10.7:0 – Idle Error Count[1]

Bits 10.7:0 indicate the Idle Error count, where 10.7 is the most significant bit. These bits contain a cumulative count of the errors detected when the receiver is receiving idles and PMA_TXMODE.indicate is equal to SEND (indicating that both the local and remote receiver status have been detected to be OK). The counter is incremented every symbol period that rx_error_status in the PMA receive function is equal to ERROR. Bits 10.7:0 are reset to all “0”s when the error count is read by the management function, or upon execution of the PCS reset function, and they are saturated to all “1”s in case of overflow.

[1]This bit applies only in 1000BASE-T mode.

17.12 Register 11 (0Bh) – Reserved Register

Register 11 (0Bh) – Reserved Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15:0	Reserved	RO		00000000 00000000

11.15:0 – Reserved

17.13 Register 12 (0Ch) – Reserved Register

Register 12 (0Ch) – Reserved Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15:0	Reserved	RO		00000000 00000000

12.15:0 – Reserved

17.14 Register 13 (0Dh) – Reserved Register

Register 13 (0Dh) – Reserved Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15:0	Reserved	RO		00000000 00000000

13.15:0 – Reserved

17.15 Register 14 (0Eh) – Reserved Register

Register 14 (0Eh) – Reserved Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15:0	Reserved	RO		00000000 00000000

14.15:0 – Reserved

17.16 Register 15 (0Fh) – 1000BASE-T Status Extension Register #1

Register 15 (0Fh) – 1000BASE-T Status Extension Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	1000BASE-X FDX Capability	RO	1 = PHY is 1000BASE-X FDX capable 0 = PHY is not 1000BASE-X FDX capable	0
14	1000BASE-X HDX Capability	RO	1 = PHY is 1000BASE-X HDX capable 0 = PHY is not 1000BASE-X HDX capable	0
13	1000BASE-T FDX Capability	RO	1 = PHY is 1000BASE-T FDX capable 0 = PHY is not 1000BASE-T FDX capable	1
12	1000BASE-T HDX Capability	RO	1 = PHY is 1000BASE-T HDX capable 0 = PHY is not 1000BASE-T HDX capable	1
11:0	Reserved	RO		000000000000

15.15 – 1000BASE-X FDX Capability

The CIS8201 is not 1000BASE-X capable, so this bit is hard-wired to “0”.

15.14 – 1000BASE-X HDX Capability

The CIS8201 is not 1000BASE-X capable, so this bit is hard-wired to “0”.

15.13 – 1000BASE-T FDX Capability

The CIS8201 is 1000BASE-T FDX capable, so this bit is hard-wired to “1”.

15.12 – 1000BASE-T HDX Capability

The CIS8201 is 1000BASE-T HDX capable, so this bit is hard-wired to “1”.

15.11:0 – Reserved

17.17 Register 16 (10h) – 100BASE-TX Status Extension Register[1]

Register 16 (10h) – 100BASE-TX Status Extension Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	100BASE-TX Descrambler Locked	RO	1 = Descrambler locked 0 = Descrambler not locked	0
14	100BASE-TX Lock Error Detected	RO SC	1 = Lock error detected since last read 0 = Lock error not detected since last read	0
13	100BASE-TX Disconnect State	RO SC	1 = PHY 100BASE-TX link disconnected 0 = PHY 100BASE-TX link not disconnected	0
12	100BASE-TX Current Link Status	RO	1 = PHY 100BASE-TX link active 0 = PHY 100BASE-TX link inactive	0
11	100BASE-TX Receive Error Detected	RO SC	1 = Receive error detected since last read 0 = Receive error not detected since last read	0
10	100BASE-TX Transmit Error Detected	RO SC	1 = Transmit error detected since last read 0 = Transmit error not detected since last read	0
9	100BASE-TX SSD Error Detected	RO SC	1 = SSD error detected since last read 0 = SSD error not detected since last read	0
8	100BASE-TX ESD Error Detected	RO SC	1 = ESD error detected since last read 0 = ESD error not detected since last read	0
7:0	Reserved	RO		00000000

16.15 – 100BASE-TX Descrambler Locked[1]

Bit 16.15 is set to “1” when the 100BASE-TX descrambler is locked; otherwise, this bit is set to “0”.

16.14 – 100BASE-TX Lock Error Detected[1]

Bit 16.14 is set to “1” if the 100BASE-TX descrambler has lost lock since the last read of this bit; otherwise, this bit is set to “0”.

16.13 – 100BASE-TX Disconnect State[1]

Bit 16.13 is set to “1” if the 100BASE-TX connection has been broken since the last read of this bit; otherwise, this bit is set to “0”.

16.12 – 100BASE-TX Current Link Status[1]

Bit 16.12 is set to “1” if the 100BASE-TX link is active; otherwise, this bit is set to “0”.

16.11 – 100BASE-TX Receive Error Detected[1]

Bit 16.11 is set to “1” if a 100BASE-TX packet with an invalid code has been received since the last read of this bit; otherwise, this bit is set to “0”.

16.10 – 100BASE-TX Transmit Error Detected[1]

Bit 16.10 is set to “1” if a 100BASE-TX packet has been received with a transmit error code since the last read of this bit; otherwise, this bit is set to “0”.

16.9 – 100BASE-TX False Carrier (SSD Error) Detected[1]

Bit 16.9 is set to “1” if a 100BASE-TX false carrier (Start-of-Stream Delimiter error) has been detected since the last read of this bit; otherwise, this bit is set to “0”.

[1]The bits in this register apply only in 100BASE-TX mode.

16.8 – 100BASE-TX Premature End (ESD Error) Detected[1]

Bit 16.8 is set to “1” if a 100BASE-TX premature end (End-of-Stream Delimiter error) has been detected since the last read of this bit; otherwise, this bit is set to “0”.

16.7:0 – Reserved

[1]The bits in this register apply only in 100BASE-TX mode.

17.18 Register 17 (11h) – 1000BASE-T Status Extension Register #2[1]

Register 17 (11h) – 1000BASE-T Status Extension Register #2				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	1000BASE-T Descrambler Locked	RO	1 = Descrambler locked 0 = Descrambler not locked	0
14	1000BASE-T Lock Error Detected	RO SC	1 = Lock error detected since last read 0 = Lock error not detected since last read	0
13	1000BASE-T Disconnect State	RO SC	1 = PHY 1000BASE-T link disconnected 0 = PHY 1000BASE-T link not disconnected	0
12	1000BASE-T Current Link Status	RO	1 = PHY 1000BASE-T link active 0 = PHY 1000BASE-T link inactive	0
11	1000BASE-T Receive Error Detected	RO SC	1 = Receive error detected since last read 0 = Receive error not detected since last read	0
10	1000BASE-T Transmit Error Detected	RO SC	1 = Transmit error detected since last read 0 = Transmit error not detected since last read	0
9	1000BASE-T SSD Error Detected	RO SC	1 = SSD error detected since last read 0 = SSD error not detected since last read	0
8	1000BASE-T ESD Error Detected	RO SC	1 = ESD error detected since last read 0 = ESD error not detected since last read	0
7	1000BASE-T Carrier Extension Error Detected	RO SC	1 = Carrier extension error detected since last read 0 = Carrier extension error not detected since last read	0
6	Non-compliant BCM5400 Detected	RO	1 = Non-compliant BCM5400 detected 0 = Non-compliant BCM5400 not detected	0
5:0	Reserved	RO		000000

17.15 – 1000BASE-T Descrambler Locked [1]

Bit 17.15 is set to “1” when the 1000BASE-T descrambler is locked; otherwise, this bit is set to “0”.

17.14 – 1000BASE-T Lock Error Detected[1]

Bit 17.14 is set to “1” if the 1000BASE-T descrambler has lost lock since the last read of this bit; otherwise, this bit is set to “0”.

17.13 – 1000BASE-T Disconnect State[1]

Bit 17.13 is set to “1” if the 1000BASE-T connection has been broken since the last read of this bit; otherwise, this bit is set to “0”.

17.12 – 1000BASE-T Current Link Status[1]

Bit 17.12 is set to “1” if the 1000BASE-T link is active; otherwise, this bit is set to “0”.

17.11 – 1000BASE-T Receive Error Detected[1]

Bit 17.11 is set to “1” if a 1000BASE-T packet with an invalid code has been received since the last read of this bit; otherwise, this bit is set to “0”.

17.10 – 1000BASE-T Transmit Error Detected[1]

Bit 17.10 is set to “1” if a 1000BASE-T packet has been received with a transmit error code since the last read of this bit; otherwise, this bit is set to “0”.

[1]The bits in this register apply only in 1000BASE-T mode.

17.9 – 1000BASE-T False Carrier (SSD Error) Detected[1]

Bit 17.9 is set to “1” if a 1000BASE-T false carrier (Start-of-Stream Delimiter error) has been detected since the last read of this bit; otherwise, this bit is set to “0”.

17.8 – 1000BASE-T Premature End (ESD Error) Detected[1]

Bit 17.8 is set to “1” if a 1000BASE-T premature end (End-of-Stream Delimiter error) has been detected since the last read of this bit; otherwise, this bit is set to “0”.

17.7 – 1000BASE-T Carrier Extension Error Detected[1]

Bit 17.7 is set to “1” if a carrier extension error has been detected since the last read of this bit; otherwise, this bit is set to “0”.

17.6 – Non-compliant BCM5400 Detected[1]

Bit 17.6 is a read-only bit set to “1” if the CIS8201 detects a non-compliant BCM5400 as its link partner; otherwise, this bit is set to “0”. This bit is valid only when the 1000BASE-T descrambler has achieved a locked state. The behavior of the PHY with regard to non-compliant BCM5400 detection is controlled by MII Register bits 18.7 and 18.6.

17.5:0 – Reserved

[1]The bits in this register apply only in 1000BASE-T mode.

17.19 Register 18 (12h) – Bypass Control Register

Register 18 (12h) – Bypass Control Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	Transmit Disable	R/W	1 = Transmitter disabled in PHY 0 = Transmitter enabled	0
14	Bypass 4B5B Encoder/Decoder	R/W	1 = Bypass 4B5B encoder/decoder 0 = Enable 4B5B encoder/decoder	0
13	Bypass Scrambler	R/W	1 = Bypass scrambler 0 = Enable scrambler	0
12	Bypass Descrambler	R/W	1 = Bypass descrambler 0 = Enable descrambler	0
11	Bypass PCS Receive	R/W	1 = Bypass PCS receive 0 = Enable PCS receive	0
10	Bypass PCS Transmit	R/W	1 = Bypass PCS transmit 0 = Enable PCS transmit	0
9	Bypass Link Fail Inhibit (LFI) Timer	R/W	1 = Bypass link_fail_inhibit timer (to enable faster Auto-Negotiation) 0 = Do not bypass link_fail_inhibit timer	0
8	Transmitter Test Clock Enable	R/W	1 = Enable TX_TCLK test output on CLK125 pin 0 = Disable TX_TCLK test output on CLK125 pin	0
7	Force Non-compliant BCM5400 Detection	R/W	1 = Force non-compliant BCM5400 detection 0 = Do not force non-compliant BCM5400 detection	0
6	Bypass Non-compliant BCM5400 Detection	R/W, RS	1 = Disable automatic non-compliant BCM5400 detection 0 = Enable automatic non-compliant BCM5400 detection	0
5	Disable Automatic Pair Swap Correction	R/W	1 = Disable pair swap correction 0 = Enable pair swap correction	0
4	Disable Polarity Correction	R/W	1 = Disable polarity inversion correction 0 = Enable polarity inversion correction	0
3	Parallel-Detect Control	R/W, RS	1 = Do not ignore advertised ability 0 = Ignore advertised ability	1
2	Disable Pulse Shaping Filter	R/W	1 = Disable pre-emphasis filter 0 = Enable pre-emphasis filter	0
1	Disable Automatic 1000BASE-T Next-Page Exchange	R/W, RS	1 = Disable automatic 1000BASE-T Next-Page exchanges 0 = Enable automatic 1000BASE-T Next-Page exchanges	0
0	125MHz Clock Output Enable	R/W, RS	1 = Enable 125MHz output clock pin (CLK125) 0 = Disable 125MHz output clock pin (CLK125)	1

18.15 – Transmit Disable

When bit 18.15 is set to “1”, the transmitter outputs are left floating (high impedance).

18.14 – Bypass 4B5B Encoder/Decoder[1]

When bit 18.14 is set to “1”, the 5B codes (TX_ER and TXD[4:0]) will be passed from the MII interface directly to the scrambler, bypassing the 4B5B encoder. Note that in this mode, J/K and T/R code insertion will not be performed. The receiver will pass descrambled/aligned 5B codes directly to the MII interface (RX_ER and RXD[4:0]), bypassing the 4B5B decoder. Carrier sense (CRS) is still asserted when a valid frame is detected.

18.13 – Bypass Scrambler[2]

When bit 18.13 is set to “1”, the scrambler is disabled.

[1]This bit applies only in 100BASE-TX mode.

[2]This bit applies only in 100BASE-TX and 1000BASE-T modes.

18.12 – Bypass Descrambler[1]

When bit 18.12 is set to “1”, the descrambler is disabled.

18.11 – Bypass PCS Receive[1]

When bit 18.11 is set to “1”, PCS receive for the four subchannels is bypassed. In 1000BASE-T mode, a 4-D symbol is encoded into a 10-bit data word and sent to the GMII interface. The RX_DV and RX_ER pins are used for the upper two bits of the encoded data, and RXD pins are used for the remaining eight bits of the encoded data. When receiving idle codes, the Viterbi decoder can by bypassed, receiving symbols through the 4-D slicer instead. In 100BASE-TX mode, to pass the unaligned symbols directly to the MII interface, this control bit should be set only when the 4B5B decoder is also bypassed.

18.10 – Bypass PCS Transmit[1]

When bit 18.10 is set to “1”, the PCS transmit for the four subchannels is bypassed.

18.9 – Bypass LFI Timer

If this bit is set, the link_fail_inhibit timer defined in Clause 28 of the IEEE 802.3 standard is bypassed under certain conditions to allow faster re-Auto-Negotiation. This timer will be bypassed if either the MASTER/SLAVE negotiation resulted in a tie, or no common capabilities were discovered during the previous negotiation. If this bit is not set, the Auto-Negotiation state machines behave as defined in the IEEE standard.

18.8 – Enable Transmit Clock TX_TCLK Output on CLK125 Pin

When bit 18.8 is written to a “1”, the CLK125 output pin becomes a test pin for the transmit clock “TX_TCLK” of the PHY port. This capability is intended to enable measurement of transmitter timing jitter, as specified in IEEE Standard 802.3-2000, section 40.6.1.2.5. When in IEEE-specified transmitter test modes 2 or 3 (see IEEE 802.3-2000, section 40.6.1.1.2 and MII Register bits 9.15:13), the peak-to-peak jitter of the zero-crossings of the differential signal output at the MDI, relative to the corresponding edge of TX_TCLK, is measured. The corresponding edge of TX_TCLK is the edge of the transmit test clock, in polarity and time, that generates the zero-crossing transition being measured.

While transmitter test mode clock TX_TCLK is intended only for characterization test purposes, CLK125 is intended, for example, to serve as a general purpose system or MAC reference clock.

Two distinct clock signals can be multiplexed onto the CIS8201’s CLK125 pin, depending on a combination of the settings of MII Register bits 9.15:13, MII Register bit 18.8, and MII Register bit 18.0 (CLK125 Output Enable), as specified in the following table.

Table 17-3. CLK125 Pin Multiplexed Clock Signals

Signal Multiplexed onto CLK125 Pin	Enabled by MII Register States
TX_TCLK	((9.15:13 == 010) || (9.15:13 == 011) || (18.8 ==1))
CLK125	PHY0, 18.0 == 1

18.7 – Force Non-compliant BCM5400 Detection[2]

When this bit is set to a “1” and MII Register bit 18.6 is set to a “1”, then the CIS8201 operates as a non-compliant BCM5400 PHY. If MII Register bit 18.6 is set to a “1” and this bit is a “0”, then the CIS8201 operates as a fully IEEE compliant PHY. If MII Register bit 18.6 is set to “0”, then this bit has no affect on the CIS8201 operation.

[1]This bit applies only in 100BASE-TX and 1000BASE-T modes.

[2]This bit applies only in 1000BASE-T mode.

18.6 – Bypass Non-compliant BCM5400 Detection

When bit 18.6 is set to “0”, the PHY automatically detects and corrects for non-compliant BCM5400 link partner PHYs. When this bit is set to “1”, automatic non-compliant BCM5400 detection is disabled, and the local PHY’s operating mode is determined by the status of MII Register bit 18.7. If bit 18.7 is a “1”, then the local PHY operates as a non-compliant BCM5400 PHY. When bit 18.7 is a “0”, the local PHY operates as a fully IEEE-compliant PHY. Note that this control bit applies only in 1000BASE-T mode.

18.5 – Disable Automatic Pair Swap Correction

When bit 18.5 is set to “0”, the PHY automatically corrects pair swaps between subchannels A and B, and between subchannels C and D, due to “MDI/MDI-X crossover”. It will also correct pair swaps between subchannels C and D due to cabling errors. When bit 18.5 is set to “1”, the PHY does not correct pair swaps. Note that this control bit applies in all modes: 10BASE-T, 100BASE-TX, and 1000BASE-T.[1]

18.4 – Disable Polarity Correction

When bit 18.4 is set to “0”, the PHY automatically corrects polarity inversion on all the subchannels. When bit 18.4 is set to “1”, the PHY does not compensate for polarity inversions.

18.3 – Parallel-Detect Control

When bit 18.3 is “1”, MII Register 4, bits [8:5], are taken into account when attempting to parallel-detect. This is the default behavior expected by the standard. Setting 18.3 to a “0” will result in Auto-Negotiation ignoring the advertised abilities, as specified in MII Register 4, during parallel detection of a non-auto-negotiating 10BASE-T or 100BASE-TX PHY.

18.2 – Disable Pulse Shaping Filter

When bit 18.2 is set to “1”, the 1000BASE-T two-tap digital transmit filter is disabled. This bit applies only in 1000BASE-T mode.

18.1 – Disable Automatic 1000BASE-T Next-Page Exchanges

Bit 18.1 is used to control the automatic exchange of 1000BASE-T Next-Pages defined in IEEE 802.3 - 2000 (Annex 40C). When this bit is set, the automatic exchange of these pages is disabled, and the control is returned to the user through the SMI after the base page has been exchanged. The user then has complete responsibility to:

- send the correct sequence of Next-Pages to the Link Partner, *and*
- determine common capabilities and force the device into the correct configuration following successful exchange of pages.

When bit 18.1 is reset to “0”, the 1000BASE-T related Next-Pages are automatically exchanged without user intervention. If the Next Page bit 4.15 was set by the user in the Auto-Negotiation Advertisement register at the time the Auto-Negotiation was restarted, control is returned to the user for additional Next-Pages following the 1000BASE-T Next-Page exchange.

If both 18.1 and 4.15 are reset when an Auto-Negotiation sequence is initiated, all Next-Page exchange is automatic, including sourcing of null pages. No user notification is provided until either Auto-Negotiation completes or fails. See the description of Register bit 4.15 for more details on standard Next-Page exchanges. Note that this control bit applies only in 1000BASE-T mode.

18.0 – Enable 125MHz Free-Running Clock Output

When bit 18.0 is set to “1”, the CIS8201 provides a free-running, general-purpose 125MHz clock on the CLK125 output pin for use, for example, by the MAC, system manager CPU, or control logic. By default, this pin is enabled, and is always toggling (active), independent of the status of any link, unless a hardware reset is active (which also powers down the PLL). When disabled, this pin is normally driven low.

[1] Consistent with 10/100/1000BASE-T PHYs on the market today, this bit applies only when Auto-Negotiation is enabled; Auto MDI/MDI-X functionality is automatically disabled when Auto-Negotiation is disabled.

17.20 Register 19 (13h) – Receive Error Counter Register

Register 19 (13h) – Receive Error Counter Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15:8	Reserved	RO		00000000
7:0	Receive Error Counter	RO SC	Number of non-collision packets with receive errors since last read	00000000

19.15:8 – Reserved

19.7:0 – Receive Error Counter

Each time the PHY detects a non-collision packet containing at least one error, 19.7:0 is incremented. The counter will saturate at 0FFh. This register is cleared only when read, or upon either a hardware or software reset. These bits are valid only in 100BASE-TX and 1000BASE-T modes.

17.21 Register 20 (14h) – False Carrier Sense Counter Register

Register 20 (14h) – False Carrier Sense Counter Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15:8	Reserved	RO		00000000
7:0	False Carrier Sense Counter	RO SC	Number of false carrier events since last read	00000000

20.15:8 – Reserved

20.7:0 – False Carrier Sense Counter

The PHY will increment 20.7:0 each time it detects a false carrier on the receive input. The counter will saturate at 0FFh. This register is cleared only when read, or upon either a hardware or software reset. These bits are valid only in 100BASE-TX and 1000BASE-T modes.

17.22 Register 21 (15h) – Disconnect Counter Register

Register 21 (15h) – Disconnect Counter Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15:8	Reserved	RO		00000000
7:0	Disconnect Counter	RO SC	Number of disconnects since last read	00000000

21.15:8 – Reserved

21.7:0 – Disconnect Counter

The PHY will increment 21.7:0 each time the Carrier Integrity Monitor (CIM) enters the “link unstable” state. The counter will saturate at 0FFh. This register is cleared only when read, or upon a hardware or software reset.

17.23 Register 22 (16h) – 10BASE-T Control & Status Register[1]

Register 22 (16h) – 10BASE-T Control & Status Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	Link Integrity Test State Machine Disable	R/W, RS	1 = Disable link integrity test 0 = Enable link integrity test	0
14	Jabber Detect Disable	R/W, RS	1 = Disable jabber detect 0 = Enable jabber detect	0
13	Echo Mode Disable	R/W, RS	1 = Disable echo mode 0 = Enable echo mode	0
12	SQE Disable Mode	R/W, RS	1 = Disable SQE transmit 0 = Enable SQE transmit	0
11:10	Squelch Control	R/W, RS	00 = 300mV 01 = 197mV 10 = 450mV 11 = Reserved	00
9	Reserved	R/W		0
8	EOF Error Detected	RO SC	1 = EOF error detected since last read 0 = EOF error not detected since last read	0
7	10BASE-T Disconnect State	RO SC	1 = 10BASE-T link disconnected 0 = 10BASE-T link connected	0
6	10BASE-T Link Status	RO	1 = 10BASE-T link active 0 = 10BASE-T link inactive	0
5:3	Current Reference Trim	R/W, RS	(See Table 17-4)	000
2:0	Reserved	RO		000

22.15 – Disable Link Integrity Test State Machine[1]

When bit 22.15 is set to “0”, the CIS8201 link integrity state machine runs automatically; it also controls link pass status. When bit 22.15 is set to “1”, the link integrity state machine is bypassed, and the PHY is forced into link pass status.

22.14 – Disable Jabber Detect[1]

When bit 22.14 is set to “0”, the CIS8201 automatically shuts off the transmitter when a transmission request exceeds the IEEE-specified time limit. When bit 22.14 is set to “1”, transmission requests are allowed to be arbitrarily long without shutting down the transmitter.

22.13 – Disable Echo Mode[1]

When bit 22.13 is set to “1”, the logical state of the TX_EN pin will *not* echo onto the CRS pin, effectively disabling CRS from being asserted in half-duplex operation. For example, when TX_EN is driven to “0”, the CRS pin will also be driven to a “0”. When bit 22.13 is set to “0”, the TX_EN pin will be echoed onto the CRS pin.

22.12 – SQE Disable[1]

When bit 22.12 is set to “1”, SQE (Signal Quality Error) pulses are not sent. Note that this control bit applies in 10BASE-T HDX mode only.

22.11:10 – Squelch Control[1]

When bits 22.11:10 are set to “00”, the CIS8201 uses 300mV as the squelch threshold level, prescribed by the IEEE’s 10BASE-T specification. When bits 22.11:10 are set to “01”, the squelch level is decreased to 197mV, which may improve the bit error rate performance on long loops. When bits 22.11:10 are set to “10”, the squelch level is increased to 450mV, which may improve the bit error rate in high-noise environments. These bits also control the ActiPHY™ comparator squelch levels (see Section 15.9: "ActiPHY(tm) Power Management" for more information).

[1]The bits in this register apply only in 10BASE-T mode, except for bit 22.13, which applies to both 10BASE-T and 100BASE-TX modes.

22.9, 22.2:0 – Reserved

22.8 – EOF Error[1]

When bit 22.8 returns a “1”, a defective EOF (End-of-Frame) sequence has been received since the last time this bit was read. This bit is automatically set to “0” when it is read.

22.7 – 10BASE-T Disconnect State[1]

Bit 22.7 is set to “1” if the 10BASE-T connection has been broken by the Carrier Integrity Monitor (CIM) since the last read of this bit; otherwise, this bit is set to “0”.

22.6 – 10BASE-T Link Status[1]

Bit 22.6 is set to “1” if the 10BASE-T link is active; otherwise, this bit is set to “0”.

22.5:3 – Current Reference Trim[1]

Bits 5:3 provide trim adjustments for the internal current reference on the CIS8201. This adjustment controls the transmit power only in 10BASE-T mode. It may be used, in particular, to trim the nominal transmit power for a particular network interface design. It has no effect on the receive operation of the CIS8201.

The current reference trim adjustments are encoded using the bit values in the following table.

Table 17-4. 10BASE-T Current Reference Trim Values

Bits 5:3	Adjustment
011	+6%
010	+6%
001	+4%
000	+2%
111	0%
110	-2%
101	-4%
100	-4%

[1]The bits in this register apply only in 10BASE-T mode, except for bit 22.13, which applies to both 10BASE-T and 100BASE-TX modes.

17.24 Register 23 (17h) – Extended PHY Control Register #1

Register 23 (17h) – Extended PHY Control Register #1				
Bit	**Name**	**Access**	**States**	**Reset Value**
15:12	MAC Interface Mode Select	R/W, RS	0000 = Enable GMII/MII (default) 0001 = Enable RGMII 0010 = Enable TBI 0011 = Enable RTBI 0100 to 1111 = Future use (reserved)	0000
11:9	MAC Interface and Digital I/O Power Supply Voltage Select	R/W, RS	000 = I/O pins will operate from 3.3V supply 001 = I/O pins will operate from 2.5V supply 010 to 111 = Future use (reserved)	000
8	RGMII Skew Timing Compensation Enable	R/W, RS	1 = Enable RGMII skew timing compensation 0 = Disable RGMII skew timing compensation	0
7	EWRAP Enable	R/W	1 = Enable EWRAP in TBI mode 0 = Disable EWRAP in TBI mode	0
6	TBI Bit Order Reversal Enable	R/W, RS	1 = Enable TBI bit order reversal 0 = Disable TBI bit order reversal (default)	0
5	ActiPHY™ Enable	R/W	1 = ActiPHY™ low power mode enabled 0 = ActiPHY™ low power mode disabled	0
4:2, 0	Reserved	RO		000000
1	GMII Transmit Pin Reversal	R/W	0 = GMII transmit pin order default 1 = GMII transmit pin order reversed	0

23.15:12 – MAC Interface Mode Select

When bits 23.15:12 are set per the values listed in the register table above, the respective MAC interfaces are enabled. The default system interface operating mode is GMII/MII.

23.11:9 – MAC Interface Voltage Select

Bits 23.11:9 specify the I/O voltage at which the MAC interface (GMII, MII, RGMII, TBI, or RTBI) and all other digital interface pins will be operated. By default, 3.3V GMII I/O operating conditions are used.[1]

23.8 – Enable RGMII Timing Skew Compensation

Bit 23.8 enables a unique, on-chip timing circuit to compensate for sensitive RGMII timings, which normally must be addressed by using a “trombone style” timing delay on the PC board. See Section 20.9: "RGMII/RTBI Mode Timing ," and the RGMII specification for more information. By default, this compensation circuit is disabled.

23.7 – EWRAP Enable

When bit 23.7 is set to “1” and bits 23.15:12 are set to “0010”, TBI loopback toward the MAC is enabled.

23.6 – TBI Bit Order Reversal Enable

Bit 23.6 allows the user to specify the bit order for the PCS only when TBI mode is selected. By default, reversing the TBI bit order, as defined in the IEEE standard, is disabled.

23.5 – ActiPHY™ Enable

The Station Manager is expected to set bit 23.5 to “1” when it detects that the PHY has not established a link for a certain period of time, thus enabling the ActiPHY™ power management mode. This bit is cleared when the PHY detects network activity. See Section 15.9: "ActiPHY(tm) Power Management" for more information.

23.4:2, 0 – Reserved

23.1 – GMII Transmit Pin Reversal

[1] To be compliant with the RGMII/RTBI standard, 23.11:9 must be set to “001” when the PHY is to be operated in RGMII/RTBI mode since the RGMII/RTBI standard specifies a 2.5V I/O supply. RGMII may also be used with a 3.3V I/O supply.

Bit 23.1 allows for flexibility in printed circuit board routing. This pin can be used to reorder the GMII transmit pins. The pin assignments are shown in the following table.

Table 17-5. GMII Transmit Pin Ordering

Bit 23.1	Pin Name	Pin Number
0	TXD0	63
	TXD1	62
	TXD2	61
	TXD3	60
	TXD4	59
	TXD5	58
	TXD6	57
	TXD7	56
1	TXD0	56
	TXD1	57
	TXD2	58
	TXD3	59
	TXD4	60
	TXD5	61
	TXD6	62
	TXD7	63

17.25 Register 24 (18h) – Extended PHY Control Register #2

Register 24 (18h) – Extended PHY Control Register #2				
Bit	**Name**	**Access**	**States**	**Reset Value**
15:13	100/1000BASE-T Edge Rate Control	R/W, RS	011 = +3 edge rate (slowest) 010 = +2 edge rate 001 = +1 edge rate 000 = Nominal edge rate 111 = -1 edge rate 110 = -2 edge rate 101 = -3 edge rate 100 = -4 edge rate (fastest)	000
12:10	100/1000BASE-T Transmit Voltage Reference Trim	R/W, RS	(See Table 17-6)	000
9:7	TX FIFO Depth Control for GMII, RGMII, TBI, and RTBI	R/W, RS	000 = 5 symbols 001 = 4 symbols 010 = 3 symbols 011 = 2 symbols 100 = 1 symbol 101 to 111 = Reserved[1]	100
6:4	RX FIFO Depth Control (TBI only)	R/W, RS	000 = 5 symbols 001 = 4 symbols 010 = 3 symbols 011 = 2 symbols 100 = 1 symbol 101 to 111 = Reserved	100
3:1	Cable Quality Status	RO	000 = cable length < 10m 001 = 10m < cable length < 20m 010 = 20m < cable length < 40m 011 = 40m < cable length < 80m 100 = 80m < cable length < 100m 101 = 100m < cable length <140m 110 = 140m < cable length <180m 111 = cable length > 180m	000
0	1000BASE-T Analog Loopback Control	R/W	1 = Enable 1000BASE-T analog loopback through the hybrid 0 = Disable 1000BASE-T analog loopback through the hybrid	0

[1] The unused bit combination “111” is used to disable IEEE 802.3z (Clause 37) Auto-Negotiation handshaking. See Section 15.4: "Auto-Negotiation" for more information.

24.15:13 – 100/1000BASE-T Edge Rate Control

Bits 24.15:13 control the transmit driver slew rate in 100BASE-TX and 1000BASE-T modes only, as shown above. The difference between each setting is approximately 200ps to 300ps, with the “+3” setting resulting in the slowest edge rate, and the “-4” setting resulting in the fastest edge rate.

24.12:10 – 100/1000BASE-T Transmit Voltage Reference Trim

Bits 12:10 provide trim adjustments for the internal voltage reference on the CIS8201. This adjustment controls the transmit power for 100BASE-TX and 1000BASE-T modes. It may be used, in particular, to trim the nominal transmit power for a particular network interface design.

The transmit voltage reference trim adjustments are encoded using the bit values in the following table

Table 17-6. 100/1000BASE-T Transmit Voltage Reference Trim Values

Bits 12:10	Adjustment
011	+6%
010	+6%
001	+4%
000	+2%
111	0%
110	-2%
101	-4%
100	-4%

24.9:7 – TX FIFO Depth Control[1]

Bits 24.9:7 control symbol buffering for the transmit synchronization FIFO used in GMII, RGMII, TBI, and RTBI modes.[2]

During symbol transmission in GMII, RGMII, TBI, and RTBI modes, bits 24.9:7 control the depth of the FIFO, which directly determines the maximum transmittable packet size. An internal FIFO is used to synchronize the clock domains between the MAC transmit clock (e.g., GTX_CLK) and the PHY's clock (e.g., XTAL1), used to transmit symbols on the local PHY's twisted pair interface. By controlling the transmit synchronization FIFO depth with these three bits, the user sets the maximum packet size which can be successfully transmitted by the CIS8201.

$$\text{FIFO Setting} = \frac{((\text{Freq. Tolerance Error of MAC Clock} + \text{Freq. Tolerance Error of PHY Clock}) \times \text{Max. Packet Size})}{1{,}000{,}000},$$

where the frequency tolerance offset is in ppm, the maximum packet size is in bytes, and the FIFO setting is in symbols.[3]

For example, when GTX_CLK = 125MHz ±100ppm, XTAL1 = 125MHz ±50ppm, and the maximum packet size is 9600 bytes (a jumbo packet):

FIFO Setting = ((100ppm+ 50ppm) x 9600 bytes)/1,000,000 = 2 symbols of FIFO buffering = Register bit setting of "011".

24.6:4 – RX FIFO Depth Control (TBI Mode Only)[1]

Used in TBI mode only, bits 24.6:4 control symbol buffering as determined by the receive synchronization FIFO.[3]

24.3:1 – Cable Quality Status

Valid only in 100/1000BASE-T modes, bits 24.3:1 indicate the *approximate* effective electrical length of the cable in meters, as shown in the register table above.

24.0 – 1000BASE-T Analog Loopback Control

This bit is valid only in 1000BASE-T mode. When asserted, bit 24.0 enables analog loopback through the CIS8201's internal hybrid. Because loopback occurs at the hybrid, the transmit/receive signal will be observed on the media (cable). This bit should always be disabled in normal operating modes. See MII Register bit 0.14 for information about the IEEE - 802.3 standard's specified loopback operation.

---

[1]The TX and RX FIFOs are not used in MII mode for 10BASE-T and 100BASE-TX.

[2]The unused bit combination "111" is used to disable IEEE 802.3z Auto-Negotiation handshaking. See Section 15.4: "Auto-Negotiation" for more information.

[3]When using standard 1518-byte packets and following the frequency tolerance for the clocks, a standard inter-packet gap (IPG) of twelve symbols is required by the IEEE 802.3 specification. When using larger, non-standard packets, a larger IPG is required due to the possible compression of the IPG at the output of the FIFO. Cicada recommends increasing the IPG size by one cycle for each additional symbol of buffering used in the FIFO. For the default FIFO buffering of 1 symbol, an IPG of 12 is recommended. For a FIFO buffering of 5 symbols, an IPG of 16 is recommended.

17.26 Register 25 (19h) – Interrupt Mask Register

Register 25 (19h) – Interrupt Mask Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	Interrupt Pin Enable	R/W	1 = Enable interrupt pin 0 = Disable interrupt pin	0
14	Speed State-Change Interrupt Mask	R/W, RS	1 = Enable Speed interrupt 0 = Disable Speed interrupt	0
13	Link State-Change / ActiPHY™ Interrupt Mask	R/W, RS	1 = Enable Link / ActiPHY™ interrupt 0 = Disable Link / ActiPHY™ interrupt	0
12	Duplex State-Change Interrupt Mask	R/W, RS	1 = Enable Duplex interrupt 0 = Disable Duplex interrupt	0
11	Auto-Negotiation Error Interrupt Mask	R/W, RS	1 = Enable Auto-Negotiation Error interrupt 0 = Disable Auto-Negotiation Error interrupt	0
10	Auto-Negotiation-Done Interrupt Mask	R/W, RS	1 = Enable Auto-Negotiation-Done interrupt 0 = Disable Auto-Negotiation-Done interrupt	0
9	Page-Received Interrupt Mask	R/W, RS	1 = Enable Page-Received interrupt 0 = Disable Page-Received interrupt	0
8	Symbol Error Interrupt Mask	R/W, RS	1 = Enable Symbol Error interrupt 0 = Disable Symbol Error interrupt	0
7	Descrambler Lock-Lost Interrupt Mask	R/W, RS	1 = Enable Lock-Lost interrupt 0 = Disable Lock-Lost interrupt	0
6	MDI Crossover Change Interrupt Mask	R/W, RS	1 = Enable MDI Crossover interrupt 0 = Disable MDI Crossover interrupt	0
5	Polarity-Change Interrupt Mask	R/W, RS	1 = Enable Polarity-Change interrupt 0 = Disable Polarity-Change interrupt	0
4	Jabber-Detect Interrupt Mask	R/W, RS	1 = Enable Jabber-Detect interrupt 0 = Disable Jabber-Detect interrupt	0
3	False Carrier Interrupt Mask	R/W, RS	1 = Enable False Carrier interrupt 0 = Disable False Carrier interrupt	0
2	Parallel-Detect Interrupt Mask	R/W, RS	1 = Enable Parallel-Detect interrupt 0 = Disable Parallel-Detect interrupt	0
1	MASTER/SLAVE Interrupt Mask	R/W, RS	1 = Enable MASTER/SLAVE interrupt 0 = Disable MASTER/SLAVE interrupt	0
0	RX_ER Interrupt Mask	R/W, RS	1 = Enable RX_ER interrupt 0 = Disable RX_ER interrupt	0

25.15 – Interrupt Pin Enable

When bit 25.15 is set to “1”, the hardware interrupt is enabled, meaning that the state of the external interrupt pin (MDINT#, which is active low) can be influenced by the state of the Interrupt Status bit (26.15). When bit 25.15 is set to “0”, the interrupt status bits (Register 26) continue to be set in response to interrupts, but the interrupt hardware pin MDINT# on the CIS8201 will not be influenced by the PHY. The MDINT# hardware pin is essentially a logical NAND function of the register bits (25.15 and 26.15).

25.14 – Speed State-Change Interrupt Mask

When bit 25.14 is set to “1”, the Speed State-Change interrupt is enabled.

25.13 – Link State-Change / ActiPHY™ Interrupt Mask

While bit 23.5 is set, setting bit 25.13 to “1” enables the ActiPHY™ interrupt. While bit 23.5 is cleared, setting this bit to “1” enables the Link State-Change interrupt.

25.12 – Duplex State-Change Interrupt Mask

When bit 25.12 is set to “1”, the Duplex State-Change interrupt is enabled.

25.11 – Auto-Negotiation Error Interrupt Mask

When bit 25.11 is set to “1”, the Auto-Negotiation Error interrupt is enabled.

25.10 – Auto-Negotiation-Done Interrupt Mask

When bit 25.10 is set to “1”, the Auto-Negotiation-Done interrupt is enabled.

25.9 – Page-Received Interrupt Mask[1]

When bit 25.9 is set to “1”, the Page-Received interrupt is enabled.

25.8 – Symbol Error Interrupt Mask[1]

When bit 25.8 is set to “1”, the Symbol Error interrupt is enabled.

25.7 – Descrambler Lock-Lost Interrupt Mask[1]

When bit 25.7 is set to “1”, the Descrambler Lock-Lost interrupt is enabled.

25.6 – MDI-Crossover Change Interrupt Mask[2]

When bit 25.6 is set to “1”, the MDI Crossover Status-Change interrupt is enabled.

25.5 – Polarity-Change Interrupt Mask

When bit 25.5 is set to “1”, the Polarity-Change interrupt is enabled.

25.4 – Jabber-Detect Interrupt Mask[3]

When bit 25.4 is set to “1”, the Jabber-Detect interrupt is enabled.

25.3 – False Carrier Interrupt Mask[1]

When bit 25.3 is set to “1”, the False Carrier interrupt is enabled.

25.2 – Parallel-Detect Error Interrupt Mask

When bit 25.2 is set to “1”, the Parallel-Detect Error interrupt is enabled.

25.1 – MASTER/SLAVE Resolution Error Interrupt Mask[4]

When bit 25.1 is set to “1”, the MASTER/SLAVE Resolution Error interrupt is enabled.

25.0 – RX_ER Interrupt Mask

When bit 25.0 is set to “1”, the RX_ER interrupt is enabled.

[1]This bit applies only in 100BASE-TX and 1000BASE-T modes.

[2]Consistent with 10/100/1000BASE-T PHYs on the market today, this bit applies only when Auto-Negotiation is enabled; Auto MDI/MDI-X functionality is automatically disabled when Auto-Negotiation is disabled.

[3]This bit applies only in 10BASE-T mode.

[4]This bit applies only in 1000BASE-T mode.

17.27 Register 26 (1Ah) – Interrupt Status Register

Register 26 (1Ah) – Interrupt Status Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	Interrupt Status	RO SC	1 = Interrupt pending 0 = No interrupt pending	0
14	Speed State-Change Interrupt Status	RO SC	1 = Speed interrupt pending	0
13	Link State-Change / ActiPHY™ Interrupt Status	RO SC	1 = Link state-change / ActiPHY™ interrupt pending	0
12	Duplex State-Change Interrupt Status	RO SC	1 = Duplex interrupt pending	0
11	Auto-Negotiation Error Interrupt Status	RO SC	1 = Auto-Negotiation Error interrupt pending	0
10	Auto-Negotiation-Done Interrupt Status	RO SC	1 = Auto-Negotiation-Done interrupt pending	0
9	Page-Received Interrupt Status	RO SC	1 = Page-Received Interrupt pending	0
8	Symbol Error Interrupt Status	RO SC	1 = Symbol Error interrupt pending	0
7	Descrambler Lock-Lost Interrupt Status	RO SC	1 = Lock-Lost interrupt pending	0
6	MDI Crossover Change Interrupt Status	RO SC	1 = MDI Crossover interrupt pending	0
5	Polarity-Change Interrupt Status	RO SC	1 = Polarity-Change interrupt pending	0
4	Jabber-Detect Interrupt Status	RO SC	1 = Jabber-Detect interrupt pending	0
3	False Carrier Interrupt Status	RO SC	1 = False Carrier interrupt pending	0
2	Parallel-Detect Interrupt Status	RO SC	1 = Parallel-Detect Error interrupt pending	0
1	MASTER/SLAVE Interrupt Status	RO SC	1 = MASTER/SLAVE Error interrupt pending	0
0	RX_ER Interrupt Status	RO	1 = RX_ER interrupt pending 0 = No RX_ER interrupt pending	0

26.15 – Interrupt Status

When bit 26.15 is set to “1”, an unacknowledged interrupt is pending. The cause of the interrupt can be determined by reading the interrupt status bits in this register. This bit is automatically cleared when read.

26.14 – Speed State-Change Interrupt Status

When the operating speed of the PHY changes, bit 26.14 is set to “1” only if bit 25.14 is also set to “1”. This bit is automatically cleared when read.

26.13 – Link State-Change / ActiPHY™ Interrupt Status

While bit 23.5 is set, bit 26.13 is set to “1” when energy is detected on the media interface. When bit 23.5 is cleared, this bit is set to “1” when the link status of the PHY changes. This bit is set to “1” only if bit 25.13 is also set to “1”. This bit is automatically cleared when read.

26.12 – Duplex State-Change Interrupt Status

When the duplex status of the PHY changes, bit 26.12 is set to “1” if bit 25.12 is also set to “1”. This bit is automatically cleared when read.

26.11 – Auto-Negotiation Error Interrupt Status

When an error is detected by the Auto-Negotiation state machine, bit 26.11 is set to “1” if bit 25.11 is also set to “1”. This bit is automatically cleared when read.

26.10 – Auto-Negotiation-Done Interrupt Status

When the Auto-Negotiation state machine finishes a negotiation process, bit 26.10 is set to “1” if bit 25.10 is also set to “1”. This bit is automatically cleared when read.

26.9 – Page-Received Interrupt Status

When a new Next-Page is received, bit 26.9 is set to “1” if bit 25.9 is also set to “1”. This bit is automatically cleared when read.

26.8 – Symbol Error Interrupt Status[1]

When a symbol error is detected by the descrambler, bit 26.8 is set to “1” if bit 25.8 is also set to “1”. This bit is automatically cleared when read.

26.7 – Descrambler Lock-Lost Interrupt Status[1]

When the descrambler loses lock, bit 26.7 is set to “1” if bit 25.7 is also set to “1”. This bit is automatically cleared when read.

26.6 – MDI Crossover Change Interrupt Status[2]

When the MDI crossover status of the PHY changes, bit 26.6 is set to “1” if bit 25.6 is also set to “1”. This bit is automatically cleared when read.

26.5 – Polarity-Change Interrupt Status

When a polarity status error of the PHY changes, bit 26.5 is set to “1” if bit 25.5 is also set to “1”. This bit is automatically cleared when read.

26.4 – Jabber-Detect Interrupt Status[3]

When “jabber” is detected, bit 26.4 is set to “1” if bit 25.4 is also set to “1”. This bit is automatically cleared when read.

26.3 – False Carrier Interrupt Status[1]

When a false carrier is detected, bit 26.3 is set to “1” if bit 25.3 is also set to “1”. This bit is automatically cleared when read.

26.2 – Parallel-Detect Error Interrupt Status

When a Parallel-Detect error is detected, bit 26.2 is set to “1” if bit 25.2 is also set to “1”. This bit is automatically cleared when read.

26.1 – MASTER/SLAVE Resolution Error Interrupt Status[4]

When a MASTER/SLAVE resolution error is detected, bit 26.1 is set to “1” if bit 25.1 is also set to “1”. This bit is automatically cleared when read.

26.0 – RX_ER Interrupt Status

When an RX_ER condition occurs, bit 26.0 is set to “1”. This bit is automatically cleared when read.

[1]This bit applies only in 100BASE-TX and 1000BASE-T modes.

[2]Consistent with 10/100/1000BASE-T PHYs on the market today, this bit applies only when Auto-Negotiation is enabled; Auto MDI/MDI-X functionality is automatically disabled when Auto-Negotiation is disabled.

[3]This bit applies only in 10BASE-T mode.

[4]This bit applies only in 1000BASE-T mode.

17.28 Register 27 (1Bh) – Parallel LED Control Register

Register 27 (1Bh) – Parallel LED Control Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	Link10 LED Force On	R/W	1 = Link10 LED forced on 0 = Link10 LED not forced on	0
14	Link10 LED Disable	R/W, RS	1 = Disable Link10 LED 0 = Enable Link10 LED	0
13	Link100 LED Force On	R/W	1 = Link100 LED forced on 0 = Link100 LED not forced on	0
12	Link100 LED Disable	R/W, RS	1 = Disable Link100 LED 0 = Enable Link100 LED	0
11	Link1000 LED Force On	R/W	1 = Link1000 LED forced on 0 = Link1000 LED not forced on	0
10	Link1000 LED Disable	R/W, RS	1 = Disable Link1000 LED 0 = Enable Link1000 LED	0
9	Duplex LED Force On	R/W	1 = Duplex LED forced on 0 = Duplex LED not forced on	0
8	Duplex LED Disable	R/W, RS	1 = Disable Duplex LED 0 = Enable Duplex LED	0
7	Activity LED Force On	R/W	1 = Activity LED forced on 0 = Activity LED not forced on	0
6	Activity LED Disable	R/W, RS	1 = Disable Activity LED 0 = Enable Activity LED	0
5	Quality LED Force On	R/W	1 = Quality LED forced on 0 = Quality LED not forced on	0
4	Quality LED Disable	R/W, RS	1 = Disable Quality LED 0 = Enable Quality LED	0
3	LED Pulse Enable	R/W, RS	1 = Enable LED pulsing 0 = Disable LED pulsing	0
2	Link/Activity LED Blink Enable[1]	R/W, RS	1 = Enable Link/Acivity LED Blink 0 = Disable Link/Activity LED Blink	0
1	Link/Acitvity LED Blink Rate	R/W, RS	1 = 10Hz blink rate 0 = 5Hz blink rate	0
0	Reserved	RO		0

[1] This bit must be set only once after reset. If cleared after it is set, a reset of the part must be performed.

27.15 – Link10 LED Force On[1]

When bit 27.15 is set to “1”, the Link10 LED status bit is asserted.

27.14 – Link10 LED Disable

When bit 27.14 is set to “1”, the Link10 LED status bit is disabled.

27.13 – Link100 LED Force On[1]

When bit 27.13 is set to “1”, the Link100 LED status bit is asserted.

27.12 – Link100 LED Disable

When bit 27.12 is set to “1”, the Link100 LED status bit is disabled.

[1]This control bit has effect only if the corresponding LED status bit is enabled.

27.11 – Link1000 LED Force On[1]

When bit 27.11 is set to “1”, the Link1000 LED status bit is asserted.

27.10 – Link1000 LED Disable

When bit 27.10 is set to “1”, the Link1000 LED status bit is disabled.

27.9 – Duplex LED Force On[1]

When bit 27.9 is set to “1”, the Duplex LED is forced on.

27.8 – Duplex LED Disable

When bit 27.8 is set to “1”, the Duplex LED is disabled.

27.7 – Activity LED Force On[1]

When bit 27.7 is set to “1”, the Activity LED is forced on.

27.6 – Activity LED Disable

When bit 27.6 is set to “1”, the Activity LED is disabled.

27.5 – Quality LED Force On

When bit 27.5 is set to “1”, the Quality LED is forced on.

27.4 – Quality LED Disable

When bit 27.4 is set to “1”, the Quality LED is disabled.

27.3 – LED Pulse Enable

When bit 27.3 is set to “1”, the LED output signals are pulsed at 5KHz with a 20% duty cycle for low-power operation.

27.2 – Link/Acivity LED Blink Enable

When bit 27.2 is set to “1”, the Link/Activity LED blink function is enabled. In the blinking state the Link/Activity LED operates as follows:

The LED is constantly on when the link is up and data is NOT being transmitted or received.
The LED will blink at the rate specified by bit 27.1 when the link is up AND data is either being transmitted or received.

27.1 – Link/Acivity LED Blink Rate

Bit 27.1 specifies the Link/Activity LED blink rate when bit 27.2 is set to “1”.

0 = 5Hz blink rate
1 = 10Hz blink rate

27.0 – Reserved

[1]This control bit has effect only if the corresponding LED status bit is enabled.

17.29 Register 28 (1Ch) – Auxiliary Control & Status Register

Register 28 (1Ch) – Auxiliary Control & Status Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	Auto-Negotiation Complete	RO	1 = Auto-Negotiation complete 0 = Auto-Negotiation not complete	0
14	Auto-Negotiation Disabled	RO	1 = Auto-Negotiation was disabled 0 = Auto-Negotiation is enabled	0
13	MDI/MDI-X Crossover Indication	RO	1 = MDI/MDI-X crossover detected 0 = MDI/MDI-X crossover not detected	0
12	CD Pair Swap	RO	1 = CD pairs are swapped 0 = CD pairs are not swapped	0
11	A Polarity Inversion	RO	1 = Polarity swapped on pair A 0 = Polarity not swapped on pair A	0
10	B Polarity Inversion	RO	1 = Polarity swapped on pair B 0 = Polarity not swapped on pair B	0
9	C Polarity Inversion	RO	1 = Polarity swapped on pair C 0 = Polarity not swapped on pair C	0
8	D Polarity Inversion	RO	1 = Polarity swapped on pair D 0 = Polarity not swapped on pair D	0
7:6	Reserved	RO		00
5	Duplex Status	RO	1 = FDX 0 = HDX	0
4:3	Speed Status	RO	00 = Speed is 10BASE-T 01 = Speed is 100BASE-TX 10 = Speed is 1000BASE-T 11 = Reserved	00
2	Mode/Duplex Pin Priority Select	R/W, RS	1 = SMI registers have priority over MODE, FRC_DPLX, and ANEG_DIS pins. 0 = MODE, FRC_DPLX, and ANEG_DIS pins have priority over SMI register settings, *unless* ANEG_DIS = 0.	0
1	Reset Control	R/W, RS	0 = MII issued reset will reset the “Reset-Sticky” bits to their default values 1 = CIS8201 MII issued reset will not reset the “Reset-Sticky” bits to their default values	0
0	Reserved	RO		00

28.15 – Auto-Negotiation Complete

This bit is a copy of bit 1.5, duplicated here for convenience.

28.14 – Auto-Negotiation Disabled

When bit 28.14 is read as a “1”, this bit indicates that the Auto-Negotiation process has been bypassed. This happens only when Register bit 0.12 is set to “0”.

28.13 – MDI/MDI-X Crossover Indication

When bit 28.13 returns a “1”, the Auto-Negotiation state machine has determined that crossover does not exist in the signal path. The crossover will therefore be performed internally to the PHY, as described by the MDI/MDI-X crossover specification.[1]

28.12 – CD Pair Swap[2]

[1]This bit is valid only after descrambler lock has been achieved.

[2]This bit is valid only in 1000BASE-T mode.

When bit 28.12 returns a “1”, the PHY has determined that subchannel cable pairs C and D have been swapped between the far-end transmitted and the receiver. When bit 28.12 returns a “1”, the PHY internally swaps pairs C and D (as long as bit 18.5 is set to “0”).[1]

28.11 – A Polarity Inversion

When bit 28.11 returns a “1”, the PHY has determined that the polarity of subchannel cable pair A has been inverted between the far-end transmitter and the near-end receiver. When bit 28.11 returns a “1”, the PHY internally corrects the pair inversion (as long as bit 18.4 is set to “0”). Polarity-inversion correction runs in all three modes; as a result, the state of 28.11 is valid only when bit 1.5 is set to “1”.

28.10 – B Polarity Inversion

When bit 28.10 returns a “1”, the PHY has determined that the polarity of subchannel cable pair B has been inverted between the far-end transmitter and the near-end receiver. When bit 28.10 returns a “1”, the PHY internally corrects the pair inversion (as long as bit 18.4 is set to “0”). Polarity-inversion correction runs in all three modes; as a result, the state of 28.10 is valid only when bit 1.5 is set to “1”.

28.9 – C Polarity Inversion[1]

When bit 28.9 returns a “1”, the PHY has determined that the polarity of subchannel cable pair C has been inverted between the far-end transmitter and the near-end receiver. When bit 28.9 returns a “1”, the PHY internally corrects the pair inversion (as long as bit 18.4 is set to “0”). Polarity-inversion correction runs in all three modes; as a result, the state of 28.9 is valid only when bit 1.5 is set to “1”.

28.8 – D Polarity Inversion[1]

When bit 28.8 returns a “1”, the PHY has determined that the polarity of subchannel cable pair D has been inverted between the far-end transmitter and the near-end receiver. When bit 28.8 returns a “1”, the PHY internally corrects the pair inversion (as long as bit 18.4 is set to “0”). Polarity-inversion correction runs in all three modes; as a result, the state of 28.8 is valid only when bit 1.5 is set to “1”.

28.7:6, 28.0 – Reserved

28.5 – Duplex Status

Bit 28.5 indicates the actual FDX/HDX operating mode of the PHY.

28.4:3 – Speed Status

Bits 27.4:3 indicate the actual operating speed of the PHY.

28.2 – Mode/Duplex Pin Priority Select

Bit 28.2 determines whether the configuration control pins (MODE10/100/1000, FRC_DPLX, and ANEG_DIS) have priority over the MII register settings in determining the operating characteristics of the PHY. If bit 28.2 is a “0” (default value), then the configuration control pins have priority over any MII register settings, *unless* all the configuration control pins are tied to an all “ones” high state, as shown in Table 17-7. If bit 28.2 is a “1”, then the MII register settings take precedence over the operating mode specified by the state of the configuration control pins.

28.1 – Reset Control

Bit 28.1 controls whether or not the “Reset-Sticky” (RS) bits are reset (Register bit 28.1 = “1”) to their default values, or remain in their current state (Register bit 28.1 = “0”) when a MII (soft) reset is issued.

[1]This bit applies ony in 1000BASE-T mode.

Table 17-7. Configuration Control Pin Settings

ANEG_DIS	FRC_DPLX	MODE10	MODE100	MODE1000	Advertised Operating Mode(s)	
					Speed	Duplex
0	X	0	0	0	None	None
	0	0	0	1	1000BASE-T	Half
	0	0	1	0	100BASE-TX	
	0	0	1	1	100BASE-TX 1000BASE-T	
	0	1	0	0	10BASE-T	
	0	1	0	1	10BASE-T 1000BASE-T	
	0	1	1	0	10BASE-T 100BASE-TX	
	0	1	1	1	All	
	1	0	0	1	1000BASE-T	Full/Half
	1	0	1	0	100BASE-TX	
	1	0	1	1	100BASE-TX 1000BASE-T	
	1	1	0	0	10BASE-T	
	1	1	0	1	10BASE-T 1000BASE-T	
	1	1	1	0	10BASE-T 100BASE-TX	
	1	1	1	1	All	
ANEG_DIS	**FRC_DPLX**	**MODE10**	**MODE100**	**MODE1000**	**Forced Operating Mode**	
					Speed	**Duplex**
1	X	0	0	0	None	None
	0	X	X	1	1000BASE-T	Half
	0	X	1	0	100BASE-TX	
	0	1	0	0	10BASE-T	
	1	X	X	1	1000BASE-T	Full
	1	X	1	0	100BASE-TX	
	1	1	0	0	10BASE-T	
1	1	1	1	1	Specified by MII register bits	

Using the MODE, FRC_DPLX, and ANEG_DIS pins as described above does *not* change the state of the PHY's MII capability register bits (e.g., MII Registers 0, 1, 4, and 9). As specified by MII Registers 0,1, 4, and 9, when bit 28.2 is set to "0", the MODE, FRC_DPLX, and ANEG_DIS pins effectively override the PHY's operating capabilities for use in any subsequent Auto-Negotiation or Parallel-Detect process:

- link speed: 10/100/1000, and
- duplex: full or half.

If the MII register settings are desired to take precedence over the configuration control pins, then bit 28.2 must be written to a "1" after a hardware or software reset is completed, or the configuration control pins can all be tied to an all "ones" high state.

17.30 Register 29 (1Dh) – Delay Skew Status Register

Register 29 (1Dh) – Delay Skew Status Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	Reserved	RO		0
14:12	Pair A Delay Skew	RO	Skew in integral symbol times	000
11	Reserved	RO		0
10:8	Pair B Delay Skew	RO	Skew in integral symbol times	000
7	Reserved	RO		0
6:4	Pair C Delay Skew	RO	Skew in integral symbol times	000
3	Reserved	RO		0
2:0	Pair D Delay Skew	RO	Skew in integral symbol times	000

29.15, 29.11, 29.7, 29.3 – Reserved

29.14:12 – Pair A Delay Skew[1]

Bits 29.14:12 indicate the additional delay (measured in integral symbol times) added internally at the pair A receiver input to align received symbols at pair A with the received symbols at the other three pairs.

29.10:8 – Pair B Delay Skew[1]

Bits 29.10:8 indicate the additional delay (measured in integral symbol times) added internally at the pair B receiver input to align received symbols at pair B with the received symbols at the other three pairs.

29.6:4 – Pair C Delay Skew[1]

Bits 29.6:4 indicate the additional delay (measured in integral symbol times) added internally at the pair C receiver input to align received symbols at pair C with the received symbols at the other three pairs.

29.2:0 – Pair D Delay Skew[1]

Bits 29.2:0 indicate the additional delay (measured in integral symbol times) added internally at the pair D receiver input to align received symbols at pair D with the received symbols at the other three pairs.

[1]This value is valid only in 1000BASE-T mode.

17.31 Register 30 (1Eh) – Reserved Register

Register 30 (1Eh) – Reserved Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15:0	Reserved	RO		00000000 00000000

30.15:0 – Reserved

17.32 Register 31 (1Fh) – Reserved Register

Register 31 (1Fh) – Reserved Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15:0	Reserved	RO		00000000 00000000

31.15:0 – Reserved

18 Electrical Specification

18.1 Absolute Maximum Ratings

Temporary or prolonged operating conditions beyond those listed below may result in device failure and/or compromise long-term device reliability.

Table 18-1. Absolute Maximum Ratings

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{Storage}$	-65		150	°C	Storage temperature range.
T_J			+125ºC	ºC	Absolute maximum junction temperature
T_A	0ºC		+70ºC	ºC	Ambient free-air operating temperature
$V_{DD(Analog)}$	-0.5		4.0	V	DC voltage on analog I/O supply pin.
$V_{DD(IO)}$	-0.5		4.0	V	DC voltage on any digital I/O supply pin.
$V_{DD(5V)}$	-0.5		5.5	V	DC voltage on any 5V-tolerant digital input pin.
$V_{DD(Dig-Core)}$	-0.5		1.8	V	DC voltage on any digital core supply pin.
$V_{DD(Analog-Core)}$	-0.5		1.8	V	DC voltage on any analog core supply pin.
$V_{Pin(DC)}$	-0.5		V_{DD} + 0.5	V	DC voltage on any non-supply pin.
$V_{ESD(HBM)}$	2			kV	ESD voltage on any pin, per event, according to the Human Body Model.[1]
$V_{ESD(MM)}$	200			V	ESD voltage on any pin, per event, according to the Machine Model.
CESD	4			kV	Cable-sourced ESD tolerance, per event, at 100 meters.
$I_{LATCHUP}$	-200		+200	mA	T = +85°C, valid for all I/O signal pins.

[1] 1.4kV for Twisted Pair Interface Pins (TPI) of the LQFP package only.

18.2 Recommended Operating Conditions

Table 18-2. Recommended Operating Conditions

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$VDDIO_{G,T,M}$	3.0	3.3	3.6	V	Digital I/O DC power supply voltage (GMII, TBI, and MII modes).
$VDDIO_{RGMII}$	2.3	2.5	2.7	V	Optional digital I/O DC power supply voltage (RGMII, RTBI modes only).[1]
VDDDIG	1.43	1.5	1.58	V	Digital core 1.5V DC power supply voltage.[2]
VDDPLL33 TXVDD VDDREC33 VREFP[3]	3.0	3.3	3.6	V	Analog 3.3V DC power supply voltage.
VDDPLL15 VDDREC15	1.43	1.5	1.58	V	Analog core 1.5V DC power supply voltage.[2]
F_{REFCLK}	25	N/A	125	MHz	Local reference clock (REFCLK) nominal frequency.
$F_{TOL\ (REFCLK)}$	-50		+50	ppm	Reference clock frequency offset tolerance over specified temperature range (25MHz or 125MHz).
$F_{Crystal}$		25		MHz	Crystal parallel resonant frequency.
$F_{TOL\ (Crystal)}$	-50		+50	ppm	Crystal parallel resonant frequency offset tolerance.
$F_{TOL\ (LINK)}$	-1500		+1500	ppm	Link partner frequency offset tolerance (for any link speed).
R_{EXT}		2.26		kΩ	External reference circuit bias resistor (1% tolerance).
C_{REF_FILT}		1.0		µF	External reference generator filter capacitor (10% tolerance).
N		1:1			Transformer nominal turns ratio (primary : secondary).

[1] RGMII may also be used with a 3.3V I/O supply.

[2] The 1.5V VDDDIG, VDDPLL15, and VDDREC15 supplies can either be provided from a fixed supply or, for single 3.3V supply designs, can be optionally regulated from a fixed 3.3V supply by an on-chip regulator control circuit and an external power FET. See Figures 10-2 and 10-3.

[3] VREFP provides the primary analog voltage reference. Careful attention to the PCB layout for this supply pin must be observed in order to avoid any bus drops, which would cause inaccuracy in the voltage reference generator. Separate traces for VREFP and VREFN to the 3.3V power regulator output and ground, respectively, are recommended. See Applications Note “CIS8201 Design and Layout Guidelines” for more information.

18.3 Thermal Application Data

Table 18-3. Thermal Application Data

Printed Circuit Board Conditions (JEDEC JESD51-9)				128-pin LQFP	100-ball LBGA
PCB Layers				6	4
PCB Dimensions (mm x mm)				7602 x 114.3	101.6 x 114.3
PCB Thickness (mm)				1.6	1.6
Environment Conditions					
Maximum operation junction temperature (ºC)				125	125
Ambient free-air operating temperature (ºC)				70	70
Worst Case Power Dissipation (W)				1.3	1.3
Symbol	**128-pin LQFP**	**100-ball LBGA**	**Unit**	**Parameter Description & Conditions**	
θ_{JA} (0 m/s airflow)	38.2	34.9	ºC/W	Junction-to-ambient thermal resistance	
θ_{JA} (1 m/s airflow)	37.1	30.1	ºC/W	Junction-to-ambient thermal resistance	
θ_{JA} (2 m/s airflow)	35.4	28.8	ºC/W	Junction-to-ambient thermal resistance	

18.4 Thermal Specifications

Table 18-4. Thermal Specifications - 128 pin LQFP

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
T_A	0		70	°C	Ambient free-air operating temperature
T_J			125	°C	Maximum operating junction temperature
θ_{JC}		14.4		°C/W	Junction-to-case thermal resistance
Ψ_{JT}		1.38		°C/W	Junction-to-top center of case thermal resistance

Table 18-5. Thermal Specifications - 100 ball LBGA

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
T_A	0		70	°C	Ambient free-air operating temperature
T_J			125	°C	Maximum operating junction temperature
θ_{JC}		21.8		°C/W	Junction-to-case thermal resistance
θ_{JB}		14.6		ºC/W	Junction-to-board thermal resistance

18.5 Current and Power Consumption - Application Scenarios

Operating Conditions, VDDPLL33/TXVDD/VDDREC33/VREFP = 3.3V, VDDIO = 2.5V, VDDDIG/VDDPLL15/VDDREC15 = 1.5V, T_A = 25ºC, 1000BASE-T RGMII 64 Byte Random data, No LED's, CLK125out disabled.

Table 18-6. Current and Power Consumption - Application I

Symbol	Min	Typ	Max[1]	Unit	Parameter Description & Conditions
I_{VDDIO}		19	28	mA	Total 2.5V digital I/O supply current
I_{VDDDIG}		340	411	mA	Total 1.5V digital core supply current
$I_{VDDPLL33} + I_{TXVDD} + I_{VDDREC33} + I_{VREFP}$		109	122	mA	Total analog 3.3V supply current
$I_{VDDPLL15} + I_{VDDREC15}$		41	51	mA	Total analog 1.5V supply current
P_D		980	1166	mW	Total power dissipation

Operating Conditions, VDDPLL33/TXVDD/VDDREC33/VREFP = 3.3V, VDDIO = 2.5V, VDDDIG/VDDPLL15/VDDREC15 = 1.50V, T_A = 25ºC, 1000BASE-T GMII 64 Byte Random data, 4 LED's, CLK125out enabled.

Table 18-7. Current and Power Consumption - Application II

Symbol	Min	Typ	Max[1]	Unit	Parameter Description & Conditions
I_{VDDIO}		34	43	mA	Total 2.5V digital I/O supply current
I_{VDDDIG}		340	411	mA	Total 1.5V digital core supply current
$I_{VDDPLL} + I_{TXVDD} + I_{VDDREC33} + I_{VREFP}$		116	131	mA	Total analog 3.3V supply current
$I_{VDDPLL15} + I_{VDDREC15}$		41	51	mA	Total analog 1.5V supply current
$P_{D(VDDIO)}$		1039	1233	mW	Total digital I/O power dissipation

Operating Conditions, VDDPLL33/TXVDD/VDDREC33/VREFP/VDDIO = 3.3V, VDDDIG/VDDPLL15/VDDREC15 = 1.5V, T_A = 25ºC, 1000BASE-T GMII 64 Byte Random data, No LED's, CLK125out disabled.

Table 18-8. Current and Power Consumption - Application III

Symbol	Min	Typ	Max[1]	Unit	Parameter Description & Conditions
I_{VDDIO}		25	30	mA	Total 3.3V digital I/O supply current
I_{VDDDIG}		340	411	mA	Total 1.5V digital core supply current
$I_{VDDPLL} + I_{TXVDD} + I_{VDDREC33} + I_{VREFP}$		109	122	mA	Total analog 3.3V supply current
$I_{VDDPLL15} + I_{VDDREC15}$		41	51	mA	Total analog 1.5V supply current
$P_{D(VDDIO)}$		1014	1195	mW	Total power dissipation

[1] Max ratings at TA = 70ºC and supplies at +10%

Operating Conditions, VDDPLL33/TXVDD/VDDREC33/VREFP/VDDIO = 3.3V, VDDDIG/VDDPLL15/VDDREC15 = 1.5V, T_A = 25ºC, 1000BASE-T GMII 64 Byte Random data, 4 LED's, CLK125 enabled.

Table 18-9. Current and Power Consumption - Application IV

Symbol	Min	Typ	Max[1]	Unit	Parameter Description & Conditions
I_{VDDIO}		50	62	mA	Total 3.3V digital I/O supply current
I_{VDDDIG}		340	411	mA	Total 1.5V digital core supply current
$I_{VDDPLL} + I_{TXVDD} + I_{VDDREC33} + I_{VREFP}$		116	131	mA	Total analog 3.3V supply current
$I_{VDDPLL15} + I_{VDDREC15}$		41	51	mA	Total analog 1.5V supply current
$P_{D(VDDIO)}$		1119	1330	mW	Total power dissipation

[1] Max ratings at TA = 70ºC and supplies at +10%

18.6 Crystal Specifications

The following component specifications should be used to select a crystal for use with the CIS8201.

Table 18-10. Crystal Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
F_{REF}		25		MHz	Fundamental mode, AT-cut type, parallel resonant crystal reference frequency.
$F_{STABILITY}$	-50		+50	ppm	Fundamental mode, AT-cut type, parallel resonant crystal frequency stability.
F_{OFFSET}	-30		+30	ppm	Fundamental mode, AT-cut type, parallel resonant crystal frequency offset.
C_L	18		20	pF	Crystal load capacitance.
C_{L-EXT}		33		pF	Crystal external load capacitors.
ESR		10	30	Ω	Equivalent Series Resistance of crystal.
P_D			0.5	mW	Crystal drive level.

A suitable crystal for use with the CIS8201 is:

- Fox Electronics, HC49S 250F-20.

18.7 Regulator Specifications

The following component specifications should be used to select a regulator FET device for use with the CIS8201.

Table 18-11. Regulator Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
V_T			1	V	Threshold voltage.

A suitable regulator FET device for use with the CIS8201 is:

- Fairchild FDT439N.

See Figure 10-3: "Power Supply Connections for a 3.3V I/O Application with a Single 3.3V Supply and Optional Fixed 1.5V Regulator" for more information.

19 DC Specifications (T_A = 0°C - 70°C)

19.1 Digital Pins

Table 19-1. Digital Pins Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$V_{OH(3.3)}$	2.4		VDDIO + 0.3	V	High Level OUtput High Voltage VDDIO = min, I_{OH} = -1.5mA, for $VDDIO_{(nom)}$= 3.3V
$V_{OH(2.5)}$	2.0		VDDIO + 0.3	V	High Level OUtput High Voltage VDDIO = min, I_{OH} = -1.0mA, for $VDDIO_{(nom)}$= 2.5V
V_{OL}	GND		0.5	V	Output Low Level Output Voltage
$V_{IH(3.3)}$	2.0			V	High Level Input Voltage, for $VDDIO_{(nom)}$= 3.3V
$V_{IH(2.5)}$	1.7			V	High Level Input Voltage, for $VDDIO_{(nom)}$= 2.5V
$V_{IL(3.3)}$			0.8	V	Low Level Input Voltage, for $VDDIO_{(nom)}$= 3.3V
$V_{IL(2.5)}$			0.7	V	Low Level Input Voltage, for $VDDIO_{(nom)}$= 2.5V
I_{Leak}	-10		10	µA	Input Leakage Current
V_{OLeak}	-10		10	µA	Output Leakage Current.

19.2 Twisted Pair Interface Pins

Table 19-2. TPI Transmitter DC Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$V_{OUT\text{-}DIFF}$ TX-10M	2.2		2.8	V	10Mb differential peak transmit output voltage.
$V_{OUT\text{-}DIFF}$ TX-100M	.95		1.05	V	100Mb differential peak transmit output voltage at nominal supply.
$V_{OUT\text{-}DIFF}$ TX-1000M	.95		1.09	V	1000Mb differential peak transmit output voltage at nominal supply.

20 AC Timing Specifications

20.1 GMII Mode Transmit Timing (1000BASE-T)

For GMII mode, the following specifications are valid only when the I/O power supply (VDDIO) is 3.0-3.6V, and the MAC I/F selection bits have been set to GMII mode. See MII Register 23 for more information.

Table 20-1. GMII Mode Transmit AC Timing Specifications (1000BASE-T)

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{GTX\_CLK-Period}$		8.0		ns	GTX_CLK clock period.
$F_{TOL-GTX\_CLK}$	-100		+100	ppm	GTX_CLK frequency offset tolerance.
$T_{GTX\_CLK-High}$	2.5			ns	GTX_CLK minimum pulse width high.
$T_{GTX\_CLK-Low}$	2.5			ns	GTX_CLK minimum pulse width low.
$T_{GTX\_CLK-Setup}$	2.5[1]			ns	GMII data TXD[7:0], TX_ER, TX_EN setup time.
$T_{GTX\_CLK-Hold}$	0.5[2]			ns	GMII data TXD[7:0], TX_ER, TX_EN hold time.
t_R			1.0	ns	GTX_CLK clock rise time, measured from 0.7V to 1.9V.
t_F			1.0	ns	GTX_CLK clock fall time, measured from 0.7V to 1.9V.

[1] This does not comply with the minimum setup time requirement of 2.0ns as specified in the IEEE802.3 GMII AC timing specifications.
[2] This does not comply with the minimum hold time requirement of 0.0ns as specified in the IEEE802.3 GMII AC timing specifications.

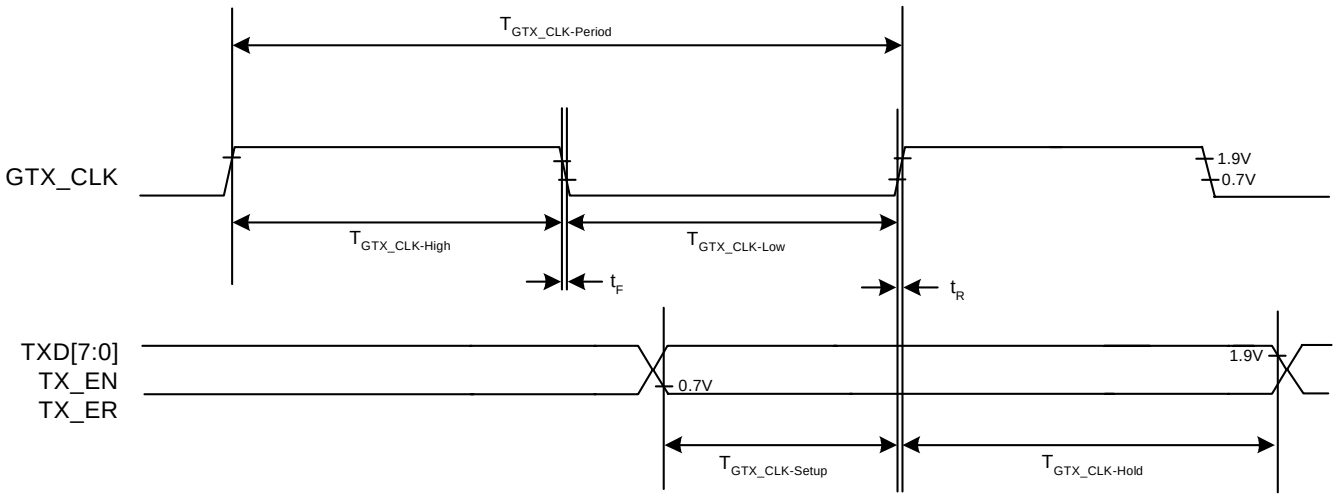


Figure 20-1. GMII Transmit AC Timing in 1000BASE-T Mode

20.2 GMII Mode Receive Timing (1000BASE-T)

For GMII mode, the following specifications are valid only when the I/O power supply (VDDIO) is 3.0-3.6V, and the MAC I/F selection bits have been set to GMII mode. See MII Register 23 for more information.

Table 20-2. GMII Mode Receive AC Timing Specifications (1000BASE-T)

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{RX\_CLK\text{-}Period}$		8.0		ns	RX_CLK clock period.
$F_{TOL\text{-}RX\_CLK}$	-100		+100	ppm	RX_CLK frequency offset tolerance.
$T_{RX\_CLK\text{-}High}$	2.5			ns	RX_CLK minimum pulse width high.
$T_{RX\_CLK\text{-}Low}$	2.5			ns	RX_CLK minimum pulse width low.
$T_{RX\_CLK\text{-}Setup}$	1.75[1]			ns	RXD[7:0], RX_DV, RX_ER setup time to RX_CLK
$T_{RX\_CLK\text{-}Hold}$	0.5			ns	RXD[7:0], RX_DV, RX_ER hold time to RX_CLK
t_R			1.0	ns	RX_CLK clock rise time, measured from 0.7V to 1.9V.
t_F			1.0	ns	RX_CLK clock fall time, measured from 0.7V to 1.9V.

[1] This does not comply with the minimum setup time requirement of 2.5ns as specified in the IEEE802.3 GMII AC timing specifications.

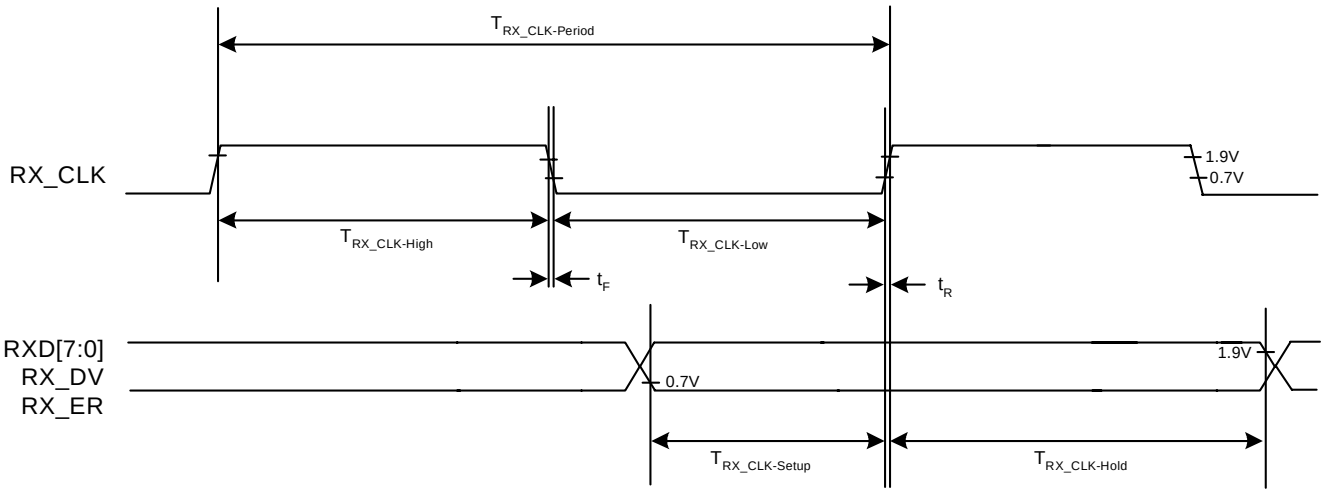


Figure 20-2. GMII Receive AC Timing in 1000BASE-T Mode

20.3 MII Transmit Timing (100Mb/s)

The following specifications are valid only when the I/O power supply (VDDIO) is 3.0-3.6V, and the MAC I/F selection bits have been set to GMII/MII mode. See MII Register 23 for more information.

Table 20-3. MII Transmit AC Timing Specifications (100Mb/s)

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{TX\_CLK-Delay}$	0		25	ns	Delay from TX_CLK to TXD[3:0], TX_EN, TX_ER.
$T_{TX\_CLK-Duty}$	35		65	%	TX_CLK duty cycle.

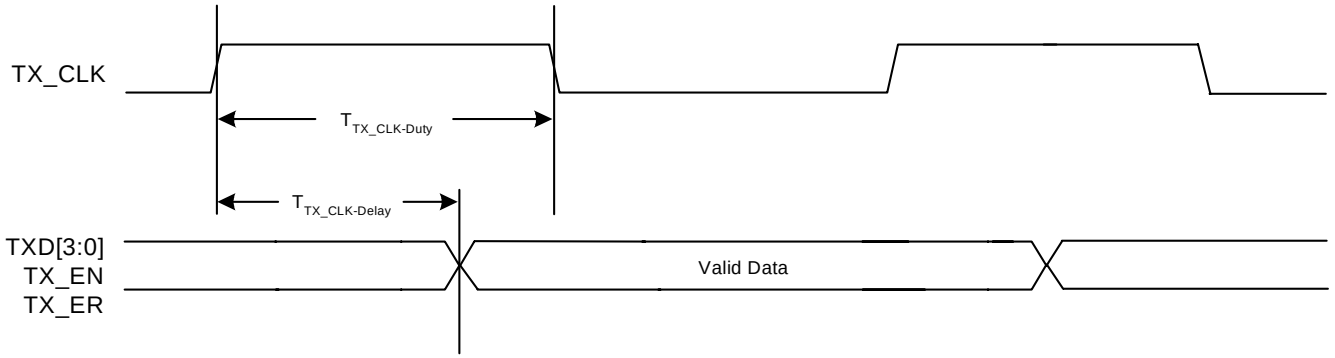


Figure 20-3. MII Transmit AC Timing (100Mb/s)

20.4 MII Receive Timing (100Mb/s)

The following specifications are valid only when the I/O power supply (VDDIO) is 3.0-3.6V, and the MAC I/F selection bits have been set to GMII/MII mode. See MII Register 23 for more information.

Table 20-4. MII Receive AC Timing Specifications (100Mb/s)

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{RX\_CLK-Setup}$	10			ns	RXD[3:0], RX_DV, RX_ER setup time to TX_CLK.
$T_{RX\_CLK-Hold}$	10			ns	RXD[3:0], RX_DV, RX_ER hold time to RX_CLK.

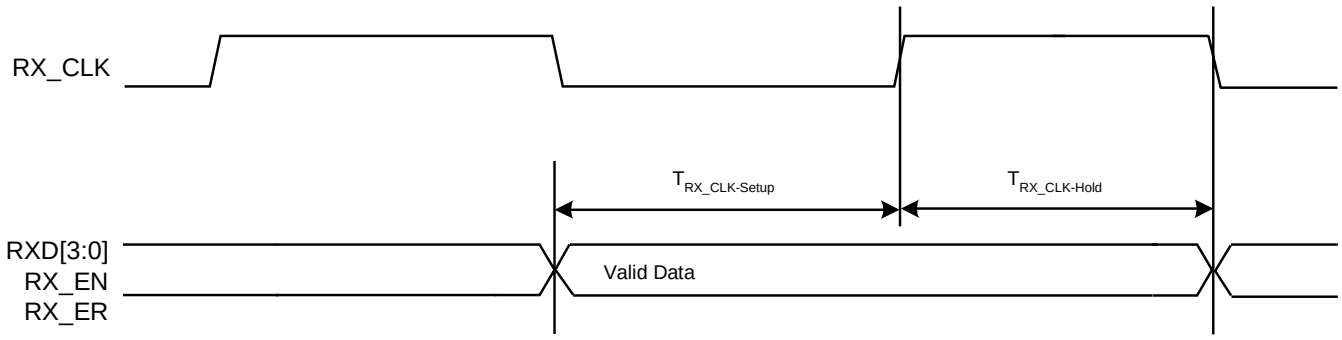


Figure 20-4. MII Receive AC Timing (100Mb/s)

20.5 100BASE-TX Transmit Packet Deassertion Timing

The following specifications are valid only when the I/O power supply (VDDIO) is 3.0-3.6V, and the MAC I/F selection bits have been set to GMII/MII mode. See MII Register 23 for more information.

Table 20-5. 100BASE-TX Transmit Packet Deassertion AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{TPI\_A\text{-}Delay}$		11		bits	TX_CLK to TPI transmit channel "A" idling time.[1]

[1] For symbol mode, because TX_EN has no meaning, deassertion is measured from the first rising edge of TX_CLK occurring after the deassertion of a data nibble on the transmit MII to the last bit (LSB) of that nibble when it deasserts on the wire. 1 bit time = 10ns in 100Mb/s mode.

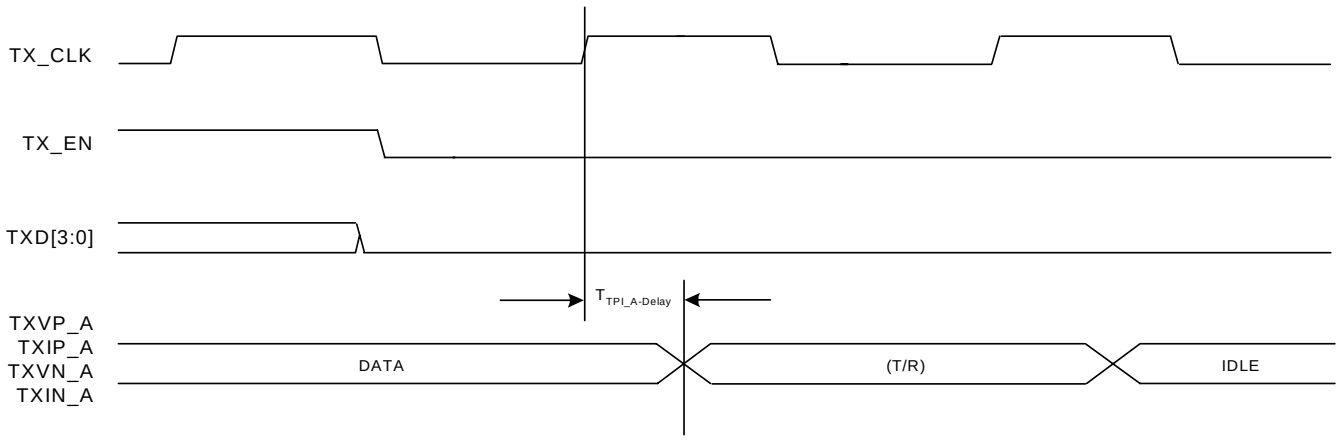


Figure 20-5. 100BASE-TX Transmit Packet Deassertion AC Timing

20.6 100BASE-TX Transmit Timing ($t_{R/F}$ & Jitter)

The following specifications are valid only when the I/O power supply (VDDIO) is 3.0-3.6V, and the MAC I/F selection bits have been set to GMII/MII mode. See MII Register 23 for more information.

Table 20-6. 100BASE-TX Transmit AC Timing Specifications ($t_{R/F}$ & Jitter)

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
t_R, t_F	3	4	5	ns	TPI transmit channel “A” rise and fall times taken at 10% and 90% of the +1 or -1 amplitude.
$t_{Mismatch}$		500		ps	Difference between the maximum and minimum of all rise and fall times of TPI transmit channel “A”.
J_{TPI_A}			1.4	ns	TPI transmit channel “A” jitter.

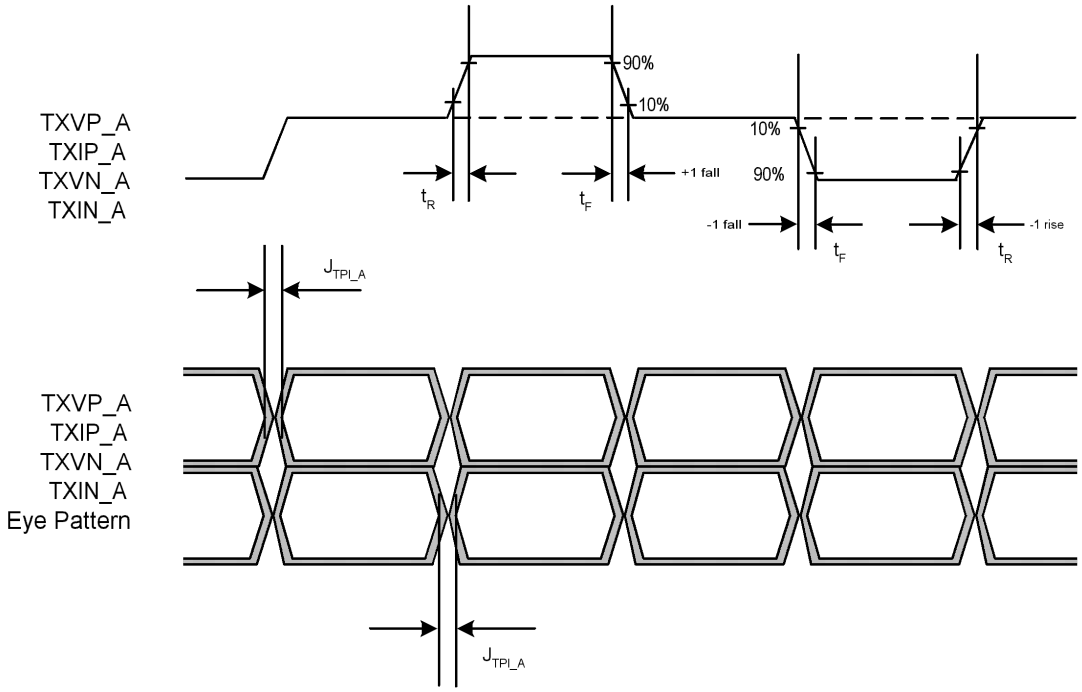


Figure 20-6. 100BASE-TX Transmit AC Timing ($t_{R/F}$ & Jitter)

20.7 100BASE-TX Receive Packet Latency Timing

The following specifications are valid only when the I/O power supply (VDDIO) is 3.0-3.6V, and the MAC I/F selection bits have been set to GMII/MII mode. See MII Register 23 for more information.

Table 20-7. 100BASE-TX Receive Packet Latency AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{CRS\_ON-Delay}$ [1]		19		bits[2]	Carrier Sense ON delay.
$T_{RXD-Delay}$		24		bits	Receive data latency.

[1] In 100BASE-TX half-duplex mode using RGMII interface, the total PHY latency (MDI to CRS) is between 65 to 68 bit times. The collision domain of a particular worst case scenario where two DTEs are linked to each other via two Class 11 repeaters (3 hops), is measured to be 305m, which exceeds the 205m diameter requirement specified in the IEEE 802.3 standard; therefore this issue is not likely to have an impact in 100BASE-T half-duplex mode when using the RGMII interface.

[2] 1 bit time = 10ns in 100Mb/s mode.

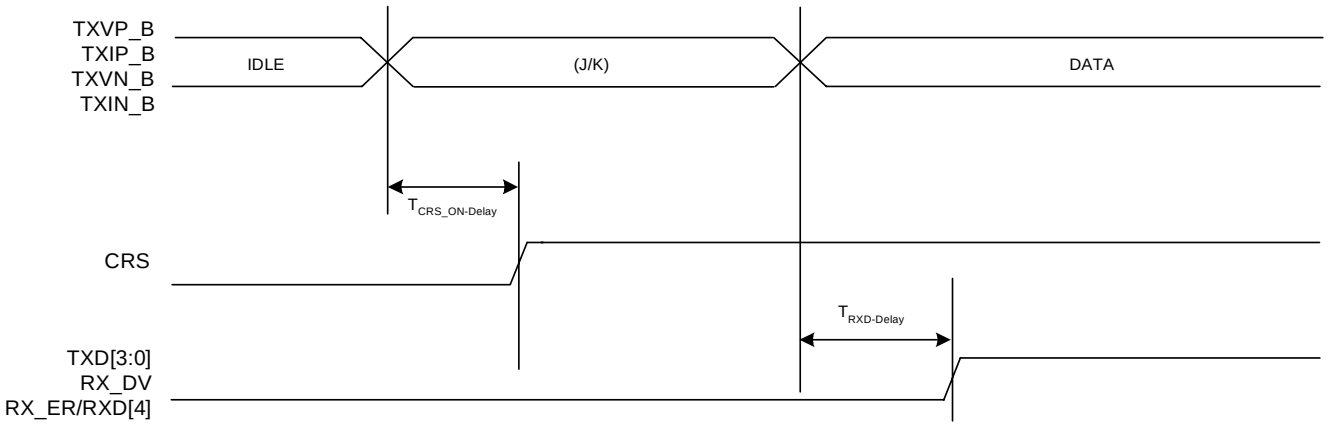


Figure 20-7. 100BASE-TX Receive Packet Latency AC Timing

20.8 100BASE-TX Receive Packet Deassertion Timing

The following specifications are valid only when the I/O power supply (VDDIO) is 3.0-3.6V, and the MAC I/F selection bits have been set to GMII/MII mode. See MII Register 23 for more information.

Table 20-8. 100BASE-TX Receive Packet Deassertion AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{CRS\_OFF\text{-}Delay}$		23		bits[1]	Carrier Sense OFF delay.

[1] 1 bit time = 10ns in 100Mb/s mode.

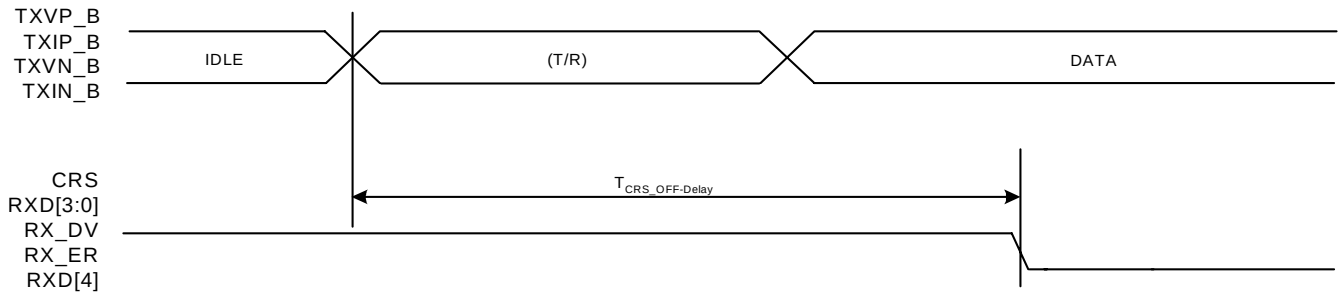


Figure 20-8. 100BASE-TX Receive Packet Deassertion AC Timing

20.9 RGMII/RTBI Mode Timing [1, 2]

The CIS8201 is a RGMII-ID[3] device, i.e. it provides the user an option to operate with or without an internal delay on the RXC and TXC clocks. The internal delays on the RXC and TXC clocks can be turned on by setting MII Register bit 23.8. This mode of operation is called “RGMII-compensated mode”. The default mode of operation is “RGMII-uncompensated mode”.

20.9.1 RGMII/RTBI-Uncompensated Mode Timing

For RGMII/RTBI-uncompensated mode, the following specifications are valid only when the I/O power supply (VDDIO) is 2.5V, ±5%, per the RGMII specification, the MAC I/F selection bits have been set to RGMII mode and MII Register bit 23.8 is set to 0. See MII Register 23 and the RGMII specification for more information. All timing specifications are referenced to a switching threshold of 1.25V (i.e., 50% of VDDIO = 2.5V).

Table 20-9A. RGMII/RTBI-Uncompensated Mode AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{skew}T$	-500	0	500	ps	Data to clock output skew (at PHY) – uncompensated mode.
$T_{skew}R$	1.0	1.8	2.6	ns	Data to clock input skew (at PHY) – uncompensated mode.[1]
T_{CYC}	7.2	8.0	8.8	ns	Clock cycle duration.[2]
Duty_G	45	50	55	%	Duty cycle for 1000BASE-T.[3]
Duty_T	40	50	60	%	Duty cycle for 10BASE-T and 100BASE-TX.[3]
T_R, T_F			0.75	ns	Rise, fall time (20% to 80%).

[1] This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns and less than 2.0ns will be added to the associated clock signal. This is normal operating mode (RGMII timing is *not* compensated). To enable RGMII timing compensation, see MII Register bit 23.8.

[2] For 10Mbps and 100Mbps, T_{CYC} will scale to 400ns (±40ns), and 40ns (±4ns), respectively.

[3] Duty cycle may be stretched or shrunk during speed changes or while transitioning to a received packet’s clock domain, as long as the minimum duty cycle is not violated, and stretching occurs for no more than three T_{CYC} of the lowest speed transitioned between.

[1]The RGMII interface is timing compatible with the v1.3 and v2.0 specifications. The RGMII interface is not electrically compatible with the v2.0 specifications as this requires HSTL voltage levels which the CIS8201 does not support. RGMII mode may also be used with a 3.3V I/O supply.

[2]See AN007 “PCB Design and Layout Guidelines for RGMII Interface on CIS8204 - Application Note”.

[3]For definition of RGMII-ID refer to v2.0 of RGMII specifications.

Figure 20-9A diagrams RGMII/RTBI timing and multiplexing in uncompensated mode.

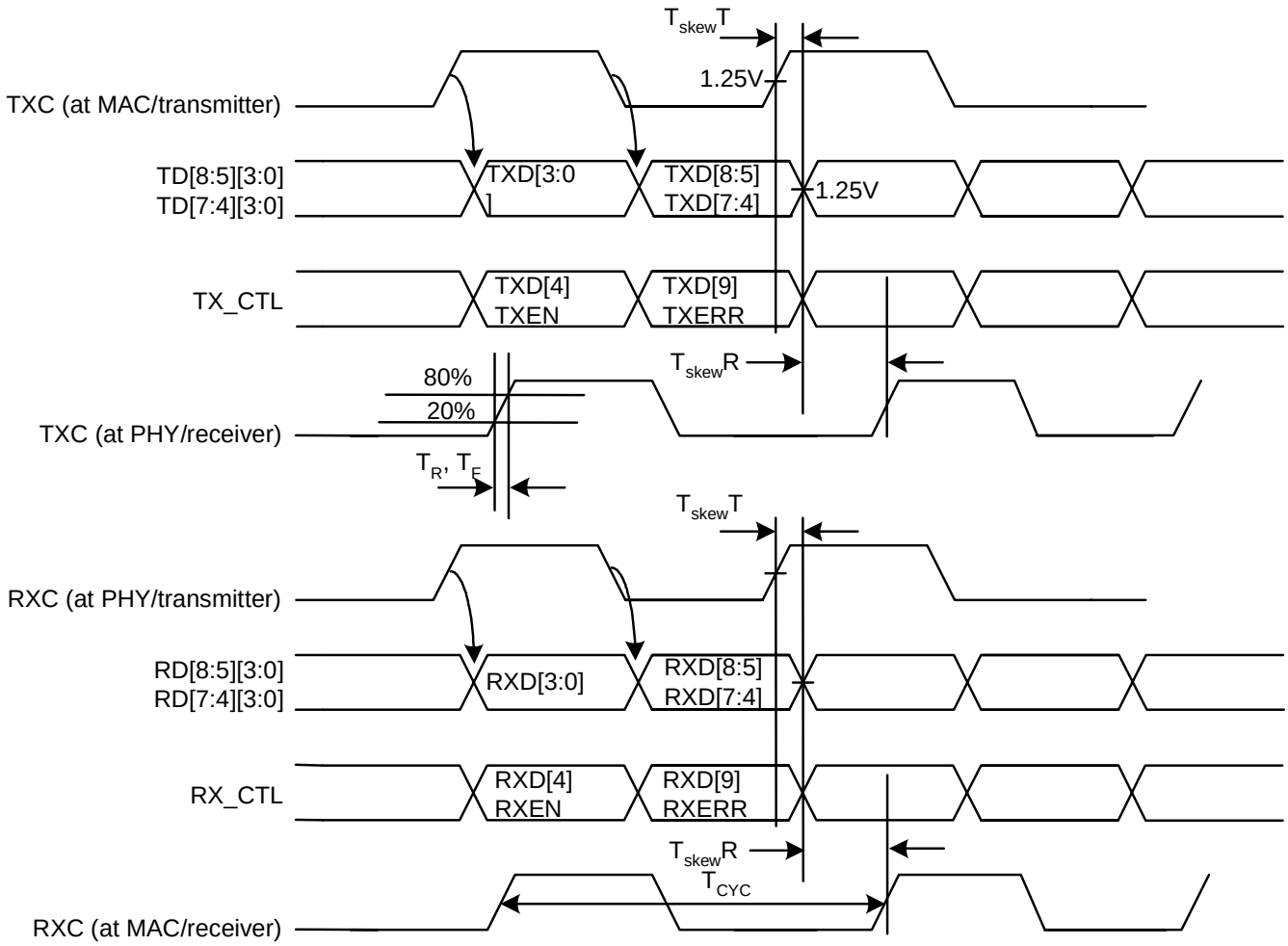


Figure 20-9A. RGMII/RTBI Uncompensated AC Timing and Multiplexing

The RGMII specification (v1.3) defines that the clock and data are coincident at the source, i.e. the TXC/TXD are coincident coming out of the MAC and the RXC/RXD are coincident coming out of the PHY.

Therefore, to meet this timing specification, a 1.5ns delay to the TXC and RXC signals is typically added on the PC board using a long “trombone shaped” trace.

20.9.2 RGMII/RTBI-Compensated Mode Timing

While the CIS8201’s default RGMII operation mode conforms to the RGMII v1.3 specification, the device also includes an optional mode of operation where the addition of the delay on RXC and TXC is handled internally to the CIS8201. This operation mode can be enabled by setting MII Register bit 23.8

For RGMII/RTBI-compensated mode, the following specifications are valid only when the I/O power supply (VDDIO) is 2.5V, ±5%, per the RGMII specification, the MAC I/F selection bits have been set to RGMII mode and MII Register bit 23.8 is set to 1. See MII Register 23 and the RGMII specification for more information. All timing specifications are referenced to a switching threshold of 1.25V (i.e., 50% of VDDIO = 2.5V).

Table 20-9B. RGMII/RTBI-Compensated Mode AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{skew}R$	-500	0	+500	ps	Data to clock input skew (at PHY) – compensated mode.
$T_{setup}T$	1.5	2.0		ns	Data to clock output Setup (at PHY)[1]
$T_{hold}T$	1.5	2.0		ns	Data to clock output hold (at PHY)[1]
T_{CYC}	7.2	8.0	8.8	ns	Clock cycle duration.[2]
Duty_G	45	50	55	%	Duty cycle for 1000BASE-T.[3]
Duty_T	40	50	60	%	Duty cycle for 10BASE-T and 100BASE-TX.[3]
$T_{R,}$ T_F			0.75	ns	Rise, fall time (20% to 80%).

[1] RGMII-ID mode - a 2ns delay is added to the TXC and RXC signals inside the PHY.

[2] For 10Mbps and 100Mbps, T_{CYC} will scale to 400ns (±40ns), and 40ns (±4ns), respectively.

[3] Duty cycle may be stretched or shrunk during speed changes or while transitioning to a received packet's clock domain, as long as the minimum duty cycle is not violated, and stretching occurs for no more than three T_{CYC} of the lowest speed transitioned between.

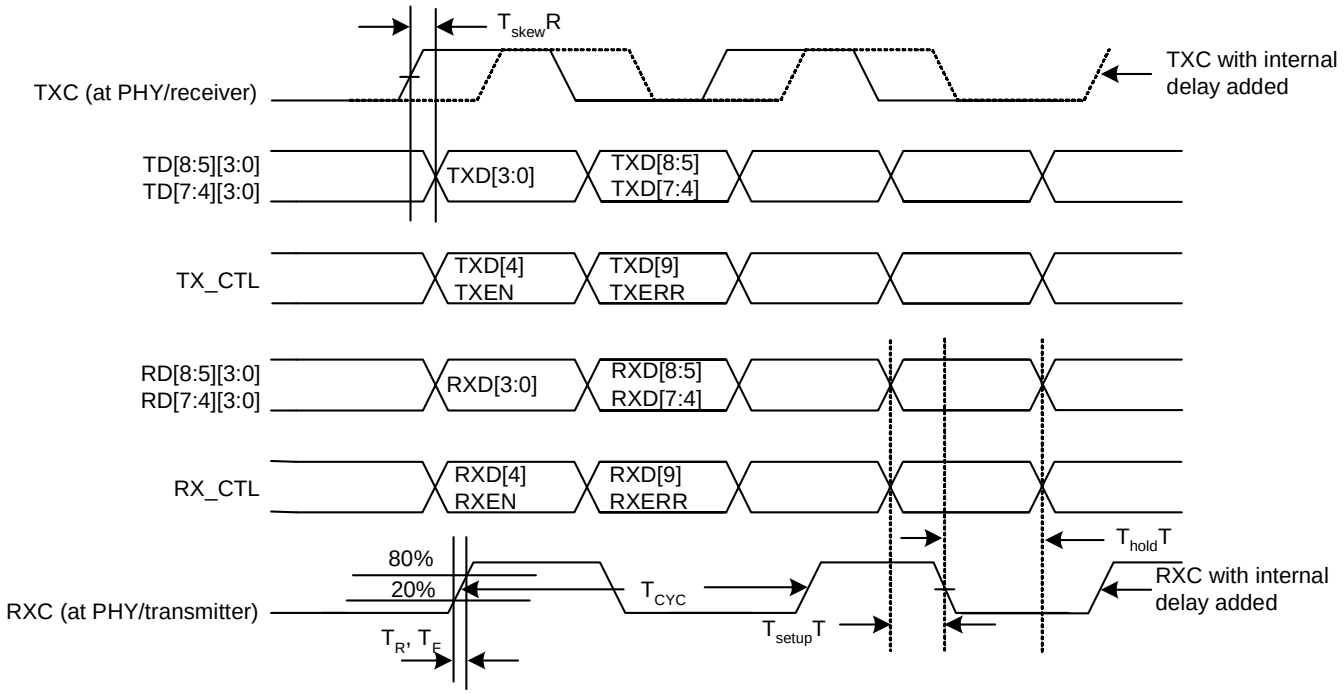


Figure 20-9B. RGMII/RTBI Compensated AC Timing and Multiplexing

TXC is internally delayed by ~1.8ns.

RXC is delayed internally by ~2ns.

Since no “trombone shaped” trace is required with this approach, the advantages of this compensated timing over RGMII v1.2a include:

- Simplified board design
- More compact routes; less board area
- Lower EMI emissions
- Greater distance possible between the MAC and PHY
- Improved signal integrity for a given distance between the MAC and PHY.

20.10 TBI Mode Transmit Timing

For TBI mode, the following specifications are valid only when the I/O power supply (VDDIO) is 3.0-3.6V, and the MAC I/F selection bits have been set to TBI mode. See MII Register 23 for more information.

Table 20-10. TBI Mode Transmit AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{PMA\_TX\_CLK}$	8.0 - 100ppm	8.0	8.0 + 100ppm	ns	PMA transmit clock period
T_{SETUP}	2			ns	Transmit data setup time to rising edge of PMA_TX_CLK.
T_{HOLD}	1			ns	Transmit data hold time to rising edge of PMA_TX_CLK.
T_{DUTY}	40		60	%	PMA_TX_CLK duty cycle.
t_R	0.7		2.4	ns	Clock rise time (0.8V to 2.0V).
t_F	0.7		2.4	ns	Clock fall time (2.0V to 0.8V).
t_R	0.7			ns	Data rise time (0.8V to 2.0V).
t_F	0.7			ns	Data fall time (2.0V to 0.8V).

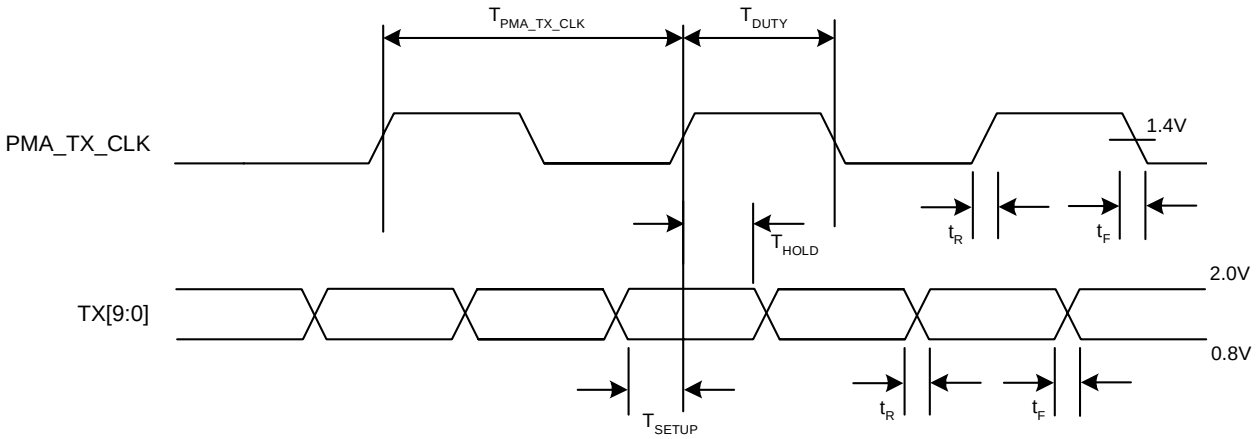


Figure 20-10. TBI Transmit AC Timing

20.11 TBI Mode Receive Timing

For TBI mode, the following specifications are valid only when the I/O power supply (VDDIO) is 3.0-3.6V, and the MAC I/F selection bits have been set to TBI mode. See MII Register 23 for more information.

Table 20-11. TBI Mode Receive AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{PMA\_RX\_CLK}$		62.5		MHz	PMA receive clock frequency (PMA_RX_CLK1 and PMA_RX_CLK0).
T_{DRIFT}	0.2			µs/MHz	PMA_RX_CLK drift rate.[1]
T_{A-B}	7.5		8.5	ns	PMA_RX_CLK skew.
T_{SETUP}	2.5			ns	Receive data setup time to rising edge of PMA_RX_CLK.
T_{HOLD}	1.5			ns	Receive data hold time to rising edge of PMA_RX_CLK.
T_{DUTY}	40		60	%	PMA_RX_CLK duty cycle.
t_R	0.7		2.4	ns	Clock rise time (0.8V to 2.0V).
t_F	0.7		2.4	ns	Clock fall time (2.0V to 0.8V).
t_R	0.7			ns	Data rise time (0.8V to 2.0V).
t_F	0.7			ns	Data fall time (2.0V to 0.8V).

[1] The drift rate is the (minimum) time for PMA_RX_CLK to drift from 63.5MHz to 64.5MHz or 60MHz to 59MHz from the PMA_RX_CLK lock value. It is applicable under all input signal conditions (except during code-group alignment), provided that the receiver clock recovery unit was previously locked to PMA_TX_CLK or to a valid input signal.

The following figure diagrams TBI receive AC timing.

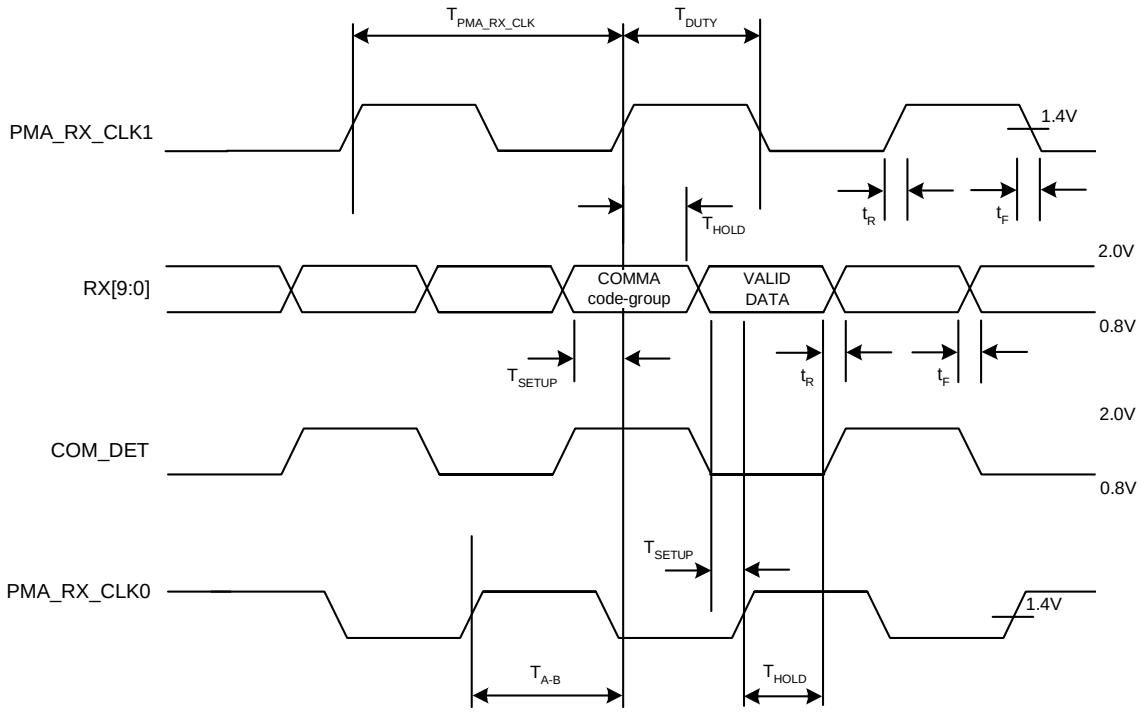


Figure 20-11. TBI Receive AC Timing

20.12 Auto-Negotiation Fast Link Pulse (FLP) Timing

The following specifications represent both transmit and receive timings. They are valid only when the I/O power supply (VDDIO) is at either 3.0-3.6V, or 2.5V, ±5%. See MII Register 23 for more information.

Table 20-12. Auto-Negotiation FLP AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{CLK\text{-}Period}$	14	121	139	µs	Clock pulse to clock pulse period.
$T_{CLK/DATA}$		100		ns	Clock/Data pulse width.
$T_{CLK/DATA\text{-}Period}$		62.5		µs	Clock pulse to data pulse period (Data = 1).
$T_{BURST\text{-}Period}$	8		24	ms	FLP burst to FLP burst period.
T_{BURST}		11		ms	FLP burst width.
n_{BURST}	17		33	#	Number of pulses in an FLP burst.

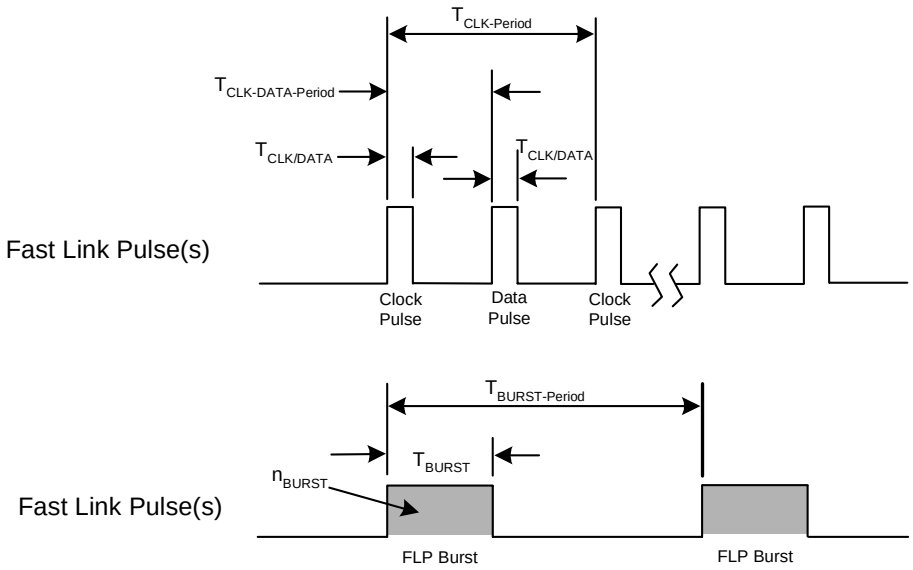


Figure 20-12. Auto-Negotiation FLP AC Timing

20.13 JTAG Timing

The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.0-3.6V, or 2.5V, ±5%. See MII Register 23 for more information.

Table 20-13. JTAG Interface AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{TCK\text{-}Period}$	100			ns	TCK period.
$T_{TCK\text{-}High}$	45			ns	TCK minimum pulse width high.
$T_{TCK\text{-}Low}$	45			ns	TCK minimum pulse width low.
$T_{TDI/TMS\text{-}Setup}$	10			ns	(TMS or TDI) to TCK setup time.
$T_{TDI/TMS\text{-}Hold}$	10			ns	(TMS or TDI) to TCK hold time.
$T_{TDO\text{-}Delay}$	0		15	ns	TDO delay from TCK.

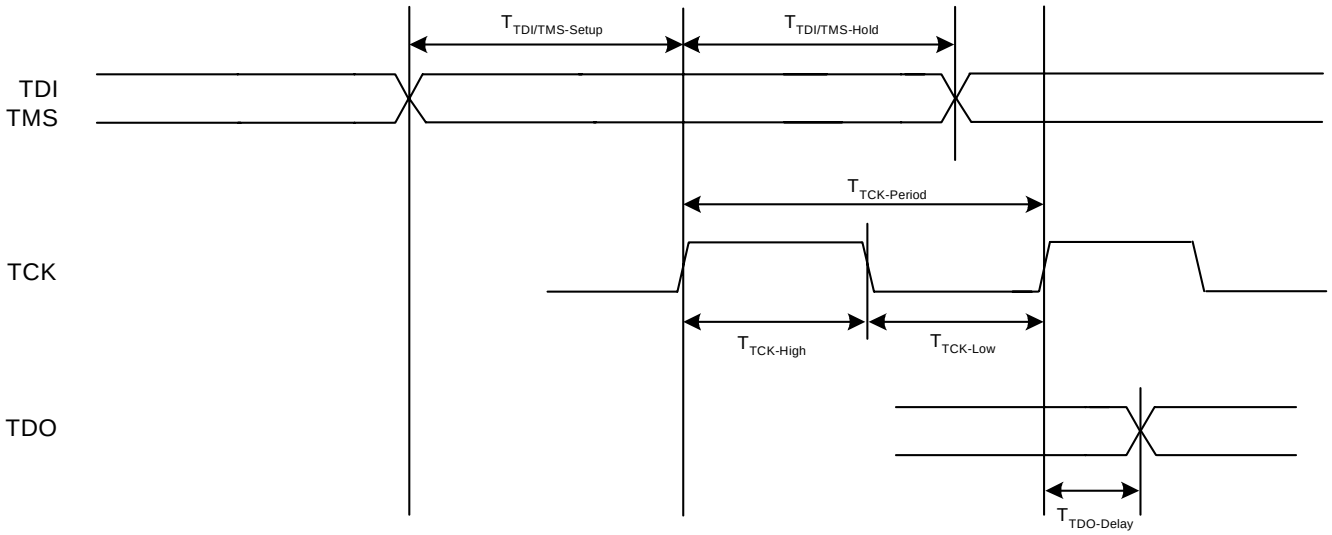


Figure 20-13. JTAG Interface AC Timing

20.14 SMI Timing

The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.0-3.6V, or 2.5V, ±5%. See MII Register 23 for more information.

Table 20-14. SMI AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
F_{MDC}		2.5	12.5	MHz	MDC clock frequency.
$T_{MDIO-Setup}$	10			ns	MDIO to MDC setup time when sourced by Station Manager.
$T_{MDIO-Hold}$	10			ns	MDIO to MDC hold time when sourced by Station Manager.
$T_{MDIO-Delay}$		10		ns	MDC to MDIO delay time from CIS8201. Delay will depend on value of external pull-up resistor on MDIO pin.

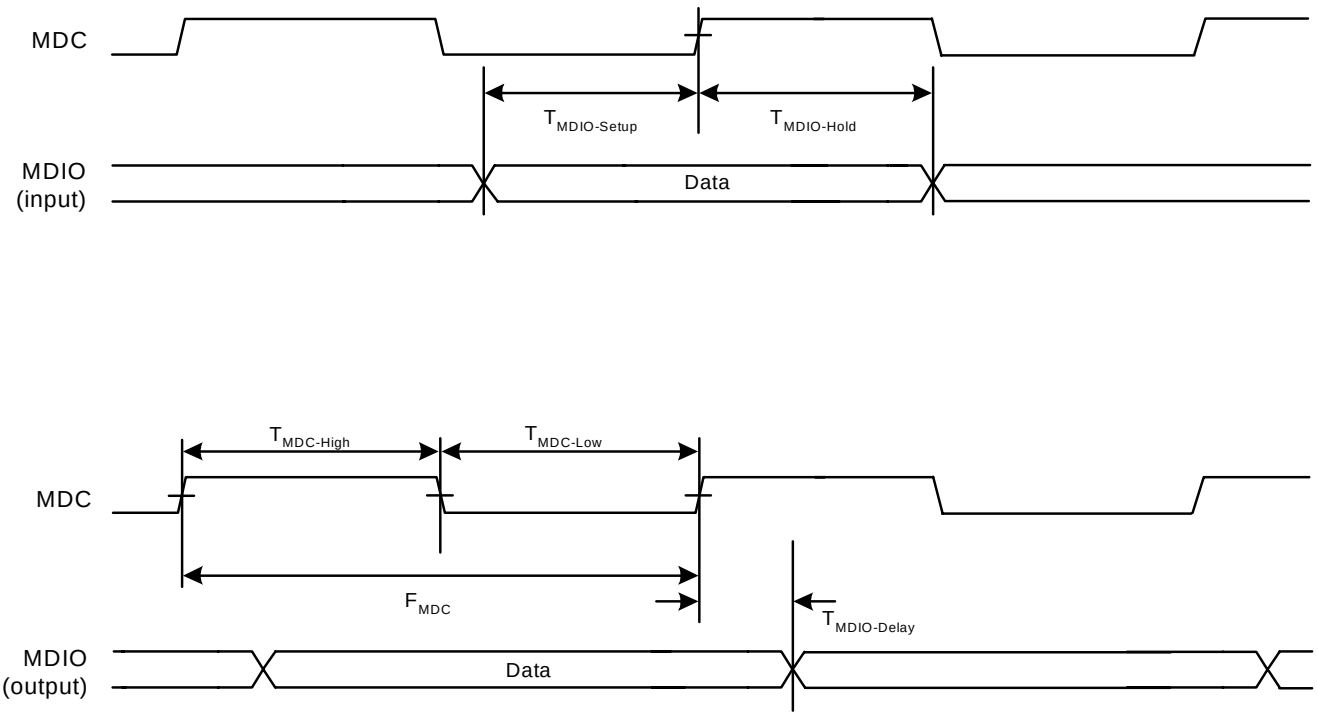


Figure 20-14. SMI AC Timing

20.15 MDINT# Timing

The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.0-3.6V, or 2.5V, ±5%. See MII Register 23 for more information.

Table 20-15. MDINT# AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
t_F			110	ns	MDINT# fall time, assuming a 2.2kΩ external pull-up resistor and a 50pF total capacitive load.

20.16 Power-Down and Reset Timing

The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.0-3.6V, or 2.5V, ±5%. See MII Register 23 for more information.

Table 20-16. Power-Down and Reset AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{SUPPLY-Stable}$	10			ms	Required supply stabilization time before RST# is deasserted.
$T_{PWDN-Deassert}$	10			ms	Required PWDN# deassertion time before RST# is deasserted.
T_{RESET}	100			ns	RST# assertion time.
T_{PLL_LOCK}			50	µs	PLL lock time.
T_{PWDN}	1			µs	PWDN# assertion time.

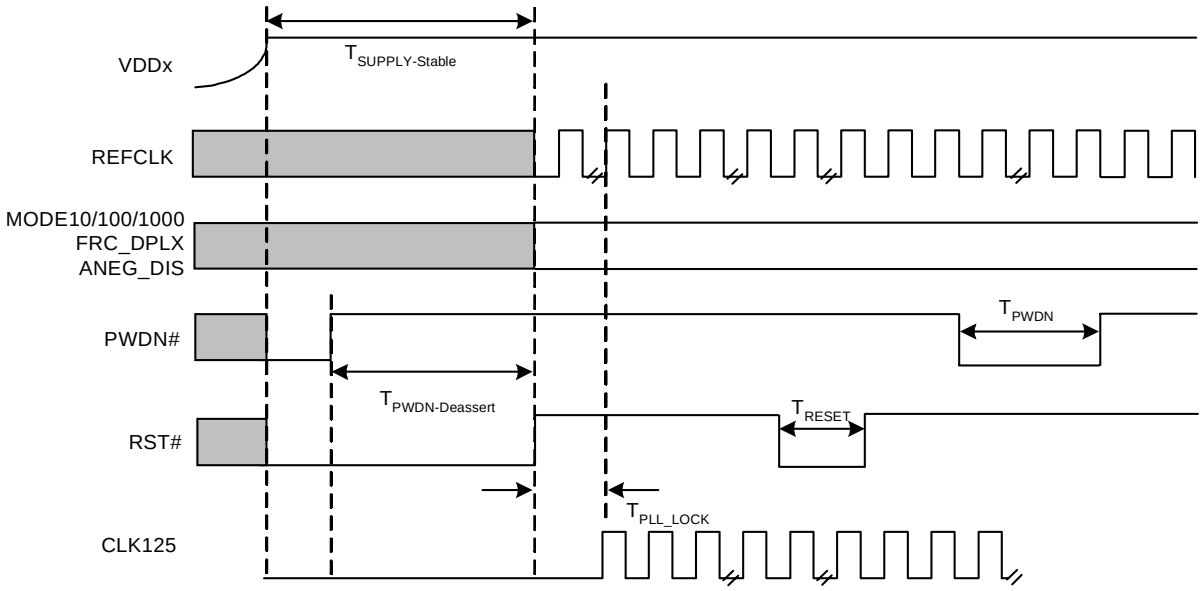


Figure 20-16. Power-Down and Reset AC Timing

20.17 REFCLK Timing

The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.0-3.6V, or 2.5V, ±5%. See MII Register 23 for more information.

Table 20-17. REFCLK AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{REFCLK25}$		40		ns	Reference clock period, PLLMODE = 0 (25MHz reference).
$T_{REFCLK125}$		8		ns	Reference clock period, PLLMODE = 1 (125MHz reference).
$F_{STABILITY}$	-100		+100	ppm	Reference clock frequency stability (0°C to 70°C).
T_{DUTY}	40		60	%	REFCLK duty cycle in both 25MHz and 125MHz modes.
$J_{REFCLK25}$, $J_{REFCLK125}$			100	ps	Total jitter of 25MHz or 125MHz reference clock (peak-to-peak).
$t_{R/F\ (REFCLK25)}$			4	ns	Reference clock rise time, 25MHz mode (20% to 80%).
$t_{R/F\ (REFCLK125)}$			1	ns	Reference clock rise time, 125MHz mode (20% to 80%).

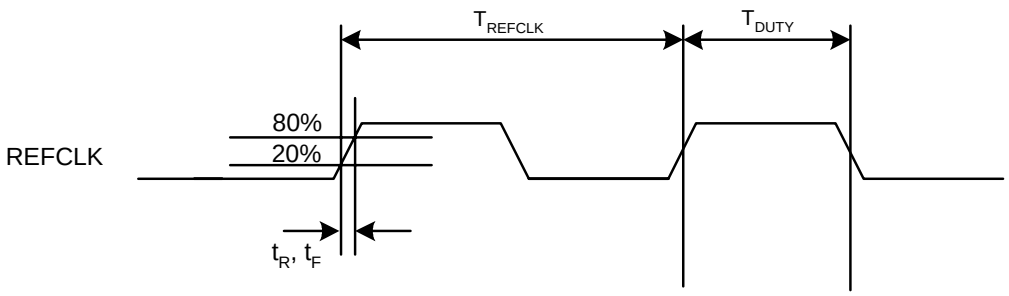


Figure 20-17. REFCLK AC Timing

20.18 CLK125 Timing

The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.0-3.6V, or 2.5V, ±5%. See MII Register 23 for more information.

Table 20-18. CLK125 AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
T_{CLK125}		8		ns	Output clock period.
$F_{STABILITY}$	-100		+100	ppm	Output clock frequency stability (0°C to 70°C).
T_{DUTY}	40		60	%	Output clock duty cycle.
J_{CLK125}		200		ps	Total jitter of output clock (peak-to-peak).
$t_{R/F\ (CLK125)}$			1	ns	Output clock rise time (20% to 80%).

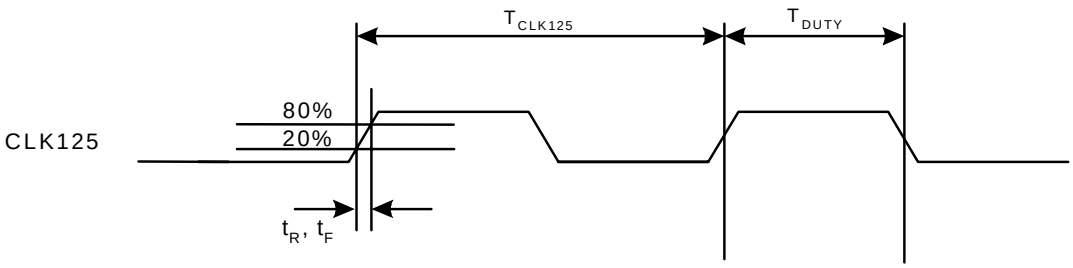


Figure 20-18. CLK125 AC Timing

20.19 Regulator Timing

The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.0-3.6V, or 2.5V, ±5%. See MII Register 23 for more information.

Table 20-19. Regulator AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
T_{REG}		1		ms	Regulator start-up time.

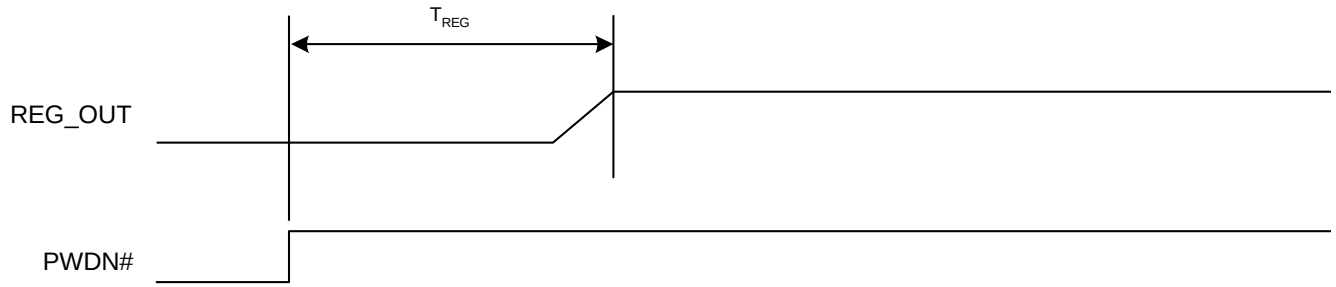


Figure 20-19. Regulator AC Timing

20.20 Oscillator Timing

The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.0-3.6V, or 2.5V, ±5%. See MII Register 23 for more information.

Table 20-20. Oscillator AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
T_{OSC}		2		ms	Oscillator start-up time.

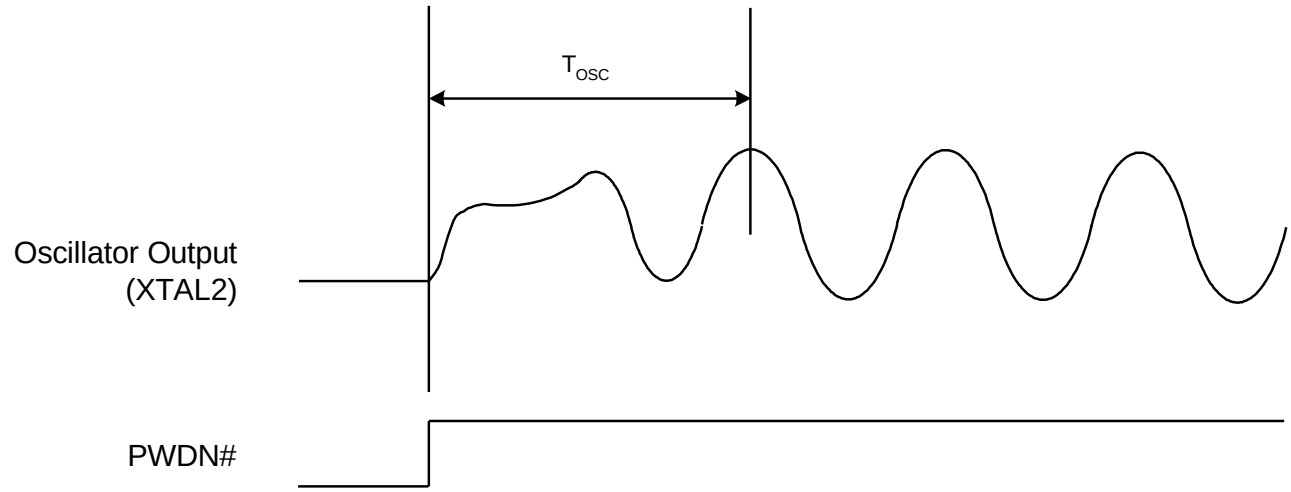


Figure 20-20. Oscillator AC Timing

20.21 Isolation Timing

Isolation mode forces all MAC interface output pins (except for MDIO) to be in a high empedance state. The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.0-3.6V, or 2.5V, ±5%. See MII Register 23 for more information.

Table 20-21. Isolation AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{ISOL-Reg}$			100	µs	Time from the software clear of Register bit 0.10 to the transition from Isolate to Normal mode.
$T_{ISOL-Reset}$			500	µs	Time from the deassertion of a hardware or software reset to the transition from Isolate to Normal mode.

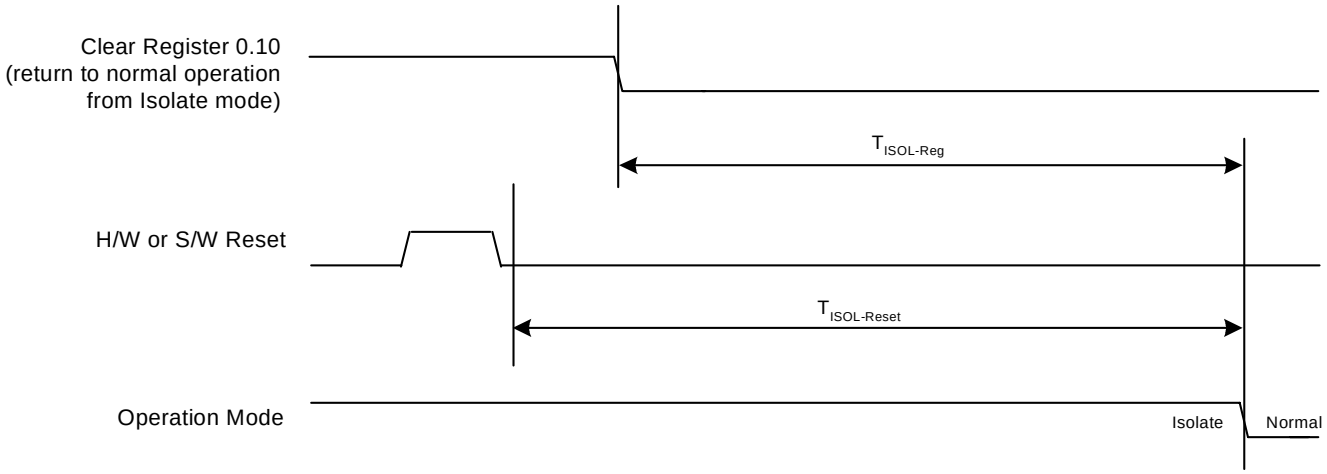


Figure 20-21. Isolation AC Timing

21 Magnetics Specifications

The following specifications are representative of an acceptable transformer for the CIS8201 twisted pair interface. Other transformers with comparable specifications should also be acceptable.

Table 21-1. Magnetics Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
N		1:1		N/A	Transformer turns ratio.
-			-0.5 -1.0 -1.5	dB	Insertion loss: 1 - 60MHz 60 - 100MHz 100 - 125MHz
-	-16 -13.5 -11.5 -10			dB	Return loss (Load 100Ω): 1 - 30MHz 30 - 40MHZ 40 - 50MHz 50 - 80MHz
-			1.5	kV	Isolation (@60Hz, input to output 1500V_{rms}, 1 minute)
L_{PRI}	350			µH	Primary inductance (@100KHz, 0.1V_{rms}, 8mA DC Bias)
-	-40 -38 -33			dB	Cross talk: 1 - 30MHz 30 - 60MHz 60 - 100MHz
CMRR	-30			dB	1 - 100MHz

Some magnetics may require an optional return-loss compensation circuit. See *AN008 'Magnetics Recommendations for CIS8201 & CIS8204 - Application Note'* for additional information.

The default operation of the PHY is to power down media pairs C and D in 10/100BASE-T modes. Consequently when the PHY is used with integrated (magnetics + RJ-45) modules that generally have the center taps of the four coils shorted together on the primary side (PHY side), the common mode of the PHY is pulled to ground. When using integrated modules with the coils shorted together on the primary side (as shown in Figure 21-1), the following writes must be performed after PHY reset:

1. 2a30h to Register 31
2. 0010h to Register 8
3. 0000h to Register 31

The register writes must be done in the sequence mentioned above. These writes disable the powering down of the C and D pairs in 10/100BASE-T modes.

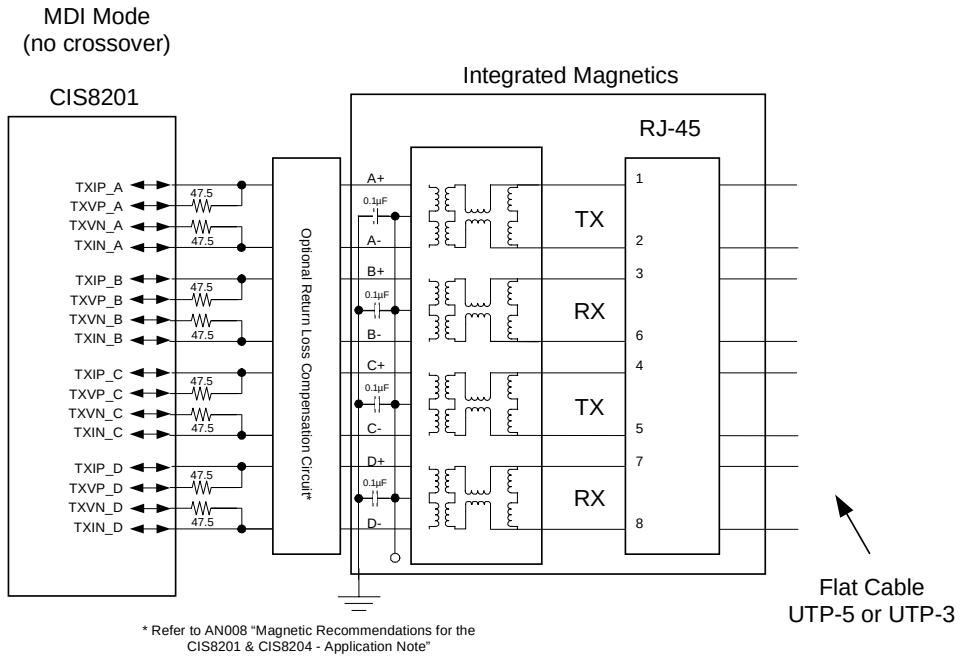


Figure 21-1. Integrated Magnetics

22 Important Design Considerations

22.1 GMII Transmit and Receive

The GMII Transmit and Receive setup/hold timings do not meet the standard. If the MAC’s/Switch’s GMII transmit setup time is not greater than 2.5ns, a PCB trace delay must be added to the GTXCLK signal.

If the GMII receive setup time required by the MAC is greater than 1.75ns, a PCB trace delay must be added to the RXCLK signal.

22.2 Return Loss Compensation

The PHY needs an external circuit to be placed between the PHY’s TPI pins and the transformer to meet the IEEE 802.3 return loss specification. This external circuit depends on the type of magnetics used. Refer to AN008 “Magnetic Recommendations for the CIS8201 & CIS8204 - Application Note” for details.

In the absence of the return loss circuit the PHY may not meet the return loss specification under the worst case TPI interface loading of 85Ω. The absence of this circuit does not effect the PHY performance.

22.3 Shorted Center Taps on TPI Interface

A sequence of Register writes is needed at startup when using magnetics with center taps on the primary side (PHY side) shorted together. Refer to Section 21: "Magnetics Specifications" above for details.

22.4 Isolate Bit Considerations

Setting MII Register bit 0.10 does not isolate the GMII/MII inputs (i.e. when isolate bit is set the GMII/MII data on TX pins will be transmitted on the MDI interface if the link is up). This behavior does not comply with the IEEE 802.3 standard. To isolate the

GMII/MII inputs, both MII Register bits 0.11 and 0.10 must be set. It should be noted that setting bits 0.11 and 0.10 will cause the link to drop.

See Section 17.1: "Register 0 (00h) – Mode Control Register" for details.

22.5 Transmit Waveforms

The 1000BASE-T output waveforms of some devices may not conform to the linearity requirements of the IEEE 802.3 standard (Section 40.6.1.2.1). Although devices have been measured to pass in typical operating environments, this parameter is not guaranteed over worst case operating conditions. This has no impact on performance or inter-operability of the PHY.

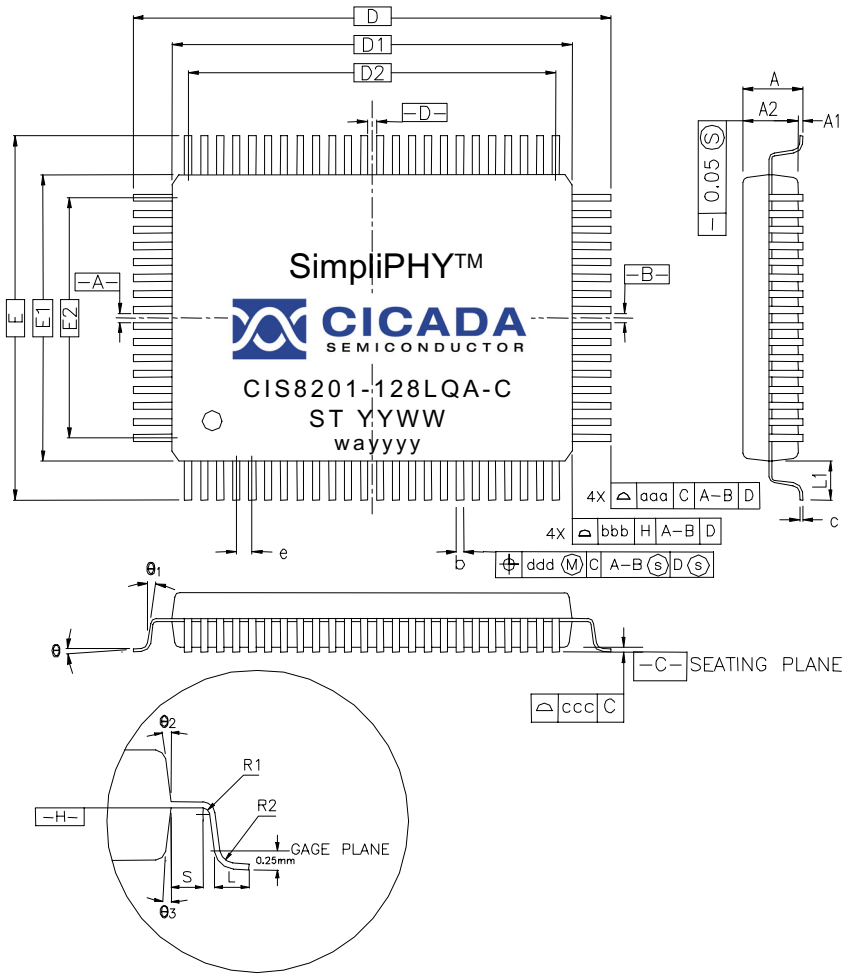
See Section 9.7: "Twisted Pair Interface Pins (TPI)" for details.

22.6 CRS Latency

In 100BASE-TX half-duplex mode using RGMII interface, the total PHY latency (MDI to CRS) is between 65 to 68 bit times. The collision domain of a particular worst case scenario where two DTEs are linked to each other via two Class 11 repeaters (3 hops), is measured to be 305m, which exceeds the 205m diameter requirement specified in the IEEE 802.3 standard; therefore this issue is not likely to have an impact in 100BASE-T half-duplex mode when using the RGMII interface.

See Section 20.7: "100BASE-TX Receive Packet Latency Timing" for details.

23 128 Pin LQFP Mechanical Specification



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	22.00 BSC.			0.866 BSC.		
D1	20.00 BSC.			0.787 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

Marking Codes: Y: Date Code Year, W: Date Code Week

SYMBOL	128L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	18.50			0.728		
E2	12.50			0.492		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.

Figure 23-1. 128 LQFP Mechanical Specification

24 100-Ball LBGA Mechanical Specification

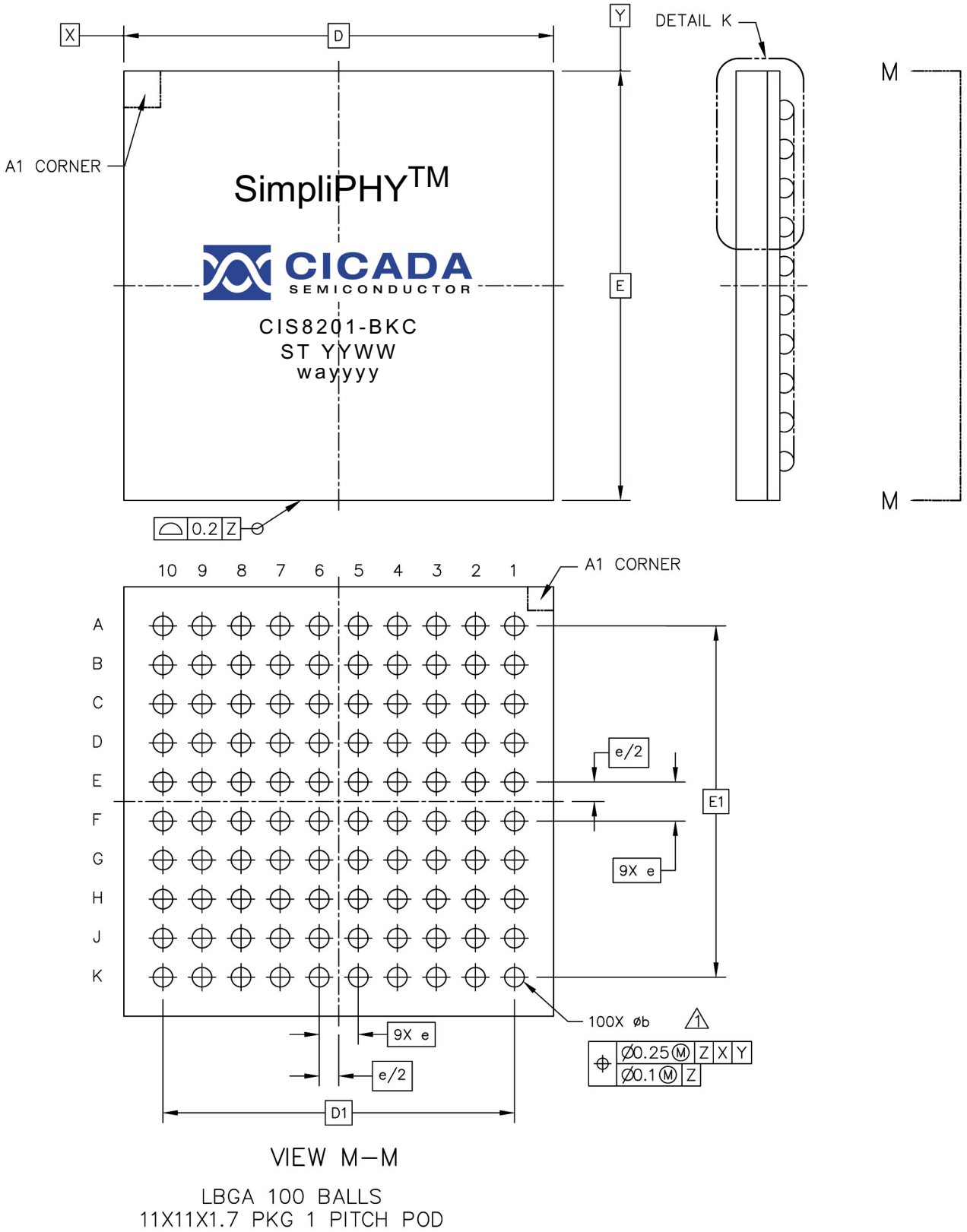
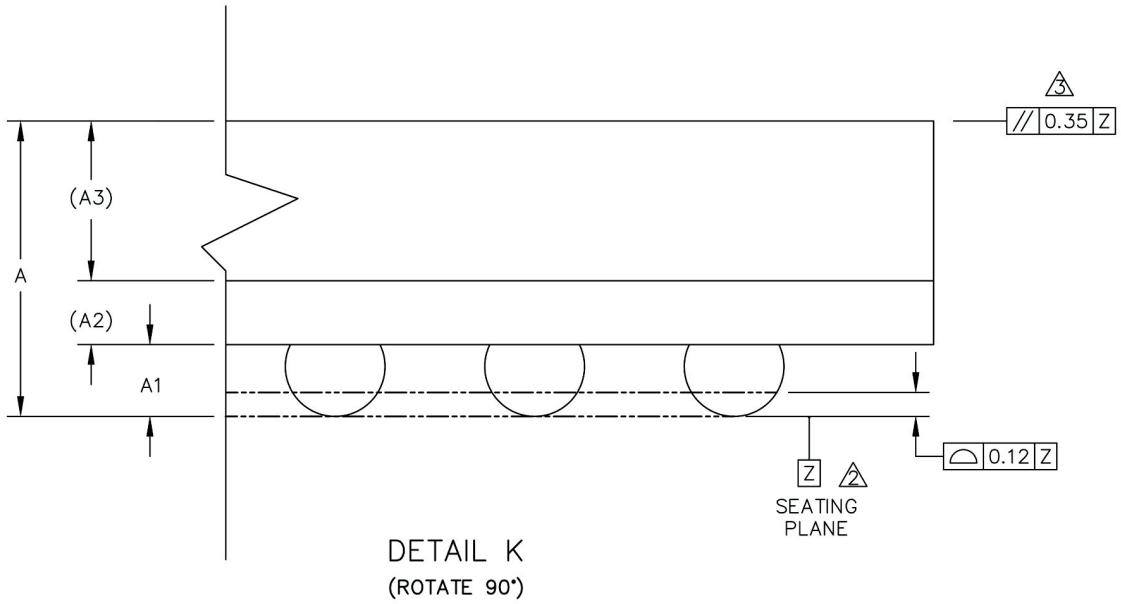


Figure 24-1. 100 LBGA Mechanical Specification - Page 1 of 2



DIM	MIN	MAX
A		1.7
A1	0.29	0.43
A2	0.38 REF	
A3	0.8 REF	
b	0.45	0.55
D	11 BSC[1]	
E	11 BSC	
e	1 BSC	
D1	9 BSC	
E1	9 BSC	
	UNIT = MM	

NOTES

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
2. DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 24-2. 100 LBGA Mechanical Specification - Page 2 of 2

[1] Basic Spacing between Centers (1mm in this case)

25 Ordering Information

25.1 Devices

Table 25-1. Device Ordering Information

Part Number	Container[1]	Package Type	Description	Temperature Range
CIS8201-128LQA-C	Tray	128 LQFP 14mm x 20mm 0.5mm pitch	Single Port SimpliPHY™ CIS8201 10/100/ 1000BASE-T PHY with: GMII/MII, RGMII, TBI, RTBI interfaces	Commercial temperature range: 0°C to +70°C
CIS8201-128LQA-C-R	Tape & Reel	128 LQFP 14mm x 20mm 0.5mm pitch	Single Port SimpliPHY™ CIS8201 10/100/ 1000BASE-T PHY with: GMII/MII, RGMII, TBI, RTBI interfaces	Commercial temperature range: 0°C to +70°C
CIS8201-BKC	Tray	100 LBGA 11mm x 11mm 1.0mm pitch	Single Port SimpliPHY™ CIS8201 10/100/ 1000BASE-T PHY with: GMII/MII, RGMII, TBI, RTBI interfaces	Commercial temperature range: 0°C to +70°C
CIS8201-BKCR	Tape & Reel	100 LBGA 11mm x 11mm 1.0mm pitch	Single Port SimpliPHY™ CIS8201 10/100/ 1000BASE-T PHY with: GMII/MII, RGMII, TBI, RTBI interfaces	Commercial temperature range: 0°C to +70°C

[1] One of the container options must be specified when ordering. All orders for tape and reel must be for an entire reel.
The “R” suffix is for ordering purposes only and will not appear on the package mark.

25.2 Evaluation Systems

Table 25-2. Evaluation System Ordering Information

Part Number	System Type	Description
CEB8201-G/T	Evaluation Board	Customer Evaluation Board for CIS8201, for GMII/MII/RGMII and TBI/RTBI interface evaluation

26 Product Support

26.1 Available Documents and Application Notes

AN001 - **SimpliPHY™ CIS8201 Design Considerations for Wake-on-LAN Compliance**
AN003 - **SimpliPHY™ CIS8201 Transformerless Ethernet Concepts and Applications**
AN005 - **SimpliPHY™ CIS8201 PCB Design and Layout Application Note**
AN008 - **Magnetics Recommendations for CIS8201 & CIS8204 - Application Note**
AN009 - **Inter-operability Notices - Application Note**
AN010 - **CIS8201 / RTL8201BL Dual Layout PCB Application Note**
User Guides - **Evaluation Kit CEB8201-G**

26.2 Contact Information

To request device data sheets, user guides, and application notes; or to submit information for schematic or PCB layout review, please visit http://www.cicada-semi.com/products/request.htm.

27 Document History & Notices

Table 27-1. Document History & Notices

Revision Number	Date	Comments
1.0.0	11 Jul 02	Complete and approved documentation for Silicon Revision A0.
1.1.0	Jan 03	Complete and approved documentation for Silicon Revision A1, A2.
1.2.0	April 03	Updated AC Timing Parameters ($T_{CRS\_OFF-DELAY}$) in Section 20.8. RGMII section rewritten for simplification, AC Timing data for skew on and off updated. Updated SMI Timing in Section 20.14. Added Power-Down and Reset Timing Specifications ($T_{SUPPLY-Stable}$,$T_{PWDN-Deassert}$, & T_{PLL_LOCK}) in Section 20.16. Updated REFCLK Timing in Section 20.17. Updated CLK125 Timing in Section 20.18.
1.2.1	May 03	Added 100-ball LBGA information Updated Magnetic Specifications in Section 21. Updated Ordering Information in Section 25.
1.2.2	Sep 03	Added thermal data for LBGA package in Section 18.4 Added references to AN008 ‘Magnetics Recommendations for CIS8201 & CIS8204 - Appnote’ Added info on shorted center taps in Section 21 Updated ordering information in Section 25 Integrated errata issues into the following sections: “Register 0 (00h) – Mode Control Register” on page 59. (Table footnote 1) “100BASE-TX Receive Packet Latency Timing” on page 112. (Table footnote 1) “Magnetics Specifications” on page 128. (Text and Figure 21-1: "Integrated Magnetics") Added Section 22 “Important Design Considerations