Parallel CMOS First-In/First-Out

GENERAL DESCRIPTION

The XR-T7201/2/3 are dual port memories which operate in a 'first-in-first-out' basis. Complementary to this particular algorithm, this devices use full and empty flags to prevent under and/or over flow and also an expansion logic to allow memory expansion in word size and depth. They are fabricated using a high speed 1.25 micron technology and are designed for applications requiring sourcing and absorption of data at different data rates (fast processors interfacing to slower peripherals for example).

Data is internally manipulated through ring pointers to avoid the use of address information to load and unload data. To toggle the bits in and out of the device, the WRITE (W) and the READ (R) pins are used (typical read/write cycle time = 50ns @ 12MHz).

A 9 bit wide data array, which is particularly useful in data communication applications, allows for control of the ninth bit which is used for parity and error checking of transmitted data bytes. Another useful feature is the RETRANSMIT (RT) option which resets the read pointer to its initial position and allows retransmission from the beginning of the data. The flag logic provides a mechanism to control over or underflow conditions and the expansion logic allows several devices to expand in word size and depth.

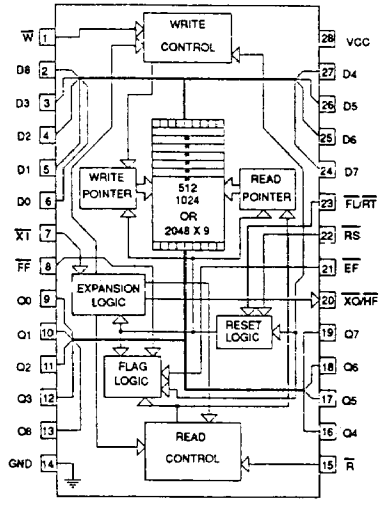
FEATURES

First In First Out Dual Port Memory
Organization: * 512 X 9 (XR-T7201)
* 1024 X 9 (XR-T7202)
* 2048 X 9 (XR-T7203)
Very Low Power Consumption
Ultra High Speed Cycle Time (typ 45ns)
Asynchronous and Simultaneous Read and Write
Expandable by Word Width and Depth
Empty and Full Warning Flags
Auto Retransmit Capability
High Speed 1.25 Micron CMOS Technology
Functionally and Pin Compatible to ID77201-3 and Mostek MK4501-3

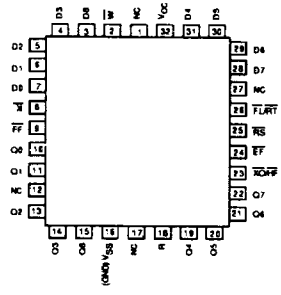
APPLICATIONS

Master / Slave Multiprocessing Applications
Bidirectional and Buffer Applications

PIN ASSIGNMENT



CP, IP PACKAGES



CJ, IJ PACKAGES

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to 150°C
Supply Voltage	-0.5V to 7V
Supply Voltage Surge (10ms)	+25V
Power Dissipation	1.0W
DC Output Current	50mA

Note: Stresses exceeding the ones specified above may cause permanent damage to the device or reliability problems.

ORDERING INFORMATION

Part Number	Package	Operating Temp.
XR-T7201	CP (Plastic)	0°C to 70°C
XR-T7201	CJ (LCC)	0°C to 70°C
XR-T7201	IP (Plastic)	-40°C to +85°C
XR-T7201	IJ (LCC)	-40°C to +85°C
XR-T7202	CP (Plastic)	0°C to 70°C
XR-T7202	CJ (LCC)	0°C to 70°C
XR-T7202	IP (Plastic)	-40°C to +85°C
XR-T7202	IJ (LCC)	-40°C to +85°C
XR-T7203	CP (Plastic)	0°C to 70°C
XR-T7203	CJ (LCC)	0°C to 70°C
XR-T7203	IP (Plastic)	-40°C to +55°C
XR-T7203	IJ (LCC)	-40°C to +55°C

* Note: Available access time = 35, 50, 65, 80, 120. Access time designator follows package information. Example order: XR-T7202CP-50

DC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5V +/- 10%, Ta = 0°C to 70°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage Current	-1		1	µA	$0.4<V_{IN}< V_{CC}$
V_{OL}	Output Leakage Current	-10			µA	Note 1
V_{OH}	Output "Logic 1"	2.4			V	I OUT = -1mA
V_{OL}	Output "Logic 0"			0.4	V	I OUT = 4mA
I_{CC}	Average Supply Current		80		mA	Note 2
I_{CC}	Average Standby Current		8		mA	Note 2
I_{CC}	Power Down Current			500	µA	Note 2

NOTE 1) R> V_{IH}, $0.4 < V_{OUT} < V_{CC}$

2) ICC Measurements are made with outputs open.

AC ELECTRICAL CHARACTERISTICS

Test Conditions: VCC = 5V +/- 10%, Ta = 0°C to 70°C
Input Pulse Level = GND to 3.0V
Input Rise and Fall Time = 5ns
Input Timing Reference Level = 1.5V
Output Reference Level = 1.5V

		Ta = 35ns		Ta = 50ns		Ta = 65ns		Ta = 80ns		Ta = 120ns		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t RC	Read Cycle Time	45	-	65	-	80	-	100	-	140	-	ns
t A	Access Time	-	35	-	50	-	65	-	80	-	120	ns
t RR	Read Recovery Time	10	-	15	-	15	-	20	-	20	-	ns
t RPW	Read Pulse Width	35	-	50	-	65	-	80	-	120	-	ns
t RLZ	Read Pulse Low to Data Bus at Low Z	5	-	10	-	10	-	10	-	10	-	ns
t WLZ	Write Pulse High to Data Bus at Low Z	10	-	15	-	15	-	15	-	15	-	ns
t DV	Data Valid from Read Pulse High	5	-	5	-	5	-	5	-	5	-	ns
t RHZ	Read Pulse High to Data Bus at High Z	-	20	-	30	-	30	-	30	-	30	ns
t WC	Write Cycle Time	45	-	65	-	80	-	100	-	140	-	ns
t WPW	Write Pulse Width	35	-	50	-	65	-	80	-	120	-	ns
t WR	Write Recovery Time	10	-	15	-	15	-	20	-	20	-	ns
t DS	Data Setup Time	18	-	30	-	30	-	40	-	40	-	ns
t DH	Data Hold Time	0	-	5	-	10	-	10	-	10	-	ns
t RSC	Reset Cycle Time	45	-	65	-	80	-	100	-	140	-	ns
t RS	Reset Pulse Width	35	-	50	-	65	-	80	-	120	-	ns
t RSR	Reset Recovery Time	10	-	15	-	15	-	20	-	20	-	ns
t RTC	Retransmit Cycle	45	-	65	-	80	-	100	-	140	-	ns
tRT	Retransmit Pulse W.	35	-	50	-	65	-	80	-	120	-	ns
tRTR	Retransmit Recovery	10	-1	15	-	15	-	20	-	20	-	ns
tEFL	Reset to EF Low	-	45	-	65	-	80	-	100	-	1	
tREF	Read Low to EF Low	-	30	-	45	-	60	-	70	-		
t RFF	Read High to FF Low	-	30	-	45	-	60	-	70	-	110	ns
t WEF	Write High to EF High	-	30	-	45	-	60	-	70	-	110	ns
t WFF	Write Low to FF Low	30	-	-	45	-	60	-	70	-	110	ns
t WHF	Write Low to HF Low	-	45	-	65	-	80	-	100	-	140	ns
t RHF	Read High to HF High	-	45	-	65	-	80	-	100	-	140	ns

Note: 1) Timing referenced as in AC Test Conditions.
2) Pulse widths less than minimum are not allowed.
3) Values guaranteed by design, not currently tested.

PIN#	MNEMONIC	DESCRIPTION
1	$\overline{W}$	(Active Low) **WRITE ENABLE** A falling edge on this pin initiates a write cycle provided the FF Flag (FIFO Full) is not set. Timing, such as hold and set-up requirements are measured with respect to the rising edge of this pin.
2-6 24-27	D0-D8	**DATA INPUT**. Data is loaded into the FIFO sequentially and is totally independent of any read operations.
7	$\overline{XI}$	(Active Low) **EXPANSION INDICATOR** pin. When grounded, the single device mode is selected. When connected to XO (Expansion Out), the device is configured in the Depth Expansion or Daisy Chain Mode.
8	$\overline{FF}$	(Active Low) **FULL FLAG**. This pin will go low when the write pointer is one location away from the read pointer and inhibit any further write operations to the device. This is done to prevent data overflow. Upon completion of a read operation the FF will go high after tRFF, and a valid write can begin.
9-13 16-19	Q0-Q8	**DATA OUTPUTS**. Data is read from the FIFO whenever the Read Enable line goes low and the EF Flag is not set. After reading the data outputs they return to a high impedance state until the next Read operation.
14	GND	**POWER GROUND**
15	$\overline{R}$	(Active Low) **READ ENABLE**. A read operation is initiated on the falling edge of the Read Enable Control, provided the Empty Flag is not set. Data is accessed on a First-In-First-Out basis and is totally independent of any Write operation. At the completion of the Read Cycle the outputs return to a high impedance state until the next read operation.
20	$\overline{XO/HF}$	(Active Low) **EXPANSION OUT/HALF FULL**. This is a dual purpose pin whose functions are: (1) When using this device in the Multiple Device mode, XI (Expansion In) is connected to XO (Expansion Out). This way the output generates a signal to alert the next device in the Daisy Chain that the previous device has reached the last location of memory. (2) When using this device in the single device mode, XI (Expansion In) is grounded and the output acts as an indication of a half full memory. The Half Full Flag will be set to low and remain set until the difference between the write pointer and the read pointer is less than or equal to half the total memory of the device. This flag will be set at the half way point on the falling edge of the Write operation and reset by the rising edge of the Read operation.
21	$\overline{EF}$	(Active Low) **EMPTY FLAG**. When all the data has been read from the FIFO, the EMPTY FLAG will go low, inhibiting further read operations from the device and putting the output buffers in a high impedance state. The flag will be reset, once a valid write operation has been accomplished.
22	$\overline{RS}$	(Active Low) **RESET**. A Reset will put the Read and Write pointers to the first location

PIN #	MNEMONIC	DESCRIPTION
		and reset the Half Full Flag to the high state. It is only required after power-up before performing a write operation and can only take place if the Read Enable and the Write Enable are in the high state.
23	$\overline{FL/RT}$	(Active Low) **FIRST LOAD / RETRANSMIT**. This pin has two functions: (1) When using this device in the Multiple Device Mode, grounding this pin will indicate that this is the first device to be loaded. (2) In the Single Device Mode this pin acts as a retransmit input. In this mode the read pointer is set to the first location and will not affect the write pointer. Note that the Read Enable and the Write Enable need to be in the high state during retransmit. The Retransmit feature is not compatible with Depth Expansion Mode and will only affect the Half Full Flag ($\overline{HF}$) depending on the relative locations of the read and write pointers.
28	VCC	**SUPPLY VOLTAGE** (+5 Volt Power Input)

APPLICATIONS

SINGLE DEVICE CONFIGURATION

This configuration is used for applications that require less than the maximum specified memory space of a single device. To configure it, the XI (Expansion Input) pin needs to be grounded (Figure 1).

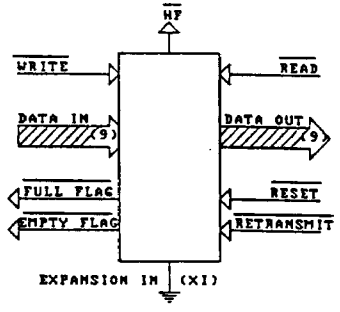


Figure 1. Block Diagram for Single Device Mode

WIDTH EXPANSION CONFIGURATION

In order to expand the width of the FIFO, the input control signals such as the Write Enable, Read Enable, Reset and Retransmit pins need to be connected together. Output Control Signals on the other hand need to be left alone. The Status Control pins such as Full, Half and Empty Flag can be detected from any one device. Figure 2 shows a typical Width Expansion configuration.

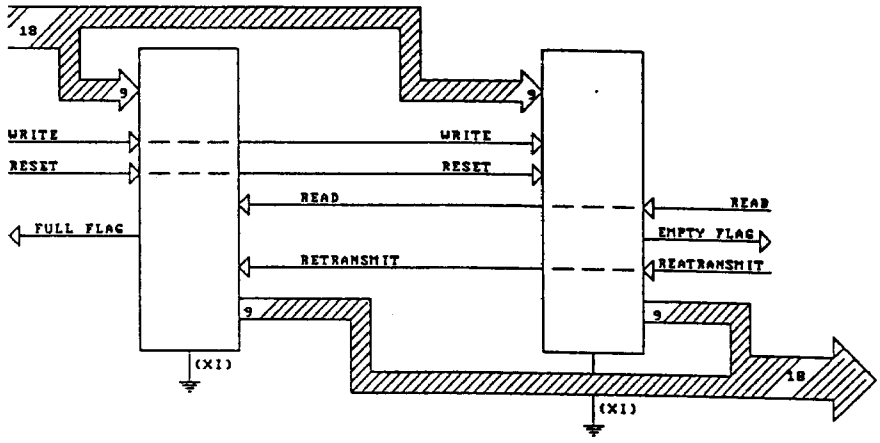


Figure 2. Block Diagram for a FIFO Width Expansion Configuration

TRUTH TABLES

RESET AND RETRANSMIT SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	RS	RT	XI	READ POINTER	WRITE POINTER	EF	FF	HF
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	X	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

Note: 1) Pointer will increment if Flag is high.

DEPTH EXPANSION CONFIGURATION

For applications requiring greater than 2048 words, several of these devices can be Daisy Chained together as long as the following conditions are met:

- The first device of the Daisy Chain is established by grounding the First Load (FL) control pin.
- All other devices must have the $\overline{FL}$ pin in the high state.
- The Expansion Out Pin $\overline{(XO)}$ of each device must be connected to the Expansion In Pin (XI) of the next device. (Figure 3)
- In order to generate a composite Full and/or Empty Flag some external logic is needed to "OR" all the outputs and generate the correct composite output signal.
- The Retransmit $\overline{(RT)}$ and the Half Full Flag $\overline{(HF)}$ are not available in the Depth Expansion Mode.

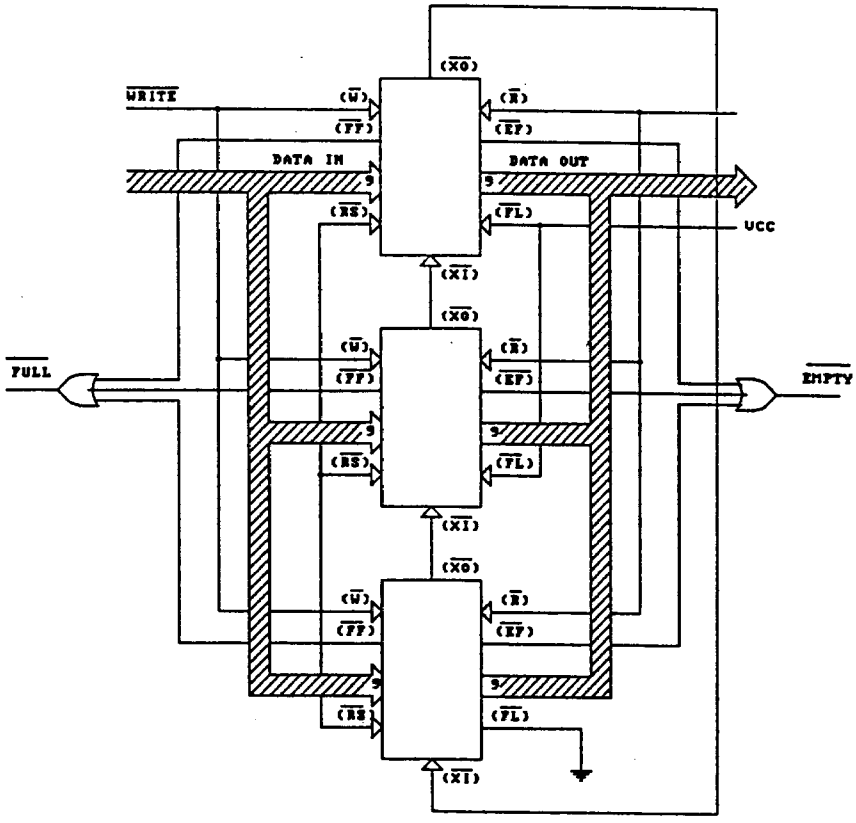


Figure 3. Block Diagram using FIFO's in Depth Expansion Mode

TRUTH TABLE

RESET AND FIRST LOAD TRUTH TABLE
DEPTH EXPANSION / COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	RS	FL	XI	READ POINTER	WRITE POINTER	EF	FF
RESET-FIRST IC	0	0	1	Location Zero	Location Zero	0	1
RESET ALL IC'S	0	1	1	Location Zero	Location Zero	0	1
READ / WRITE	1	X	1	X	X	X	X

NOTE: 1) $\overline{XI}$ is connected to $\overline{XO}$ of previous device.
2) See definition on Pin Description for $\overline{RS}$, $\overline{FL}$, $\overline{XI}$, $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$.

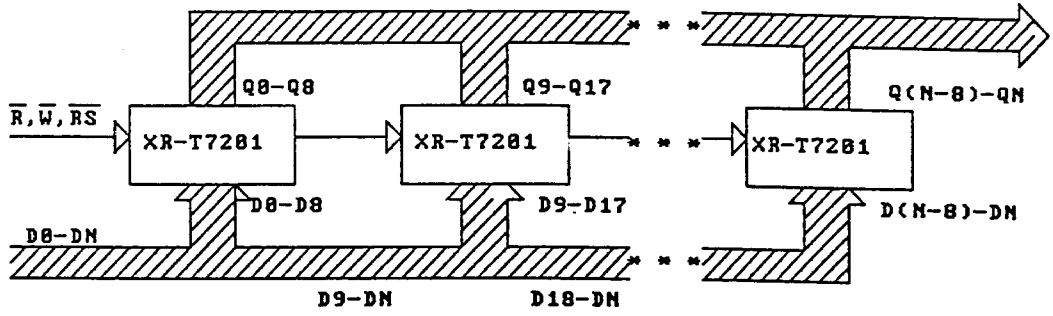


Figure 4. Block Diagram using a Compounded Depth Expansion Approach

BIDIRECTIONAL MODE

For applications that require data buffering between two systems which use independent read and write operations, care must be taken to insure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both, Depth and Width Expansion Modes can be used in this mode.

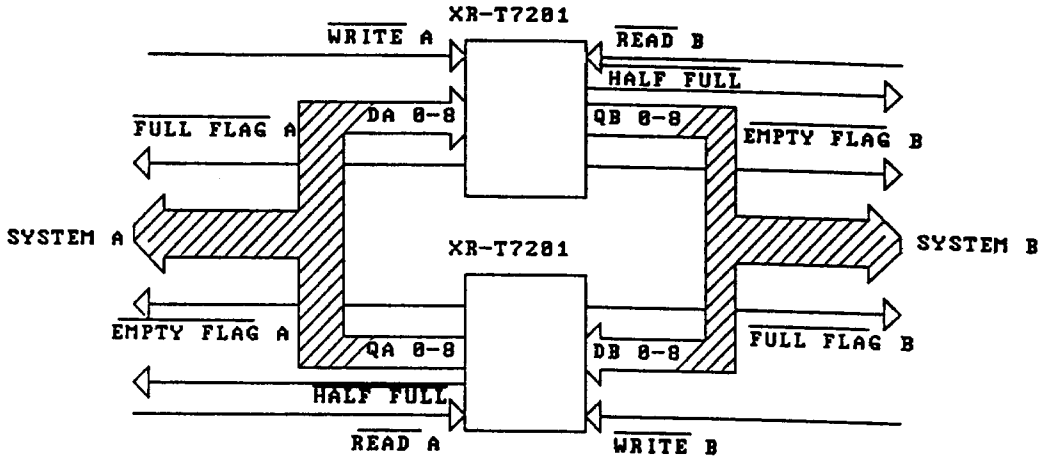


Figure 5. Bidirectional FIFO Mode

DATA FLOW THRU MODE

The XR-T7201-3 allows for two types of flow through modes:

- A read flow through mode permits a reading of a single word of data immediately after writing one word of data into the completely empty FIFO.
- A write flow through mode permits a writing of a single word of data immediately after reading one word of data from a completely full FIFO.

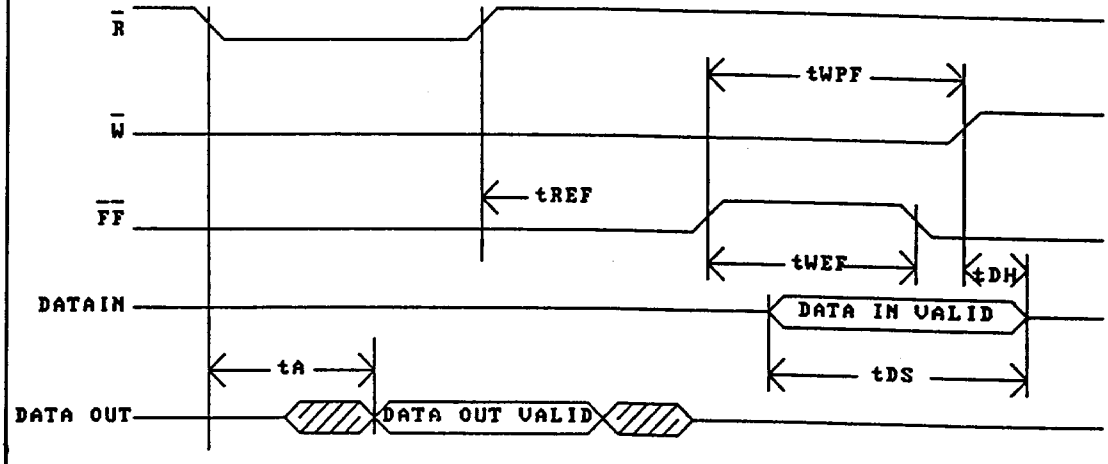


Figure 6. Write Flow Through Mode

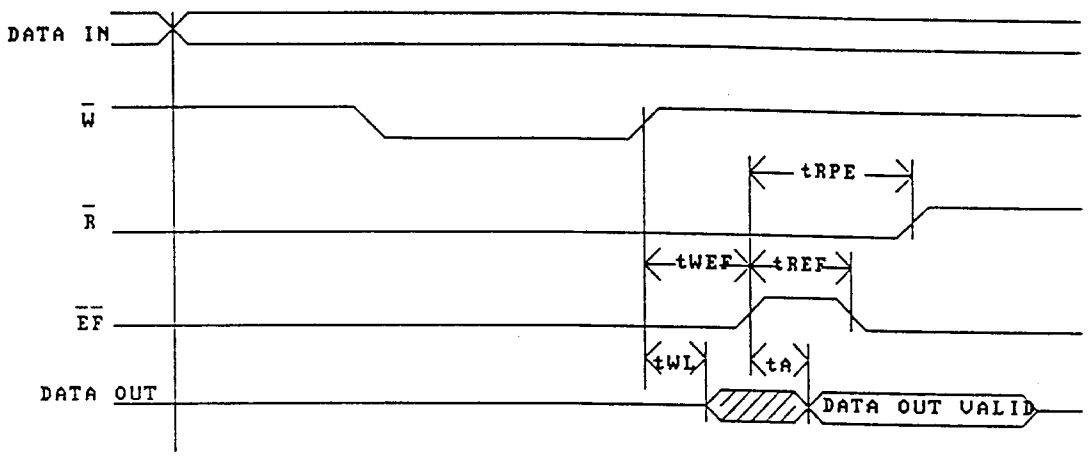


Figure 7. Read Flow Through Mode

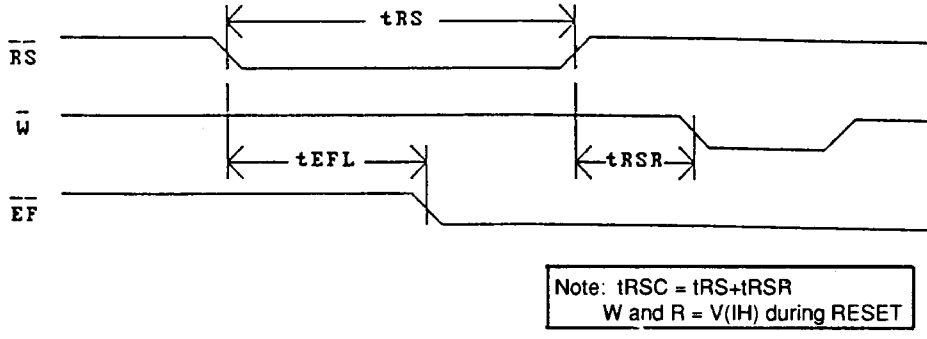


Figure 8. Reset Timing

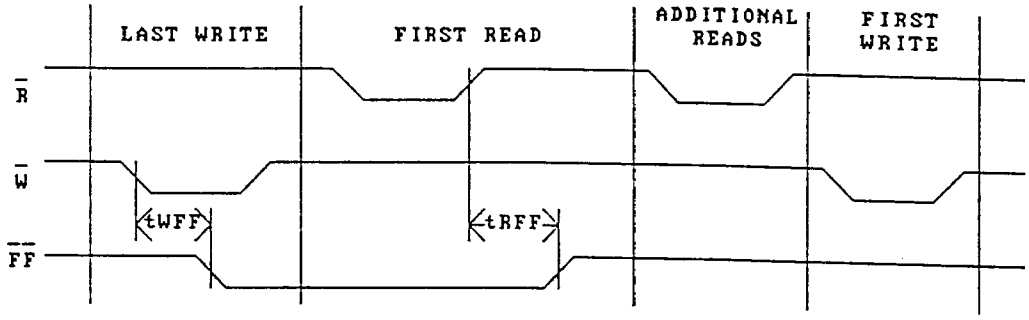


Figure 9. Full Flag From Last Write To First Read

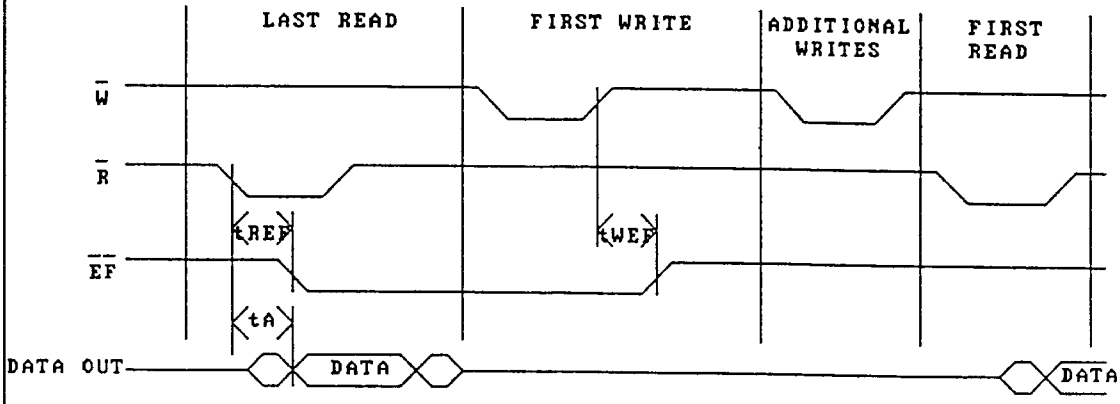
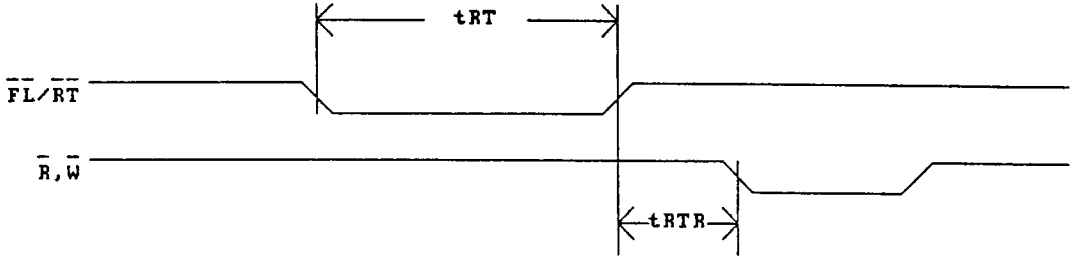


Figure 10. Empty Flag From Last Read To First Write



Note: 1) tRTC = tRT + tRTR
2) EF, HF, and FF may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at tRTC.

Figure 11. Retransmit

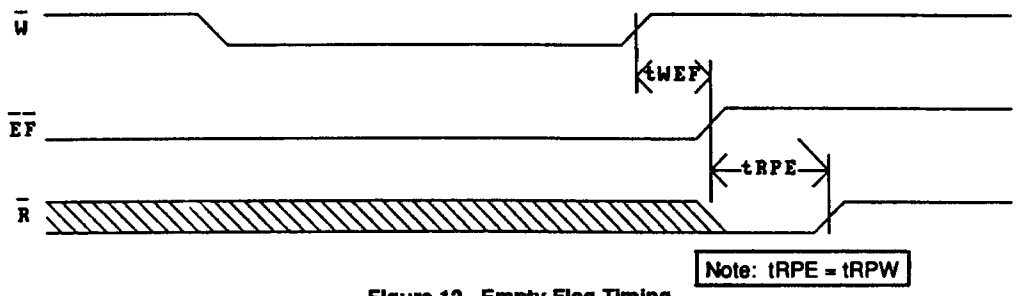


Figure 12. Empty Flag Timing

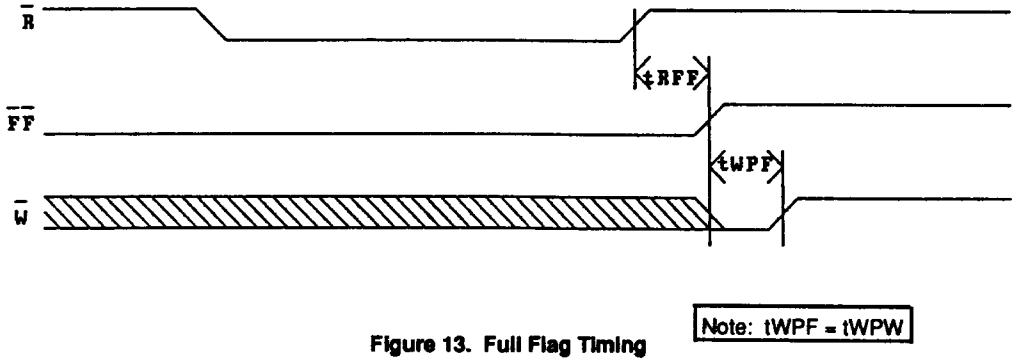


Figure 13. Full Flag Timing

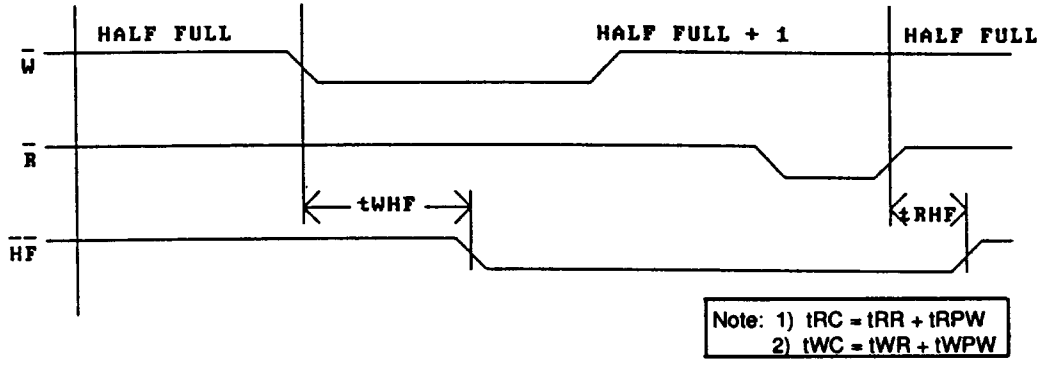


Figure 14. Half Full Flag Timing

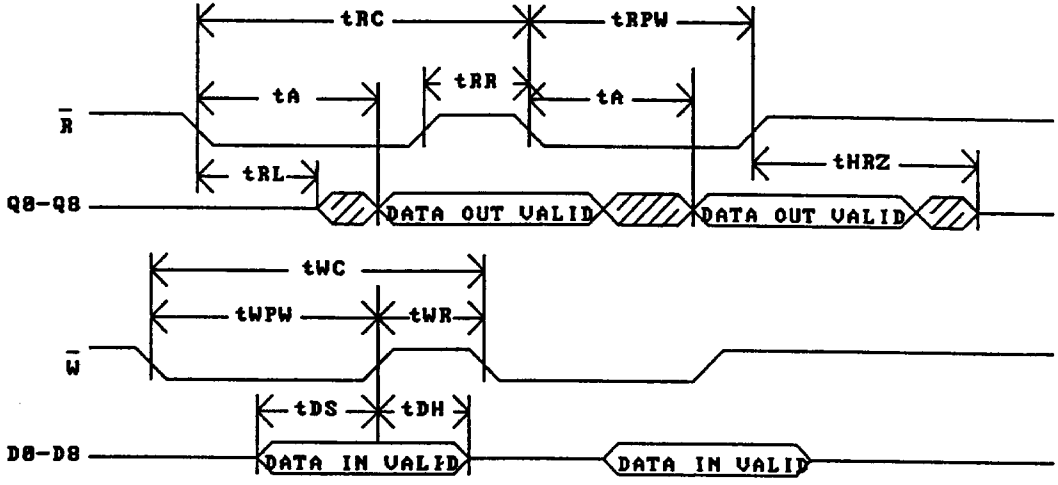


Figure 15. Asynchronous Write And Read Operation