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**About the change in the name such as "Oki Electric Industry Co. Ltd." and "OKI" in documents to OKI Semiconductor Co., Ltd.**

The semiconductor business of Oki Electric Industry Co., Ltd. was succeeded to OKI Semiconductor Co., Ltd. on October 1, 2008. Therefore, please accept that although the terms and marks of "Oki Electric Industry Co., Ltd.", "Oki Electric", and "OKI" remain in the documents, they all have been changed to "OKI Semiconductor Co., Ltd.". It is a change of the company name, the company trademark, and the logo, etc. , and NOT a content change in documents.

October 1, 2008  
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# MSC1212-01

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## 48-Bit Grid/Anode Driver

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### GENERAL DESCRIPTION

The MSC1212-01 is a driver IC for VFD implemented in BiCMOS technology.

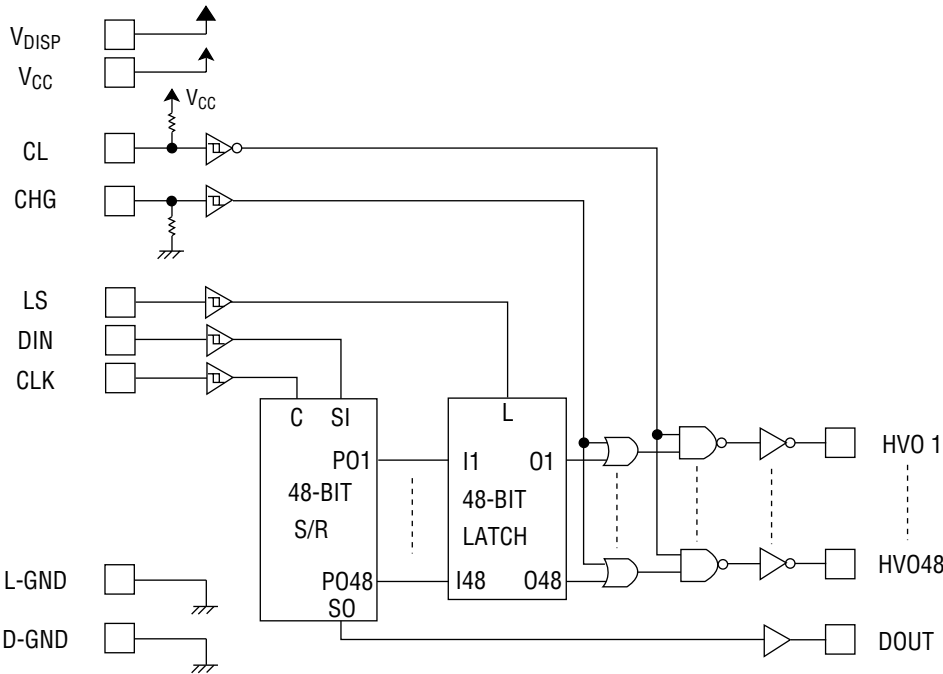
The circuit consists of a 48-bit shift register and a 48-bit latch; they control display data, which is output from the display drivers.

Since a 64-pin plastic QFP package is used, the display unit size can be reduced.

### FEATURES

- Logic supply voltage ( $V_{CC}$ ) : 4.5 to 5.5 V
- Driver supply voltage ( $V_{DISP}$ ) : 8 to 18 V
- Operating temperature range : -40 to +105°C
- Driver output current :  $I_{O2-1} = -6$  mA (for only one driver on state)  
 $I_{O2-2} = -50$  mA (total current for all drivers on state)  
 $I_{O2-3} = 0.2$  mA
- Built-in 48-bit output Driver (with latch)
- Built-in 48-bit shift register
- Clock frequency : 0.5 MHz
- Package:  
64-pin plastic QFP (QFP64-P-1414-0.80-BK) (Product name: MSC1212-01GS-BK)

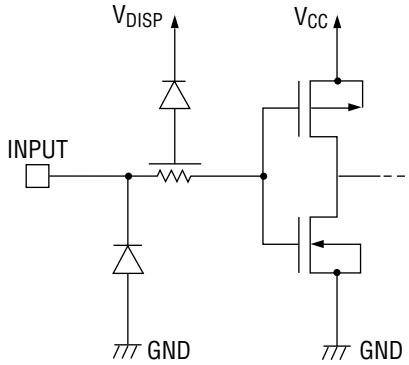
BLOCK DIAGRAM



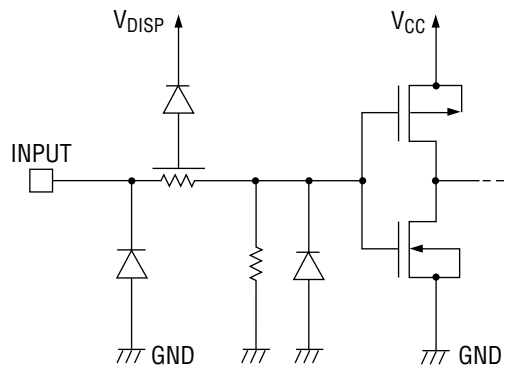
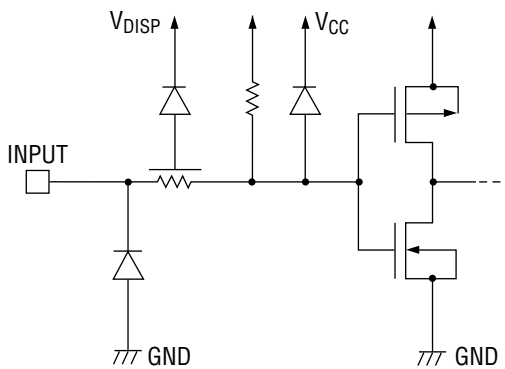


## INPUT AND OUTPUT CONFIGURATION

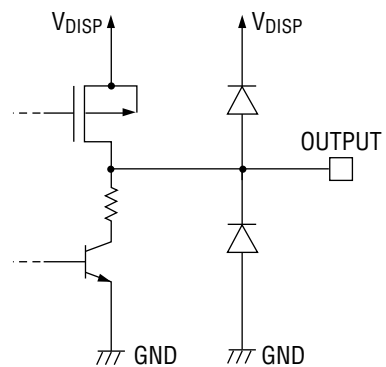
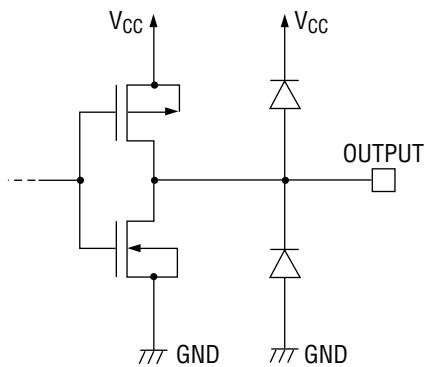
- Schematic Diagrams of Logic Portion Input Circuit



- Schematic Diagrams of Logic Portion Input Circuit (Pull-up)
- Schematic Diagrams of Logic Portion Input Circuit (Pull-down)



- Schematic Diagrams of Logic Portion Output Circuit
- Schematic Diagrams of Driver Output Circuit



## PIN DESCRIPTION

Function	Pin	Symbol	Description
Driver Output	1 to 17 32 to 48 50 to 63	HVO1 to HVO48	Driver output pins, applicable to each bit of shift register.
Driver Power Supply	19, 30	V <sub>DISP</sub>	Power supply pins for driver circuit. Both Pin 19 and 30 should be connected externally.
Logic Power Supply	27	V <sub>CC</sub>	Power supply pin for logic.
Driver GND	20, 29	D-GND	GND pins for the driver circuit. Both Pin 20 and 29 should be connected externally.
Logic GND	21	L-GND	GND pin for the logic circuit.
Data Input	22	DIN	Input pin without pull-up or pull-down resistor. Input pin of shift register. Display data input is synchronized with clock signal. (positive logic)
Clock Input	23	CLK	Input pin without pull-up or pull-down resistor. Data of shift register is shifted from one stage to the next on application of each clock rising edge.
Latch Strobe Input	24	LS	Input pin without pull-up or pull-down resistor. When LS is at "H" level, the latch is shunted and the shift register output becomes the latched output. When LS is at "L" level, the latch holds the shift register output just before LS goes to "L" level.
Clear Input	25	CL	Clear input pin with pull-up resistor. Normally "L" level. In this condition, driver output changes to "H" or "L" according to latch output level. When CL is "H", all driver output pins are fixed to "L".
Test Input	26	CHG	Test input pin with pull-down resistor. Normally "L" level, but here, if CL="H", then driver output changes to "H" or "L" according to latch output level. If CL = "L" when CHG is at "H" level, all driver output is fixed to "H" for test.
Data Output	28	DOUT	Serial output pin of shift register.

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition	Rating	Unit
Logic Supply Voltage *1	$V_{CC}$	—	-0.3 to +6.5	V
Driver Supply Voltage *1, *2	$V_{DISP}$	—	-0.3 to +20	V
Input Voltage *1	$V_{IN}$	Applicable to all input pins	-0.3 to $V_{CC} + 0.3$	V
Data Output Voltage *1	$V_{O1}$	Applicable to data output pin	-0.3 to $V_{CC} + 0.3$	V
Driver Output Voltage *1	$V_{O2}$	Applicable to driver output pin	-0.3 to $V_{DISP} + 0.3$	V
Power Dissipation	$P_D$	$T_a \leq 25^\circ\text{C}$	1.0	W
Thermal Resistance *3	$R_{j-a}$	—	120	$^\circ\text{C}/\text{W}$
Storage Temperature	$T_{STG}$	—	-55 to +150	$^\circ\text{C}$

\*1 Maximum supply voltage with respect to L-GND and D-GND

\*2 Catastrophic breakdown may occur if the applied voltage is more than the rating.

\*3 Thermal resistance of package (between junction and atmosphere)

The junction temperature ( $T_j$ ) given by the following formula should not exceed  $150^\circ\text{C}$ .

$$T_j = P \times R_{j-a} + T_a \quad (P \text{ is the maximum power dissipation})$$

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Condition	Min.	Max.	Unit
Logic Supply Voltage	$V_{CC}$	Applicable to logic supply voltage pin	4.5	5.5	V
Driver Supply Voltage	$V_{DISP}$	Applicable to driver supply voltage pin	8	18	V
High Level Input Voltage	$V_{IH}$	Applicable to all input pins	$0.8 V_{CC}$	—	V
Low Level Input Voltage	$V_{IL}$	Applicable to all input pins	—	$0.2 V_{CC}$	V
Logic Output Current	$I_{O1}$	Applicable to DOUT pin	-0.1	0.1	mA
Driver High Level Output Current	$I_{O2-1}$	Only one driver is ON state	—	-6	mA
	$I_{O2-2}$	Total current at all driver outputs are ON state	—	-50	mA
Driver Low Level Output Current	$I_{O2-3}$	Applicable to all driver output pins	—	0.2	mA
CLK Frequency	$f_{CLK}$	See Timing Diagram	—	0.5	MHz
Data Setup Time	$t_{DS}$	See Timing Diagram	400	—	ns
Data Hold Time	$t_{DH}$	See Timing Diagram	300	—	ns
LS Pulse Width	$t_{WLS}$	See Timing Diagram	125	—	ns
CHG Pulse Width	$t_{WCHG}$	See Timing Diagram	10	—	$\mu$ s
CL Pulse Width	$t_{WCL}$	See Timing Diagram	10	—	$\mu$ s
CLK Pulse Width	$t_{WCLK}$	See Timing Diagram	500	—	ns
CLK-LS Delay Time	$t_{DCLK-LS}$	See Timing Diagram	525	—	ns
LS-CLK Delay Time	$t_{DLS-CLK}$	See Timing Diagram	0	—	ns
LS-CHG Delay Time	$t_{DLS-CHG}$	See Timing Diagram	0	—	ns
LS-CL Delay Time	$t_{DLS-CL}$	See Timing Diagram	0	—	ns
Operating Temperature	$T_{op}$	—	-40	105	$^{\circ}$ C

## ELECTRICAL CHARACTERISTICS

### DC Characteristics

( $V_{CC} = 4.5$  to  $5.5$  V,  $V_{DISP} = 8$  to  $18$  V,  $T_a = -40$  to  $+105^{\circ}\text{C}$ )

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Logic Power Supply Current	$I_{CC1}$	No Load	$f_{CLK} = 0$ Hz	—	2	4	mA
	$I_{CC2}$		$f_{CLK} = 0.5$ MHz	—	4	6	
Driver Power Supply Current	$I_{DISP}$	No Load		—	—	5	$\mu\text{A}$
High Level Input Threshold Voltage	$V_P$	All input pins	$V_{CC} = 4.5$ V	2.4	2.75	—	V
			$V_{CC} = 5.5$ V	2.9	3.25	—	V
Low Level Input Threshold Voltage	$V_N$	All input pins	$V_{CC} = 4.5$ V	—	1.75	2.1	V
			$V_{CC} = 5.5$ V	—	2.25	2.6	V
Hysteresis Voltage	$V_H$	All input pins		0.3	1	—	V
High Level Input Current	$I_{IH1}$	$V_I = V_{CC}$	CHG pin	100	—	600	$\mu\text{A}$
	$I_{IH2}$		Input pins except CHG pin	-1	—	1	$\mu\text{A}$
Low Level Input Current	$I_{IL1}$	$V_I = 0$ V	CL pin	-600	—	-100	$\mu\text{A}$
	$I_{IL2}$		Input pins except CL pin	-1	—	1	$\mu\text{A}$
High Level Data Output Current	$I_{OH1}$	$V_{CC} - V_{OH1} = 1.0$ V		-0.1	—	—	mA
Low Level Data Output Current	$I_{OL1}$	$V_{OL1} = 1.0$ V		0.1	—	—	mA
Driver High Level Output Current	$I_{OH2}$	Only one driver is ON state $V_{DISP} - V_{OH2} = 1.0$ V		-6	—	—	mA
Driver Low Level Output Current	$I_{OL2}$	$V_{OL2} = 1.0$ V		0.2	—	—	mA
Voltage Difference Between GND Pins	$V_{GND}$	Voltage difference between D-GND and L-GND *1		-0.1	0	0.1	V

\*1 Pin D-GND and Pin L-GND are not connected internally.

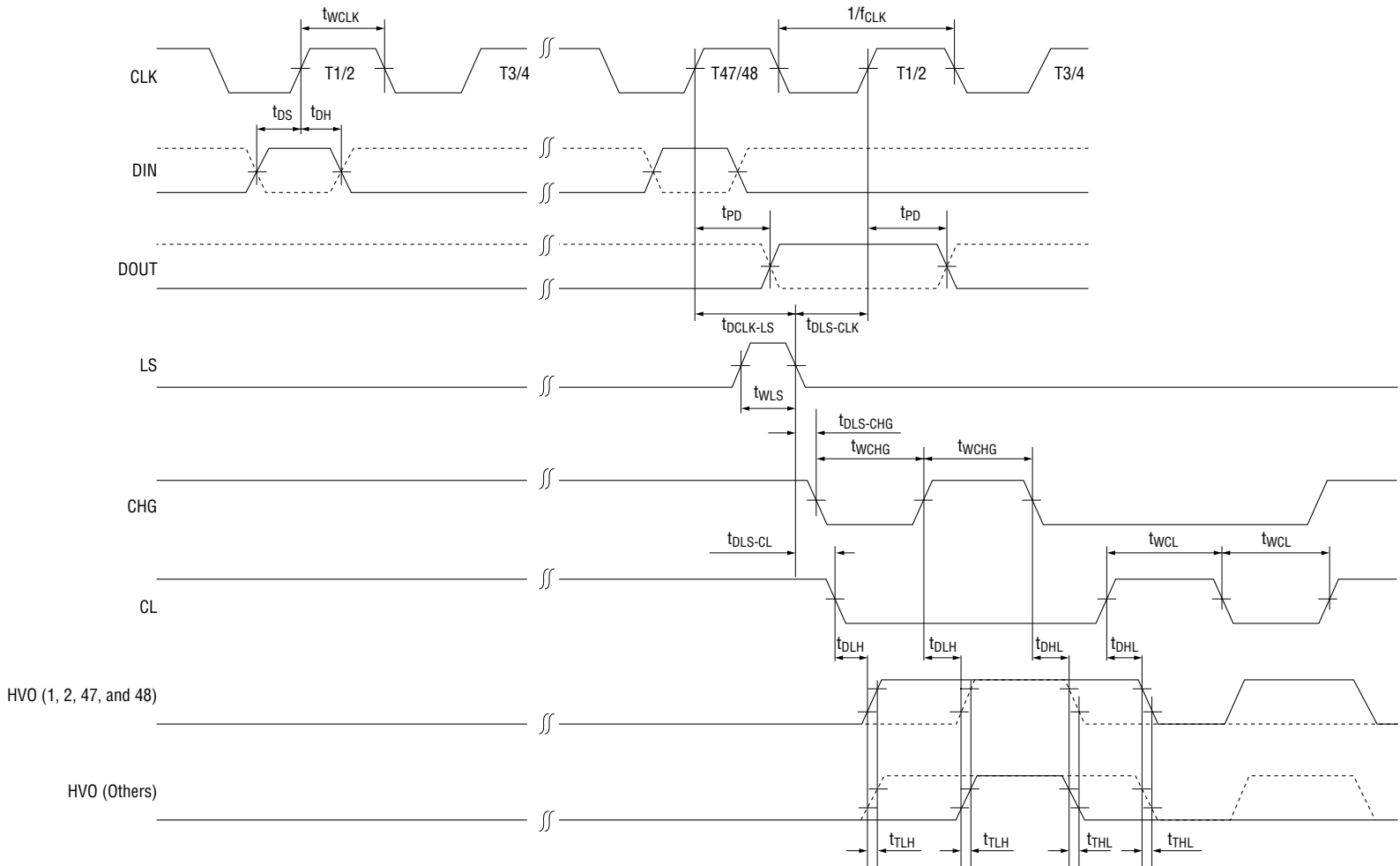
Therefore, set the voltage between D-GND and L-GND at the same level by connecting both pins externally.

### AC Characteristics

( $V_{CC} = 4.5$  to  $5.5$  V,  $V_{DISP} = 8$  to  $18$  V,  $T_a = -40$  to  $+105^{\circ}\text{C}$ )



Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLK-Dout Delay Time	$t_{PD}$	See Timing Diagram	0.3	—	1.6	$\mu\text{s}$
Delay Time Low $\rightarrow$ High	$t_{DLH}$	See Timing Diagram	—	1.0	2.0	$\mu\text{s}$
Transit Time Low $\rightarrow$ High	$t_{TLH}$	See Timing Diagram	—	2.0	5.0	$\mu\text{s}$
Delay Time High $\rightarrow$ Low	$t_{DHL}$	See Timing Diagram	—	1.0	2.0	$\mu\text{s}$
Transit Time High $\rightarrow$ Low	$t_{THL}$	See Timing Diagram	—	2.0	5.0	$\mu\text{s}$

**TIMING DIAGRAM**



## FUNCTIONAL DESCRIPTION

### Function Table

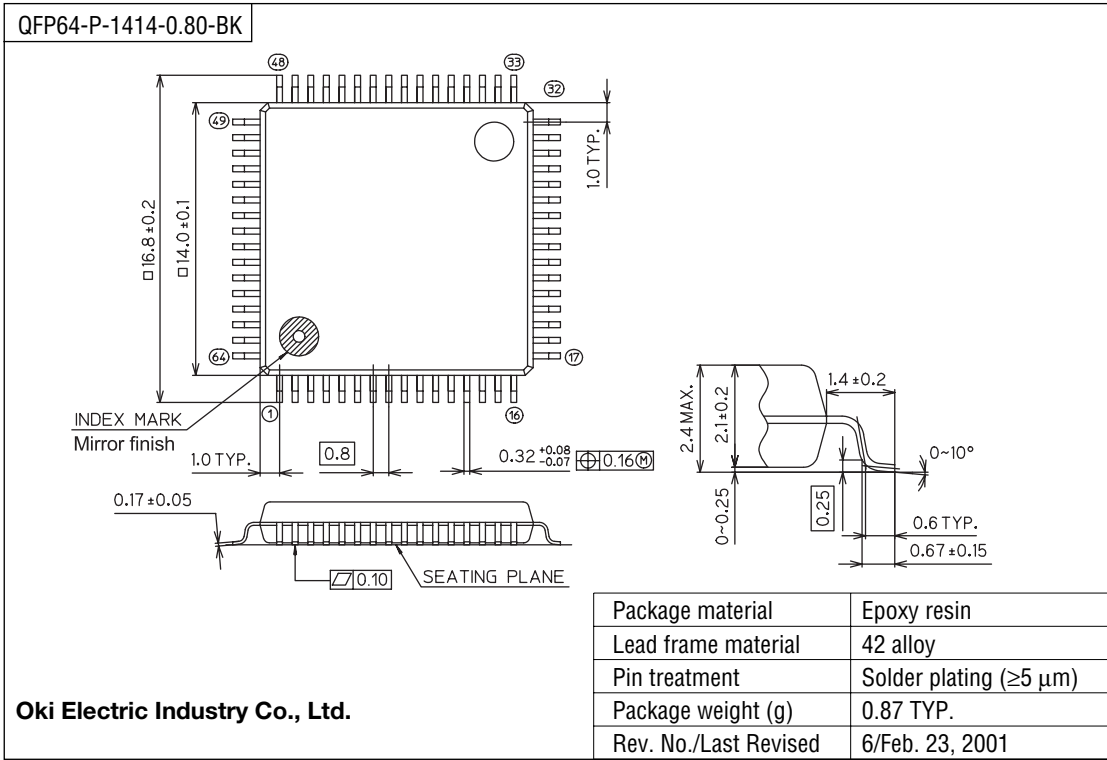
CLOCK	DIN	P01	P02	P03	P04	.....	P046	P047	P048	DOUT
	H	H	P01k	P02k	P03k	.....	P045k	P046k	P047k	P047k
	L	L	P01k	P02k	P03k	.....	P045k	P047k	P047k	P047k

CL	CHG	LS	P0n	HV0n
H	X	X	X	L
L	H	X	X	H
L	L	H	H	H
L	L	H	L	L
L	L	L	X	NC

L: Low Level, H: High Level, X: Don't Care, NC: No Change

PACKAGE DIMENSIONS

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki’s responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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