TM4256EQ5, TM4257EQ5
262,144 BY 5-BIT DYNAMIC RAM MODULES

OCTOBER 1985– REVISED NOVEMBER 1985

- 262,144 X 5 Organization
- Single 5-V Supply (10% Tolerance)
- 24-Pin Single-in-Line Package (SIP)
- Utilizes Five 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

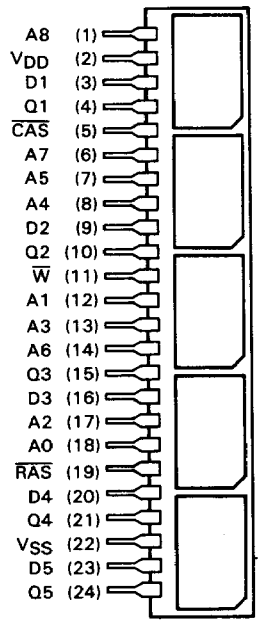
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
TM425_EQ5-12	120 ns	60 ns	230 ns	275 ns
TM425_EQ5-15	150 ns	75 ns	260 ns	305 ns
TM425_EQ5-20	200 ns	100 ns	330 ns	370 ns

- Common $\overline{CAS}$ Control with Separate Data-Input and Output Lines
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM425_EQ5-12	1625 mW	65 mW
TM425_EQ5-15	1375 mW	65 mW
TM425_EQ5-20	1125 mW	65 mW

- Operating Free-Air Temperature . . . 0°C to 70°C
- Downward Compatible with 64K X 5 Single-in-Line Package (TM4164EQ5)

Q SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D1-D5	Data Inputs
NC	No Connection
Q1-Q5	Data Outputs
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM425_EQ5 is a 1280K, dynamic random-access memory module organized as 262,144 × 5 bits in a 24-pin single-in-line package comprising five TMS425_FML, 262,144 × 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with five 0.1 μF decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing the TM425_EQ5 has a density of ten devices per square inch (approximately 4X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

The TM425_EQ5 features $\overline{RAS}$ access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation as low as 1125 mW typical operating and 65 mW typical standby.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

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All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM425_EQ5 is rated for operation from 0°C to 70°C.

operation

address (A0 through A8)

Eight address bits are required to decode 1 of 262,144 storage cell locations on each of the five chips. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, the data-outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data-in (D1-D5)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data-out (Q1-Q5)

The three-state output buffers provide direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The outputs become valid after the access time has elapsed and remain valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

The $\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CLRL}) and holding it low after $\overline{RAS}$ falls (see parameter t_{RLCHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

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hidden refresh

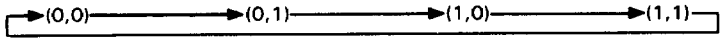
Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a "$\overline{RAS}$-only" refresh cycle. The external address is also ignored during the hidden refresh cycles.

page-mode (TM4256EQ5)

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single module, the row address and $\overline{RAS}$ are applied to multiple modules. $\overline{CAS}$ is then decoded to select the proper module.

nibble mode (TM4257EQ5)

Nibble-mode operation allows high-speed serial read, write, or read-modify-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time. The next sequential nibble bits can be read or written by cycling $\overline{CAS}$ while $\overline{RAS}$ remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Column A8 and row A8 (CA8, RA8) provide the two binary bits for initial selection of the nibble addresses. Thereafter, the falling edge of $\overline{CAS}$ will access the next bit of the circular 4-bit nibble in the following sequence:



In nibble-mode, all normal memory operations (read, write, or read-modify-write) may be performed in any desired combination.

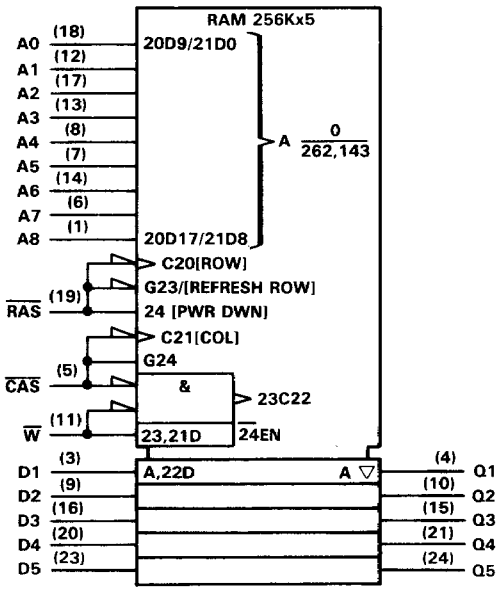
power up

To achieve proper device operation, an initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles.

single-in-line package and components

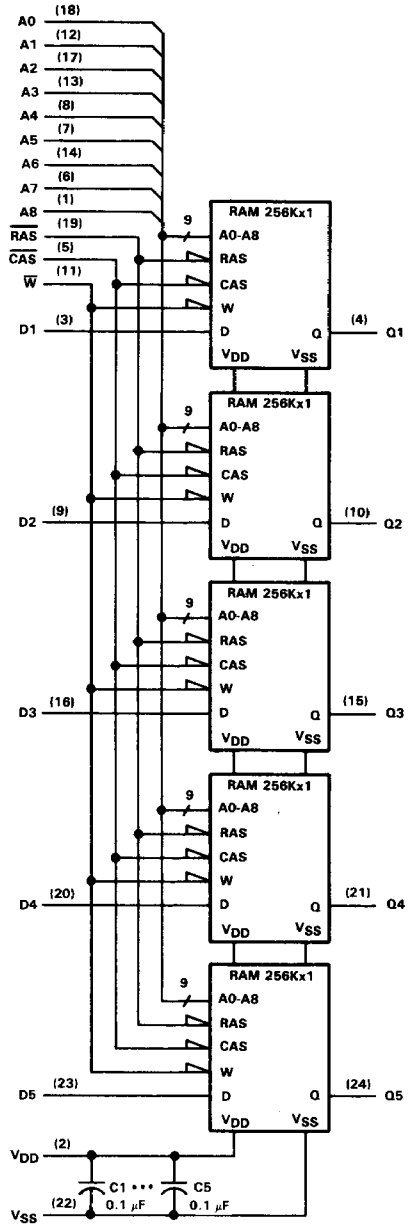
PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range for any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage range on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current for any output . . . . . 50 mA
Power dissipation . . . . . 5 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM425_EQ5-12			TM425_EQ5-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		V_{DD}	2.4		V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0		0.4	0		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		325	390		275	340	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		13	23		13	23	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		225	300		200	265	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		175	240		150	215	mA
I_{DD5}	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		160	220		135	160	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM425_EQ5-20			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		225	290	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		13	23	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		175	240	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		125	175	mA
I_{DD5}	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		110	160	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		35	pF
$C_{i(D)}$	Input capacitance, data inputs		35	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ input		40	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		40	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ input		40	pF
$C_{o(Q)}$	Output capacitance, data outputs		10	pF
$C_{o(VDD)}$	Decoupling capacitance	0.6		μF

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switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM425_EQ5-12		TM425_EQ5-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		60		75	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	35	0	35	ns

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM425_EQ5-20		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		100	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	35	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM425_EQ5-12		UNIT
			MIN	MAX	
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	120		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	165		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	275		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	50		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	60	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	120	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	40		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	40		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	80		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	35		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	35		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	35		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	95		ns

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

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timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TMS425_EQ5-12 MIN	TMS425_EQ5-12 MAX	UNIT
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	25		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	25		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RPC}	20		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	60		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	30	60	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	120		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

¶$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TM425_EQ5-15		TM425_EQ5-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	145		190		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	190		245		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	305		370		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	60		80		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		30		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	75	10,000	100	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	45		60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	45		60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	25		30		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	100		130		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	45		55		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	120		155		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	45		55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		15		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	45		55		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	120		155		ns

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

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timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TM425_EQ5-15		TM425_EQ5-20		UNIT
			MIN	MAX	MIN	MAX	
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	75		100		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	30		35		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	30		35		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RPC}	20		25		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	70		90		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	30	75	30	100	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	145		190		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.
¶$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

NIBBLE-MODE CYCLE

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TM4257EQ5-12		TM4257EQ5-15		TM4257EQ5-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CN)}$	Nibble-mode access time from $\overline{CAS}$	t_{NCAC}		30		40		50	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM4257EQ5-12		TM4257EQ5-15		TM4257EQ5-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(N)}$	Nibble-mode cycle time	t_{NC}	60		75		90		ns
$t_{c(rdWN)}$	Nibble-mode read-modify-write cycle time	t_{NRMW}	85		105		130		
t_{CLRHN}	Nibble-mode delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{NRSH}	30		40		50		
t_{CLWLN}	Nibble-mode delay time, $\overline{CAS}$ to $\overline{W}$ delay	t_{NCWD}	25		30		40		
$t_{w(CLN)}$	Nibble-mode pulse duration, $\overline{CAS}$ low	t_{NCAS}	30		40		50		
$t_{w(CHN)}$	Nibble-mode pulse duration, $\overline{CAS}$ high	t_{NCP}	20		25		30		
$t_{w(CRWN)}$	Nibble-mode read-modify-write pulse duration, $\overline{CAS}$ low	t_{NCRW}	55		70		90		
$t_{su(WCHN)}$	Nibble-mode write command setup time before $\overline{CAS}$ high	t_{NCWL}	25		35		45		

PARAMETER MEASUREMENT INFORMATION

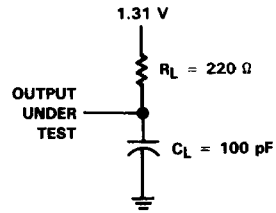
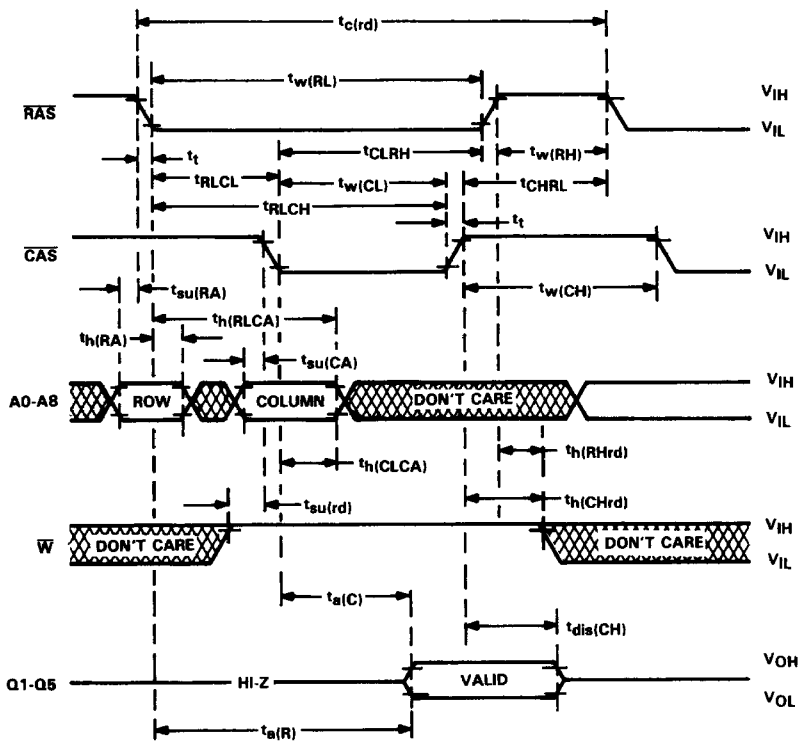


FIGURE 1. LOAD CIRCUIT

read cycle timing



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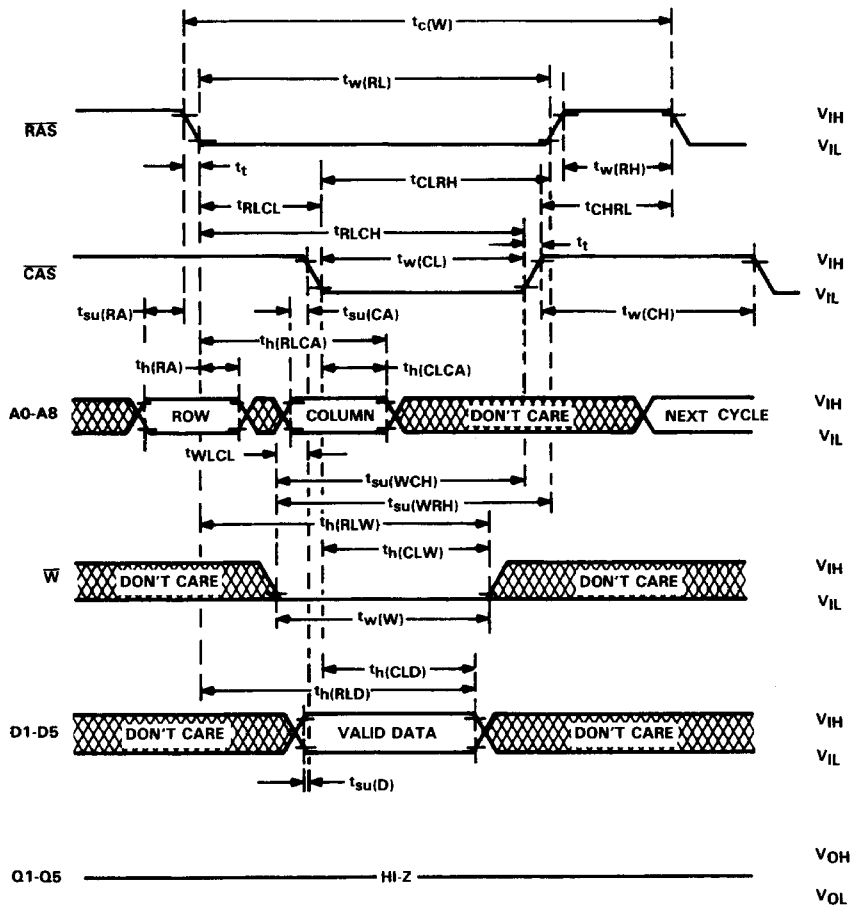
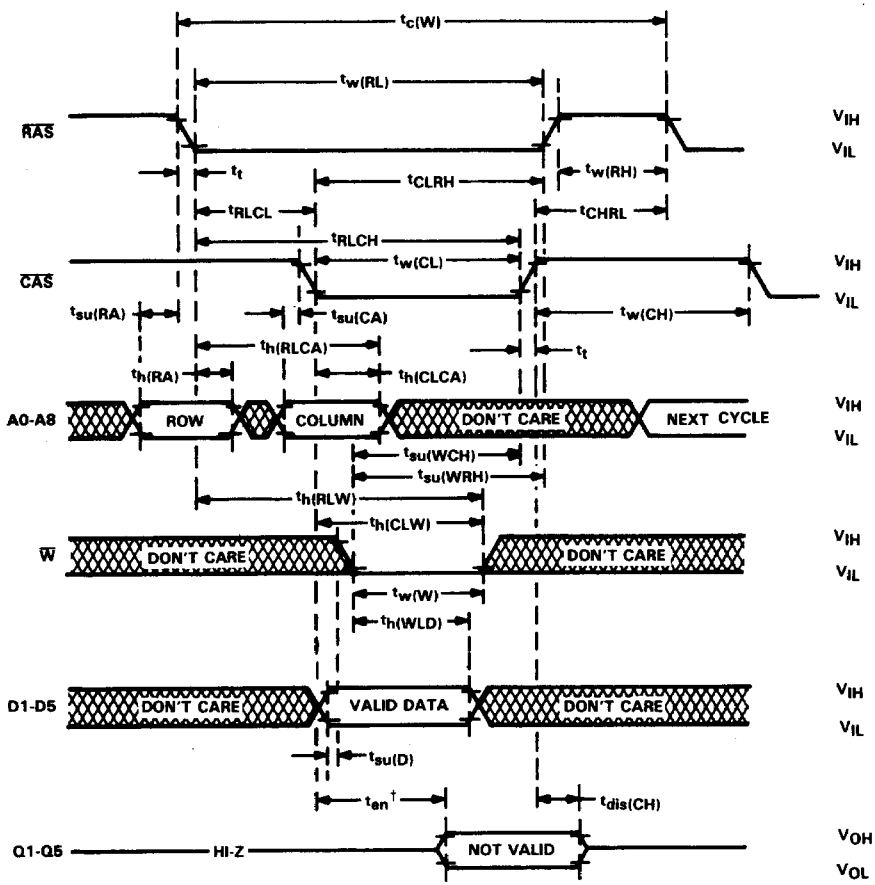
early write cycle timing

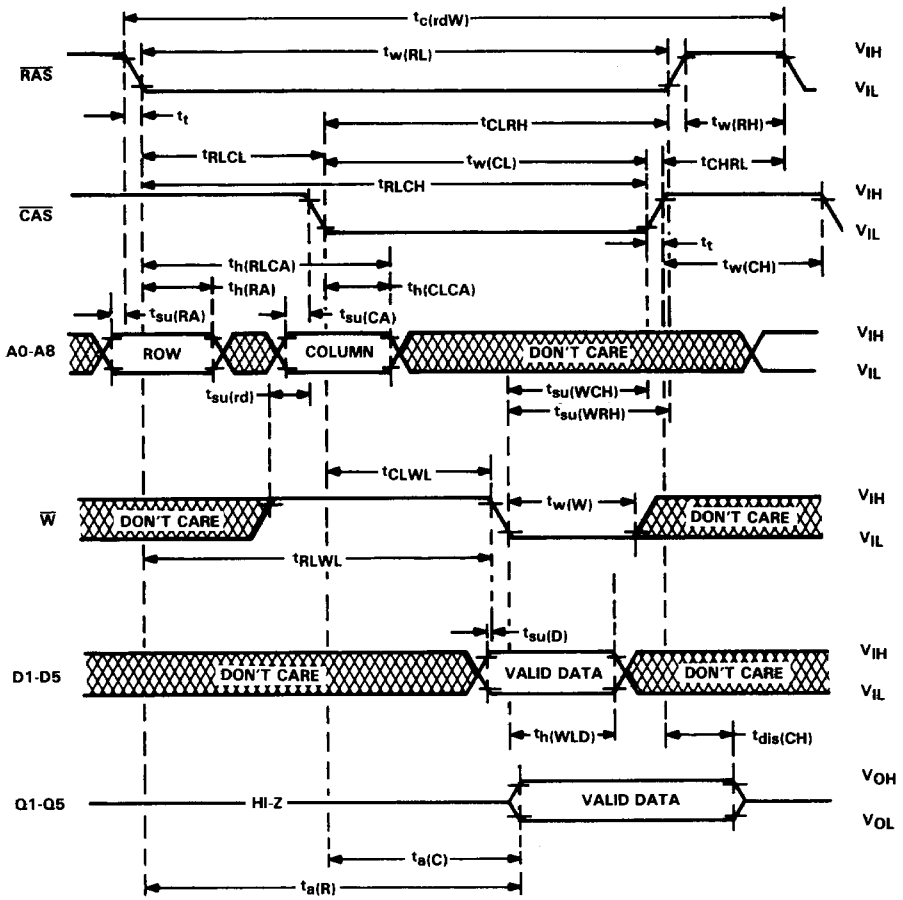


write cycle timing

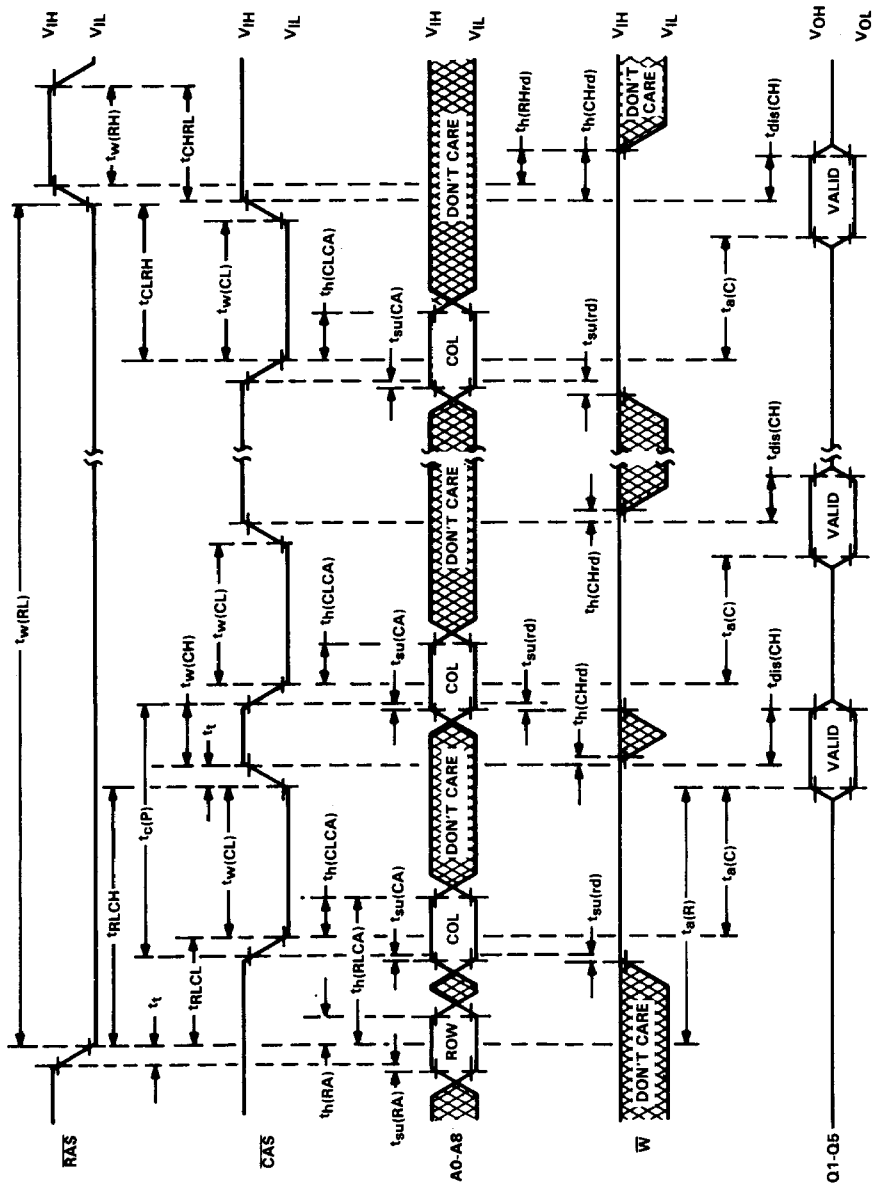


†The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

read-write/read-modify-write cycle timing

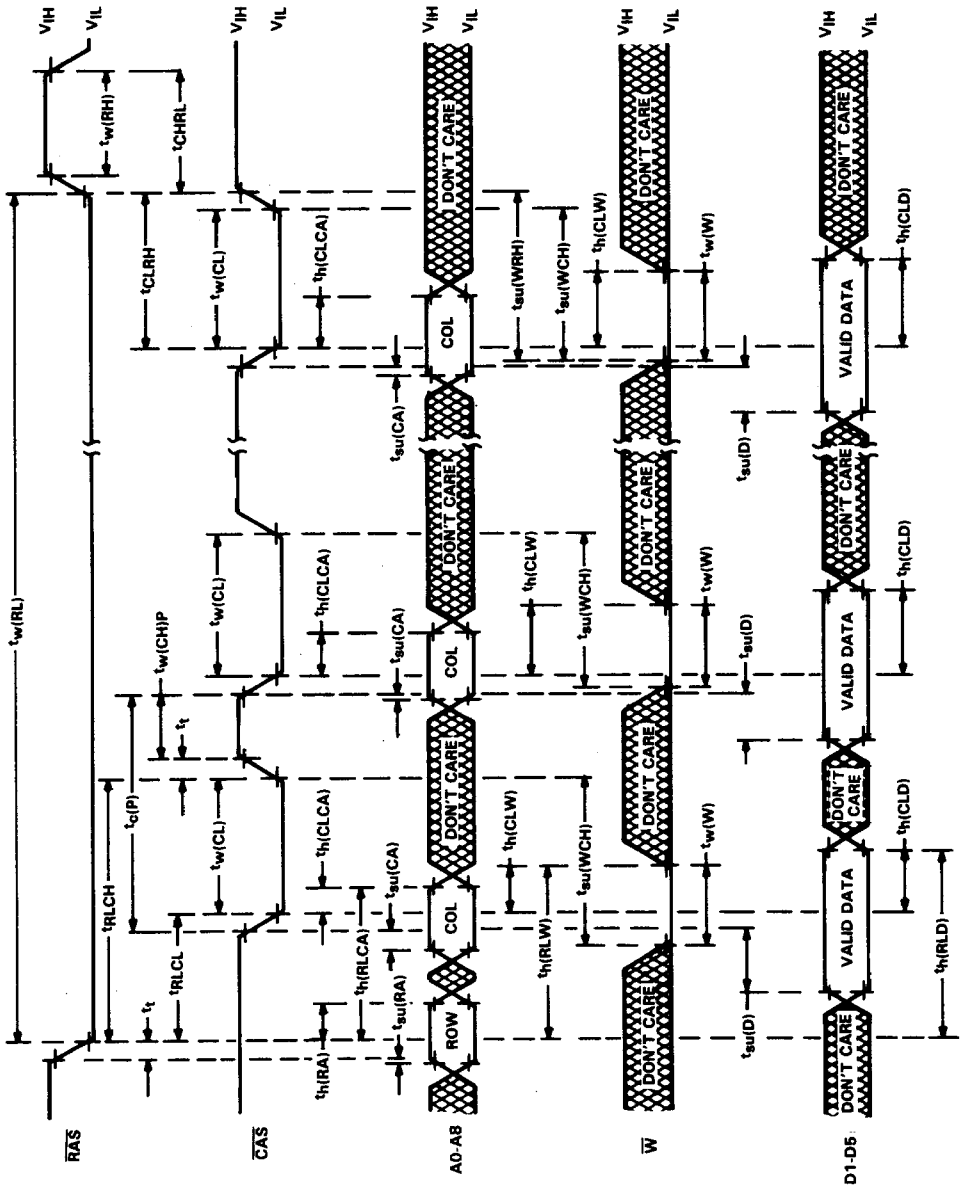


page-mode read cycle timing



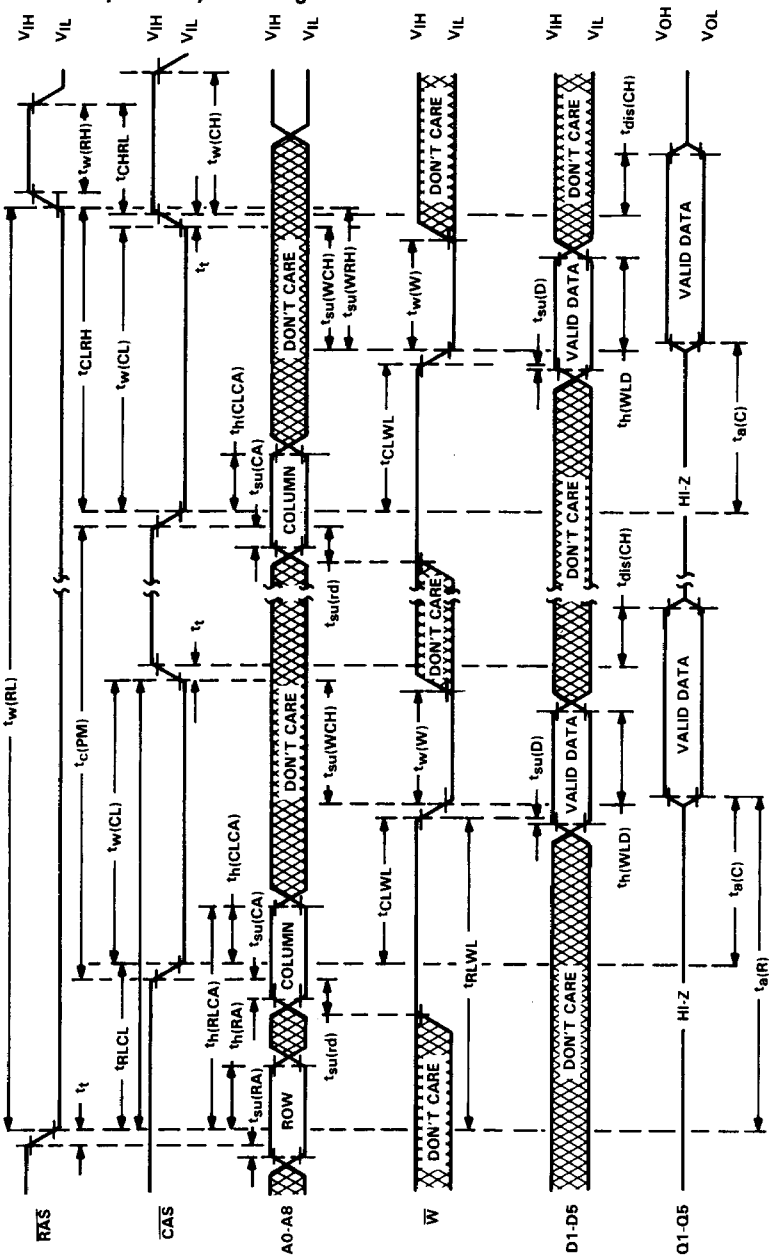
NOTE 4: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify write timing specifications are not violated.

page-mode write cycle timing



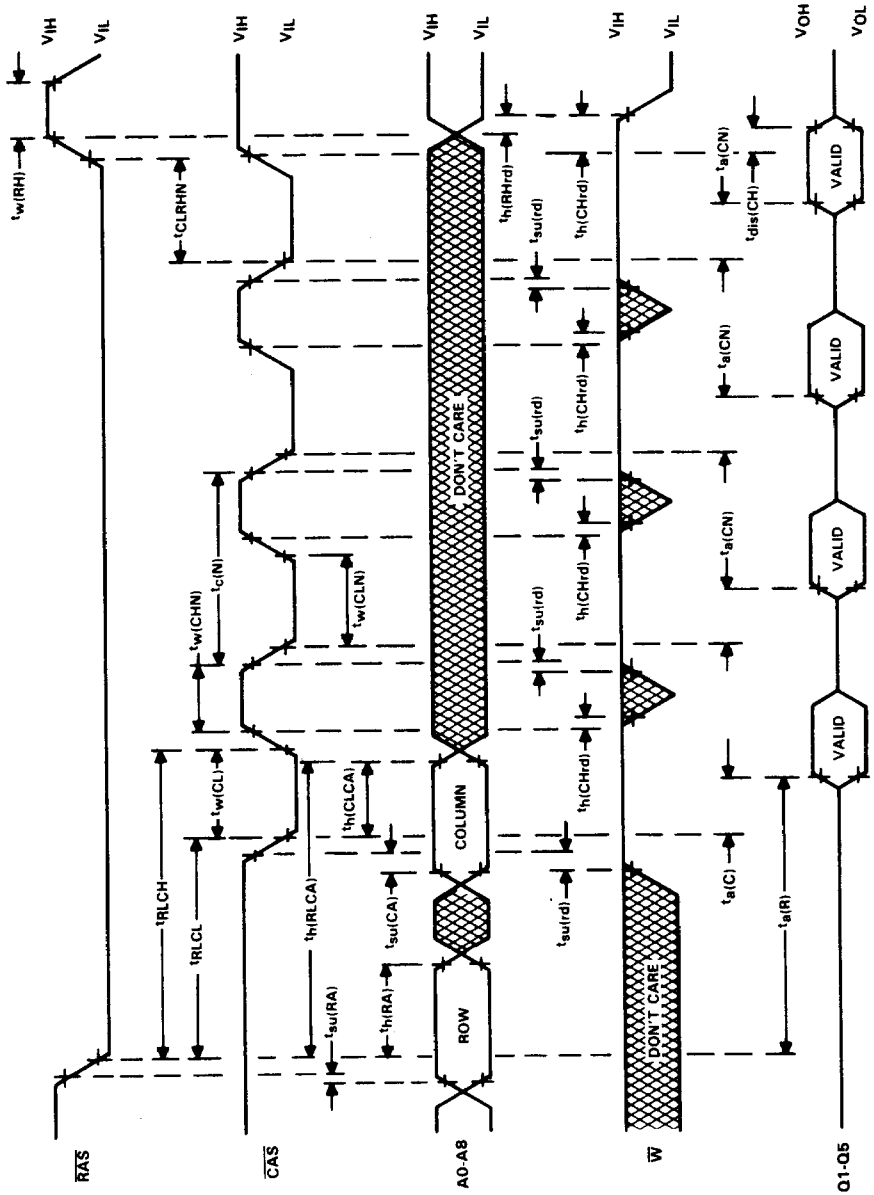
NOTE 5: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing

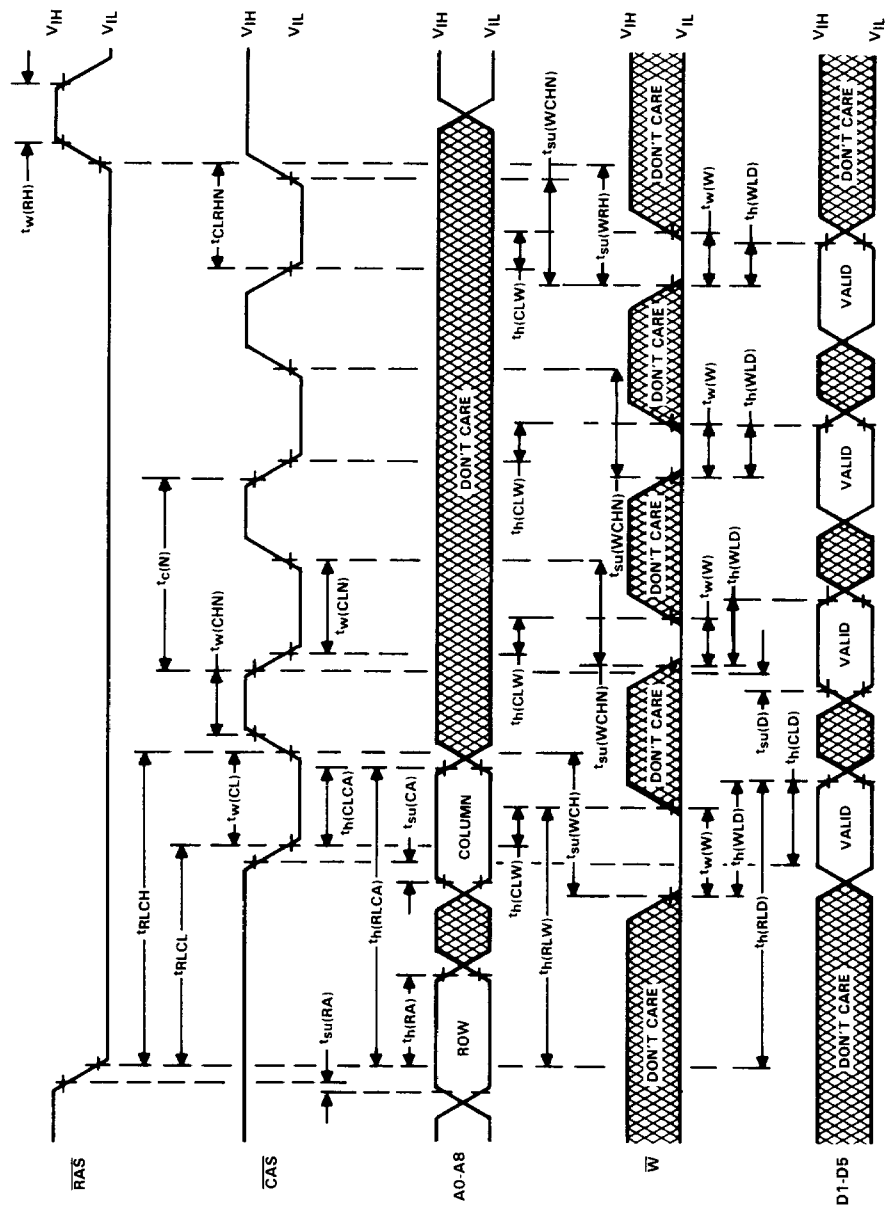


NOTE 6: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

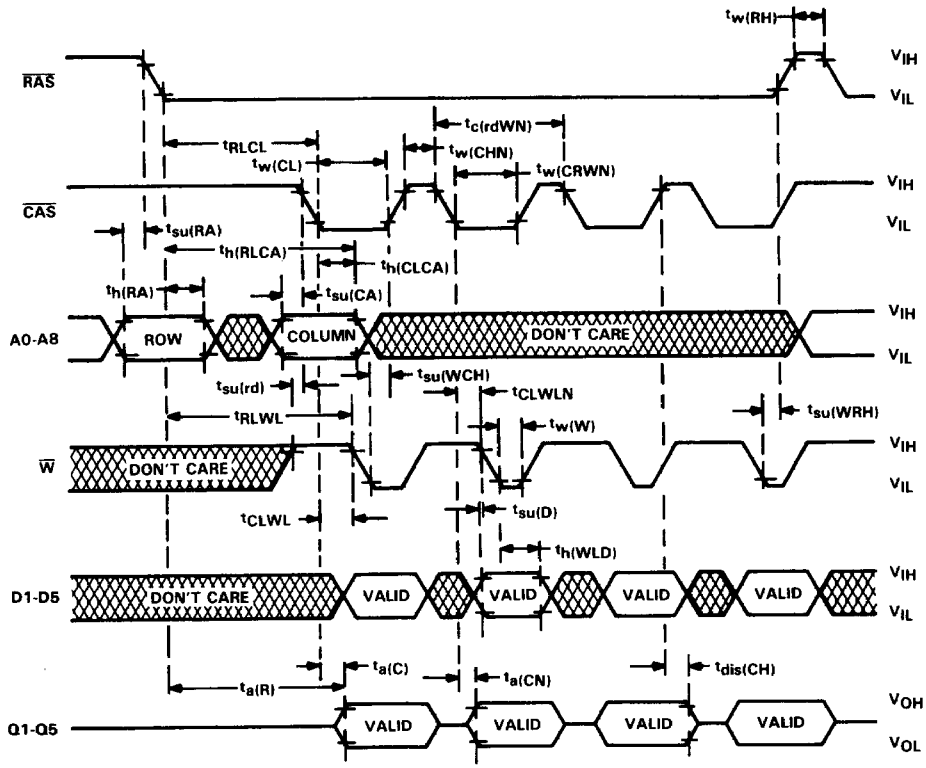
nibble-mode read cycle timing



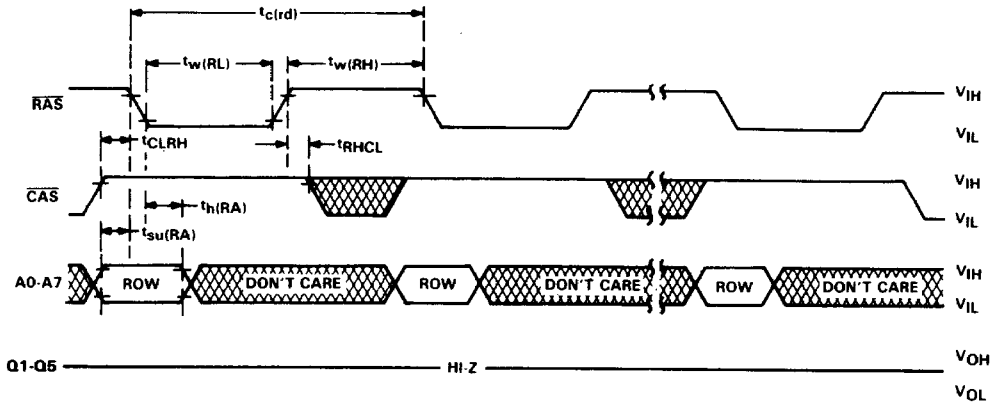
nibble-mode write cycle timing



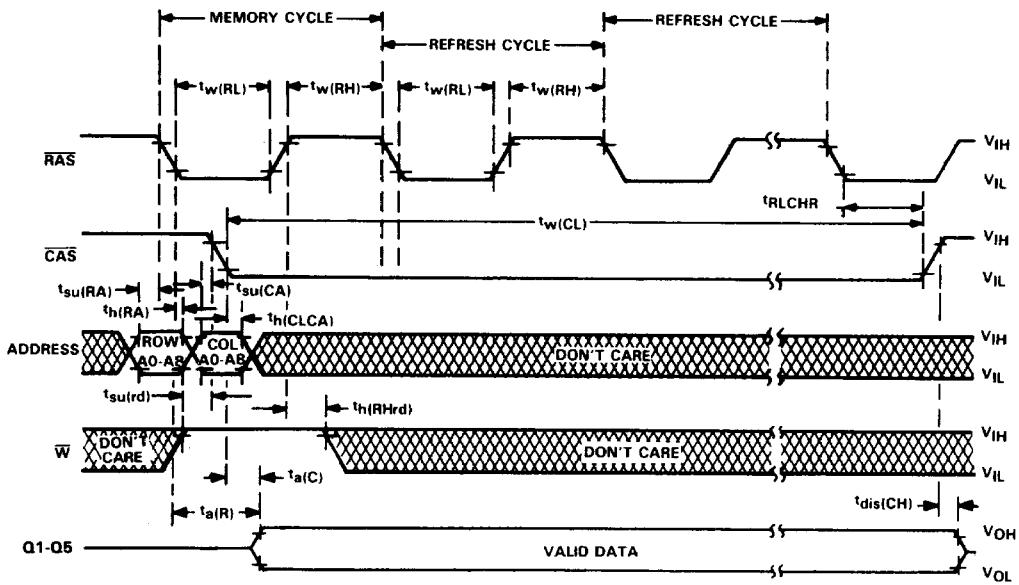
nibble-mode read-modify-write-cycle timing



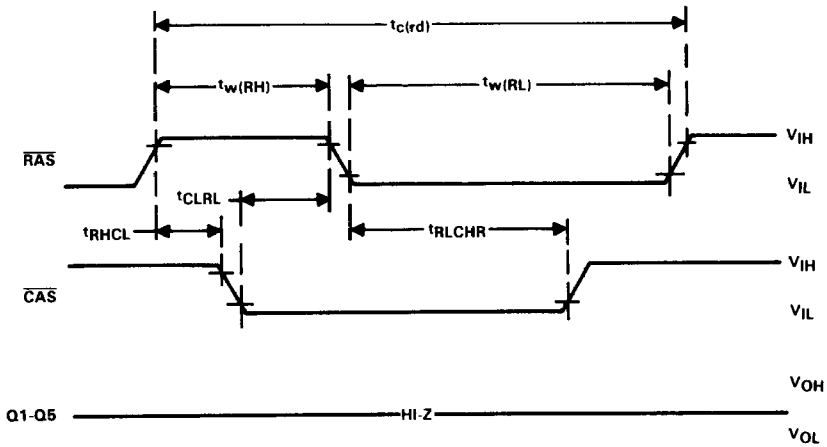
RAS-only refresh cycle timing



hidden refresh cycle timing



automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing



TI single-in-line package nomenclature