PIN DESCRIPTIONS

MC145026 ENCODER

A1/D1-A9/D9, ADDRESS/DATA INPUTS (PINS 1, 2, 3, 4, 5, 6, 7, 9, 10) – These inputs are encoded and the data is serially output from the encoder.

R_S, C_{TC}, R_{TC}, OSCILLATOR COMPONENTS (PINS 11, 12, 13) – These pins are part of the oscillator section of the encoder. If an external signal source is used instead of the internal oscillator, it should be connected to the R_S input and the R_{TC} and C_{TC} pins should be left open.

$\overline{TE}$, TRANSMIT-ENABLE INPUT (PIN 14) This active low input initiates transmission when forced low. An internal pullup device keeps this input normally high.

Data Out, DATA OUTPUT (PIN 15) – This is the output of the encoder that serially presents the encoded word.

V_{DD}, POSITIVE SUPPLY (PIN 16) – The most positive power supply.

V_{SS}, NEGATIVE SUPPLY (PIN 8) – The most negative supply (usually ground).

MC145027, MC145028, MC145029 DECODERS

A1-A5 (MC145027), A1-A9 (MC145028), A1-A4 (MC145029), ADDRESS INPUTS – These address inputs must match the corresponding encoder inputs in order for the decoder to output data.

D6-D9 (MC145027), D5-D9 (MC145029), DATA OUTPUTS – These outputs present the information that is on the corresponding encoder inputs. Note: only binary data will be acknowledged; a trinary open will be decoded as a logic one.

R_1, C_1, PULSE DISCRIMINATOR (PINS 6, 7) – These pins accept a resistor and capacitor that are used to determine whether a narrow pulse or a wide pulse has been encoded. The time constant $R_1 \times C_1$ should be set to 1.72 encoder (transmitter) clock periods. $R_1C_1 = 3.95\ R_{TC}C_{TC}$.

R_2/C_2, DEAD TIME DISCRIMINATOR (PIN 10) This pin accepts a resistor and a capacitor to V_{SS} that are used to detect both the end of an encoded word and the end of transmission. The time constant $R_2 \times C_2$ should be 33.5 encoder (transmitter) clock periods (four data bit periods): $R_2C_2 = 77\ R_{TC}C_{TC}$. This time constant is used to determine that Data In has remained low for four data bit times (end of transmission). A separate comparator looks at a voltage-equivalent two data bit times ($0.4\ R_2C_2$) to detect the dead time between transmitted words.

VT, VALID TRANSMISSION (PIN 11) – This output goes high when the following conditions are satisfied:

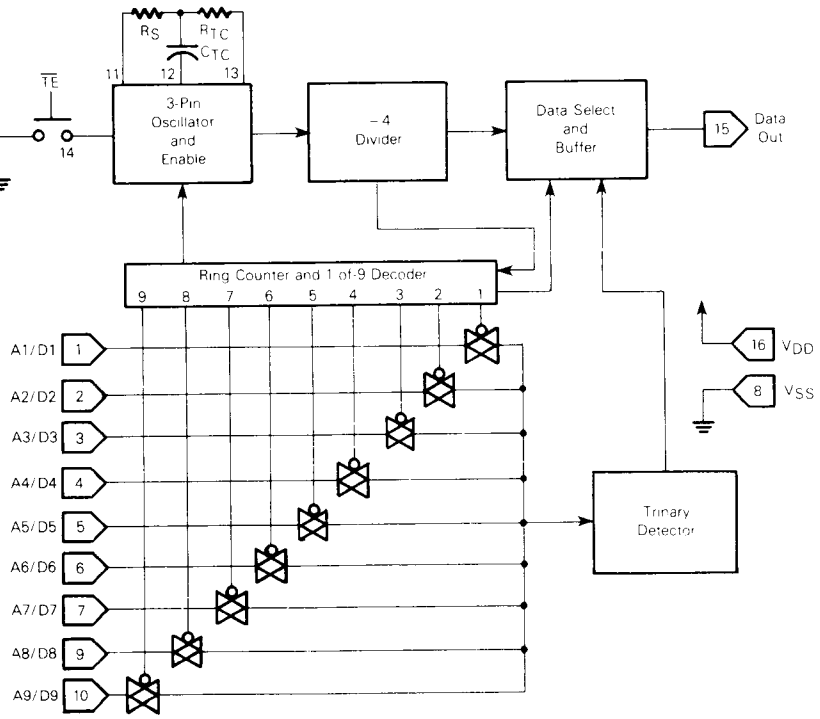
1. the transmitted address matches the receiver address, and
2. the transmitted data matches the last valid data received (MC145027 and MC145029, only).

VT will remain high until a mismatch is received, or no input signal is received for four data bit times.

V_{DD}, POSITIVE SUPPLY (PIN 16) – The most positive power supply.

V_{SS}, NEGATIVE SUPPLY (PIN 8) The most negative supply (usually ground).

FIGURE 1 – MC145026 ENCODER BLOCK DIAGRAM



TRANSMITTER—MC14457

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Output Voltage "0" Level $V_{in}=V_{DD}$ or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
		10	–	0.05	–	0	0.05	–	0.05	
$I_{out}=0\ \mu A$ "1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	V
		10	9.95	–	9.95	10	–	9.95	–	
Input Voltage # "0" Level	V_{IL}									V
(V_O = 4.5 or 0.5 V)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
"1" Level	V_{IH}									V
(V_O = 0.5 or 4.5 V)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 V)		10	7.0	–	7.0	5.50	–	7.0	–	
Output Drive Current — Pins 14, 15	I_{OH}									mA
(V_{OH} = 2.5 V) Source		5.0	−6.0	–	−5.0	−9.0	–	−3.5	–	
(V_{OH} = 9.5 V)		10	−3.2	–	−2.6	−4.5	–	−1.8	–	
(V_{OL} = 2.5 V) Sink	I_{OL}	5.0	6.0	–	5.0	9.0	–	3.5	–	mA
(V_{OL} = 0.5 V)		10	3.2	–	2.6	4.5	–	1.8	–	
Output Drive Current — Pin 13	I_{OH}									mA*
(V_{OH} = 4.6 V) Source		5.0	−0.26	–	−0.22	−0.44	–	−0.18	–	
(V_{OH} = 9.5 V)		10	−0.6	–	−0.55	−1.12	–	−0.45	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.26	–	0.22	0.44	–	0.18	–	mA
(V_{OL} = 0.5 V)		10	0.6	–	0.55	1.12	–	0.45	–	
Input Current — Pull-ups	I_{in}	10	–	–	50	500	1000	–	–	μA
Input Current — Pin 11	I_{in}	10	–	±0.3	–	±0.00001	±0.3	–	±1.0	μA
Input Capacitance	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current — Per Package	I_{DD}	5.0	–	50	–	0.008	50	–	375	μA
Osc_{in} = 0 V, Other Inputs = Open, $I_{out}=0\ \mu A$		10	–	100	–	0.016	100	–	750	
Total Supply Current at an External Load Capacitance (C_L) of Figure 4 f = 500 kHz (with any Analog command)	I_T	5.0	–	–	–	5.0	–	–	–	μA
		10	–	–	–	10	–	–	–	

RECEIVER—MC14458

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Output Voltage "0" Level $V_{in}=V_{DD}$ or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
$I_{out}=0\ \mu A$ "1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	V
Input Voltage# "0" Level	V_{IL}									V
(V_O = 4.5 or 0.5 V)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 0.5 or 4.5 V) "1" Level	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	V
Output Drive Current	I_{OH}									mA
(V_{OH} = 2.5 V) Source		5.0	−0.5	–	−0.5	−1.7	–	−0.4	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.45	–	0.4	0.78	–	0.34	–	mA
Input Current (Osc_{in}, D_{in})	I_{in}	5.0	–	±0.3	–	±0.00001	±0.3	–	±1.0	μA
Input Current ($\overline{POR}$)	I_{in}	5.0	–	–	10	50	400	–	–	μA
Input Capacitance	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current, Per Package $\overline{POR}=V_{DD}$, Other Inputs = V_{DD} or 0, $I_{out}=0\ \mu A$	I_{DD}	5.0	–	5.0	–	250	1000	–	–	μA
Data Input Hysteresis	V_{Hys}	5.0	–	–	–	0.25	–	–	–	V
Total Supply Current at an External Load Capacitance (C_L) of Figure 6 f = 500 kHz	I_T	5.0	–	–	–	400	–	–	–	μA

#Noise immunity specified for worst-case input combination
Noise Margin for both "1" and "0" level = 1.0 V min @ V_{DD} = 5.0 V
2.0 V min @ V_{DD} = 10 V

SWITCHING CHARACTERISTICS (MC14457 – Transmitter, V_{DD} = 5 to 15 V; MC14458 – Receiver, V_{DD} = 5 V)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Rise and Fall Time – Receiver C_L = 100 pF	t_{TLH}, t_{THL}	–	0.3	1.0	μs
Oscillator Start-Up Time – Transmitter	t_{on}	–	8.0	–	μs
Clock Pulse Frequency	PRF	–	1500	600	kHz

MC14457 – TRANSMITTER

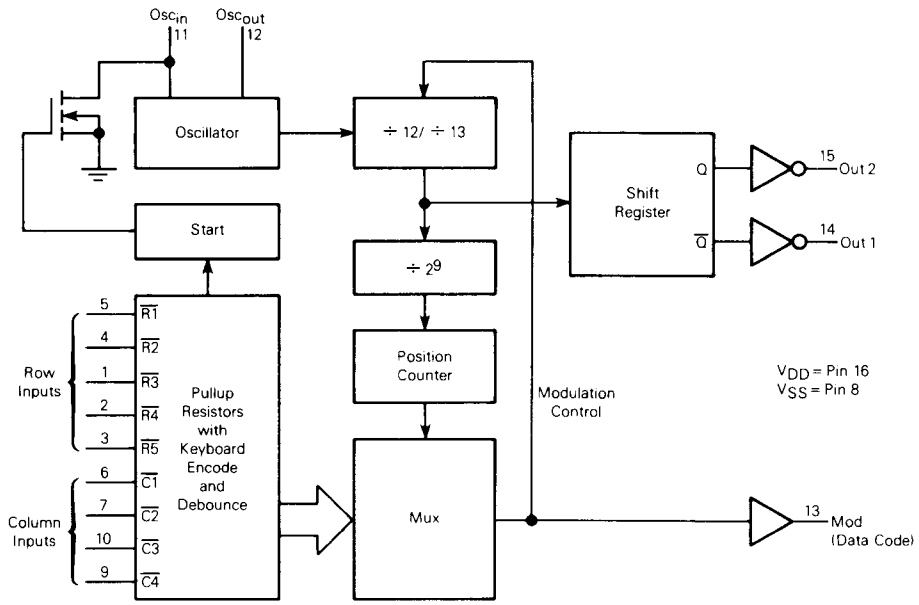


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FIGURE 1 — EXAMPLE OF TRANSMITTED WORD

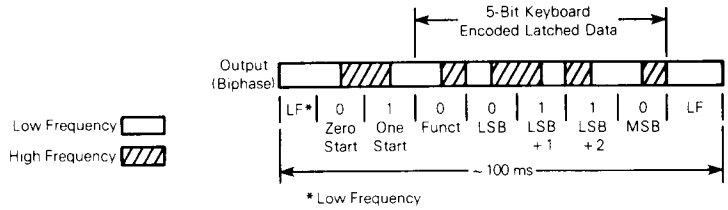
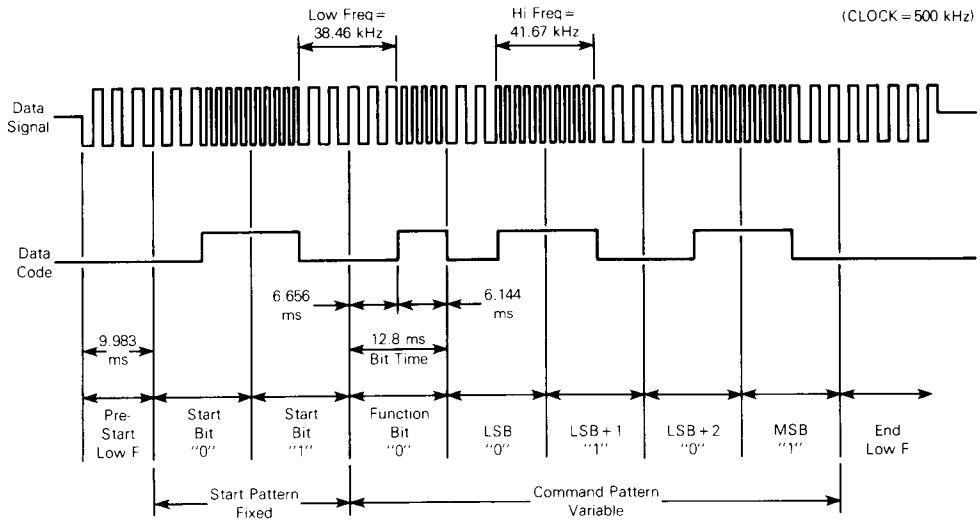


FIGURE 2 — DATA SIGNAL



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MC14457 TRANSMITTER PIN DESCRIPTIONS

$\overline{R1}$, $\overline{R2}$, $\overline{R3}$, $\overline{R4}$, $\overline{R5}$, ROW INPUTS (PINS 5, 4, 1, 2, 3) — These pins are the row inputs and are active in the low state. On-chip pullup resistors are provided on each of these inputs.

$\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$, COLUMN INPUTS (PINS 6, 7, 10, 9) — These pins are the column inputs and are active in the low state. On-chip pullup resistors are provided on each of these inputs.

Out 1, Out 2, OUTPUTS (PINS 14, 15) — These pins provide push-pull output and can be used with ceramic transducers or LEDs. In the non-operating condition, both outputs are at ground potential.

Osc_{in}, Osc_{out}, OSCILLATORS (PINS 11, 12) — These pins are the input/output terminals of the oscillator. They can be used with a ceramic resonator or crystal. The oscillator is automatically turned off after the data is transmitted for low current quiescent operation.

If an external oscillator is used, a current limiting resistor should be added, due to the presence of an internal pull-down device on the oscillator input.

Mod, MODULATION (PIN 13) — This pin is a data code output. Note that there is no power-up reset.

TABLE 1 – DATA CODE

Key Number	Operation	Row (Active Low)	Column (Active Low)	Transmitter Data and Receiver Output Address					$\overline{VA}$ Pulse	Notes
				MSB/A3	LSB+2/A2	LSB+1/A1	LSB/A0	Function*		
1	Digit 0	R1	C1	0	0	0	0	0	–	1
2	Digit 1	R1	C2	0	0	0	1	0	–	1
3	Digit 2	R2	C1	0	0	1	0	0	–	1
4	Digit 3	R2	C2	0	0	1	1	0	–	1
5	Digit 4	R3	C1	0	1	0	0	0	–	1
6	Digit 5	R3	C2	0	1	0	1	0	–	1
7	Digit 6	R4	C1	0	1	1	0	0	–	1
8	Digit 7	R4	C2	0	1	1	1	0	–	1
9	Digit 8	R5	C1	1	0	0	0	0	–	1
10	Digit 9	R5	C2	1	0	0	1	0	–	1
11	Chan. Search ↓	R1	C3	0	0	0	0	1	⌐	2
12	Chan. Search ↑	R1	C4	0	0	0	1	1	⌐	2
13	Fine Tuning ↓	R2	C3	0	0	1	0	1	⌐	3
14	Fine Tuning ↑	R2	C4	0	0	1	1	1	⌐	3
15	Spare	R3	C3	0	1	0	0	1	⌐	3
16	Spare	R3	C4	0	1	0	1	1	⌐	3
17	Volume ↓	R4	C3	0	1	1	0	1	⌐	3
18	Volume ↑	R4	C4	0	1	1	1	1	⌐	3
19	Mute on/off	R5	C3	1	0	0	0	1	⌐	2
20	Off	R5	C4	1	0	0	1	1	⌐	2
21	Digit 10	R2•R5	C1	1	0	1	0	0	–	1
22	Digit 11	R2•R5	C2	1	0	1	1	0	–	1
23	Digit 12	R3•R5	C1	1	1	0	0	0	–	1
24	Digit 13	R3•R5	C2	1	1	0	1	0	–	1
25	Digit 14	R2•R3•R5	C1	1	1	1	0	0	–	1
26	Digit 15	R2•R3•R5	C2	1	1	1	1	0	–	1
27	Spare	R2•R5	C3	1	0	1	0	1	⌐	3
28	Spare	R2•R5	C4	1	0	1	1	1	⌐	3
29	Spare	R3•R5	C3	1	1	0	0	1	⌐	3
30	Spare	R3•R5	C4	1	1	0	1	1	⌐	3
31	Spare	R2•R3•R5	C3	1	1	1	0	1	⌐	3
32	Spare	R2•R3•R5	C4	1	1	1	1	1	⌐	3

Notes:
1. Channel Select Keys (Function Bit = 0). Data is transmitted once each time a key is activated.
2. Toggling type On/Off or counter advance type keys. Data is transmitted once each time a key is activated.
3. Analog Up/Down or On/Off keys, i.e., one key for Down or Off and another key for Up or On. Data transmission is repeated as long as the key is operated.

* The function bit is used only internally by the MC14458 receiver as a steering bit.

In Table 1, all channel select data is noted by the function bit equal to zero. For functions other than channel, the function bit equals one.

The four toggling or counter advance type keys that transmit data once each time a key is activated are Mute, Off, Channel Search Up, and Channel Search Down.

The twelve remaining analog keys (Vol, Tint, Color, etc.) transmit data as long as the key is activated. The keys' functions are arranged to provide the most typical application without grounding of multiple row or columns required.

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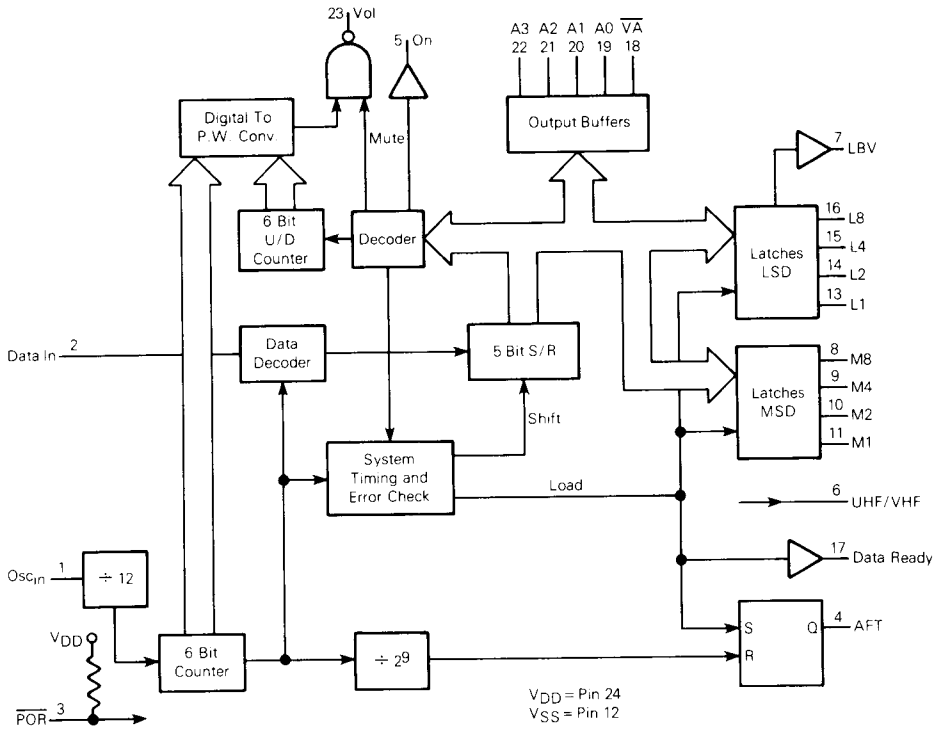
MC14458 — RECEIVER



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MC14458 RECEIVER PIN DESCRIPTIONS

Data In, DATA INPUT (PIN 2) — The amplified ultrasonic data signal (after amplification and limiting forms a square wave with a peak-to-peak value of V_{DD}) is applied to this input terminal.

Osc$_{in}$, OSCILLATOR INPUT (PIN 1) — The oscillator input pin of the receiver is connected to an oscillator that provides, for example, a 500 kHz square wave signal. A typical oscillator circuit is shown in Figure 5. Accuracy of one percent, relative to the oscillator frequency in the transmitter, is recommended for satisfactory performance in very high echo producing environments.

L1, L2, L4, L8, M1, M2, M4, M8, CHANNEL OUTPUTS (PINS 13, 14, 15, 16, 11, 10, 9, 8) — The eight data output pins provide latched data corresponding to the channel selected on the transmitter keyboard. L1 through L8 are the least significant bits; M1 through M8 are the most significant bits. The data on these pins is accompanied by a Data Ready signal.

Data Ready, DATA READY SIGNAL (PIN 17) — A positive pulse with a duration of 768 μs appears at Pin 17 of the receiver approximately 0.1 second after a complete command is entered on the remote control transmitter keyboard. The negative going edge of this pulse may be used for triggering purposes.

NOTE: A complete command is one digit in the single entry mode or two digits in the double entry mode.

AFT, AUTOMATIC FINE TUNING ENABLE (PIN 4) — The voltage level at this pin is low for a time duration of 0.393 seconds following a change in selected channel to allow disabling the tuner AFT circuit. Also, miscellaneous commands 0000, 0001, 0010, and 0011 (Channel Search Up/Down, Fine Tuning Up/Down) will cause this disable feature.

$\overline{POR}$, POWER-ON RESET (PIN 3) — This pin is low for power-on reset of the analog output to 0 pulse width and off/on output to 0. An internal pull-up device delivers 10 to 400 μA to charge an external capacitor. Reset occurs until the input voltage reaches 70 percent V_{DD}. All internal registers will also be reset.

A0, A1, A2, A3, ADDRESS OUTPUTS (PINS 19, 20, 21, 22) – The address outputs of the receiver identify selected analog and on/off commands for use in system expansion. The data on these lines is valid when accompanied by a Valid Address pulse.

$\overline{VA}$, VALID ADDRESS (PIN 18) – A negative going pulse with a duration of 768 μs appears at Pin 18 approximately 0.1 seconds after an analog on/off key on the remote control transmitter keyboard is operated. Either edge of this pulse may be used for control of add-on circuits.

The Valid Address pulse is repeated every 102.4 ms for as long as a key is operated which provides repeated transmission of data when held down.

The Valid Address signal may be used in conjunction with the Address Outputs to drive memories to provide additional control functions such as color, tint, etc.

The Valid Address pulse may be used to provide a stepping clock for up/down counters in a memory. The least significant address line (A0) is used to identify the up or down mode, and the remaining address lines (A1, A2, A3) are decoded to enable each individual control circuit.

By adding up/down counters to the Data Outputs, it is possible to use the Valid Address pulse and a decoded address for implementing a channel up/down stepping function from the remote control. Additional On/Off functions may be obtained by using the Valid Address pulse in combination with a decoded address for setting and resetting of latches. The Valid Address signal is disabled in the standby mode (ON output at logical 0).

UHF/VHF, ULTRA HIGH FREQUENCY/VERY HIGH FREQUENCY OUTPUT (PIN 6) – This pin of the receiver provides a low level when the selected channel is a VHF channel (00 to 13, or 84 to 99). A high level on Pin 6 identifies selection of a UHF channel (14 to 83). This signal is provided to permit switching of VHF and UHF tuners.

On, ON (PIN 5) – This pin of the receiver provides a low level following operation of the Off command (1001) on the remote-control transmitter. The signal on this pin changes to a high level when a channel is selected.

Vol, VOLUME CONTROL (PIN 23) – An analog output voltage in the range between 0 V and V_{DD} is obtained by integrating the signal at the Vol pin through a low-pass filter. The analog voltage resolution has been chosen to be 64 steps. The value can be incremented or decremented in steps of one by keys providing commands 0111 and 0110, respectively (see Table 1).

This analog voltage can be varied up or down at a speed of approximately 10 steps per second. The D/A conversion is performed with an underflow and an overflow limiting circuit. The Vol pin is normally used for the control of volume. The first time power is applied to the remote-control receiver, the volume output is 0 volts.

The Vol signal may be increased after a channel has been selected by operating the key providing a command 0111 (Volume Up).

The Vol signal may be muted by operating a key on the transmitter providing command 1000. Return to the original output prior to muting may be achieved by operating the mute key a second time or by operating the volume-up key.

In the muted mode, the analog level is memorized and cannot be varied by the up/down controls on the transmitter.

LBV, LOW BAND (PIN 7) – This pin will go HIGH whenever channels 02, 03, 04, 05, or 06 are selected. The output is LOW for channels 00, 01, and 07 through 99.

OPERATION

The receiver can be placed in a single-digit mode of operation by connecting the M4 data output (Pin 9) to V_{DD} and the UHF output (Pin 6) to V_{SS}. In this mode, the L1 through L8 channel outputs will change immediately after the entry of a single digit on the transmitter keys. The M1 through M8 outputs are not used in this mode (see Figure 6).

As one example of operation, a free-running ceramic resonator oscillator (at 500 kHz), triggered by the depression of any key, is divided by 12 or 13 to provide frequencies of 41.67 or 38.46 kHz. The transmitted data "zero" consists of 256 periods of the lower frequency followed by an equal number of the higher frequency. Mark to space ratio is kept at 1:1 in each case. A data "one" reverses the order of the two frequencies.

Row and column information from the keyboard is encoded into a 5-bit word and loaded onto data latches on the edge of transmit enable. This data, preceded by two bits, 0 and 1, is used in sequence to provide biphase control of the divider and, consequently, the bit pattern transmitted from the unit. Each 7-bit word begins and ends with a low frequency burst. Operation of a channel select key produces an output data stream for a duration of approximately 100 ms.

APPLICATIONS INFORMATION

Typical circuits for the transmitter and receiver chips are shown in Figures 3 through 7.

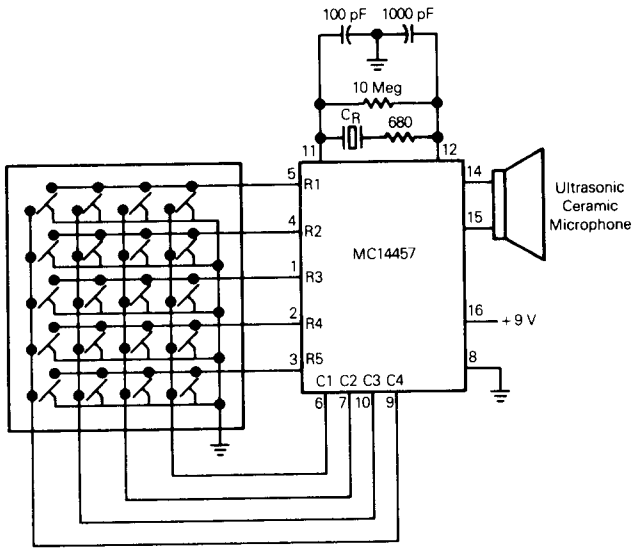
The transmitters, with the keyboard shown, transmit the first twenty codes from Table 1. The circuits of Figure 3 transmit via ultrasonic; whereas, the circuit of Figure 4 transmits infrared light. In Figure 3, a push-pull output at Pins 14 and 15 allows a balance drive to the ceramic microphone, which virtually doubles the transmitted power, compared to a single-ended output.

The diagram in Figure 5 shows an amplifier connected to a remote receiver. The bias resistor (photodiode) of the amplifier requires bias. The bias voltage is determined by the choice of photodiode and system considerations such as ambient light. Most of the required gain is realized using three of the hex inverters in the MC14069UB package. A fourth inverter from the same package operates a 500 kHz oscillator circuit.

Figure 6 shows a block diagram of a PLL system. The receiver directly addresses a synthesizer. In this diagram, a complete command consists of two channel digits followed by an Enter code. The Enter code into the synthesizer is a 0101 in complementary logic. The transmitted code from the transmitter is 1010, which is Function 10 from Table 1.

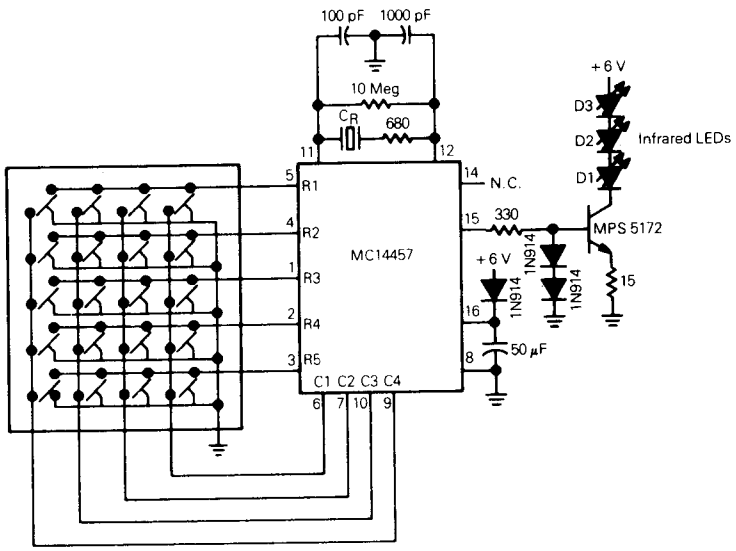
A block diagram of a tuning address system is shown in Figure 7. This block diagram incorporates a one-chip microcomputer that would be programmed to the system's needs. The system can be expanded up to 256 channels.

FIGURE 3 – TYPICAL ULTRASONIC SYSTEM



Note: C_R is a ceramic resonator, Radio Materials Corp. type CR30 or equivalent.

FIGURE 4 – TYPICAL INFRARED SYSTEM



Note: C_R is a ceramic resonator, Radio Materials Corp. type CR30 or equivalent.

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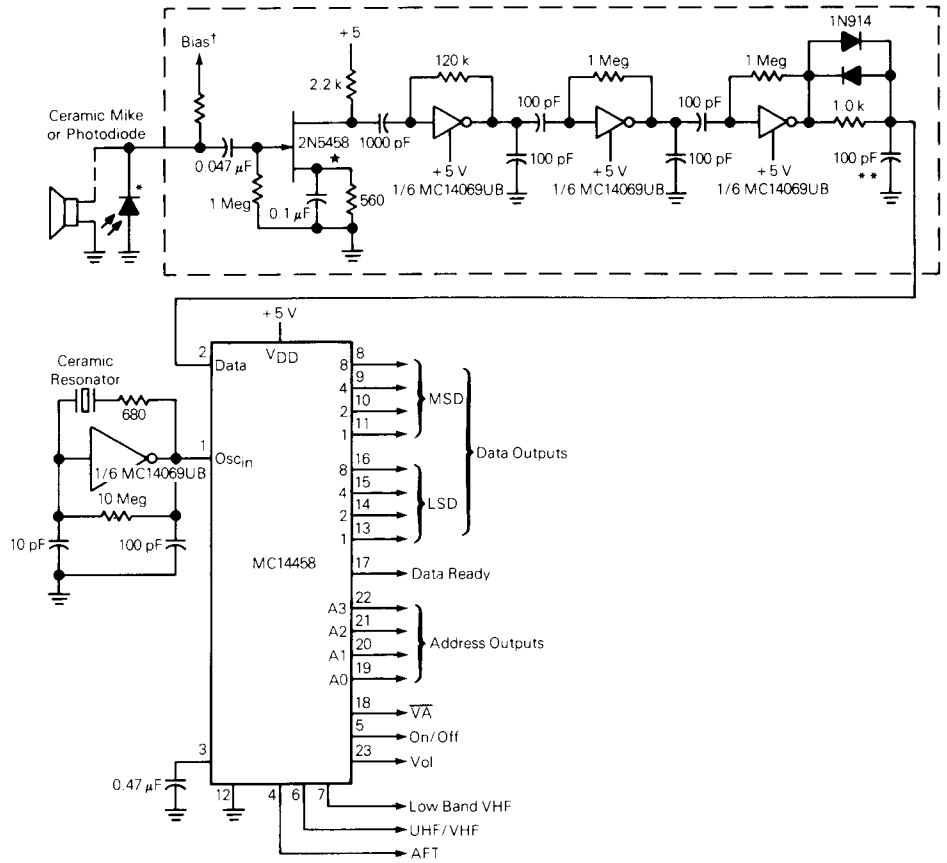
FIGURE 5 – TYPICAL REMOTE CONTROL RECEIVER CIRCUIT DIAGRAM



NOTES:

†Bias used for photodiode only.
*It is mandatory to use an infrared filter in front of the photodiode. Type Kodak 87C or similar.
★Select 2N5458 FETs with an I_{DSS} of 2 to 4 mA.
**100 pF capacitor should be placed as close as possible to Pin 2 of the MC14458.

FIGURE 6 — BLOCK DIAGRAM OF A PLL SYSTEM

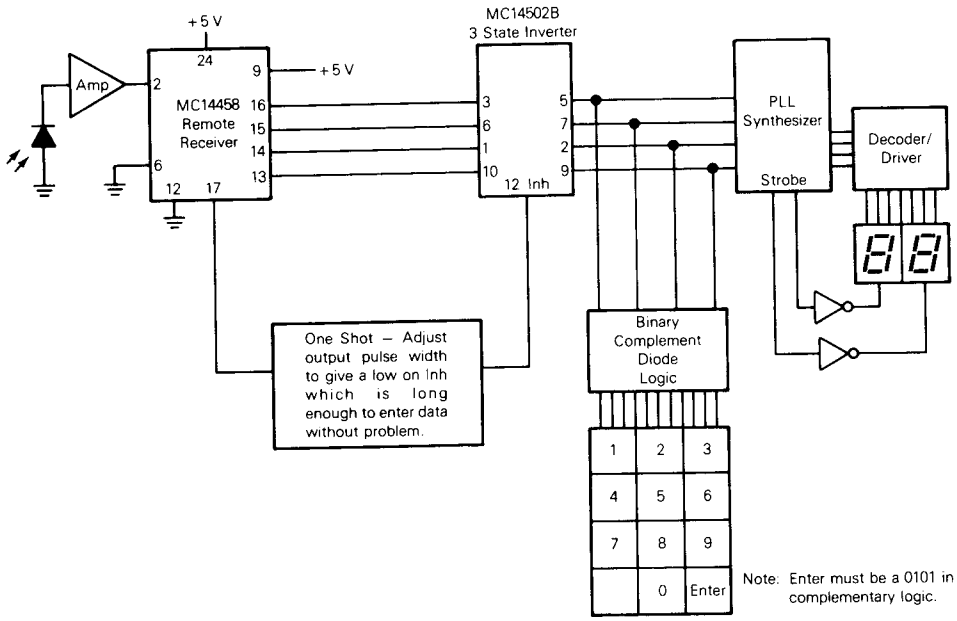


FIGURE 7 — BLOCK DIAGRAM OF A TUNING ADDRESS SYSTEM FOR UP TO 256 CHANNELS