80C04
Ethernet Data Link Controller

PRODUCT PREVIEW *June 1991*

Features

- ***Conforms to IEEE 802.3 standard for Ethernet (10BASE5), Cheapernet (10BASE2) and Twisted Pair (10BASE-T).***
- ***High performance, low power CMOS technology.***
- ***Connects directly to 8020 and 8023 Manchester Converters (MCC™).***
- ***Pin and function compatible with the 8005 Advanced Ethernet Data Link Controller (AEDLC™).***
- ***Fast bus cycle to support 16-bit, 12Mhz ISA bus architecture.***
- ***Support packet chaining and easy transmit/ receive error handling.***
- ***Sustained transfer rates of 6 Mbytes/sec minimum in 8-bit and 16-bit mode.***
- ***Group address packet reception.***
- ***Sleep mode to conserve power when not in use.***
- ***Hash Function and Table for multicast address filtering.***
- ***68-pin surface mount plastic leaded chip carrier package.***

Description

The 80C04 has three major blocks: the Ethernet Data Link Controller, Buffer Controller and Bus Interface.

The Ethernet Data Link Controller block supports the link layer (Layer 2) of the IEEE 802.3 standard. It performs serialization and deserialization, preamble generation and stripping, CRC generation and stripping, transmission deferral, collision handling, and multicast and broadcast addressing.

The Buffer Controller block provides management for a 64K byte local packet buffer consisting of two 64Kx4 DRAMs. This block provides arbitration and control for four memory ports: the transmitter, for network transmit packets; the receiver, for received frames; the Bus Interface, for system data and control; and an internal DRAM refresh generator. To minimize the pin count, dynamic RAM addresses and data are time multiplexed on a single 8-bit bus. A control line and 8-bit address is also provided to permit reading from a locally attached EEPROM or PROM. This permits configuration of an adapter board with its station address and configuration data, independent of the network layer software used.

The Buffer Controller interfaces to the system bus via the Bus Interface block and provides access to internal configuration and status registers, the local packet buffer and a control signal interface to permit DMA or programmed I/O transfer of packet data. The data path between the system bus and the local DRAM buffer is buffered by 16 byte FIFO called System FIFO. This permits high speed data transfer to occur even when the Buffer Controller is busy servicing the transmitter or receiver or refreshing the DRAM. Both 8 and 16 bit transfers are supported. Byte ordering on a 16 bit bus is available under software control. The 80C04 supports both Intel-compatible and Motorola-compatible buses.

Pin Description

(An asterisk after a signal name signifies an active low signal)

D0-D15: *A 16 bit bidirectional system data bus. If BUSSIZE = 0, the bus is configured as 8 bits and D8-D15 are not used for data transfer. Byte order for local buffer data transfers on a 16 bit bus is software configured. D8-D15 are used to provide address information to the optional external address PROM in both 8 and 16 bit modes.*

EN*: *An output which can be used to control the three-state control pin of external bi-directional drivers such as the 74LS245.*

APEN*: *Active low address PROM enable output.*

IOW*(R/W): *If BUSMODE = 1, this input defines the current bus cycle as a write. If BUSMODE = 0, this input defines the bus cycle as a read if a 1 or a write if a 0.*

IOR* (LDS*): *IOR* when BUSMODE = 1; LDS* when BUSMODE = 0.*

CS*: *The chip select input, used to access internal registers and the packet buffer.*

A0-A3: *Address select inputs used to select internal registers for reading or writing. A0 is not used in 16-bit mode.*

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MEMW*: *Memory Write Strobe input when BUSMODE = 1; not used when BUSMODE = 0.*

READY(DTACK*): *A three-state output. When BUSMODE = 1, this output functions as a READY pin (Intel compatible); when BUSMODE = 0, this output is DTACK* (Motorola compatible).*

INT/INT*: *When BUSMODE = 1, this is a high active interrupt output; when BUSMODE = 0 this output is low active.*

MEMR*: *Memory Read Strobe input when BUSMODE = 1; not used when BUSMODE = 0.*

RESET*: *The low active reset input. Asserting RESET* clears all configuration and pointer to 00. Following reset, a wait of 4 µs is necessary before accessing the part.*

BHE* (UDS*): *BHE* when BUSMODE = 1; and UDS* when BUSMODE = 0.*

BUSMODE: *An input which selects Intel-compatible bus signals when high or Motorola-compatible bus signals when low.*

BUSSIZE: *An input that selects the 8-bit system bus when low or 16-bit system bus when high.*

AD0-AD7: *A multiplexed address and data bus used to provide row and column address and read/write data to the packet buffer dynamic RAM.*

RAS*: *Row Address Strobe to the packet buffer memory.*

CAS*: *Column Address Strobe to the packet buffer memory. Page mode addressing is used when possible to speed access to the buffer.*

W*: *An output to the dynamic RAM buffer that indicates the current cycle is a write.*

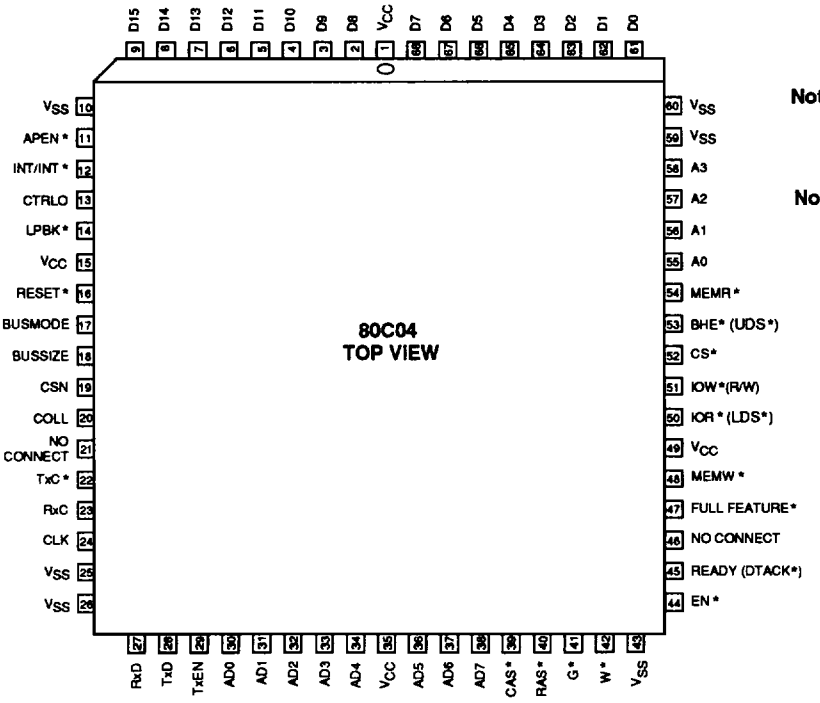
G*: *An output to the dynamic RAM buffer that enables read data onto the AD bus.*

TxEN: *An output to the Manchester Code Converter that indicates a transmission is in progress.*

FULL FEATURE*: *An input used to set the 80C04 to Full Feature mode when this pin is driven low. When not connected this pin is pulled up internally to set the 80C04 to non-Full Feature mode.*

TxC*: *An input from the Manchester Code Converter that is used to synchronize transmitted data.*

Pin Configuration



Note: Signal names in paranthesis apply when BUSMODE = 0

Note: Do not connect any signals to pin 21 & 46 to allow for future compatibility

TxD: *The transmit data output to the Manchester Code Converter.*

RxC: *An input from the Manchester Code Converter used to synchronize received data.*

RxD: *The receive data input from the Manchester Code Converter.*

COLL: *The collision input from the Manchester Code Converter.*

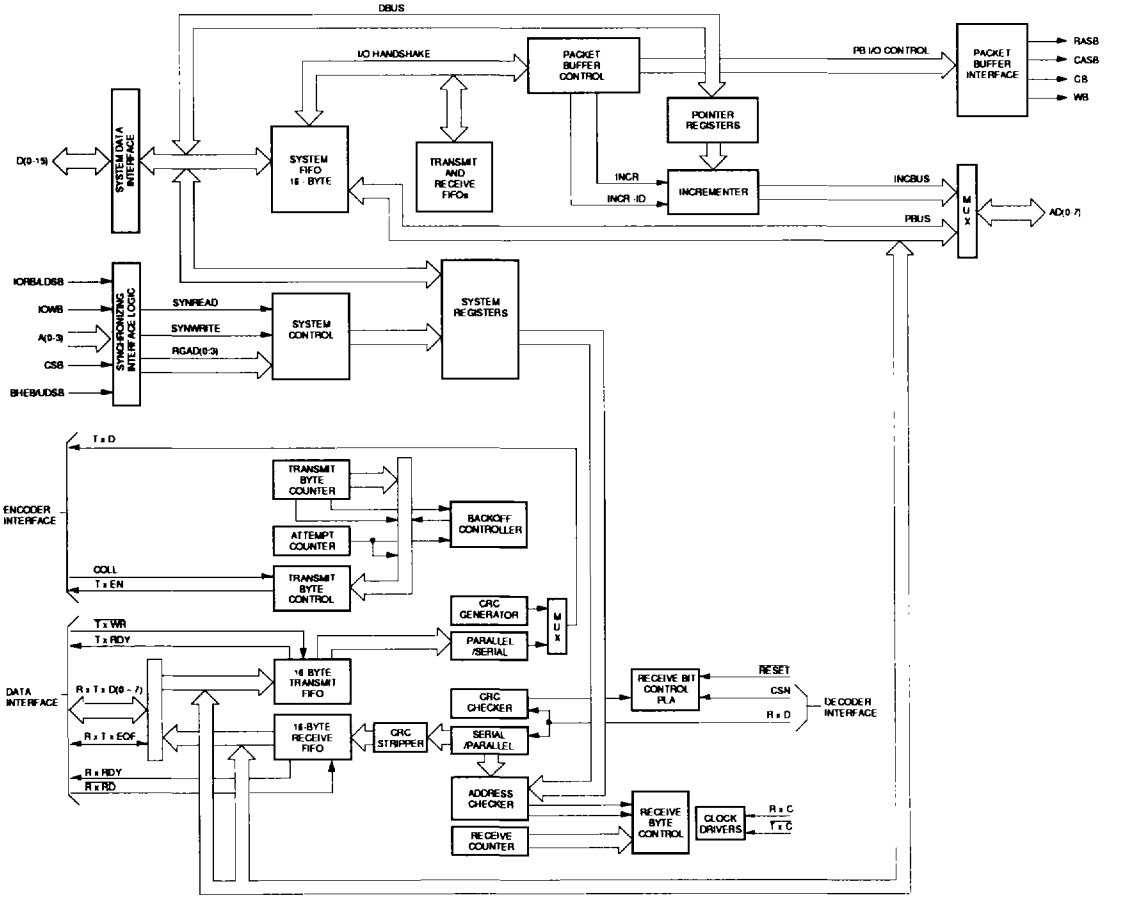
CSN: *The carrier sense input from the Manchester Code Converter.*

CTRLO: *Control/Output, a general purpose control pin, level follows bit 12 of Configuration Register #2.*

LPBK*: *The loopback control output.*

CLK: *The master 20 MHz input clock.*

Functional Block Diagram



System Diagram

IEEE 802.3 Compliant Ethernet/Cheapernet/10BASE-T System Connections