STANDARD
MICROSYSTEMS
CORPORATION

SLC90E42
ADVANCE INFORMATION

SLC90E42 NorthBridge
(Member of High Performance TeXas Chipset)

FEATURES

- 324 Pin BGA North Bridge Chip
- Supports the Pentium Compatible Processor with Host Bus from 60 MHz to 75 MHz at 3.3V and 2.5V.
- PCI 2.1 Compliant
- Integrated 64 Bit Data Path
- Integrated DRAM Controller
  - Four Mbytes to 256 Mbytes Main Memory
  - Supports 64Mbit DRAM/SDRAM
  - Supports Fast Page Mode ("FPM"), EDO and SDRAM DRAM Devices
  - Supports 6-Bank of FPM or EDO Memory, or up to 5 Banks of SDRAM
  - Programmable-Strength DRAM Interface Buffers
  - Dual Buffered Drivers for Fast Transition Control/Address Signals
  - 8 Level QWord CPU to DRAM Write Buffer
  - Four Level QWord DRAM To CPU Read Buffer
  - CAS-Before-RAS Refresh, Extended Refresh and Self Refresh for EDO/FPM Memory
  - CAS-Before-RAS and Self Refresh for SDRAM
- Integrated L2 Cache Controller
  - Supports 256K And 512K Pipelined Burst SRAM
  - Direct Mapped Organization With Write Back Updating Scheme
  - 64MB DRAM Cacheability
  - Cache Hit Read/Write Cycle Timing at 3-1-1-1 Back-To-Back Read/Write Cycles at 3-1-1-1-1-1-1-1 or 3-1-1-1-2-1-1-1 (Double Bank)
  - Supports Concurrent Copy-Back and Line-Fill During Cache-Read-Miss-Dirty Cycle
  - Embeds A 16Kb Altered Static RAM
- Optional Synchronous or Asynchronous Fast Response 33 MHz PCI Bus Interface
  - Supports Five PCI Bus Masters (Including A PCI-ISA Bridge Chip)
  - 32-DWord PCI-To-DRAM Read Prefetch Buffer
  - 32-DWord PCI-To-DRAM Post Write Buffer
  - 4-DWord CPU-To-PCI Write Buffer For 0-WS CPU-To-PCI Burst Memory Write
  - Supports 0 WS PCI Master Burst Read/Write System Memory
  - PCI 2.1 Compliant
- Comprehensive Power Management Capability

- Supports ACPI 1.0 Specification
- Supports PCI nCLKRUN Protocol
- Supports Various System Suspend Modes
- Supports Clock Control
- Supports Suspend Refresh to System Memory
- Supports Both Compatible SMRAM and Extended SMRAM Mapping
- SMM Write-Back Cacheable in Extended SMRAM Mode Up To 1MB

GENERAL DESCRIPTION

The SMSC TeXas chipset consists of the SLC90E42 System Controller and the SLC90E46 PCI ISA Bridge chip. The SLC90E42 north bridge integrates the cache and DRAM controller and provides bus control for data transfers between the CPU, cache, main memory, and the PCI Bus. The second level (L2) cache controller supports a write-back cache policy for cache sizes of 256 Kbytes and 512 Kbytes. Cacheless designs are also supported. Pipelined burst SRAM is supported for the L2 cache. An external Tag RAM is used for the address tag and an embedded 16 Kbit SRAM for the cache line status bits (Altered and Valid bits). The DRAM controller supports 6 rows up to 256 Mbytes of main memory. The SLC90E42 also integrates the Data Path into the same BGA chip. Through the deep buffers and sophisticated pre-fetch and post-write policies, the SLC90E42 allows PCI masters to achieve full PCI bandwidth. The SLC90E42 also integrates many power management features that will enable the system to save power whenever the system resources become idle.

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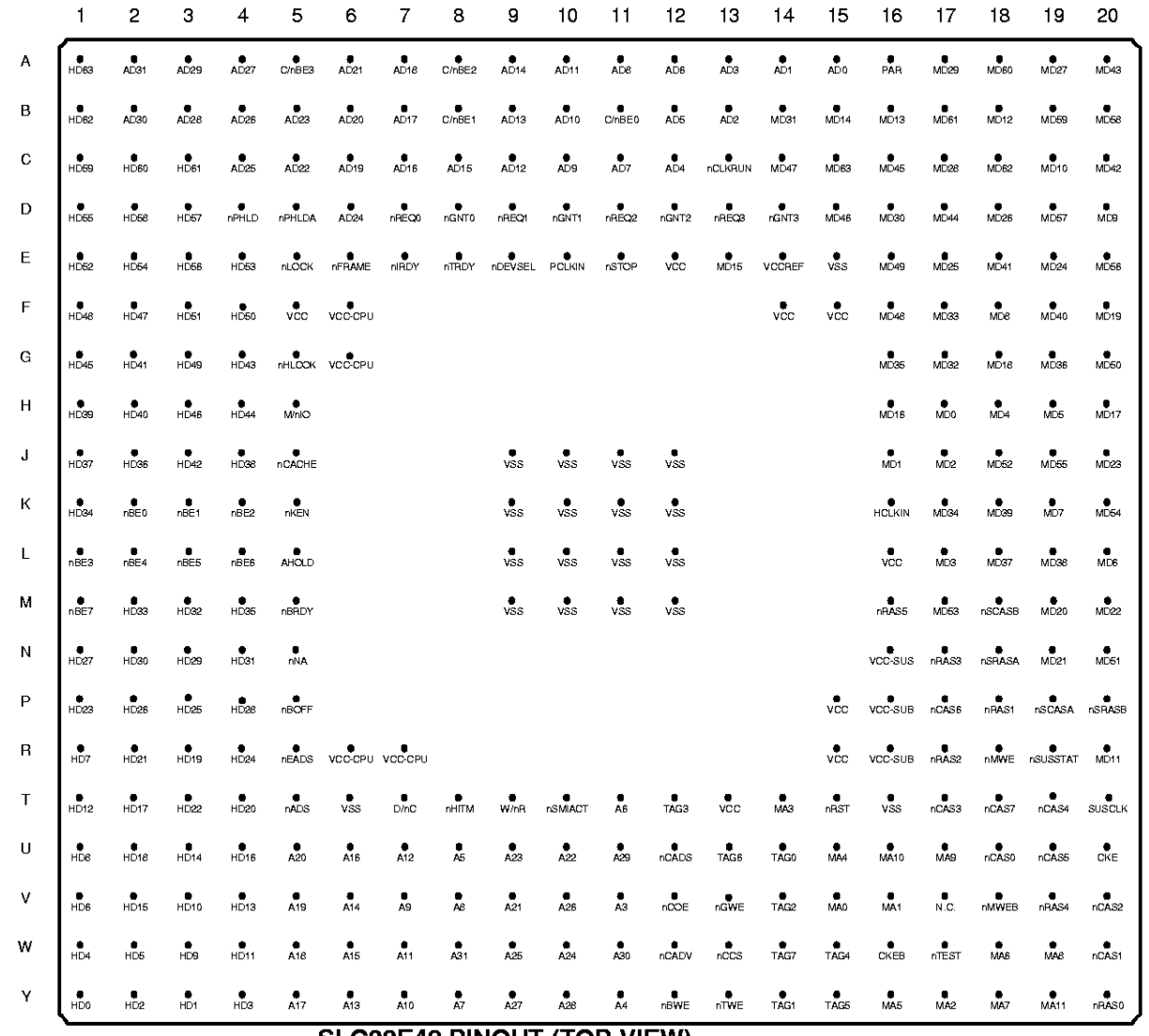
1. SLC90E42 BGA PINOUT AND PACKAGE INFORMATION

1.2. SLC90E42 PINOUT

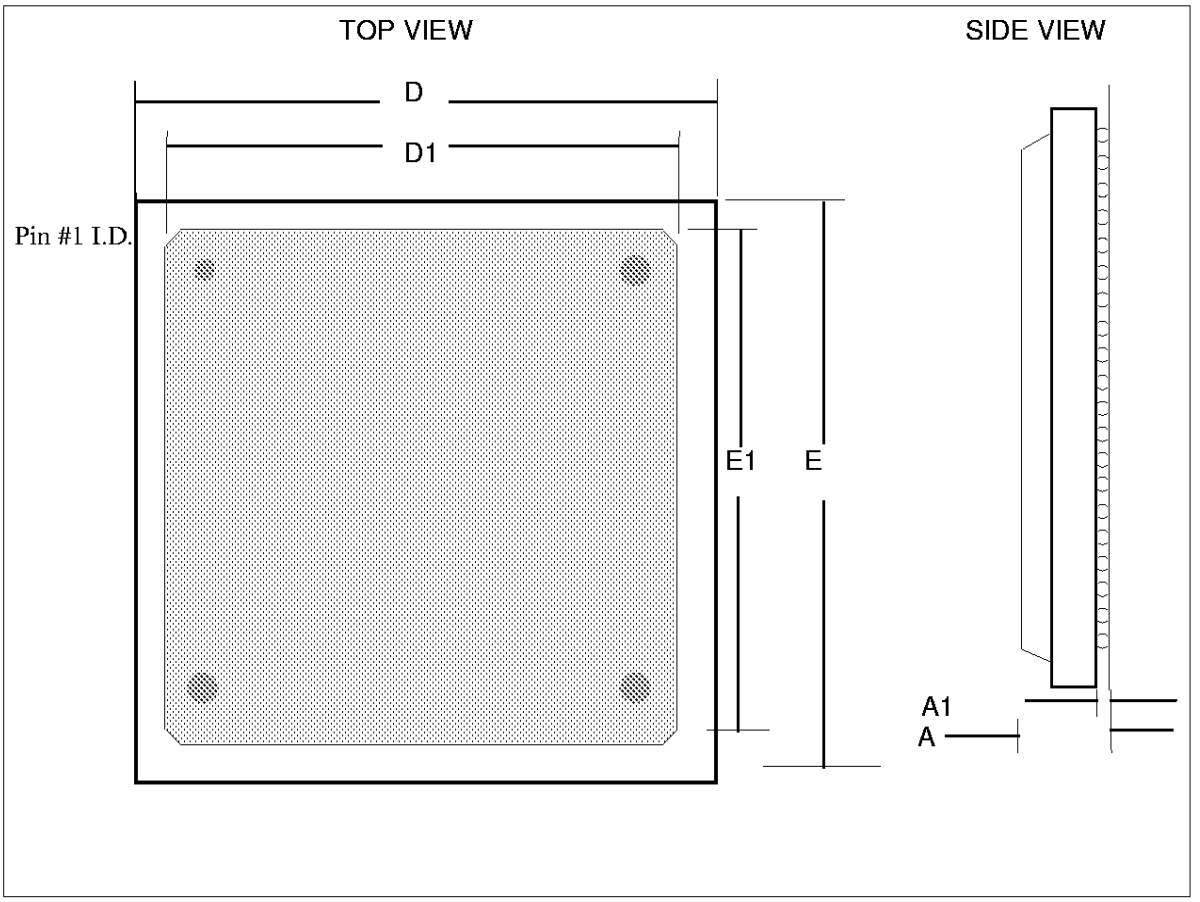
The following diagram shows the pin assignment for the SLC90E42.

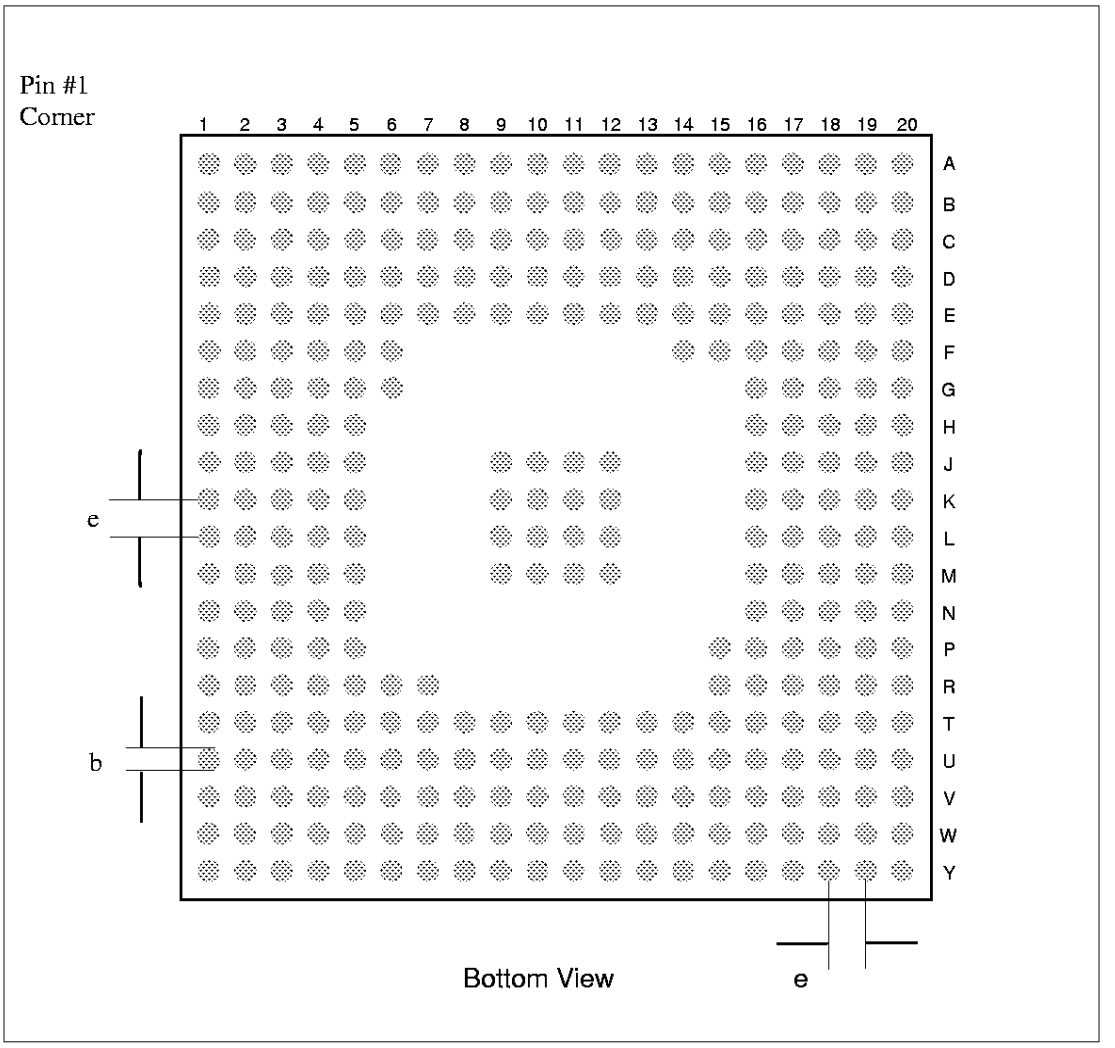


	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	HD63	AD31	AD29	AD27	C/nBE3	AD21	AD18	C/nBE2	AD14	AD11	AD8	AD6	AD3	AD1	AD0	PAR	MD29	MD60	MD27	MD43
B	HD62	AD30	AD28	AD26	AD23	AD20	AD17	C/nBE1	AD13	AD10	C/nBE0	AD5	AD2	MD31	MD14	MD13	MD61	MD12	MD59	MD58
C	HD59	HD60	HD61	AD25	AD22	AD19	AD16	AD15	AD12	AD9	AD7	AD4	nCLKRUN	MD47	MD63	MD45	MD28	MD62	MD10	MD42
D	HD55	HD58	HD57	nPHLD	nPHLDA	AD24	nREQ0	nGNT0	nREQ1	nGNT1	nREQ2	nGNT2	nREQ3	nGNT3	MD46	MD30	MD44	MD26	MD57	MD9
E	HD52	HD54	HD56	HD53	nLOCK	nFRAME	nIRDY	nTRDY	nDEVSEL	PCLKIN	nSTOP	VCC	MD15	VCCREF	VSS	MD49	MD25	MD41	MD24	MD56
F	HD48	HD47	HD51	HD50	VCC	VCC-CPU								VCC	VCC	MD48	MD33	MD8	MD40	MD19
G	HD45	HD41	HD49	HD43	nHLOCK	VCC-CPU										MD35	MD32	MD18	MD36	MD50
H	HD39	HD40	HD46	HD44	M/nIO											MD16	MD0	MD4	MD5	MD17
J	HD37	HD36	HD42	HD38	nCACHE				VSS	VSS	VSS	VSS				MD1	MD2	MD52	MD55	MD23
K	HD34	nBE0	nBE1	nBE2	nKEN				VSS	VSS	VSS	VSS				HCLKIN	MD34	MD39	MD7	MD54
L	nBE3	nBE4	nBE5	nBE6	AHOLD				VSS	VSS	VSS	VSS				VCC	MD3	MD37	MD38	MD6
M	nBE7	HD33	HD32	HD35	nBRDY				VSS	VSS	VSS	VSS				nRAS5	MD53	nSCASB	MD20	MD22
N	HD27	HD30	HD29	HD31	nNA											VCC-SUS	nRAS3	nSRASA	MD21	MD51
P	HD23	HD26	HD25	HD28	nBOFF										VCC	VCC-SUB	nCAS6	nRAS1	nSCASA	nSRASB
R	HD7	HD21	HD19	HD24	nEADS	VCC-CPU	VCC-CPU								VCC	VCC-SUB	nRAS2	nMWE	nSUSSTAT	MD11
T	HD12	HD17	HD22	HD20	nADS	VSS	D/nC	nHITM	W/nR	nSMIACT	A6	TAG3	VCC	MA3	nRST	VSS	nCAS3	nCAS7	nCAS4	SUSCLK
U	HD8	HD18	HD14	HD16	A20	A16	A12	A5	A23	A22	A29	nCADS	TAG6	TAG0	MA4	MA10	MA9	nCAS0	nCAS5	CKE
V	HD6	HD15	HD10	HD13	A19	A14	A9	A8	A21	A26	A3	nCOE	nGWE	TAG2	MA0	MA1	N.C.	nMWEB	nRAS4	nCAS2
W	HD4	HD5	HD9	HD11	A18	A15	A11	A31	A25	A24	A30	nCADV	nCCS	TAG7	TAG4	CKEB	nTEST	MA6	MA8	nCAS1
Y	HD0	HD2	HD1	HD3	A17	A13	A10	A7	A27	A28	A4	nBWE	nTWE	TAG1	TAG5	MA5	MA2	MA7	MA11	nRAS0

SLC90E42 PINOUT (TOP VIEW)

1.2.1. SLC90E42 BGA PACKAGE INFORMATION





SLC90E42 324-BALL BGA BALL PATTERN

SLC90E42 324-Pin Ball Grid Array Package

SYMBOL	MIN	NOMINAL	MAX
A	2.16 mm	2.36 mm	2.56 mm
A1	0.50 mm	0.60 mm	0.70 mm
D	26.80 mm	27.00 mm	27.20 mm
D1	23.90 mm	24.00 mm	24.10 mm
E	26.80 mm	27.00 mm	27.20 mm
E1	23.90 mm	24.00 mm	24.10 mm
b	0.60 mm	0.75 mm	0.90 mm
e	1.07 mm	1.27 mm	1.47 mm

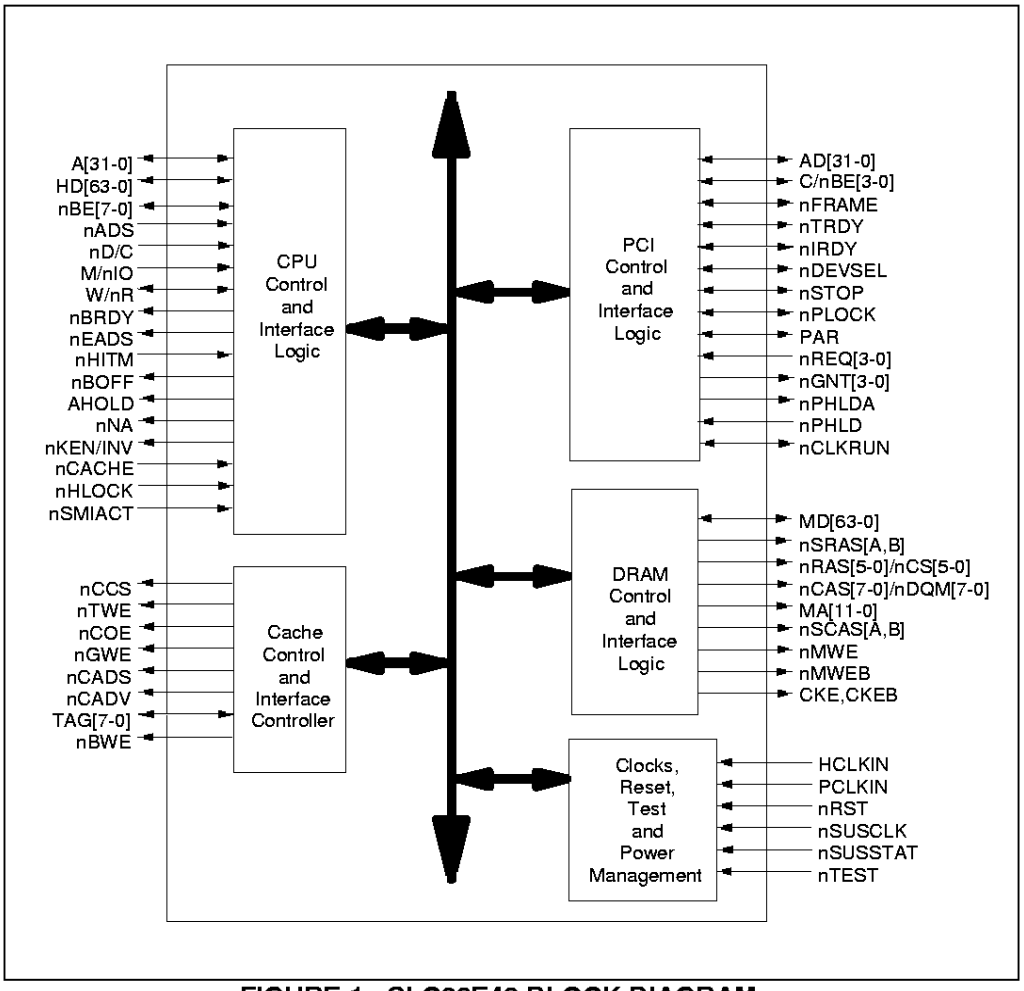


FIGURE 1 - SLC90E42 BLOCK DIAGRAM

2. SLC90E42 FUNCTIONAL OVERVIEW

The SLC90E42 host bridge provides an integrated solution for the system controller and datapath components in a Pentium Processor system. It supports all Pentium family and compatible processors. It has 64 bit Host, Cache and DRAM interface, 32 bit PCI bus interfaces, and it also integrates the PCI arbiter.

The SLC90E42 bus interfaces are designed to interface with 2.5V, 3.3V and 5V busses. It implements 2.5 and 3.3V drivers and 5V tolerant receivers. The SLC90E42 connects directly to the Pentium processor 3.3V or 2.5V host bus, directly to the 3.3V or 5V DRAMs, and directly to the 5V or 3.3V PCI bus. It can also directly interface to 3.3V or 5V TAGRAM and 3.3V cache RAM. Figure 2 shows the system block diagram of the TeXas chipset.

The SLC90E42 works with PCI-ISA bridge chip SLC90E46. The SLC90E46 provides the PCI-to-ISA/EIO bridge functions along with other functions such as a fast IDE interface, Plug-n-Play, SMBus interface, USB host controller, and legacy and ACPI compliant power management capabilities.

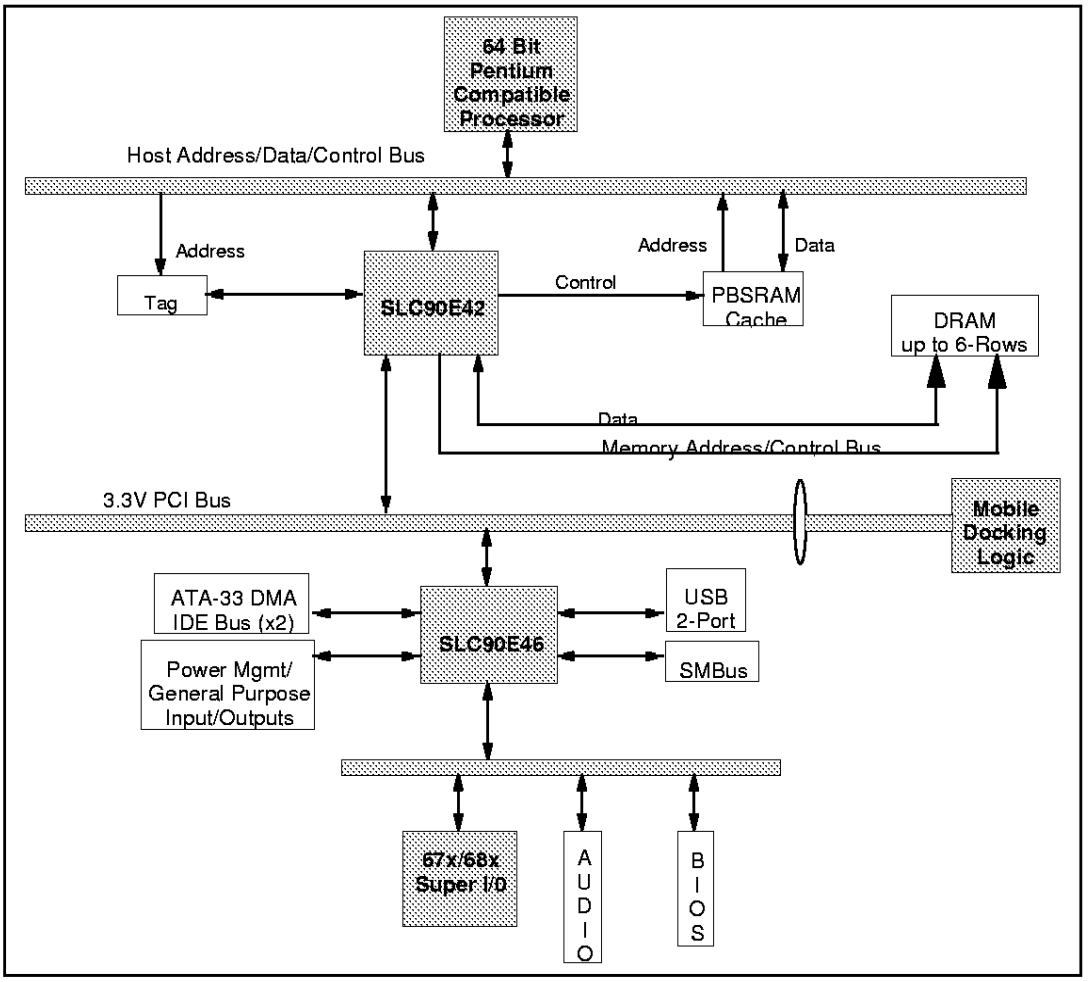


FIGURE 2 - TeXas SYSTEM BLOCK DIAGRAM

3. THE SLC90E42 SIGNAL DESCRIPTION

This section provides a detailed description of each SLC90E42 signal. The signals are arranged in functional groups according to their associated function.

The 'n' symbol at the beginning of a signal name indicates that it is an active low signal. When 'n' is not present before the signal name, it indicates an active high signal.

The term assert or assertion indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate or negation indicates that a signal is inactive.

3.3V/2.5V indicates that the buffer is 3.3V or 2.5V only, depending on the voltage connected to V_{cc} X pins.

3.3V/5V indicates that the output is 3.3V and input is 3.3V receiver with 5V tolerance. 5V indicates 3.3V receiver with 5V tolerance.

Table 1 - Host Interface

NAME	TYPE	DESCRIPTION
A[31-3]	I/O 3.3V/2.5V	**Address Bus:** During CPU cycles A[31-3] are inputs from the processor. The SLC90E42 drives A[31-3] during inquiry cycles and L2 cache access cycles on behalf of PCI masters. A[31-26] acts as inputs (strapping pins) when nRST is asserted.
HD[63-0]	I/O 3.3V/2.5V	**Host Data:** Connected to the CPU data bus. These signals have internal pull-down resistors.
nBE[7-0]	I/O 3.3V/2.5V	**Byte Enables:** The CPU byte enables indicates which byte lane the current CPU cycle is accessing. A full 64-bit data must be provided to the CPU if it is a cacheable read cycle regardless of the state of nBE[7-0]. The SLC90E42 drives nBE[7-0] during L2 cache access cycles on behalf of PCI masters.
nADS	I 3.3V/2.5V	**Address Status:** CPU asserts nADS in T1 of the CPU bus cycle.
nBRDY	O 3.3V/2.5V	**Bus Ready:** When it is asserted indicates to the processor that data is available on reads or has been received on writes.
nNA	O 3.3V/2.5V	**Next Address:** When it is asserted to the processor indicates that it is ready to process a second cycle.
M/nIO, W/nR, D/nC	I 3.3V/2.5V	**Memory/IO:** Write/Read; Data/Code: Asserted with nADS to indicate the type of cycle that the processor is currently performing. The SLC90E42 drives W/nR during L2 cache access cycles on behalf of PCI masters.
AHOLD	O 3.3V/2.5V	**Address Hold:** The SLC90E42 asserts AHOLD to the processor when the PCI host controller is performing read/write memory cycle to DRAM/L2 cache to fill up/flush PCI Read/Write buffers. The SLC90E42 negates AHOLD when there is no immediate needs to serve the buffer or during PCI peer transfers.
nEADS	O 3.3V/2.5V	**External Address Strobe:** The SLC90E42 asserts this signal to inquire the L1 cache when PCI master is accessing system memory.
nHITM	I 3.3V/2.5V	**Hit Modified:** The CPU asserts the signal to indicate that the address presented with the last assertion of nEADS is modified in the L1 cache and needs to be written back (to L2 cache or DRAM).
nBOFF	O 3.3V/2.5V	**Back Off:** The SLC90E42 asserts this signal to terminate the present CPU cycle (without the assertion of nBRDY). The back-offed cycle will be re-issued after SLC90E42 negates nBOFF.
nHLOCK	I 3.3V/2.5V	**Host Lock:** All CPU cycles sampled with the assertion of nHLOCK and nADS until the negation of HLOCK must be atomic (i.e. no PCI accessing system memory is allowed).
nCACHE	I 3.3V/2.5V	**Cache Enable:** It is asserted by the CPU during a read cycle to indicate a burst line. When it is asserted during a write cycle indicates that the CPU will perform a burst write-back cycle. When nCACHE is asserted, the SLC90E42 will assert nKEN either with the first nBRDY, or with nNA if nNA is asserted before the first nBRDY.

NAME	TYPE	DESCRIPTION
nKEN/INV	O 3.3V/2.5V	**Ken/Invalidate:** This signal pin functions as both the nKEN signal during CPU read cycles, and the INV signal during L1 snoop cycles. During CPU cycles, nKEN/INV will be driven high during the 1st nBRDY or nNA assertion of a non-L1-cacheable CPU read cycle. nKEN/INV is driven high (low) during the PCI master memory write (read) snoop cycle.
nSMIACT	I 3.3V/2.5V	**System Management Interrupt Active:** The CPU asserts this signal when it is in system management mode as a result of an SMI. This signal must be sampled active with nADS for the processor to access the SMM space in system memory after SMM space has been loaded and locked by BIOS at system boot.

Table 2 - DRAM Interface

NAME	TYPE	DESCRIPTION
nRAS[3-0]/ nCS[3-0] nRAS4/ nCS4/BA1 nRAS5/ nCS5/MA13	O 3.3V	**Row Address Strobe (EDO/FPM):** These signal pins select the active DRAM row. **Chip Select (SDRAM):** These pins activate the SDRAMs to accept commands. When 64Mbit SDRAM support is enabled, BA1/MA12 and MA13 are muxed with nRAS4 and nRAS5 signals, respectively.
nCAS[7-0]/ DQM[7-0]	O 3.3V	**Column Address Strobe (EDO/FPM):** These signal pins select the columns. **Data Mask (SDRAM).** These pins act as synchronized output enables during a read cycle and a byte mask during a write cycle.
MA[11-0]	O 3.3V	**Memory Address (EDO/FPM/SDRAM):** This is the row and column address bus for DRAM. The driving capability of these output buffers are programmable through the DRAMEC register. When 64Mbit SDRAM support is enabled, the required MA12/BA1 and MA13 are muxed with the nRAS4 and nRAS5 signals, respectively.
MD[63-0]	I/O 3.3V/5V	**Memory Data:** These signals are connected to the DRAM data bus. These signals have internal pull-down resistors.
nMWE	O 3.3V	**Memory Write Enable (FPM/EDO/SDRAM):** This signal has programmable buffer size selection.
nMWEB	O 3.3V	**Memory Write Enable (FPM/EDO/SDRAM, second copy):** This signal also has programmable buffer size selection
nSRAS[A,B]	O 3.3V	**SDRAM Row Address Strobe:** When active, this signal latches Row Address on the positive edge of the clock. This signal also allows Row Access and pre-charge. Two copies are provided for loading purpose. These signals have programmable buffer size selection.

NAME	TYPE	DESCRIPTION
nSCAS[A,B]	O 3.3V	**SDRAM Column Address Strobe:** When active, this signal latches column Address on the positive edge of the clock. This signal also allows Column Access. Two copies are provided for loading purpose. These signals have programmable buffer size selection.
CKE/MAA0	O 3.3V	**SDRAM Clock Enable:** When this signal is negated, SDRAM enters into power-down mode. The SLC90E42 negates CKE when nSUSSTAT is asserted. Memory Address MAA0: This signal is also muxed to provide a second copy of memory address MA0 (MAA0). Bit2 of register DRTH (at offset 67H) is used to enable the MA function.
CKEB/MAA1	O 3.3V	**SDRAM Clock Enable (second copy):** When this signal is negated, SDRAM enters into power-down mode. This pin is not implemented through the Suspend Well and should not be used if Suspend-to-RAM is implemented. The SLC90E42 negates CKEB when nSUSSTAT is asserted. Memory Address MAA1: This signal is also muxed to provide a second copy of memory address MA1 (MAA1). Bit2 of register DRTH (at offset 67H) is used to enable the MA function.

Table 3 - L2 Cache Interface

NAME	TYPE	DESCRIPTION
nCADS	O 3.3V	**Cache Address Strobe:** Assertion causes the L2 cache PBSRAM to latch the PBSRAM address pins into the PBSRAM address register.
nCADV	O 3.3V	**Cache Address Advance:** Assertion causes the L2 cache PBSRAM to advance to the next QWord in the cache line.
nCCS	O 3.3V	**Cache Chip Select:** The PBSRAM will power up and perform an access if nCCS and nCADS are both asserted. The PBSRAM will power down if nCCS is negated when nCADS is asserted. The PBSRAM will ignore the nADS when nCCS is negated. The PBSRAM will power up and perform an access if nCCS and nADS are asserted.
nCOE	O 3.3V	**Cache Output Enable:** When asserted, the L2 cache data RAMs will drive the host data bus.
nGWE	O 3.3V	**Global Write Enable:** When asserted, all the 64-bit data on the data bus will be written into L2 PBSRAM during the L2 cache write cycle.
nBWE	O 3.3V	**Byte Write Enable:** When nBWE is asserted with nGWE negated, the L2 PBSRAM will store data bytes which have their corresponding nBEx signals asserted into its memory array.
TAG[7-0]	I/O 3.3V/5V	**TAG Address:** These are inputs (to the internal address comparator) during CPU accesses and outputs (to the external TAG RAM) during L2 cache line fill. These signals have internal pull down resistors.
nTWE	O 3.3V	**Tag Write Enable:** When asserted new state and tag addresses are written into the external tag.
NC/nCS4	O 3.3V	**No Connection:** This is a no connection pin. **Chip Select (64Mb SDRAM):** This line becomes a chip select pin when 64Mb SDRAM option is enabled.

Table 4 - PCI Interface

NAME	TYPE	DESCRIPTION
AD[31-0]	I/O 3.3V/5V	**Address/Data:** PCI address and data lines. Address is driven with nFRAME asserted, data is driven or received in following clocks.
C/nBE[3-0]	I/O 3.3V/5V	**Command/Byte Enable:** The command is driven with nFRAME asserted, byte enables corresponding to supplied or requested data is driven in following clocks.
nFRAME	I/O 3.3V/5V	**FRAME:** Its assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer will be followed.
nDEVSEL	I/O 3.3V/5V	**Device Select:** The signal is asserted by the SLC90E42 when a PCI initiator is attempting to access DRAM. The signal is asserted by a PCI target in respond to PCI cycles which access the target's memory or IO spaces. nDEVSEL is asserted or sampled at medium decode time.
nIRDY	I/O 3.3V/5V	**Initiator Ready:** The signal is asserted when the initiator is ready for a data transfer.
nTRDY	I/O 3.3V/5V	**Target Ready:** The signal is asserted when the target is ready for a data transfer.
nSTOP	I/O 3.3V/5V	**Stop:** The signal is asserted by the target to request the master to stop the current transaction.
nLOCK	I/O 3.3V/5V	**Lock:** This signal is used to request, maintain, and release resource locks on PCI.
nREQ[3-0]	I 3.3V/5V	**PCI Bus Request:** PCI bus request signals for up to four master devices.
nGNT[3-0]	O 3.3V	**PCI Bus Grant:** PCI bus grant signals for the bus request signals from the PCI bus masters.
nPHLD	I 3.3V/5V	**PCI Hold:** PCI hold request signal coming from the bridge chip (i.e. SLC90E46). PHLD has the highest priority among the five bus request signals.
nPHLDA	O 3.3V/5V	**PCI Hold Acknowledge:** This signal is driven by the SLC90E42 to grant PCI bus to requesting bridge chip.
nCLKRUN	I/O 3.3V/5V	**Clock Run Enable:** This is an open drain output and also an input. The SLC90E42 uses this signal to request the Clock Run Central Resource, which is the SLC90E46, to start or maintain the PCI clock by the assertion of nCLKRUN. SLC90E42 will tri-state nCLKRUN open negation of reset. This signal requires external pull-up.
PAR	I/O 3.3V/5V	**Parity:** Parity bit for AD[31-0] and C/nBE[3-0]. This signal has an internal pull-down resistor.
nRST	I 3.3V/5V	**Reset:** When asserted, this signal will asynchronously reset the SLC90E42. The PCI signals will also tri-state compliant to PCI specifications.

Table 5 - Power Management Interface

NAME	TYPE	DESCRIPTION
SUSCLK	I 3.3V	**Suspend Clock:** 32 kHz input for DRAM refresh circuitry and clocking events in Suspend state. The DRAM refresh request is generated based on this clock during both Suspend and Normal states. This signal has an internal pull-down resistor.
nSUSSTAT	I 3.3V	**Suspend Status:** The assertion of this signal will place the SLC90E42 into Suspend state. Its negation will return the SLC90E42 to the normal working state. This signal has an internal pull-up resistor.

Table 6 - Clock & Test

NAME	TYPE	DESCRIPTION
HCLKIN	I 3.3V/2.5V	**Host Clock In:** This is a buffered host clock input. This clock is used by all of the SLC90E42 logic that is in the Host Clock domain.
PCLKIN	I 3.3V/5V	**PCI Clock In:** This is a buffered PCI clock input. This clock is used by all of the SLC90E42 logic that is in the PCI clock domain.
nTEST	I 3.3V	**Test In:** This pin should be pulled high with an external pull-up during normal operation.

Table 7 - Power and Ground Pins

NAME	TYPE	DESCRIPTION
V_{CC}	3.3V	**Main Power Supply:** These pins are the main voltage supply for the SLC90E42 core and IO pads. Should be connected to 3.3V.
V_{CC} (CPU)	3.3V or 2.5V	**CPU interface Voltage Supply:** These pins are the main voltage supply for the IO pads that interface to the CPU bus. These pins should be connected to either 2.5V or 3.3V, depending on the voltage level of the CPU interface. If connected to 3.3V, they can be connected to the same 3.3V source that the V_{CC} pins are connected to.
V_{CC} (SUS)	3.3V	**Suspend Well Voltage Supply:** These pins are the main voltage supply for the SLC90E42 suspend logic and IO pads. If the system supports Suspend-to-RAM, then these pins should be on an isolated power plane; Otherwise, they can be connected to the same 3.3V source that the V_{CC} pins are connected to.
VREF	3.3V or 5V	**Voltage Reference:** This pin is connected to 5V if SLC90E42 signals are required to be 5V tolerant.
VSS	0V	**Ground**

The following table shows the state of all the SLC90E42 output and bi-directional signals when nRST is asserted.

Table 8 - Signal States During and After a Hard Reset

NAME	STATE DURING RESET	STATE AFTER RESET
A[31-3]	Tri-State*	Tri-State
HD[63-0]	Tri-state	Tri-State
nBRDY	High	High
nNA	High	High
AHOLD	High	Low
nEADS	High	High
nBOFF	High	High
nKEN/INV	Low	Low
nRAS[5-0]	High	High
nCAS[7-0]	High	High
MA[11-0], BA1, MA13	Undefined	Undefined
nMWE, nMWEB	High	High
nSRAS[A,B]	High	High
nSCAS[A,B]	High	High
CKE, CKEB	Low	High
MD[63-0]	Tri-State	Tri-State
nCADV	High	High
nCADS	High	High

NAME	STATE DURING RESET	STATE AFTER RESET
nTAG[7-0]	Tri-State	Tri-State
nTWE	High	High
nGWE	High	High
nBWE	High	High
nCCS	Low	Low
nCOE	High	High
NC/nCS4	Undefined	High
AD[31-0]	Tri-Stated	Tri-State
C/nBE[3-0]	Tri-Stated	Tri-State
nFRAME	Tri-State	Tri-State
nDEVSEL	Tri-State	Tri-State
nIRDY	Tri-State	Tri-State
nTRDY	Tri-State	Tri-State
nSTOP	Tri-State	Tri-State
nLOCK	Tri-State	Tri-State
nGNT[3-0]	Tri-State	High
nPHLDA	High	High
PAR	Tri-State	Undefined
nCLKRUN*	Tri-state	Tri-State

*A[31-27], nGNT[3-0] and nPHLDA act as inputs during reset period, and nCLKRUN acts as an input during suspend mode.

4. SLC90E42 REGISTER DESCRIPTION

There are two sets of accessible registers, namely I/O mapped and PCI configuration registers. The IO mapped registers are used to control access to the PCI configuration registers. Other than the PCI bus arbiter, which is controlled by an IO mapped register, the SLC90E42 configuration registers are managed through PCI configuration mechanism "1".

The SLC90E42 internal registers can be accessed as Byte, Word, or DWord. They are only accessible by the host processor and cannot be accessed by the PCI masters.

Some of the SLC90E42 registers contain reserved bits. Software must ensure that the value of the reserved bit positions are preserved. That is, Software must first get the value of the reserved bits, merged the value with the new values for the other bits and then write back to the register.

Upon reset, the SLC90E42 sets its internal registers to predetermined default states, which represents the minimum functionality feature set required to bring up the system. It is the responsibility of the BIOS to properly program the configuration registers to achieve optimal system performance.

4.1. IO Mapped Registers

There are three registers reside in the CPU IO address space. Two of the three, Configuration Address Register (CONFIG_ADDR) and Configuration Data Register (CONFIG_DATA), are used to control access to the PCI configuration registers. The third one, PM2_CNTRL, is used when ACPI power management mode is enabled.

4.1.1. PM2_CNTRL - PM2 Register Block

I/O Address: 0022h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
7-1	Reserved
0	Arbiter Disable (ARB_DIS): When this bit is "1", the SLC90E42 will not respond to any PCI master request (including the south bridge request) until it is reset to "0".

This register is used during ACPI mode to disable the PCI bus arbiter before the processor is put in deep sleep mode, i.e. stop clock, without the capability to maintain data coherency.

4.1.2. CONFIG_ADDRESS - PCI Configuration Address Register

I/O Address: 0CF8h
Default Value: 00000000h
Access: Read/Write

CONFIG_ADDRESS is a 32 bit register accessed only when referenced as a DWord.

BIT	FUNCTION
31	1: Enable PCI configuration cycle. 0: Disable.
30-24	Reserved
23-16	PCI Bus number: When the value is "00", the target device is connected to the PCI bus that is directly connected to the SLC90E42, and a type 0 configuration cycle is generated on PCI bus. Any other bus number indicates that the target device is connected to a lower level PCI bus, and a type 1 configuration cycle is generated on PCI bus.
15-11	Device number: This is binary coded device number. SLC90E42 is assigned the device number "0".
10-8	Function number: This field is mapped to AD[10-8] during PCI configuration cycle. The function number should always be '000b' to address registers on SLC90E42.
7-2	Register number: This field is mapped to AD[7-2] during PCI configuration cycle.
1-0	Reserved

4.1.3. CONFIG_DATA - PCI Configuration Data Register

I/O Address: 0CFC - 0CFFh
Default Value: 00000000h
Access: Read/Write

CONFIG_DATA is a four byte IO space that is mapped to a portion of PCI configuration space, which is determined by the contents of CONFIG_ADDRESS. Either Byte, Word, or DWord access is allowed to access the CONFIG_DATA register.

BIT	FUNCTION
31-0	Data of the mapped-to PCI configuration space.

4.2. PCI Configuration Registers

The configuration register access mechanism uses the CONFIG_ADDRESS register and CONFIG_DATA register. To reference a configuration register, a DWord I/O write is used to place the address of the register into the CONFIG_ADDRESS register, followed by an I/O read/write from/to the register CONFIG_DATA.

The following table lists the offset address, mnemonic, name and access right of all SLC90E42 PCI configuration registers.

The following nomenclature is used for access attributes:

RD Read only - meaning a register or a field of the register can only be read, write to the register has no effect.

R/W Read/Write - meaning a register or a field of the register can be read and written.

R/WC Read and Write Clear - meaning a register bit can be read and written. A write of 1, however, clears (set to 0) the corresponding bit and a write of 0 has no effect.

Table 9 - PCI Configuration Registers

PCI OFFSET ADDRESS	MNEMONIC	REGISTER NAME	ACCESS RIGHT
00-01h	VID	Vendor Identification	RO
02-03	DID	Device Identification	RO
04-05	PCICMD	PCI Command Register	R/W
06-07	PCISTS	PCI Status Register	RO, RWC
08	RID	Revision ID	RO
09-0B	CLASSCODE	Class Code	RO
0C		Reserved	
0D	MLT	Master Latency Timer	R/W
0E	HEDT	Header Type	
0F	BIST	BIST Register	R/W
10-4E		Reserved	
4F	ACON	Arbitration Control	R/W
50	PCON	PCI Control Register	R/W
51	Reserved		
52	CC	Cache Control	R/W
53	DRAMCACHE	DRAM Cache Control	R/W
54-55	SDRAMC	SDRAM Control	R/W
56	DRAMEC	DRAM Extended Control	R/W
57	DRAMC	DRAM Control	R/W
58	DRAMT	DRAM Timing	R./W
59-5F	HMM	High Memory Mapping	R/W
60-65	DRB	DRAM Row Boundary	R/W
66		Reserved	
67-68	DRT	DRAM Row Type	R/W

PCI OFFSET ADDRESS	MNEMONIC	REGISTER NAME	ACCESS RIGHT
69-6F		Reserved	
70	MTT	Multiple Transaction Timer	R/W
71	ESMRAMC	Extended System Management RAM Control	R/W
72	SMRAMC	System Management RAM Control	R/W
73-78		Reserved	
79	MCTL	Miscellaneous Control	R/W
7A-BF		Reserved	
C0	SCPUC	Supplemental CPU Control	R/W
C1	SCACHEC	Supplemental Cache Control	R/W
C2	SRAMC	Supplemental DRAM Control	R/W
C3	SPCIBC	Supplemental PCI Buffer Control	R/W
C4	SPCICH	Supplemental PCI Control High	R/W
C5	SPCICL	Supplemental PCI Control Low	R/W
C6-FF		Reserved	

4.2.1. VID - Vendor Identification Register

Offset Address: 00 - 01h
Default Value: 10B8h
Access: Read

4.2.2. DID - Device Identification Register

Offset Address: 02 - 03h
Default Value: 9042h
Access: Read

4.2.3. PCICMD - PCI Command Register

Offset Address: 04 - 05h
Default Value: 06h
Access: Read

BIT	FUNCTION
15-10	Reserved
9	Fast Back-to-Back: not implemented, hardwired to "0".
8	nSERR Enable: not implemented, hardwired to "0".
7	Address/Data Stepping: not implemented, hardwired to "0"
6	Parity Error Enable: not implemented, hardwired to "0".
5	Video Pallet Snooping: not implemented, hardwired to "0".
4	Memory Write and Invalidate Enable: The SLC90E42 never uses this PCI command. Hardwired to "0".
3	Special Cycle Enable: The SLC90E42 never responds to PCI special cycle. Hardwired to "0".
2	Bus Master Enable: SLC90E42 does not support disabling of its bus master capability on the PCI bus. Always "1".
1	Memory Access Enable: The SLC90E42 always allow PCI masters to access main memory if the PCI address selects enabled DRAM space. Always "1".
0	IO Access Enable: The SLC90E42 does not respond to PCI IO cycles. Always "0".

4.2.4. PCISTS - PCI Status Register

Offset Address: 06 - 07h
Default Value: 0200h
Access: Read/Write

BIT	FUNCTION
15	Detected Parity Error. Not implemented, hardwired to "0".
14	Signaled System Error: Hardwired to "0". The SLC90E42 does not support nSERR.
13	Received Master Abort: When SLC90E42 terminates a HOST-to-PCI transaction with an master abort, this bit is set to "1". To reset this bit, write a "1" to it. Master abort is the normal and expected termination of PCI special cycle.
12	Received Target Abort: When a SLC90E42 initiated PCI transaction is terminated with a target abort, this bit is set to "1". To reset the bit, write a "1" to it.
11	Signaled Target Abort: Always "0", since the SLC90E42 never terminates a PCI cycle with target abort.
10-9	nDEVSEL timing: Always "01" to select "medium" timing, which is two PCI clocks after the assertion of nFRAME, when the SLC90E42 asserts nDEVSEL as a PCI target.
8	Data Parity Detected: Always "0", not implemented.
7	Fast Back-to-Back: Always "0", as the SLC90E42 never generates this type of cycle.
6	User Defined Format: Always "0", not implemented.
5	66MHz PCI Capable: Always "0", the SLC90E42 does not support 66 MHz PCI bus.
4-0	Reserved

4.2.5. RID - Revision Identification Register

Offset Address: 08h
Default Value: 00h
Access: Read

BIT	FUNCTION
7-0	SLC90E42 revision number

4.2.6. CLASSC - Class Code Register

Offset Address: 09 - 0Bh
Default Value: 060000h
Access: Read

BIT	FUNCTION
23-16	Base Class Code: always "06" indicating that the SLC90E42 is a bridge device
15-8	Sub-Class Code: "00", indicating that this is a host bridge
7-0	Programming Interface: "00"

4.2.7. MLT - Master Latency Register

Offset Address: 0Dh
Default Value: 00h
Access: Read/Write
Size: 8 bits

MLT controls the amount of time the SLC90E42 as a bus master can burst data on the PCI bus. The count value is an 8 bit quantity, however bits 2-0 are reserved and assumed to be "0". MLT gives the host CPU a minimum amount of PCI bandwidth in a multiple master environment. The MLT value represents the guaranteed time slice (measured in PCI clocks) allocated to the SLC90E42, after which it must surrender the bus as soon as other PCI masters request the bus.

BIT	FUNCTION
7-6	Reserved. Read as '00'.
5-3	Timer Initial Value.
2-0	Reserved. Read as '00'.

4.2.8. HEDT - Header Type Register

Offset Address: 0Eh
Default Value: 00h
Access: Read

BIT	FUNCTION
7-0	These bits are hardwired to be 00.

4.2.9. BIST - BIST Register

Offset Address: 0Fh
Default Value: 00h
Access: Read/Write

The Built In Self Test function is not supported by the SLC90E42. Write to this register has no effect.

BIT	FUNCTION
7-0	These bits have default value "00".

4.2.10. ACON - Arbitration Control Register

Offset Address: 4Fh
Default Value: 00h
Access: Read/Write

This is a dummy R/W register. Writing to this register has no effect on the SLC90E42.

BIT	FUNCTION
7-0	These bits have default value "00".

4.2.11. PCON - PCI Control Register

Offset Address: 50h
Default Value: 00h
Access: Read/Write.

This is dummy R/W register. Writing to this register has no effect on the SLC90E42.

BIT	FUNCTION
7-0	These bits have default value "00".

4.2.12. CC - Cache Control Register

Offset Address: 52h
Default Value: SSSS0000b (S = Strapping option)
Access: Read/Write

BIT	FUNCTION
7-6	Secondary cache size: This field reflects the inverted signal level on the A[31:30] pins at the rising edge of the RESET signal. The options are: 00: Cache not populated (cache disabled) 01: 256K bytes 10: 512K bytes 11: Reserved The RESET value can be overwritten by subsequent writes to the bit.
5-4	L2 cache Type: This field reflects the inverted signal level on the A[29-28] pins at the rising edge of the RESET signal. The reset value can be overwritten with subsequent writes to the CC register. 00: Pipelined Burst SRAM 01: Reserved 10: Reserved 11: Two banks of PB SRAM When two banks of PBSRAM is selected, nCCS is negated after nNA is asserted, and reasserted after a pipelined nADS is detected. nCADS is asserted along with the final nBRDY for a cycle if a pipelined cycle is outstanding (i.e. an nADS was detected).
3	NA disable: When it is "1", nNA is never asserted. In normal operation, this pin should be "0".
2	Reserved
1	L2 cache force miss or Invalidate: When L2 cache is enabled (and L1 cache is enabled) and this bit is a '1', memory read cycle causes the corresponding L2 cache entry to be flushed to the main memory. When L2 cache is populated but L1 is disabled, and this bit is a "1", any CPU read cycle will invalidate the selected tag entry. Memory write cycle possibly creates incoherent DRAM/L2 data when this bit is "1". When this bit is a "0", normal cache hit/miss detection and cycle processing occurs.
0	L1 cache enable: This bit enables and disables the first level cache. When this bit is set to a "1", nKEN is asserted during cacheable memory cycles. When the bit is set to "0", nKEN is always negated.

4.2.13. DRAMCACHE - DRAMCACHE Control Register

Offset Address: 53h
Default Value: 00h
Access: Read

BIT	FUNCTION
7-6	Reserved
5	DRAM cache as L2 cache: Hardwired to "0", indicating no DRAM cache is installed.
4-0	DRAM cache refresh timer: The values of HCLKs allocated for the DRAM cache to refresh the memory array. This field is hardwired to "0" since DRAM cache is not supported.

4.2.14. SDRAMC - SDRAM Control Register

Offset Address: 54-55h
Default Value: 0000h
Access: Read/Write

BIT	FUNCTION
15-9	Reserved
8-6	Special SDRAM mode select. These bits select "1" of four special SDRAM modes for testing and initialization. The NOP command must be programmed first before any other command can be issued. After the DRAM detection process has completed, these bits must remains at '000' During normal DRAM operation. 000: Normal SDRAM mode (default) 001: NOP command enable. This setting enables a mode where all CPU to DRAM cycles are converted to an SDRAM NOP command on the memory interface. 010: All bank precharge command enable. This setting enables a mode where all CPU to DRAM cycles are converted to an all banks precharge command on the memory interface. 011: Mode register command enable. In this setting all CPU to DRAM cycles are converted to MRS commands to the memory interface. The command is driven on the MA[11:0] lines. MA[2:0] should be always driven to "010" for a burst of four modes. MA3 should be always driven to "1" for interface wrap type mode. MA4 should be driven to the value in the nCAS latency bit. MA[6:5] should be driven to "01" in all cases, and MA[11:7] is always "0". The BIOS will select an appropriate host address for each row of memory such that the right commands are generated on the memory address MA[11:0]. For example, a memory address of 1D0h will set up the mode register in row "0" of SDRAM with a burst length of four, wrap type of interleaved and a CAS latency of three. 100: CBR cycle enable. This setting enables a mode where all CPU to DRAM cycles are converted to SDRAM CBR refresh cycles on the memory interface. 101: Reserved 11x: Reserved
5	nRAS to nCAS override: When set to "1", and bit four is "0" (CAS latency is three), then a nRAS to nCAS delay of two HCLKs is used for SDRAM. Otherwise, bit four determines the nRAS to nCAS latency.
4	nCAS latency. When set to "1", the nCAS latency is two HCLKs. Otherwise, it is three HCLKs nCAS latency for all SDRAM cycles.
3	nRAS timing. This field has no effect on the nRAS timing. The nRAS Precharge timing is fixed at three HCLKs, nRAS active to Precharge is fixed at 5 HCLKs, and Refresh to nRAS Active is fixed at 12 HCLKs.
2	Reserved
1	64Mbit SDRAM enable. When set to "0", the SLC90E42 supports 64Mbit EDO/FPM DRAM but not SDRAM. When set to "1", 64Mb SDRAM is also supported by the SLC90E42. In this mode, the system is limited to five rows of DRAM. The RAS5/nCS5 signal becomes MA13, and RAS4/nCS4 becomes BA1. The KRQAK/nCS4 signal becomes nCS4.
0	Reserved

The following table lists the nCAS latency, nRAS to nCAS, nRAS precharge and Refresh to nRAS active programmable timings.

HOST FREQUENCY	SDRAMC BITS [5:3]	CAS LATENCY (CL)	ACTUAL nRAS TO nCAS (TRCD)	nRAS PRECHARGE (TRP)	REFRESH TO nRAS (TRC)
60/66 MHz	00X	3 HCLKs	3 HCLKs	3 HCLKs	12 HCLKs
60/66 MHz	10X	3 HCLKs	2 HCLKs	3 HCLKs	12 HCLKs
60/66 MHz	01X	2 HCLKs	2 HCLKs	3 HCLKs	12 HCLKs

4.2.15. DRAMEC - DRAM Extended Control Register

Offset Address: 56h
Default Value: 52h
Access: Read/Write

BIT	FUNCTION
7	SDRAM Single Read nBRDY Assertion Control Bit: 0: Normal nBRDY assertion timing. 1: Delay one HCLK for nBRDY assertion.
6	Refresh nRAS assertion: This bit has no effect on the refresh nRAS assertion, which is fixed at 5 HCLKs.
5	Fast EDO leadoff. This feature is not implemented.
4	Speculative leadoff. This feature is not implemented.
3	Reserved
2-1	MA Drive Strength: This field controls the strength of the IO buffers driving the MA, nSRASx, nSCASx, nMWEx and CKEx pins. MA13 and BA1, like nRASx and nCASx signals, have 8mA driving capability. **MA[11:0]** — **nSRAS[A,B], nSCAS[A,B], nMWEx** — **CKEx** 00 — 10mA — 10mA 01 — 10mA — 16mA 10 — 16mA — 10mA 11 — 16mA — 16mA
0	Reserved

4.2.16. DRAMC - DRAM Control Register

Offset Address: 57h
Default Value: 01h
Access: Read/Write

BIT	FUNCTION
7-6	Hole Enable (HEN): This field creates a memory hole in DRAM space. CPU cycles matching an enabled hole are passed on to PCI. For PCI cycles that match the enabled hole are ignored by the SLC90E42. **Hole Enabled** 00 None 01 512KB-640KB 10 15MB-16MB 11 14MB-16MB
5	Reserved
4	Enhanced Paging Disable (EPD): This field is hardwired to "0".
3	EDO Detect Mode Enable: This bit, when set to "1", enables a special timing mode for BIOS to detect EDO DRAM type. Once all DRAM row banks have been tested, this bit should be reset to "0".
2-0	DRAM refresh rate: This field selects the DRAM refresh rate for FPM/EDO only system. If any row is populated with SDRAM this field must be set to 15.6µs refresh rate. DRAM refresh is implemented using SUSCLK. **DRAM Refresh Rate** 000 Disabled, no refresh 001 15.6µs (default) 010 31.2µs 011 64.4µs 100 125µs 101 256µs 110 Reserved 111 Reserved

4.2.17. DRAMT - DRAM Timing Register

Offset Address: 58h
Default Value: 28h
Access: Read/Write

BIT	FUNCTION
7	Reserved
6-5	DRAM read burst timing: This field controls the DRAM burst read timing. **EDO burst rate** / **FPM burst rate** 00 x333 / x333 01 x333 / x333 (default) 10: x222 / x333 11: Reserved / Reserved
4-3	DRAM write burst timing. **EDO burst rate** / **FPM burst rate** 00: x333 / x333 01: x333 / x333 (default) 10: x222 / x333 11: Reserved
2	Reserved
1-0	DRAM leadoff timing: This field controls the DRAM leadoff timings during page miss or row miss. **Read Leadoff** / **Write Leadoff** / **nRAS Precharge** / **nRAS to nCAS Latency** 00 11 hclks / 7 hclks / 3 hclks / 4 hclks (default) 01 10 hclks / 6 hclks / 3 hclks / 3 hclks 10 11 hclks / 7 hclks / 4 hclks / 4 hclks 11 10 hclks / 6 hclks / 4 hclks / 3 hclks

4.2.18. HMM - High Memory Mapping Register

Offset Address: 59-5Fh
Default Value: 00h
Access: Read/Write

The memory space in the 640Kbytes to 1Mbytes address range is divided into 14 memory segments of various size. Seven HMM registers are used to set up these memory segments for various read, write and cacheable capability. The following table lists the data flow for possible memory attribute setups.

MEMORY ATTRIBUTES	MEMORY READ CYCLES	MEMORY WRITE CYCLES	COMMENTS
Read Only	Treated as normal memory read cycles Code accesses are L1 cacheable. Data accesses are not cacheable in either L1 or L2.	Passed to PCI bus	1. This option is used after shadow is done. 2. Can be used to program flash ROM.
Write Only	Passed to PCI bus.	Treated as normal memory write cycle. When cacheable is enabled, it is L1/L2 cacheable.	This option can be used to shadow PCI/ISA BIOS onto main memory.
Read/Write	The memory segment is used as normal memory. Both CPU and PCI masters can access this memory segment. When cacheable is enabled, it is L1/L2 cacheable.	The memory segment is used as normal memory. Both CPU and PCI masters can access this memory segment.	This option makes the memory segment available for normal usage.
Disabled	Passed to PCI	Passed to PCI	

PCI master access to the high memory space is also controlled by the HMM registers:

A. If the HMM indicates a region is writeable, then PCI master writes will be accepted (nDEVSEL asserted, and the cycle is passed to DRAM controller).
B. If the HMM indicates a region is readable, PCI master reads is accepted (nDEVSEL is asserted, and the cycle is passed to DRAM controller).
C. If a PCI write to a non-writeable region, or a PCI read to a non-readable DRAM region occurs, the SLC90E42 will not asserted the nDEVSEL (the cycle is not considered a main memory cycle).

BIT	FUNCTION
7,3	Reserved
6,2	Cache enable: This bit controls the cacheability of the memory segment. “1”: enable. “0”: disable.
5,1	Write enable: This bit controls whether the memory segment is writeable. “1”: enable. “0”: disable.
4,0	Read enable: This bit controls whether the memory segment is readable. “1”: enable. "0": disable.

HMM REGISTER	ADDRESS OFFSET	MEMORY SEGMENTS	COMMENTS
HMM0[3:0]	59h	Not Used	
HMM0[7:4]	59h	0F0000h-0FFFFFh	BIOS Area
HMM1[3:0]	5Ah	0C0000h-0C3FFFh	ISA Add-on BIOS
HMM1[7:4]	5Ah	0C4000h-0C7FFFh	ISA Add-on BIOS
HMM2[3:0]	5Bh	0C8000h-0CBFFFh	ISA Add-on BIOS
HMM2[7:4]	5Bh	0CC000h-0CFFFFh	ISA Add-on BIOS
HMM3[3:0]	5Ch	0D0000h-0D3FFFh	ISA Add-on BIOS
HMM3[7:4]	5Ch	0D4000h-0D7FFFh	ISA Add-on BIOS
HMM4[3:0]	5Dh	0D8000h-0DBFFFh	ISA Add-on BIOS
HMM4[7:4]	5Dh	0DC000h-0DFFFFh	ISA Add-on BIOS
HMM5[3:0]	5Eh	0E0000h-0E3FFFh	BIOS Extension
HMM5[7:4]	5Eh	0E4000h-0E7FFFh	BIOS Extension
HMM6[3:0]	5Fh	0E8000h-0EBFFFh	BIOS Extension
HMM7[7:4]	5Fh	0EC000h-0EFFFFh	BIOS Extension

The Video Buffer Area (A0000h - BFFFFh) is always mapped to PCI/ISA bus except during SM mode (when nSMIACT is asserted).

4.2.19. DRB - DRAM Row Boundary Register

Offset Address: 60-65h
Default Value: 00h
Access: Read/Write

The six DRAM row boundary registers define the upper and lower addresses for each DRAM row. Contents of these 8 bit registers represent the boundary addresses in 4 Mbytes granularity.

DRB0 = Total amount of memory in row 0 (in 4Mbytes).
DRB1 = Total amount of memory in row 0 + row 1 (in 4Mbytes).
DRB2 = Total amount of memory in row 0 + row 1 + row 2. (in 4Mbytes).
DRB3 = Total amount of memory in row 0 + row 1 + row 2 + row 3. (in 4Mbytes).
DRB4 = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4. (in 4Mbytes).
DRB5 = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 + row 5. (in 4Mbytes).

Each DRAM array can be configured with 512K (i.e. 4M bytes row size), 1M (i.e. 8M bytes row size), 4M, or 16M deep by 32/64 or 36/72 bit wide SIMM/DIMM. Each register defines an address range that will cause a particular nRAS line to be asserted.

BIT	FUNCTION
7	Reserved
6-0	Row boundary address: This seven bit value is compared against the address lines A[28:22] to determine the upper address limit of a particular row. The row size is then equal to DRB - previous DRB.

For an unpopulated row, the corresponding DRB register has a value equal to the previous row, which implies row size of 0 byte. The DRB5 reflects the maximum amount of DRAM in the system. The top of memory is determined by the value written into DRB5. If DRB5 is greater than 256M bytes, then 256M bytes of DRAM are available. BIOS must make sure that the DRB registers do not reflect more than 256M bytes of main memory.

DRB0 offset address is 60h, and it is corresponding to DRAM row 0.
DRB1 offset address is 61h, and it is corresponding to DRAM row 1.
DRB2 offset address is 62h, and it is corresponding to DRAM row 2.
DRB3 offset address is 63h, and it is corresponding to DRAM row 3.
DRB4 offset address is 64h, and it is corresponding to DRAM row 4.
DRB5 offset address is 65h, and it is corresponding to DRAM row 5.

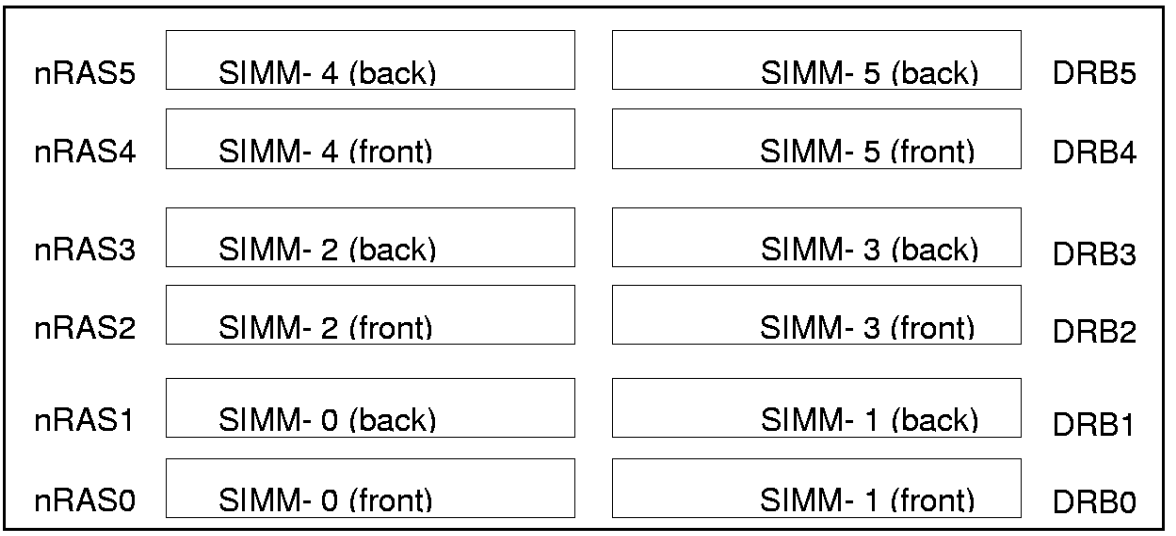


FIGURE 3 - DRB REGISTERS IN TYPICAL MEMORY CONFIGURATION

Example 1: The memory sockets are populated with four single-sided 1MB x 32 SIMMs, a total of 16M bytes of DRAM. Since two SIMMs are required for each populated row that makes each populated row 8M bytes in size.

DRB0=02h Populated with 2x4 (8) Mbytes of memory.
DRB1=02h No memory populated.
DRB2=04h Populated with another 8 Mbytes memory that makes total 4x4 (16) Mbytes of memory.
DRB3=04h No memory populated.
DRB4=04h No memory populated.
DRB5=04h No memory populated.

Example 2: The memory array is populated with two 2M bytes x 32 double-sided SIMMs (one physical row) and four 4M bytes x 32 single-sided SIMMs (two physical rows), makes a total of 96M bytes.

DRB0=04h Populated with 16 Mbytes of memory (front side).
DRB1=08h Populated with another 16 Mbytes of memory (back side), total memory now is 32M bytes.
DRB2=10h Populated with 32 Mbytes of memory (single side), total memory now is 64Mbytes.
DRB3=10h No memory populated.
DRB4=18h Populated with another 32 Mbytes of memory (single side), total memory is 96Mbtyes.
DRB5=18h No memory populated.

4.2.20. DRTH - DRAM Row Type Register High

Offset Address: 67h
Default Value: S0000000h
Access: Read/Write

BIT	FUNCTION
7	66MHz Host Frequency. This bit indicates the host clock frequency, 60MHz or 66MHz. This bit is initialized to the inverted level on A[27] at the rising edge of the nRST. Since the A[27] pin has an internal weak pulldown, unless an external pull-up resistor exists, the field should be initialized to "1", indicating 66MHz. Subsequent writes to this bit can override the reset strap value.
6	Reserved
5,1	DRAM type of row 5: 00 FPM DRAM 01 EDO DRAM 10 SDRAM 11 Reserved
4,0	DRAM type of row 4: 00 FPM DRAM 01 EDO DRAM 10 SDRAM 11 Reserved
3	Reserved
2	Function definition for the CKE and CKEB pins. 0. CKE and CKEB lines are used to propagate CKE and CKEB control signals. 1. CKE becomes MAA0, and CKEB becomes MAA1. It provides a second copy of MA0/MA1 signals to share the loading on these two signals. This feature is mainly used in desktop applications where four rows of EDO memory with x4 EDO devices could be used.

4.2.21. DRTL - DRAM Row Type Register Low

Offset Address: 68h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
7,3	**DRAM Type of Row 3:** 00 FPM DRAM. 01 EDO DRAM 10 SDRAM 11 Reserved
6,2	**DRAM Type of Row 2:** 00 FPM DRAM. 01 EDO DRAM 10 SDRAM 11 Reserved
5,1	**DRAM Type of Row 1:** 00 FPM DRAM. 01 EDO DRAM 10 SDRAM 11 Reserved
4,0	**DRAM Type of Row 0:** 00 FPM DRAM. 01 EDO DRAM 10 SDRAM 11 Reserved

4.2.22. MTT - Multiple Transaction Timer Register

Offset Address: 70h
Default Value: 20h
Access: Read/Write

This register is implemented as a dummy R/W register and has no effect on the SLC90E42.

BIT	FUNCTION
7-2	MTT Count Value: (measured in PCICLKs) Any value in this field has no effect on the SLC90E42.
1-0	00

4.2.23. ESMRAMC - Extended System Management RAM Control Register

Offset Address: 71h
Default Value: 00h
Access: Read/Write

The SLC90E42 supports dual SMRAM mode: compatible (C-SMRAM) and Extended SMRAM (E-SMRAM) modes. The two modes are mutually exclusive, meaning that when enable E-SMRAM the memory range A0000h-BFFFFh, which is the C-SMRAM space, is considered on the PCI bus.

The C-SMRAM provides non-cacheable memory space in the range of A0000h to BFFFFh. No address remapping is performed during System Management Mode.

The E-SMRAM space is cacheable with size from 128KB up to 1MB. Two types of E-SMRAM are supported: the H-SMRAM that is physically located at A0000h to 0FFFFFh (below 1Mbytes), or the TSEG that chops off 128K bytes to 1M bytes from top-of-memory (above 1Mbytes). The CPU address range of the H-SMRAM is from 100A0000h to 100FFFFFh. Any memory space that is not used as shadowed RAM can be used as H-SMRAM .

The CPU address range for the TSEG is from 10000000h + Top-Of-Memory - TSEG_SIZE to 10000000h + Top-Of-Memory. When TSEG is enabled, the BIOS should report memory size of (total memory - TSEG_Size) to OS.

BIT	FUNCTION
7	H_SMRAM_EN: When it is "1", SMRAM space appears in the CPU address space: 100A0000h to 100FFFFFh (above 256MB). Otherwise, the H-SMRAM is disabled.
6	E_SMRAM_ERR: This bit is set when CPU accesses the E-SMRAM space (either H-SMRAM or TSEG), while not in SMM mode and with the D-OPEN bit = 0. The software should write a "1" to this bit to clear it. The cycle is forwarded to the PCI bus.
5	SMRAM_Cache: This bit is hardwired to 0 to select write-back cache mode for the E_SMRAM when the cacheable control is enabled.
4	SMRAM_L1_EN: This bit should set to "1" if extended SMRAM is being used and the system wants this memory space to be L1 cacheable. When set to "1", the E-SMRAM space is L1 cacheable. Default is "0".
3	SMRAM_L2_EN: This bit should set to "1" if extended SMRAM is being used and there is less than 32MB memory installed. Setting this bit to "1" enable L2 write back cache scheme for E-SMRAM when bit 4 is enabled. Default is "0". The E_SMRAM is mapped to the high 32M bytes space of the total 64M bytes of cacheable memory.
2-1	TSEG_SIZE: This memory is taken from the top of DRAM space, which is then no longer claimed by the memory controller (all normal memory cycles are passed to the PCI bus). 00: 128KB => appears in (TOM-128K) to TOM 01: 256KB => appears in (TOM-256K) to TOM 10: 512KB => appears in (TOM-512K) to TOM 11: 1MB. => appears in (TOM-1M) to TOM
0	TSEG_EN: When G_SMRAME = "1" (bit 3 of SMRAMC) and TSEG_EN = "1", the TSEG is enabled to appear in the appropriate space.

4.2.24. SMRAMC - System Management RAM Control Register

Offset Address: 72h
Default Value: 02h
Access: Read/Write

BIT	FUNCTION
7	Reserved
6	D_OPEN: This bit can be used to initialize SMM space. When D_OPEN = "1" and D_LOCK = 0, the SMM space is available for read/write access even though nSMIACT is negated (not asserted). When D_LOCK is set to a 1, the D_OPEN is set to a 0, and the bit becomes read-only. D_CLOSE and D_OPEN should be mutually exclusive, they should not be set to 1 simultaneously.
5	D_CLOSE: When set to "1", **data reference**, read and write, to the SMM space DRAM is passed to the PCI bus even when nSMIACT is asserted. **Code reference** still access SMM space DRAM. When set to "1", the software can "read" video frame buffer, page A & B, during System Management Mode.
4	D_LOCK: When power-on reset, this bit is set to "0", which allows the SMM space to be initialized with SMI handler. Through normal PCI configuration cycle, this bit can be set to a 1, which make the SMM space protected from further modification (not even from BIOS). This bit can only be cleared by a power-on reset. After it is set to a 1, this bit, as well as D_OPEN, becomes read-only.
3	G_SMRAME: Set this bit to "1" enables either C_SMRAM or E_SMRAM.
2-0	C_BASE_REG: These bits select the location of compatible SMM space. SMM DRAM is not re-mapped. These bits are set to 010 to select A0000h-BFFFFh as SMM space. All other values are reserved.

4.2.25. MCTL - Miscellaneous Control Register

Offset Address: 79h
Default Value: 04h
Access: Read/Write

BIT	FUNCTION
7	Reserved
6	ACPI Control Register Enable: When set to "1", CPU accesses to IO address 0022h is processed internally in the SLC90E42. When it is "0", any CPU access to IO address 0022h is passed on to the PCI bus.
5	Suspend Refresh Type. Decides which type of refresh is used during Power On Suspend or Suspend to DRAM modes. "0": CBR mode is selected. "1": self refresh is selected.
4	Normal Refresh Enable. Setting this bit to "1" switches refresh mode from suspend refresh to normal refresh. After reset, this bit is set to "0"; it is the software executing out of the EPROM to set this bit to "1" for the SLC90E42 to exit out of suspend refresh mode.
3	Reserved
2	Internal Clock Control. Set to "1" enabled the Gated Clock logic, which allows the SLC90E42 to turn off its internal clocks to certain logic blocks to reduce its power consumption when in standby mode.
1-0	Reserved

4.2.26. SNBC - Supplemental North Bridge Configuration Register

Offset Address: C0h
Default Value: 13h
Access: Read Only

BIT	FUNCTION
7-5	Reserved
4	Synchronous PCI: This bit reflects the status of the signal nPHLDA during RESET. 1: Enable synchronous PCI (Default) 0: Enable asynchronous PCI
3	Internal SRAM Test Mode: This bit reflects the status of the signal nGNT3 during RESET. 1: Normal working mode (default) 0: SRAM test mode
2	SDRAM Initialization Mode: This bit reflects the status of the signal nGNT2 during RESET. 1: Hardware initialization mode 0: Software (default)
1	SDRAM CAS Latency: This bit reflects the status of the signal nGNT1 during RESET. 1: 3 clocks 0: 2 clocks
0	SDRAM Burst Sequence: This bit reflects the status of the signal nGNT0 during RESET. 1: Interleaved 0: Linear

4.2.27. SCACHEC - Supplemental Cache Control Register

Offset Address: C1h
Default Value: A0h
Access: Read/Write

BIT	FUNCTION
7	Cache Write Leadoff 0: 3- 1:4- (default)
6	CPU Back-off Control Bit : 0: Back-off CPU after PCI post-write buffer is cleared when there is any outstanding PCI bus request (default). 1: Back-off CPU right away after any PCI bus request signal is asserted.
5	Cache Read Leadoff 0: 3- 1:4- (default)
	Reserved.
3	SDRAM Single Post Write Cycle Timing: 0: Normal timing. (default). 1: Faster timing (3 cycles write).
2	64Mb SDRAM Operating Mode. 0: 4-bank mode (default) 1: 2-bank mode
1	All DRAM Write Leadoff Cycle Timing (from the assertion of nADS) 0: Delay one HCLK, i.e. 6-x-x-x, when bit 0 is set to a 1 (default). 1: No delay, i.e. 5-x-x-x when bit 0 is set to a 1.
0	EDO DRAM Page Hit Write Cycle Timing: 0: Delay nCAS assertion for one HCLK for Page Hit Write Cycle (default). 1: Normal nCAS assertion timing, i.e. one HCLK after the assertion of nDWE.

4.2.28. SRAMC - Supplemental DRAM Control Register

Offset Address: C2h
Default Value: 0Ch
Access: Read/Write

BIT	FUNCTION
7	Delay nBRDY in Cache Miss and Non-dirty cycle: When set to "1", the nBRDY is asserted one CPU clock later than normal for the leadoff cycle.
6	Single Read Pipeline Enable: When set to "1" together with bit 3 of register CC being set to "0" enables the Single Read Pipeline logic.
5	Single Write Pipeline Enable: When set to "1" together with bit 3 of register CC being set to "0" enables the Single Write Pipeline logic.
4	DRAM Burst Read Miss Pipeline Enable: When set to "1" together with bit 3 of register CC being set to "0" enables the DRAM Burst Read Pipeline logic.
3	Enable nNA Assertion for INTA Cycle 0: Disable (default) 1: Enable
2	Enable nNA Assertion for Write Cycle When Post Write Buffer Is Full 0: Disable (default) 1: Enable
1	CPU-to-Memory and PCI peer-to-peer concurrence 0: Disable (default) 1: Enable.
0	Single 64 bit Memory Write Pipeline Enable: (Internal Use) 1: Enable 0: Disable

4.2.29. SPCIBC - Supplemental PCI Buffer Control Register

Offset Address: C3h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
7	PBSRAM Power Down Mode Enable: This bit is used to enable the PBSRAM power down mode during nSTPCLK acknowledge period or nSUSSTAT assertion period. 0: Disable 1: Enable
6-5	Pre-fetched Cache Line Count. This field determines the number of cache lines the SLC90E42 will pre-fetch during PCI master burst read transaction before turning the host bus to the CPU. For instance, if four cache lines are selected, the CPU will regain the host bus after four cache lines of memory data have been fetched and filled into PCI pre-fetch buffer. 00: 4 cache lines 01: 5 cache lines 10: 6 cache lines 11: 7 cache lines
4	Disable DRAM Refresh during PCI master cycles: When set to a 0, the SLC90E42 continues the DRAM refresh operation during PCI master cycles. Otherwise, DRAM refresh is disabled during the PCI master cycles.
3	Global CPU-to-PCI Memory Cycles Post Write Enable: When set to a 1 enables the SLC90E42's post write logic for the following memory space: page A & B, and memory space where A31, A30, A29 or A28 are equal to "1" (PCI memory space) except the 4GB BIOS memory space.
2-0	Minimum CPU Allocation: This field selects a minimum number of HCLKs allocated to CPU during PCI bus master burst read transaction. The SLC90E42 grants the host bus from the CPU to a burst reading PCI master when (a) the pre-fetch buffer contains less than 8 DW of data. (b) the CPU owns the host bus more than the Minimum CPU Clock Count. Both conditions must be met to trigger the SLC90E42 to switch the ownership of host bus. 000: 0 hclk 001: 1 hclk 010: 2 hclks 011: 3 hclks 100: 4 hclks 101: 5 hclks 110: 6 hclks 111: 7 hclks

4.2.30. SPCICH - Supplemental PCI Control Register High

Offset Address: C4h
Default Value: 20h
Access: Read/Write

BIT	FUNCTION
7	Fast CPU-to-PCI IO Read Enable: When set to "1", the SMC90E42 will reduce one HCLK for the CPU IO read cycle.
6	Reserved.
5	PCI Abort Retry Enable: When set to a "1", the SMC90E42 will retry PCI target abort cycle when it is the cycle initiator. This bit is default to be "1".
4	PCI Address Stepping Enable: When set to a "1", the SMC90E42 will setup PCI cycle address one PCICLK earlier before asserting nFRAME to improve the address setup time.
3-2	Disconnect Retry Timer Value: The SMC90E42 will retry the Disconnect Retry cycle following the setup of this field. 00: Retry immediately after disconnected. 01: Retry after 16 PCI clocks. 10: Retry after 32 PCI clocks. 11: Retry after 64 PCI clocks.
1-0	Reserved.

4.2.31. SPCICL - Supplemental PCI Control Register Low

Offset Address: C5h
Default Value: 00h
Access: Read/Write

BIT	FUNCTION
7	PCI Bus Park Enable: When set to "1", the SLC90E42 will park on the PCI bus during idle states.
6-5	PCI Master Burst Transfer Disconnect Timer Value: This timer decides when to assert PCI Disconnect cycle during a PCI master burst transaction when a pending PCI master or CPU-to-PCI request presents. The timer starts to count once a PCI bus master is granted the PCI bus. Since then, any pending PCI bus request has to wait until the timer is expired, the SLC90E42 will then wait until the memory address of the master burst transaction is aligned to a cache line address then asserts a Disconnect cycle. This timer is used to ensure that every PCI bus master has been granted with sufficient bandwidth for data transfer while not imposing too much latency on the other requesters. 00: 256 PCI cycles 01: 64 PCI cycles 10: 32 PCI cycles 11: 16 PCI cycles
4-3	Reserved.
2	CPU-to-PCI Burst Memory Write Enable: When set to "1", the SLC90E42 will perform burst memory write to the PCI target. This is mainly for Video Frame Buffer Write to improve graphics bandwidth.
1	Reserved
0	Early nIRDY Assertion Enable: When set to a "0", nIDRY is asserted in the second PCI clock after the assertion of nFRAME. When it is a "1", nIRDY assertion is in the PCI cycle following the assertion of nFRAME.

5. THE SLC90E42 FUNCTIONAL DESCRIPTION

5.1. The CPU Interface Logic

5.1.1. The CPU Type

The SLC90E42 is designed to support the Intel Pentium/Pentium MMX, the Cyrix 6x86/6x86MX and the AMD K5/K6 processors.

5.1.2. CPU L1 Cache Update Policy

The SLC90E42 supports both write back and write through cache update policies for the CPU internal (L1) cache. When write-back scheme is selected, the SLC90E42 asserts nEADS signal to the processor whenever a PCI or an ISA master reads from or writes to the system memory. nEADS is used to snoop the L1 cache to keep data integrity among the L1 cache, the L2 cache and the system memory. When write-through scheme is selected, the SLC90E42 asserts nEADS signal to the processor only in write cycles when a PCI or an ISA master generates the write cycles to the system memory.

The SLC90E42 implements a snoop filter which activates nEADS signal only when a cache line is first accessed in a master transaction period. The snoop filter avoids the assertions of nEADS signal for the subsequent accesses to the same cache line to reduce overhead introduced by the snooping operations.

5.1.3. Pipelined Addressing Mode

The SLC90E42 supports pipelined addressing mode by asserting nNA (next address) signal to the processor before the completion of present CPU cycle. The pipelined addressing mode reduces the access time of single and leadoff memory cycles and achieves better memory bandwidth.

5.1.4. Concurrence

The SLC90E42 allows the CPU to access memory (cache or DRAM) while a PCI master is transferring data to/from system memory or another PCI device. The SLC90E42 asserts the AHOLD signal to the CPU when the PCI master is first granted the PCI bus, or when the PCI data buffer is waiting to be flushed to the system memory (PCI Master Write) or when the buffers need to be filled with data from system memory (PCI Master Read). The SLC90E42 will deassert the AHOLD signal while PCI master is fetching data from or writing data to the internal PCI data buffers.

5.1.5. The Reset Logics

The SLC90E42 is asynchronously reset by the input signal: nRST. When it is asserted, the PCI signals will go tri-state compliant to the PCI 2.0 and 2.1 specifications.

5.1.6. The Clock Logics

The SLC90E42 takes three clock inputs. The HCLKIN receives a buffered host clock. This clock is used by the SLC90E42 internal logic that resides in the Host clock domain. The PCLKIN received a buffered divide-by-2 host clock for synchronous PCI mode or 33MHz clock for asynchronous PCI mode. This clock is used by the SLC90E42 logic that resides in the PCI clock domain.

In addition, the SLC90E42 also receives a suspend clock (SUSCLK). The SUSCLK is a 32KHz clock for DRAM refresh circuitry and clocking events in suspend state. The DRAM refresh is performed based on this clock in either suspend or non-suspend states.

5.2. External (L2) Cache Controller

The SLC90E42 incorporates a 64-bit direct mapped L2 cache controller with an on-chip tag comparator and a 16 Kbits of SRAM for cache validation. Each cache line is 32-byte wide, the same as Pentium processors. The cache controller supports write-back cache update policy, double (cache size: 512KB) or single (cache size: 256/512KB) bank of pipelined synchronous SRAMs for superb system performance.

In the 256KB configuration, the L2 cache contains 8K lines, while the 512KB configuration contains 16K lines. Cacheability of the entire memory space in L1 cache is supported, while only the lower 64MB of main memory is cacheable in the L2 cache. The section "Cache Memory Configurations and Requirements" lists the cache configurations that are supported by the cache controller, and the requirements of the cache SRAMs.

The on-chip tag comparator is implemented to improve system performance and reduce board component count. The comparator is used to determine if the current memory cycle hits the L2 cache or not. A cache hit occurs if the contents of the memory location which is being accessed is stored in the cache. If the cache hit does not occur for the current memory cycle, it is a cache miss cycle, and the cycle is forwarded to system memory controller. The contents of the cache entry may be updated by the access.

In the 256KB L2 cache configuration, the 16 Kbits on-chip SRAM is used to store "ALTER" and "VALID" status of the 8K cache lines. It is used to store "ALTER" information of the cache lines in the 512KB configuration. The "VALID" bits of the cache lines are stored in the external TAG RAM with the Tag Addresses in the 512KB configuration. In this case, the tag address becomes seven bits instead of eight bits.

5.2.1. Cache Memory Configuration

The cacheable memory size can be calculated from the cache size, the tag size, and the tag width (bits), and vice versa.

tag size = cacheable size/line size
for the SLC90E42, the line size = 32 bytes

tag width = log2 (cacheable size/cache memory size)

For example, a board with 256Kbytes of cache and intend to have 64M bytes of cacheable memory, the tag size is equal to:

tag size = 256K/32 = 8K

The tag width is 8-bit as shown in the following calculation:

tag width = log2 (64MB/256KB) = 8

The table on the following page lists the cache memory sizes, the corresponding tag RAM sizes, the address bits stored in the tag RAM, the cache memory configurations, the cache RAM address bits, and the cacheable system memory sizes that are supported by the SLC90E42.

CACHE SIZE	TAG SIZE/ ADDRESS BITS STORED IN TAG RAM	PBSRAM SIZE / ADDRESS BITS	CACHEABILITY
256 KBytes	8K x 8 bits A18 - A25	(32Kx32 bits) x 2 A3 - A17	64 MBytes
512 KBytes	16K x 8 bits (includes one valid bit) A19 - A25	(32Kx32 bits) x 4 or (64Kx32 bits) x 2 A3 - A17 (A18 is used as bank select) or A3 - A18	64 MBytes

The following table shows the SRAM access time requirements for different host clock frequencies.

HOST CLOCK FREQUENCY (MHz)	PIPELINED BURST SRAM CLOCK-TO-OUTPUT ACCESS TIME	TAG RAM CYCLE TIME
60	10	15ns
66	9	15ns

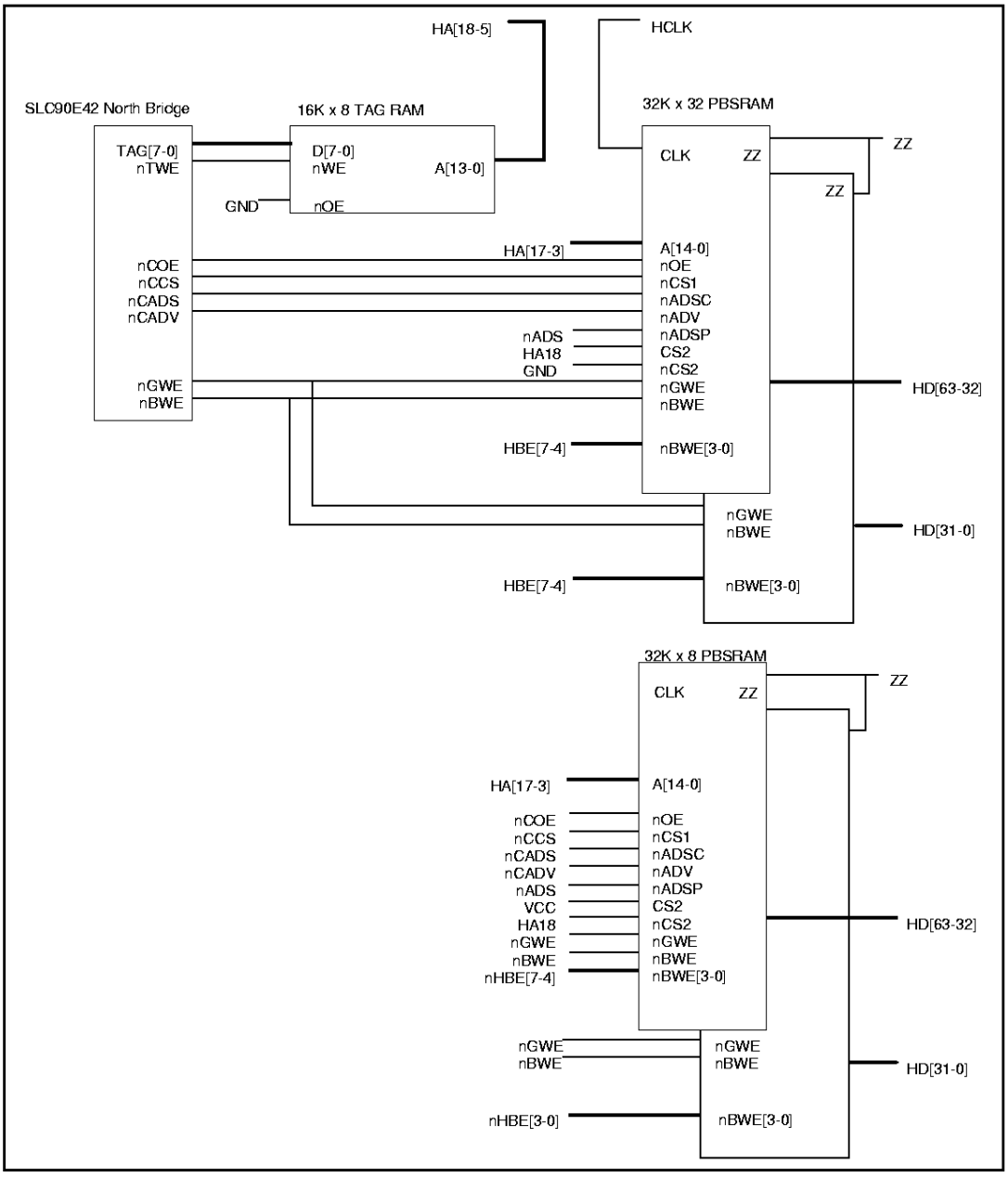


FIGURE 4 - 512KB L2 CACHE CONFIGURATION (2-BANK)

Figure 5 shows the connections between SLC90E42, Tag RAM and data RAMs in a 256KBytes cache configuration.

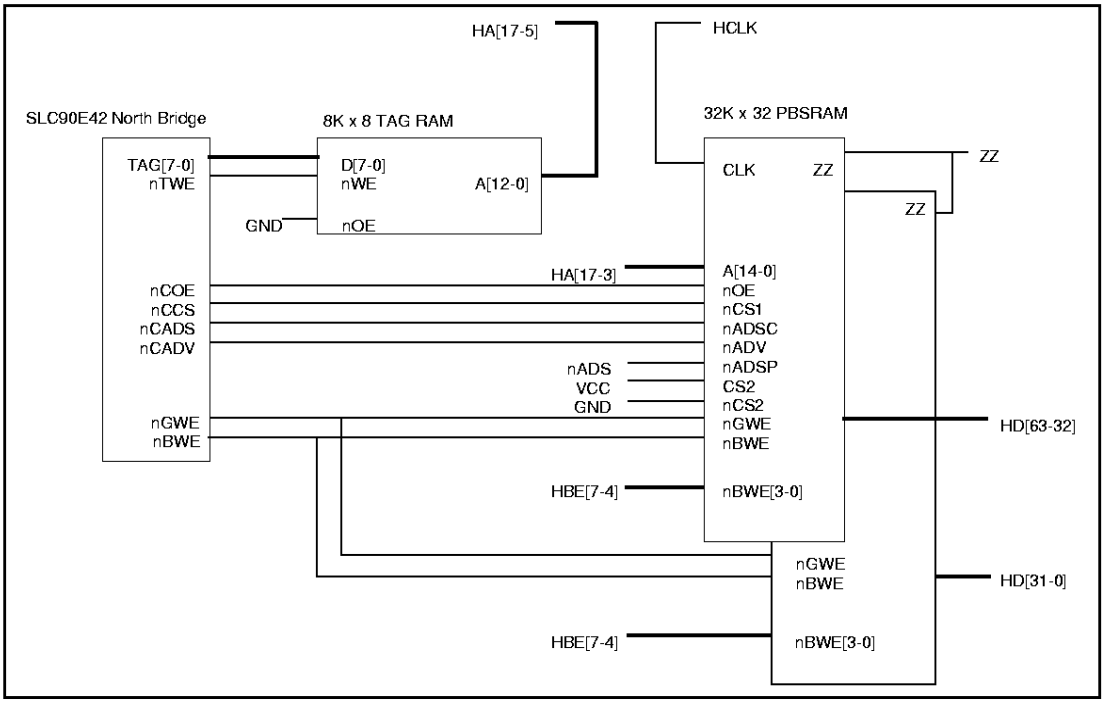


FIGURE 5 - 256KB L2 CACHE CONFIGURATION

5.2.2. Cache Data Latency

The following table shows the latencies for various cache memory data transfer cycles.

CACHE MEMORY CYCLE	HCLK COUNT
Burst Read	3-1-1-1
Burst Write (write back)	3-1-1-1
Single Read	3
Single Write	3
Pipelined Back-to-Back Burst Reads (single bank)	3-1-1-1-1-1-1-1

5.2.3. Cache Initialization

External cache can be easily initialized by enabling L2 cache, disabling L1 cache, and turning the "L2 Cache Force Miss or Invalidate" feature on. Each processor read memory cycle will invalidate the corresponding cache entry in the L2 cache memory.

5.2.4. Cache Flushing

External cache can be easily flushed to the main memory by enabling L2 & L1 cache, and turning the "L2 Cache Force Miss or Invalidate" feature on. Each processor read memory cycle will flush data of the corresponding cache entry of the L2 cache memory to the main memory.

5.2.5. Cache Write Hit Cycles

When a cache write hit occurs, the cache controller does not pass the cycle on to system memory controller. Instead, it updates the cache memory entry and marks the entry as altered (modified) by setting ALTER bit of the cache entry to a 1.

5.2.6. Cache Write Miss Cycles

When the cache controller determines that the current cycle is a cache write miss cycle (the tag comparator does not show "address match" to the corresponding cache entry), it bypasses the cycle to system memory controller without updating the cache memory, the tag memory or the ALTER bit. An access to the same memory location at later time will still be a miss cycle (no write allocation is performed).

A post write buffer is used to complete the processor write cycle at the same latency as Cache Write Hit cycle (3 for single write, 3-1-1-1 for burst write). The cycle is completed and the processor is free for other operation after the data and the associated memory address are written to the post write buffer. The data in the post write buffer can then be written to system memory at later time to update system memory.

5.2.7. Cache Read Miss and not Alter Cycles

In a cache read miss cycle, the cycle is forwarded to system memory controller. At the same time when the data is transferred to the processor, it is also stored in the L2 cache so that, the subsequent access to the same memory location can be performed on the faster cache instead of the slower system memory. In this case, the corresponding tag entry is updated, and the ALTER bit stays cleared.

5.2.8. Cache Read Miss and Altered Cycles

In this case, the cache line needs to be written back to the system memory before its contents being overwritten with the new data. The copy back operation is used to maintain the data integrity between the cache memory and the system memory. The SLC90E42 cache controller uses a scheme named "concurrent write back" to perform the "line fill" and "copy back" operations simultaneously.

The operation of "concurrent write back" can be described as follows:

1) The cycle is determined to be a read miss cycle and it is forwarded to the DRAM controller to read the data from the DRAMs.
2) The entry to be replaced is determined ALTERed (modified). The content of the entry is then written to the SLC90E42 Write Buffer. At the same time, the data read from system memory is stored in the SLC90E42 Read Buffer.
3) After the cache write back (to the Write Buffer) operation is completed, the Read Buffer data is then transferred to the processor and, at the same time, is used to update the cache entry. After the read process is completed (nBRDY de-asserted), the processor is free to continue with the next operation.
4) The cache controller will update the cache tag entry and clear the ALTER bit of the entry to complete the cache update process.
5) The DRAM Controller, in the meantime, is invoked to flush the contents of the Write Buffer to the corresponding system memory location to complete the whole operation.

5.2.9. Cache Read Hit Cycles

In this case, the processor retrieves data from the L2 cache entry directly and there is no system memory access cycle issued. No entry in the L2 cache is updated either.

5.2.10. The PCI Masters, DMA or ISA Master Cycles

Other than the processor, the DMA controllers, the PCI masters and the ISA master devices may access system memory. All these cycles are considered as the PCI master cycles since the ISA master cycles and the DMA cycles are transformed into PCI master cycles by the SLC90E46 south bridge.

During the PCI master cycles, the L2 cache memory is treated as a write through cache with the following behavior:

For a write hit cycle, the data is written to the L2 cache entry as well as the entry in system memory; for a write miss cycle, the data is written to system memory only.

For a read hit cycle, the data is read from the L2 cache; for a read miss cycle, the data is read from system memory but the cache is not updated. The line is still not a valid line in the L2 cache and the next access to the same line will cause a miss to the L2 cache again.

If the processor is configured in write through mode for the L1 cache, nEADS is generated to snoop the CPU L1 cache in a PCI master writes memory cycle. If the snoop cycle hits a CPU L1 cache entry, the cache entry is invalidated.

If the processor is configured in write back mode, nEADS is generated to the processor in both PCI master writes memory cycles and PCI master reads memory cycles. When the write snooping cycle hits a CPU L1 cache line and the line is modified, nHITM is asserted and the line is written back to system memory before it is invalidated. If the line is clean (unmodified), the line is invalidated immediately.

When the read snooping cycle hits a CPU L1 cache line and the line is modified, the line is written back to system memory before system memory is read. If the line is clean (unmodified), the data in system memory is read immediately.

5.2.11. Burst Mode Control

The processor asserts nCACHE to indicate a cacheable memory read cycle or a burst memory write-back cycle (write back mode only).

Burst read occurs when the nCACHE signal is valid for the memory read cycle, and nKEN signal is detected active for the first nBRDY or nNA, whichever comes first. The cycle is then converted to a burst read cycle. In a burst read cycle, nADS is asserted once, and the bus definition signals and the address lines stay valid from the time when nADS is asserted until two CPU clocks after the first nBRDY or nNA is detected active. nBRDY is asserted four times, each to indicate the completion of 64-bit data, so, in total, in a burst read cycle, 32 bytes of data is read by the processor to fill the whole line of the processor's internal cache.

Burst write occurs in two occasions when the processor is in write back mode. The first occasion happens when the snoop cycle hits the modified cache line of the processor's internal cache. The cache line is then burst written to the external system memory (or the L2 cache if the line hits the L2 cache), if the system supports burst write cycles. The second occasion occurs when the processor is doing cache line replacement to a line that has been modified. The line is burst written back to the external system memory to keep the data coherency.

During the burst write-back cycle, nKEN is not monitored. nCACHE is asserted in a memory write cycle to indicate a burst write-back cycle and it is required that nBRDY be asserted four clocks to complete the burst write-back cycle.

5.2.12. The DRAM Interface Overview

The SLC90E42 integrates a DRAM controller that supports a 64 bit memory array from 4Mbytes to 256 Mbytes of main memory. The SLC90E42 supports page mode (FPM), Extended Data Out (EDO) and Synchronous DRAM (SDRAM) memories using 32 bit wide SIMM modules, 64 bit wide unbuffered DIMM modules and 64 bit wide unbuffered SO-DIMM modules. The SLC90E42 does not support

PARITY, and for loading reasons, parity modules should not be used. The SLC90E42 supports memory type mixed and matched on a per-row basis.

The SLC90E42 provides twelve multiplexed address lines, MA[11-0], to support 4Mbit, 16Mbit, and 64Mbit FPM and EDO memory both symmetrical and asymmetrical addressing. The SLC90E42 drives six nRAS lines to support up to six rows of DRAM. The SLC90E42 is designed to target 60ns (also supports 50ns and 70ns) DRAMs, both single and double-sided DRAM modules. The SLC90E42 provides CBR refresh and extended CBR refresh in the normal mode and self refresh or CBR during suspend mode.

The SLC90E42 also supports SDRAMs. The fourteen multiplexed address lines, MA[13-0], allow the SLC90E42 to support 16Mbit and 64Mbit SDRAM devices. The SLC90E42 has six nCS lines to support up to six rows of 16Mbit SDRAM, and 5 nCS to support five rows of 64Mbit SDRAM. Eight DQM lines, which are muxed with nCAS[7-0], allow byte control over the array during the write operation. Two copies of nSRAS and nSCAS lines are provided for encoded SDRAM commands. The SLC90E42 is designed to target 60 and 66 MHz SDRAM and support single and double sided SDRAM modules.

The DRAM interface is configured by the DRAM Control Mode Register (DRAMC), DRAM Extended Control Register (DRAMEC), DRAM Timing Register (DRAMT), SDRAM Control Register (SDRAMC), six DRAM Row Boundary Registers (DRB), and the DRAM Row Type (DRT) registers.

Seven High Memory Mapping (HMM) registers are used to specify the cacheability, PCI enable, and read/write status of the memory space between 640 Kbytes and 1 Mbytes. Each HMM register defines a specific address area enabling the system to selectively mark specific memory ranges as cacheable, read-only, write-only, read/write, or disabled. When a memory range is disabled, all CPU accesses are forwarded to PCI bus.

The SLC90E42 also supports one of two memory holes, either from 512K to 640K or from 14/15M to 16M in memory space. Accesses to the memory hole are forwarded to PCI. The memory hole can be enabled/disabled through the DRAM Control Register. All other memory from 1M to 256 MB is read/write L1 cacheable, and is L2 cacheable up to 64 MB.

The SLC90E42 also supports an optional Extended SMRAM DRAM memory space in the 256 MB to 512 MB address range. It consists of the 640 K - 1 MB DRAM area with address aliased at the 256 MB memory segment, or an optional 128K/256K/512K/1M DRAM area chopped from the Top-of-DRAM memory with address aliased above 256MB in a similar manner.

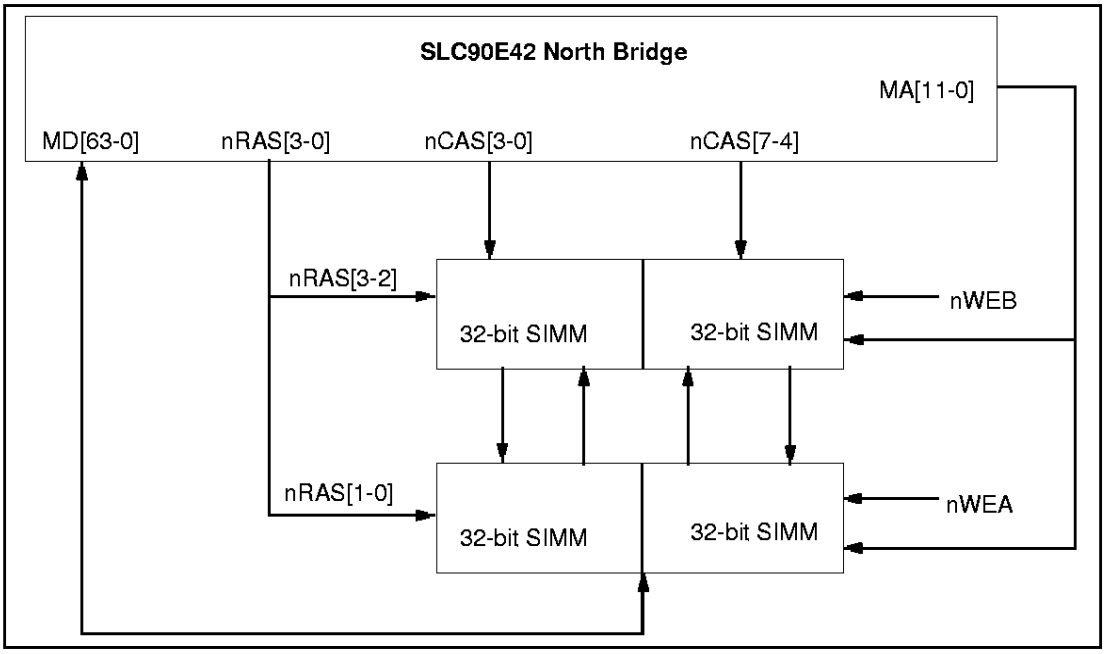


FIGURE 6 - EDO/FPM CONFIGURATION USING x32 SIMM MODULES

5.2.13. DRAM Organization

The SLC90E42 supports six rows of memory. For maximum memory flexibility and performance, it is recommended that a DRAM configuration of four (or five) rows be used. This allows 64Mbit DRAM devices to be used as well as the mixing of SDRAM and EDO/FPM. When DRAM types are mixed a given row must contain only one type of DRAM.

It is not recommended to mix SDRAM with 5V EDO/FPM SIMMs, unless the SDRAM and EDO/FPM DRAM are properly isolated (e.g. isolate the memory data lines with Q switches). Mixing 5V and 3V memory is not recommended for reliability reasons. Not all SDRAM devices are 5V tolerant.

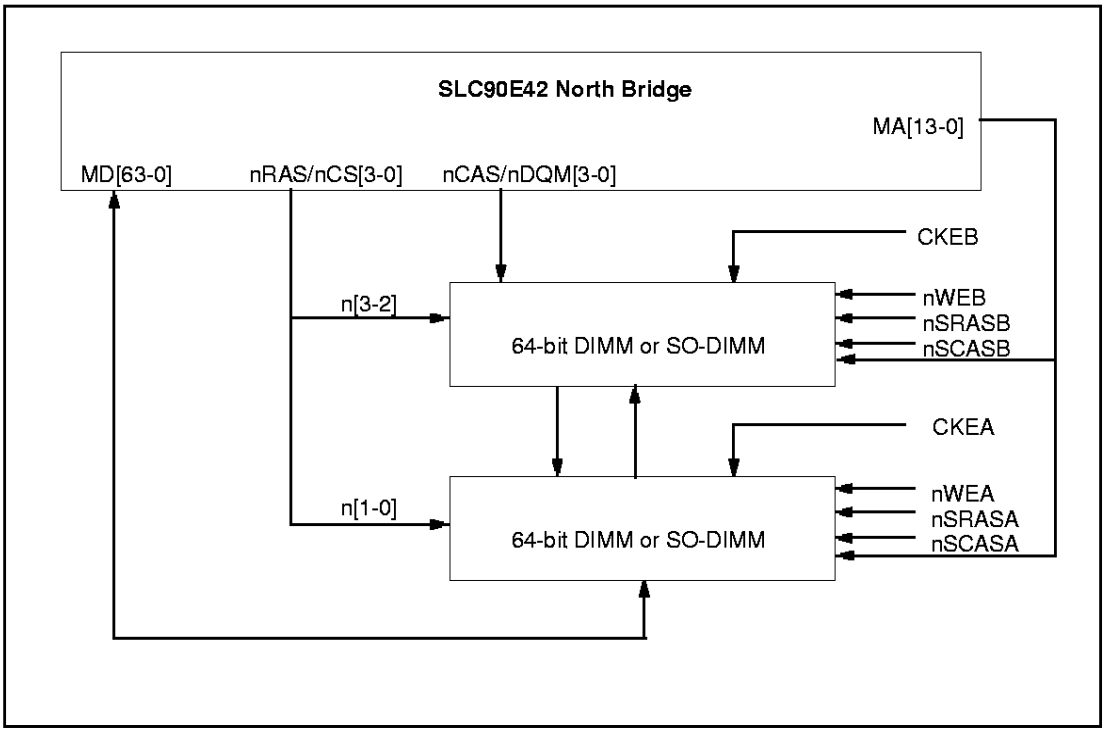


FIGURE 7 - FOUR ROW EDO/FPM/SDRAM CONFIGURATION USING x64 DIMM MODULES (OR x64 SO-DIMM)

5.2.14. DRAM Populating Rules

Rules for populating SIMM (or x32 SO-DIMM) modules:

- SIMM sockets can be populated in any order: for instance, memory for nRAS0 does not have to be populated before memory for nRAS[2-1] is used.
- SIMM socket pairs (of each row) need to be populated with the same densities. However, different SIMM socket pairs may use different density of SIMM modules.
- EDOs and standard page mode can both be used, however only one type should be used per SIMM socket pair. If different memory type is used for different rows, each row will be optimized for that type of memory.
- The DRAM Timing Register which provides the DRAM speed grade control for the entire memory array must be programmed to use the timings of the slowest DRAM installed.

Rules for Populating DIMM or SO-DIMM modules:

- DIMM or SO-DIMM can be populated in any order.

5.2.15. DRAM Configuration Requirements

5.2.16. General Configuration Requirements:

- If 64Mbit SDRAM devices are supported (bit 1 in the SDRAMC register = "1"), then the configuration is restricted to a maximum of five rows of DRAM. The nRAS5/nCS5 signal becomes MA13, and nRAS4/nCS4 becomes MA12/BA1. The NC/nCS4 signal becomes nCS4.
- In a FPM/EDO only configuration, there are no restrictions on using 64Mbit devices (i.e. all six rows can support 64Mbit DRAM devices).
- If SDRAM and EDO/FPM are mixed in a system, then the configuration is limited to a maximum of four rows.
- Due to loading, using SDRAM with x4 configuration is not recommended.
- Buffering of SDRAM Rows is not supported.
- The total memory supported is 256M, even though it is possible to populate the sixth row with more than 256M. This limit must be ensured by the system BIOS.

5.2.17. EDO/FPM Only Configuration Requirements:

- Maximum rows supported without buffer - Four rows of x4 DRAM devices + one row of x8 DRAM devices.
- If more than four rows of x4 DRAM devices + one row of x8 DRAM devices is supported, it is recommended that all six rows be buffered.

5.2.18. SDRAM Only Configuration Requirements:

- Maximum rows supported - Five rows of x8 devices

5.2.19. SDRAM/EDO/FPM Mixing Configuration Requirements:

- SDRAM can be mixed with EDO/FPM on a row by row basis.
- Maximum rows supported: Four rows total - Two rows of x4 EDO/FPM devices + two rows of x8 SDRAM.

Table 10 gives a summary of the memory configurations supported by the SLC90E42. Minimum values listed are obtained with single-sided SIMMs or DIMMs. Maximum values are obtained with double-sided SIMMs or DIMMs. The minimum values used are also the smallest upgradeable memory size.

Table 10 - Minimum (Upgradeable) and Maximum Memory Size for Each Configuration

DRAM TECH.	DRAM DENS-ITY	DRAM WIDTH	DRAM SIMM		DRAM ADDRESS-ING	ADDRESS SIZE		DRAM SIZE	
			SS (X32)	DS (X32)		ROW	COL.	MIN. (1 ROW)	MAX. (6 ROWS)
EDO/ FPM									
4M	512K	x8	512K	1M	Asymmetric	10	9	4MB	24MB
	1M	x4	1M	2M	Symmetric	10	10	8MB	48MB
16M	1M	x16	1M	2M	Symmetric	10	10	8MB	48MB
	1M	x16	1M	2M	Asymmetric	12	8	8MB	48MB
	2M	x8	2M	4M	Asymmetric	11	10	16MB	96MB
	4M	x4	4M	8M	Symmetric	11	11	32MB	192MB
	4M	x4	4M	8M	Asymmetric	12	10	32MB	192MB
64M	2M	x32	2M	4M	Asymmetric	12	9	16MB	96MB
	4M	x16	4M	8M	Symmetric	11	11	32MB	192MB
	4M	x16	4M	8M	Asymmetric	12	10	32MB	192MB
	8M	x8	8M	16M	Asymmetric	12	11	64MB	256MB
	16M	x4	16M	32M	Symmetric	12	12	128MB	256MB
SDRAM			**DIMM** SS (x64)	**DIMM** DS (x64)					
16M	1M	x16	1M	2M	Asymmetric	12	8	8MB	48MB
	2M	x8	2M	4M	Asymmetric	12	9	16MB	96MB
	4M	x4	4M	8M	Asymmetric	12	10	32MB	192MB
64M	2M	x32	2M	4M	Asymmetric	12	9	16MB	80MB
	2M	x32	2M	4M	Asymmetric	13	8	16MB	80MB
	4M	x16	4M	8M	Asymmetric	14	8	32MB	160MB
	8M	x8	8M	16M	Asymmetric	14	9	64MB	256MB
	16M	x4	16M	32M	Asymmetric	14	10	128MB	256MB

Accesses to memory space above Top-of-Memory (<256MB), video buffer, or the memory hole are forwarded to the PCI bus, and these regions are not cacheable. Below 1MB, several memory segments are optionally cacheable. The DRAM spaces occupied by the video buffer (except for SMM usage) or the memory holes are not re-mapped and are therefore lost.

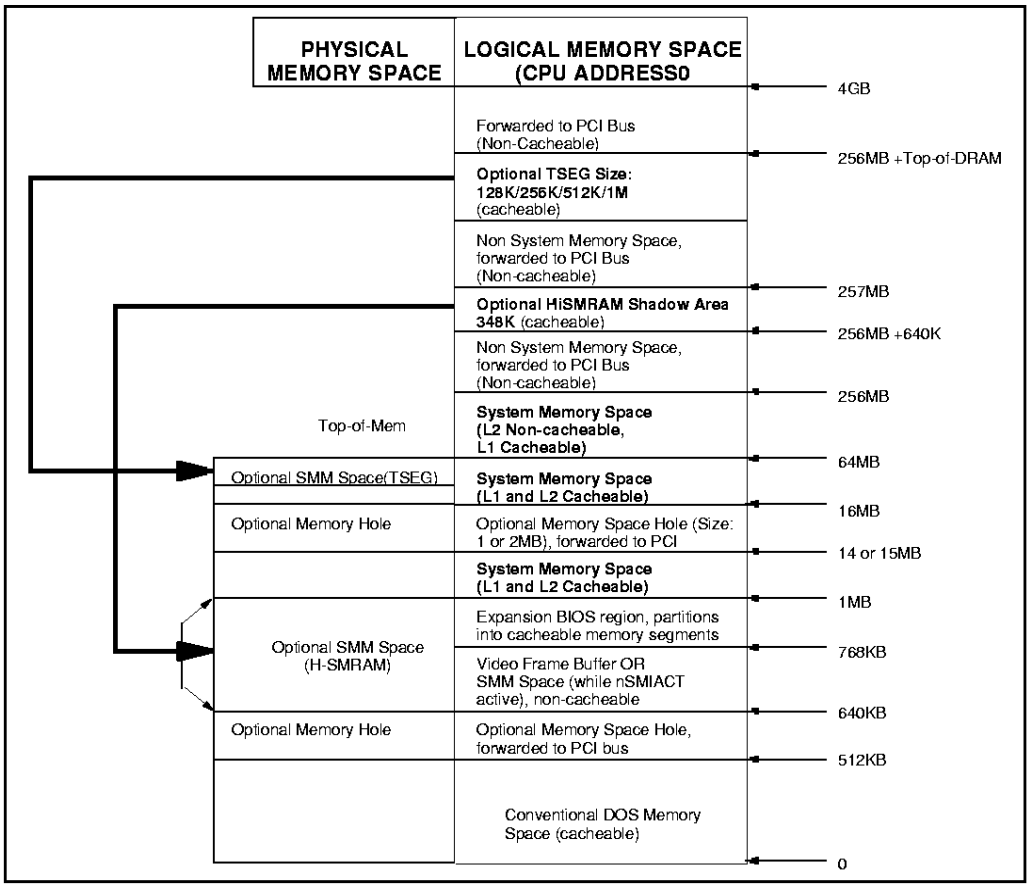


FIGURE 8 - SLC90E42 MEMORY SPACE ORGANIZATION

5.2.20. DRAM Address Translation

The multiplexed DRAM address is provided through MA[11-0] signals (or MA[13-0] for 64Mbit SDRAM support). The MA signals are derived from the host or PCI address bus as defined by the table below. The MA signals are translated from the address lines A[26-3] for all memory addresses.

MA Mapping for 4MByte Memory (EDO/FPM) Row

			MA 11	MA 10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Row			A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Col			A11	A11	A11	A11	A10	A9	A8	A7	A6	A5	A4	A3

MA Mapping for 8MB Memory (EDO/FPM) Row

			MA 11	MA 10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Row			A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Col			A11	A11	A11	A22	A10	A9	A8	A7	A6	A5	A4	A3

MA Mapping for 16MB Memory (EDO/FPM) Row

			MA 11	MA 10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Row			A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Col			A11	A11	A11	A23	A10	A9	A8	A7	A6	A5	A4	A3

MA Mapping for 32MB Memory (EDO/FPM) Row

			MA 11	MA 10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Row			A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Col			A11	A11	A24	A23	A10	A9	A8	A7	A6	A5	A4	A3

MA Mapping for 64MB Memory (EDO/FPM) Row

			MA 11	MA 10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Row			A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Col			A11	A25	A24	A23	A10	A9	A8	A7	A6	A5	A4	A3

MA Mapping for 128MB Memory (EDO/FPM) Row

			MA 11	MA 10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Row			A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Col			A26	A25	A24	A23	A10	A9	A8	A7	A6	A5	A4	A3

MA Mapping for 8MB Memory (16Mb SDRAM) Row

			MA 11 BA0	MA 10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Row			A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Col			A11	"V"	A11	A11	A10	A9	A8	A7	A6	A5	A4	A3

MA Mapping for 16MB Memory (SDRAM) Row

	MA 13	MA 12 BA1	MA 11 BA0	MA 10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Row	*A24*	*A23*	A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Col		*A23*	A11	"V"	A11	A23	A10	A9	A8	A7	A6	A5	A4	A3

MA Mapping for 32MB Memory (SDRAM) Row

	MA 13	MA 12 BA1	MA 11 BA0	MA 10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Row	*A24*	*A23*	A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Col		*A23*	A11	"V"	A24	A23	A10	A9	A8	A7	A6	A5	A4	A3

MA Mapping for 64MB Memory (64Mb SDRAM) Row

	MA 13	MA 12 BA1	MA 11 BA0	MA 10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Row	*A24*	*A23*	A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Col		*A23*	A11	"V"	A11	A25	A10	A9	A8	A7	A6	A5	A4	A3

MA Mapping for 128MB Memory (64Mb SDRAM) Row

	MA 13	MA 12 BA1	MA 11 BA0	MA 10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
Row	*A24*	*A23*	A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Col		*A23*	A11	"V"	A26	A25	A10	A9	A8	A7	A6	A5	A4	A3

*Shaded columns are defined only when 64Mb SDRAM is enabled.

*V is Valid level (either 1 or 0) used for SDRAMs. It is "1" during the initialization sequence. It is "0" during normal mode of operation.

5.2.21. DRAM Types

The SLC90E42 supports three types of DRAM devices: the standard fast page mode (FPM) DRAM, Extended Data Out (EDO) DRAM, and Synchronous DRAM.

EDO DRAM is designed to improve the DRAM read performance. It holds the memory data valid until the next nCAS falling edge. Compared to FPM DRAM which tri-states the memory data when nCAS negates to precharge, with EDO, the nCAS precharge overlaps the memory data valid time, this allows nCAS to negate earlier while still satisfying the memory data valid window time.

5.2.22. SDRAM Mode

SDRAM implements a fully synchronous interface as compared to a conventional DRAM whose timing delays are related to the rising and falling edges of the nRAS, nCAS and nWE input signals. The SLC90E42 supports all of the features and timings of the SDRAM PC Specification. The following table shows three grade parts of SDRAM which can be used with the SLC90E42 North Bridge chip.

SPEED GRADE	CAS LATENCY (CL)	RAS TO CAS (TRCD)	SYSTEM FREQUENCY
66.67 MHz	3	3	60/66 MHz
66.67 MHz	3	2	60/66 MHz
66.67 MHz	2	2	60/66 MHz

5.2.23. SDRAM Commands Reference

The SLC90E42 supports the following SDRAM commands:

Mode Register Set
Activate Bank
Read Bank
Write Bank
Precharge All Banks
Deselect Device
No Operation
Auto Refresh CBR
Data Write/Output Enable
Data Mask/Output Disable
Self Refresh Entry
Self-Refresh Exit

5.2.24. Mode Register Set (MRS) Command

The MRS command supported by the SLC90E42 is as follows:

A11-A7	A[6-4]	A3	A[2-0]
00000	CL	WT	BL

Where:

CL = 010, CAS latency is set to two
CL = 011, CAS latency is set to three
All other CL values are don't care

WT must be "1" to select Interleave mode

BL = 010, Burst Length is set to four
All other BL values are don't care

5.2.25. DRAM Cycle Timing

The DRAM performance is controlled by the DRAM timing register, pipelined CPU cycles, and by the type of DRAM used. The following tables depict the optimum DRAM timings for both EDO/FPM DRAM and SDRAM.

For memory read cycles, clock counts are measured from the nADS assertion to the nBRDY assertion.

For memory write cycles, the measurement is broken up into two parts. The first part consists of the speed of posting data into the DRAM post write buffer. This is measured from the nADS assertion to the nBRDY assertion. The second part is to retire data from the posted write buffer to the DRAM. The leadoff for retiring is measured from the first clock after the nBRDY assertion to the nCAS assertion.

Table 11 shows the performance summary for 60ns EDO/FPM DRAM. It is assumed that each DRAM row is populated with a maximum of 16 (x 4) DRAM devices except in the case of five rows memory array. In that case, the fifth row is assumed to be populated with a maximum of 8 (x 8) DRAM devices while the first four rows are assumed to be populated with x 4 DRAM devices, which comes out totally 72 DRAM devices used in a 5-row memory array.

Table 11 - EDO/FPM DRAM Cycle Timing

PROCESSOR CYCLE		60/66MHz FOUR ROWS	60/66MHz FIVE ROWS	60/66MHz SIX ROWS BUFFERED
Burst Read Page Hit	EDO: FPM:	5-2-2-2 5-3-3-3	6-3-3-3 6-4-4-4	6-3-3-3 6-4-4-4
Read Row Miss[1] (nRAS high)	EDO: FPM:	9-2-2-2 9-3-3-3	9-3-3-3 9-4-4-4	10-3-3-3 9-4-4-4
Read Page Miss	EDO: FPM:	12-2-2-2 12-3-3-3	12-3-3-3 12-4-4-4	13-3-3-3 12-4-4-4
Back-to-Back Burst Reads Page Hit	EDO: FPM:	5-2-2-2-3-2-2-2 5-3-3-3-3-3-3-3	6-3-3-3-3-3-3-3 6-4-4-4-4-4-4-4	6-3-3-3-3-3-3-3 6-4-4-4-4-4-4-4
Write Page Hit (EDO/FPM) [2,3,4]		3	3	3
Write Row Miss (EDO/FPM) [2,3,4]		6	6	7
Write Page Miss (EDO/FPM) [2,3,4]		9	9	10
Posted Write (EDO/FPM) [3,4]		3-1-1-1	3-1-1-1	3-1-1-1
Write Retire Rate from Posted Write Buffer (EDO/FPM)		-3-3-3	-3-3-3	-3-3-3
Single Writes (EDO/FPM)		3	3	3
DRAM Configuration Register Setup				
Reg 56 Bit 4 / Speculative leadoff		0	0	0
Reg 56 Bit 5 / Fast EDO leadoff		0	0	0
Reg 56 Bit 6 / Refresh nRAS Assertion		0	0	0
Reg 58 Bit [6-5] / Read Burst Timing		10b	01b	01b
Reg 58 Bit [4-3] / Write Burst Timing		10b	10b	10b
Reg 58 Bit [1-0] / Burst Leadoff Delay		01b	01b	00b

Notes:

1. The Row Miss cycles assumes that the new page is closed from the prior cycle.
2. Assumes DRAM Write Buffer is available.
3. DRAM Write Timing is measured from the clock after the nBRDY is asserted up to nCAS assertion for that cycle.
4. Processor write data is always posted as 3-1-1-1 (nADS to nBRDY) as long as the DRAM Write Buffer is available.

Table 12 lists the performance summary for SDRAM. The CL= 3 column represents a CAS latency of three part with RAS to CAS (Trcd) equals to 2 clocks. The CL= 2 column represents a CAS latency of two part. It is assumed that each SDRAM row is populated with a maximum of 8 (x 8) DRAM devices.

Table 12 - SDRAM Cycle Timing

PROCESSOR CYCLE	60/66MHz W/ FOUR ROWS		60/66MHz W/ FIVE ROWS	
	CL=2	CL=3	CL=2	CL=3
Burst Read Page Hit	5-1-1-1	6-1-1-1	6-1-1-1	7-1-1-1
Read Row Miss[1] (nRAS high)	8-1-1-1	9-1-1-1	8-1-1-1	9-1-1-1
Read Page Miss	11-1-1-1	12-1-1-1	11-1-1-1	12-1-1-1
Back-to-Back Burst Reads Page Hit	5-1-1-1-2-1-1-1	6-1-1-1-2-1-1-1	6-1-1-1-2-1-1-1	7-1-1-1-2-1-1-1
Write Page Hit [2,3]	3	3	3	3
Write Row Miss[2,3]	5	6	5	6
Write Page Miss [2,3]	8	9	8	9
Posted Write[2,3]	3-1-1-1	3-1-1-1	3-1-1-1	3-1-1-1
Burst Write Retire Rate from Posted Write Buffer	-1-1-1	-1-1-1	-1-1-1	-1-1-1
Single Writes	3	3	3	3
SDRAM Configuration Register Setup				
Reg 54 Bit 5 / RAS to CAS Override [4]	0	1	0	1
Reg 54 Bit 4 / CAS Latency	1	0	1	0
Reg 54 Bit 3 / RAS Timing	1	0	1	0
Reg 56 Bit 4	0	0	0	0

Notes:

1. The row miss cycles assumes that the new page is closed from the prior cycle.
2. Assumes DRAM Write Buffer is available.
3. Processor write data is always posted as 3-1-1-1 (nADS to nBRDY) as long as the DRAM Write Buffer is available.
4. For a CL= 3 part that can not meet a RAS to CAS timing (Trcd) of two HCLKs, this bit can be set to “0”, which will add one HCLK to the leadoff cycle for Row Miss and Page Miss cycles.

5.2.26. DRAM Refresh

The SLC90E42 supports CAS_Before_RAS (CBR) refresh and self refresh.. The refresh rate is decided by the DRAM Refresh Rate field (bit [2-0]) of DRAM control register (offset address: 57h). The Refresh request is generated through the SUSCLK (32Khz).

During the refresh period, the SLC90E42 generates Refresh Requests for the six DRAM rows through a stagger scheme (i.e. every one half of CPU clock generates a row refresh request until all six rows are covered), which greatly reduces the length of the refresh period.

5.2.27. PCI Interface Overview

The SLC90E42 integrates a high performance PCI 2.1 compliant host controller. The table below lists the PCI bus command supported. The SLC90E42 forwards each of the CPU Shutdown, Halt and Stop Grant cycles to the PCI bus as special cycles. These cycles are terminated as Master Abort and a nBRDY is returned to the CPU. The Stop Grant cycle is propagated with 12h as address and 00120002h as data. The Halt cycle is encoded with 02h as address and 00120001h as data. The Shutdown cycle is encoded with 00h as address and 00120000h as data.

Table 13 - PCI Bus Commands Supported

COMMAND CODE	COMMAND	TARGET SUPPORT	INITIATOR SUPPORT
0000	Interrupt Acknowledge	No	Yes
0001	Special Cycle	No	Yes
0010	I/O Read	No	Yes
0011	I/O Write	No	Yes
0100	Reserved	No	No
0101	Reserved	No	No
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	No	No
1001	Reserved	No	No
1010	Configuration Read	No	Yes
1011	Configuration Write	No	Yes
1100	Memory Read Multiple	As Memory Read	No
1101	Dual Address Cycle	No	No
1110	Memory Read Line	As Memory Read	No
1111	Memory Write and Invalidate	As Memory Write	No

Including the SLC90E46 South Bridge chip, the bus arbiter of the host controller supports five PCI bus master devices. The PCI bus can be clocked at one half the frequency of the CPU clock, which provides minimum latency for data transfers between CPU bus and PCI bus, or at a fixed 33MHz, which delivers reliable PCI bus while CPU is clocked at a frequency higher than 66MHz.

5.2.28. PCI Data Buffers

The SLC90E42 integrates a 4-Dword buffer as CPU Write Buffer ("CWRBUF"). During CPU write accesses to the PCI bus, back-to-back sequential memory writes are first written to CWRBUF, then converted to burst writes on PCI bus. It allows the CPU to continue posting DWORD writes at the maximum bandwidth for the highest possible transfer rate to the graphics frame buffer.

The SLC90E42 also integrates two 32-Dword buffers as PCI Read Buffer ("PRDBUF") and PCI Write Buffer ("PWRBUF"), through which, the SLC90E42 supports Read Pre-fetching and Write Posting for PCI masters. During PCI master read memory cycles, the host controller fills the 32-DW deep PRDBUF with pre-fetched memory data, which allows the host controller to continuously burst data to the PCI master. During PCI master write memory cycles, the host controller continuously receives data from PCI master and stores the data into the deep PWRBUF. The data is then burst transferred into L2 cache or system memory. Without interruption from other bus master devices or CPU to PCI cycles, the SLC90E42 can support a long zero wait state burst stream on the PCI bus, effectively better than 120 MB per second bandwidth.

In order to provide optimal system performance, the SLC90E42 supports CPU and PCI concurrence. The PCI data buffers serve as the foundation for the concurrent operation. During PCI master memory read transaction, the SLC90E42 negates AHOLD and releases the memory bus to the processor after PRDBUF is filled up with pre-fetched data or a programmable number of cache lines has been moved into PRDBUF. The AHOLD signal is re-asserted (the processor is therefore temporarily suspended) and the memory bus is re-granted to the PCI host controller when PRDBUF contains less than eight DWords of data.

During PCI master memory write transaction, the AHOLD signal is asserted when one half of PWRBUF has been filled with received PCI data. The CPU is then halted until the piled up write buffer data are moved into L2 cache or system memory, then it re-gains control of the host and memory busses.

5.2.29. PCI System Arbitration

The SLC90E42 PCI arbiter supports five PCI masters. nREQ[3-0] and nGNT[3-0] are used by PCI master devices. nPHLD/nPHLDA is a pair of arbitration request and grant signals for the SLC90E46 South Bridge chip, which provides guaranteed access time capability for ISA masters.

5.2.30. Priority Scheme and Bus Grant

The SLC90E42 bus arbiter divides the system bus requesters into two groups: the processor and the PCI masters. The later includes the SLC90E46, which, when acting as a PCI master, represents ISA masters and DMA requests.

In this arbitration level, the SLC90E42 arbiter treats the two bus request agents equally: the bus arbiter will hold (through AHOLD assertion) the processor when there is a Bus Master Request from the PCI bus. Equally, the bus arbiter will pre-empt (i.e. disconnect) the master device which owns the PCI bus once the processor has a pending PCI cycle to be executed and the bus master device has owned the PCI bus for a pre-programmed time period defined via bits[6-5] of the SPCICL register. This scheme gives the processor a fair amount of time to access the PCI bus so that program execution will not be stalled by a pending PCI cycle while a PCI master is bursting data on the bus. The SLC90E42 does allow the processor and PCI master to alternately use the host and memory busses while maintaining PCI bus bursting data transfer without interruption.

In the PCI master group, the SLC90E42 bus arbiter further divides the bus requesters into two classes: PCI masters that uses the four pairs of bus requests/grant signals for bus requests and the SLC90E46 south bridge which uses the nPHLD and nPHLDA for bus requests. The bus arbiter gives the SLC90E46 nPHLD request the highest priority for the bus. The bus arbiter will pre-empt (i.e. disconnect) the master device that is currently transferring data on the PCI bus once there is pending PCI bus request and the bus master device has owned the PCI bus for a pre-programmed time period which can be defined via bits [6-5] of the SPCICL register. After the disconnection, the bus arbiter will grant the bus to the SLC90E46 via asserting nPHLDA.

Within the PCI master class, the bus arbiter rotates the priority for the four master devices. The last granted device is always dropped to the bottom of the priority queue for the next arbitration cycle. The bus arbiter still pre-empts (i.e. disconnects) the master device that is currently transferring data on the PCI bus once there is a pending bus request and the bus master device has owned the PCI bus for a pre-programmed time period.

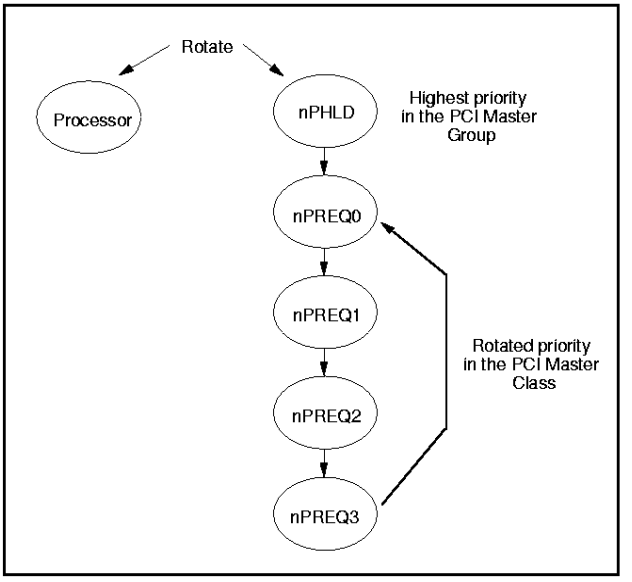


FIGURE 9 - PCI MASTER CLASS/BUS ARBITER

5.2.31. PCI Clock Control - nCLKRUN

The SLC90E42 supports the PCI nCLKRUN protocol as specified in the "PCI Mobile Design Guide". In this protocol, the SLC90E42 serves as a nCLKRUN Master device and will behave according to the rules for a master. The SLC90E46, as a nCLKRUN Central Resource, controls the clocks in the system.

5.2.32. SMRAM Memory Space

The SLC90E42 supports the use of main memory as System Management RAM (SMRAM). Two SMRAM modes are supported: Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM).

5.2.33. Compatible SMRAM - C_SMRAM

When this feature is enabled via setting G_SMRAME to "1" and C_BASE_SEG[2-0] to "010", the SLC90E42 treats 000A0000h to 000BFFFFh of the main memory as non-cacheable SMRAM. CPU accesses to the C_SMRAM range while not in SMM (i.e. nSMIACT is de-asserted) are forwarded to PCI bus. CPU accesses to the C_SMRAM range while in SMM are forwarded to either DRAM or PCI bus depending on the value of bits [6-4] of the SMRAMC register (offset address: 72h). The SLC90E42 will not respond to PCI master cycles (i.e. nDEVSEL is not asserted) which try to access the C_SMRAM space.

5.2.34. Extended SMRAM - E_SMRAM

The SLC90E42 allows the SMRAM space be extended to 1Mbytes and provide write-back cacheability. This feature requires the SMI handler executes in the above 1 Mbytes area (i.e. Protected Mode), however, it provides full processor performance for programs executed in SMM.

The SLC90E42 set an error status bit in the Extended SMRAM control register if the CPU tries to access the extended SMRAM space while nSMIACT is de-asserted and D_OPEN bit is reset. This access will be forwarded to PCI bus and may result in a Master Abort condition.

Extended SMRAM space consists of unused DRAM segments with address between A0000h and 100000h (this memory space is referred to as High Memory), and an optional block of memory referred to as the "TSEG". The TSEG is either 128 Kbytes, 256 Kbytes, 512 Kbytes, or 1 Mbytes block of memory as defined by TSEG_SIZE field of the ESMRAMC register (offset address: 71h). When TSEG is enabled, via TSEG_EN of the ESMRAMC register, the TSEG block of memory is disabled from the system memory and the system BIOS should report a main memory size of (Top of Memory "TOP" - TSEG block size) to the OS.

The two memory blocks available for SMRAM when the Extended SMRAM feature is enabled are:

	CPU Address		DRAM Address
•	100A0000h - 100FFFFFFh	map to	000A0000h - 000FFFFFh (H-SMRAM)
•	(10000000h + TOM - TSEG_SIZE) - (10000000h + TOM)	map to	(TOM - TSEG_SIZE) - TOM

Following DRAM memory blocks are available to the Extended SMRAM option:

Table 14 - DRAM Memory Blocks/Availability

DRAM BLOCK	SIZE / AVAILABILITY
A Segment (0A0000h - 0AFFFFh)	64Kbytes always available when H_SMRAM = "1" and G_SMRAME = "1"
B Segment (0B0000h - 0BFFFFh)	64Kbytes always available when H_SMRAM = "1" and G_SMRAME = "1"
C Segment (0C0000h - 0CFFFFh)	64Kbytes available if not used for shadowing when H_SMRAM = "1" and G_SMRAME = "1"
D Segment (0D0000h - 0DFFFFh)	64Kbytes available if not used for shadowing when H_SMRAM = "1" and G_SMRAME = "1"
E Segment (0E0000h - 0EFFFFh)	64Kbytes available if not used for shadowing when H_SMRAM = "1" and G_SMRAME = "1"
F Segment (0F0000h - 0FFFFFh)	64Kbytes available only for suspend/resume if not used for shadowing when H_SMRAM = "1" and G_SMRAME = "1"
TSEG	128K/256K/512K/1M bytes available when TSEG_EN = "1" and G_SMRAME = "1"

Like the Compatible SMRAM option, the SLC90E42 does not claim any bus master cycle to the Extended SMRAM memory space. The CPU accesses the Extended SMRAM space by the following mechanisms:

- When nSMIACT is active, the processor may access to the E-SMRAM memory blocks. A processor access to any of the E-SMRAM memory ranges while nSMIACT is negated and D_OPEN bit is reset will be forwarded to PCI bus and the E_SMRAM_ERR bit of the ESMRAMC register is set.
- The processor generates an access to one of the defined memory ranges while the D_OPEN bit is set.
- Any modified write access of the processor is allowed to write into the SMRAM space regardless of the state of the D_OPEN, D_CLOSE or nSMIACT signals.

The cacheability of SMRAM space is dependent on how much physical DRAM is available in the system. If the system has less than 32Mbytes of DRAM, then the SMRAM can be cached in both L1 and L2. On the other hand, if the system have more than 32 Mbytes of DRAM, the SMRAM is cacheable only in L1.

5.2.35. SMRAM Programming Considerations

When using the Extended SMRAM configuration, the SMI handler should be very careful when accessing DRAM memory in the 100A0000h to 100FFFFFh range. If this area of memory is accessed while the CPU is not in SMM mode and the D_OPEN bit is not set, the SLC90E42 will forward the cycle to PCI bus. In addition, only areas within the 100A0000h to 100FFFFFh region that have been selected as SMRAM space should be accessed, otherwise the L1 and L2 cache may become incoherent.

5.2.36. Power Saving State

The SLC90E42 supports four types of Power Saving modes: Standby, Dynamic Stop Clock, Suspend, and PowerOff modes. In PowerOff state, which includes Mechanical Off, Soft Off and Suspend to Disk power saving mode, the whole system including SLC90E42 is powered off after system state and memory image is stored into disk.

5.2.37. Standby Mode

The SLC90E42 supports a chip standby mode, which is enabled when the SLC90E42 determines that both CPU interface and PCI interface are idle during normal operating state (RESET is negated). In this state, the SLC90E42 dynamically places itself into a low power state while remains capable to respond to new CPU or PCI bus master accesses without performance penalty. The Standby mode provides very optimized power/performance characteristics because the CPU interface is idle for large periods of time.

5.2.38. Dynamic Stop Clock Mode

During Stop Clock periods, the SLC90E42 automatically disables the bus arbiter to inhibit all PCI master activities.

5.2.39. Suspend Mode

When the system is in Power-on-Suspend or Suspend-to-RAM state, the SLC90E42 switches to Suspend Refresh mode and maintains DRAM refresh from the SUSCLK clock source. In the Power-on-Suspend state, the SLC90E42 remains powered except that the host clock is stopped. In the Suspend-to-RAM mode, only the DRAM refresh logic is supplied with power from the SUSPEND power plane. When exiting from the Suspend-to-RAM mode, the SLC90E42's core well is reset and its context is lost with the power management context remained intact.

Table 15 shows the suspend state correspondence between the SLC90E46 south bridge and the SLC90E42 north bridge.

Table 15 - Suspend State Correspondence

SLC90E46 SUSPEND STATE	SLC90E42 SUSPEND STATE	SLC90E42 ACTIONS
Power-on-Suspend	Suspend	Host clock is stopped; Enable Suspend Refresh; The chip is still power-on.
Suspend-to-RAM	Suspend	Host clock is off. Enable Suspend Refresh; The chip is power-off except the Suspend well.
Suspend-to-Disk	PowerOff	Power is removed from the chip.
Soft Off/ Off	PowerOff	Power is removed from the chip.

5.2.40. The SLC90E42 Strapping Pins

The SLC90E42 latches the status of the strapping pins at the rising edge of the nRESET signal.

A[31-30] - L2 Cache Size

These two strapping pins configure the L2 cache size:

00: Cache not populated (or cache disabled)
01: 256K bytes
10: 512K bytes
11: Reserved

A[29-28] - L2 Cache Architecture

These two strapping pins configure the L2 cache architecture:

00: Single Bank of Pipelined Burst SRAM
01/10: Reserved
11: Two Banks of Pipelined Burst SRAM

A[27] - System Frequency

This bit tells the system bus frequency. The system is 60MHz if there is an external Pull-Up, or it is 66MHz if no external strapping is present. Bit 7 of the DRTH register is initialized with the inverted value on A[27] at the rising edge of the nRST. Since A[27] input buffer has an internal weak pulldown, unless an external pull-up resistor exists, the field should be initialized to "1", indicating 66MHz. BIOS can use this bit to determine the system frequency.

A[26] - Host Voltage

This bit is used to determine the voltage level of the host clock connected to the host clock pin and the voltage on the V_{CC} (CPU) pins. An external pull-down or pull-up resistor is required on this pin. When pulled down, it indicates 2.5v. When pulled high, 3.3v is indicated.

5.2.41. Power Planes

The SLC90E42 uses three primary internal power planes, which allows parts of the chip to power down and conserve battery life.

5.2.42. Suspend Power Plane

Contains all the logic needed to resume from the Suspend-to-RAM state. The power supply should be able to provide a trickle current in this state. The input signals attached to this power plane must not exceed V_{CC} (SUS).

Signals Powered by the Suspend Power Plane

DRAM interface signals, such as nMWE, nMWEB, CKE, nRAS[5-0], nCAS[7-0], SUSCLK and nSUSSTAT.

Power Pins of the Suspend Power Plane

VCC (SUS)

Ground Pins of the Suspend Power Plane

GND

5.2.43. CPU Power Plane

Contains all the IO pads that interface to the CPU.

Signals Powered by the CPU Power Plane

A[31-3], nBE[7-0], nADS, nBRDY, nNA, AHOLD, nEADS, nBOFF, nHITM, nM/IO, nD/C, nW/R, nLOCK, nCACHE, nKEN/INV, nSMIACT, D[63-0] and HCLKIN.

Power Pins of the CPU Power Plane

VCC(CPU)

Ground Pins of the CPU Power Plane

VSS

5.2.44. Main Power Plane

Contains all the rest of the SLC90E42 logic. This plane is powered by the main system power supply.

Signals Powered by the MAIN Power Plane

All other signal pins and internal logic.

Power Pins of the Main Power Plane

VCC

Ground Pins of the Main Power Plane

VSS

5.2.45. Power Sequencing Requirements

There are no power sequencing requirements for the various V_{CC} power supplies of the SLC90E42.

5.2.46. Clock Generation and Distribution

The SLC90E42 and CPU should be clocked from one clock driver output to minimize skew between the two parts.

5.2.47. Reset Sequencing

The SLC90E42 is asynchronously reset when the nRST signal is asserted. During reset or when the PCI bus is idle, the SLC90E42 drives the PCI bus signals, including AD[31-0], nC/BE[3-0], and the PAR signals, to "0".