

## MM54HC283/MM74HC283 4-Bit Binary Adder with Fast Carry

### General Description

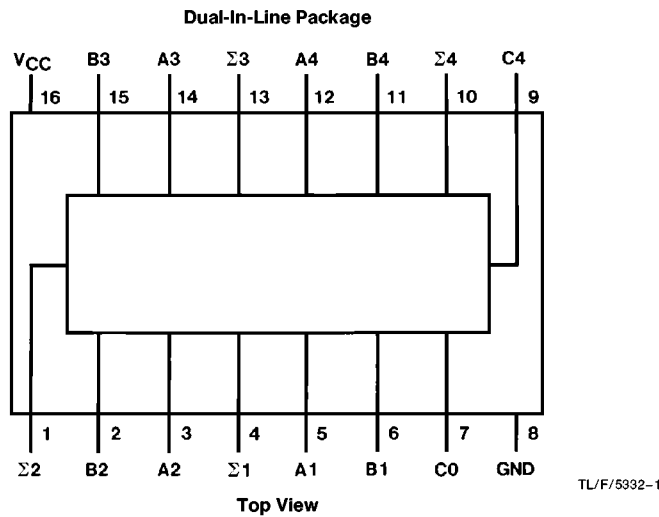
This full adder performs the addition of two 4-bit binary numbers utilizing advanced silicon-gate CMOS technology. The sum ( $\Sigma$ ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion. All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Wide supply range: 2V to 6V
- Low quiescent power consumption: 8  $\mu$ A at 25°C
- Low input current: 1  $\mu$ A maximum

### Connection Diagram



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## Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5 to +7.0V
DC Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC}$ + 1.5V
DC Output Voltage ( $V_{OUT}$ )	-0.5 to $V_{CC}$ + 1.5V
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	±20 mA
DC Output Current, per pin ( $I_{OUT}$ )	±25 mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	±50 mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature ( $T_L$ )	
(Soldering 10 seconds)	260°C

## Operating Conditions

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	2	6	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temp. Range ( $T_A$ )			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times ( $t_r, t_f$ )			
$V_{CC}=2.0V$		1000	ns
$V_{CC}=4.5V$		500	ns
$V_{CC}=6.0V$		400	ns

## DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$			Units	
				74HC $T_A = -40$ to $85^\circ C$		54HC $T_A = -55$ to $125^\circ C$		
				Typ	Guaranteed Limits			
$V_{IH}$	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
$V_{IL}$	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
$V_{OH}$	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
$V_{OL}$	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160	μA

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

**Note 4:** For a power supply of 5V ± 10% the worst case output voltages ( $V_{OH}$ , and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

\*\* $V_{IL}$  limits are currently tested at 20% of  $V_{CC}$ . The above  $V_{IL}$  specification (30% of  $V_{CC}$ ) will be implemented no later than Q1, CY'89.

**AC Electrical Characteristics**  $V_{CC} = 5V, T_A = 25^\circ C, C_L = 15 \text{ pF}, t_r = t_f = 6 \text{ ns}$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay From C0 to $\Sigma 1$ or $\Sigma 2$		18	27	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay From C0 to $\Sigma 3$		18	27	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay From C0 to $\Sigma 4$		20	30	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay From A1 or B1 to $\Sigma 1$		17	26	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay From C0 to C4		22	32	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay From A1 or B1 to C4		22	32	ns

**AC Electrical Characteristics**  $C_L = 50 \text{ pF}, t_r = t_f = 6 \text{ ns}$  (unless otherwise specified)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		74HC	54HC	Units
				Typ	Guaranteed Limits		$T_A = -40 \text{ to } 85^\circ C$	
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay From C0 to $\Sigma 1$ or $\Sigma 2$		2.0V	60	150	188	225	ns
			4.5V	21	30	37	45	ns
			6.0V	18	26	32	39	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay From C0 to $\Sigma 3$		2.0V	60	150	188	225	ns
			4.5V	21	30	37	45	ns
			6.0V	18	26	32	39	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay From C0 to $\Sigma 4$		2.0V	65	162	202	243	ns
			4.5V	24	34	43	51	ns
			6.0V	19	28	35	42	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay From A1 or B1 to $\Sigma 1$		2.0V	60	150	188	225	ns
			4.5V	22	33	41	50	ns
			6.0V	18	27	34	41	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay From C0 to C4		2.0V	70	175	219	263	ns
			4.5V	26	39	49	59	ns
			6.0V	21	32	40	46	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay From A1 or B1 to C4		2.0V	70	175	219	263	ns
			4.5V	26	39	49	59	ns
			6.0V	21	32	40	46	ns
$t_{THL}, t_{TLH}$	Maximum Output Rise and Fall Time		2.0V	28	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
$C_{IN}$	Maximum Input Capacitance			6	10	10	10	pF
$C_{PD}$	Power Dissipation Capacitance (Note 5)			150				pF

**Note 5:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

## Truth Table

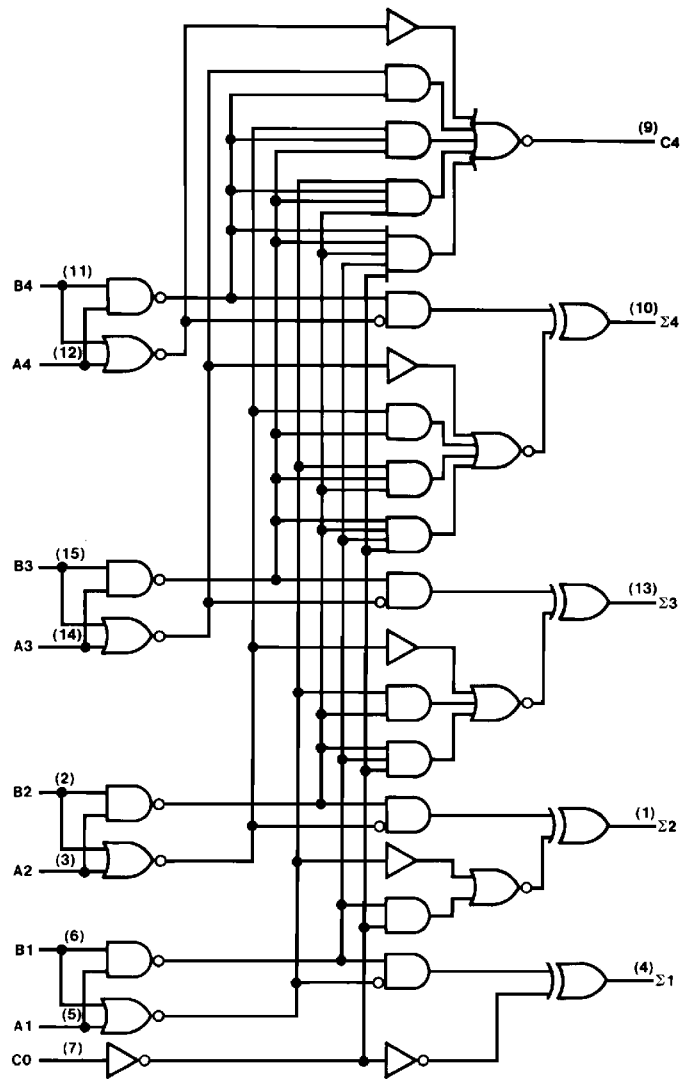
Input								Output											
								When C0 = L				When C0 = H							
								When C2 = L				When C2 = H							
A1	A3	B1	B3	A2	A4	B2	B4	Σ1	Σ3	Σ2	Σ4	C2	C4	Σ1	Σ3	Σ2	Σ4	C2	C4
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	L	L	L
L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	L	L	L
H	H	L	L	L	L	L	L	L	H	L	L	L	L	H	L	H	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	H
H	L	H	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L	L	H
L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	H	L	L	H	L	L	L	L	H	L	H	L	L	L
H	L	L	L	L	L	H	L	H	H	L	L	L	L	L	L	L	L	L	H
L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	H
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L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	L	L	L	L	H
H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	H
L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	H
H	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	H

H = high level, L = low level

**Note:** Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4

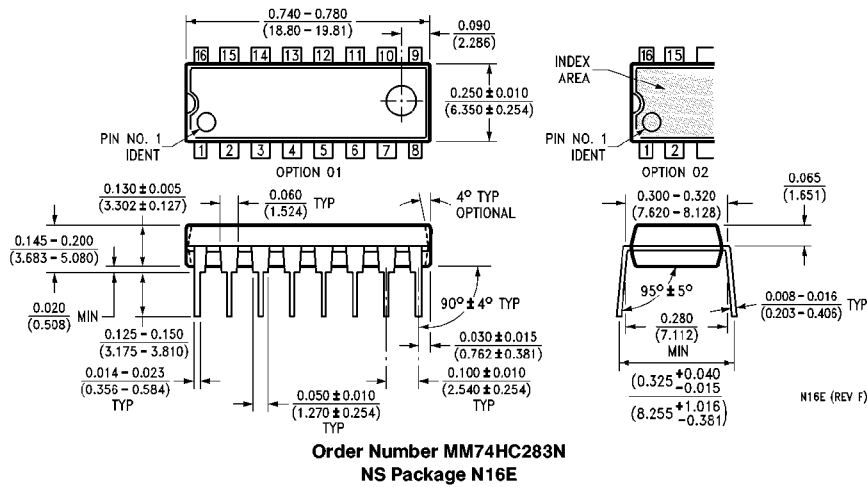
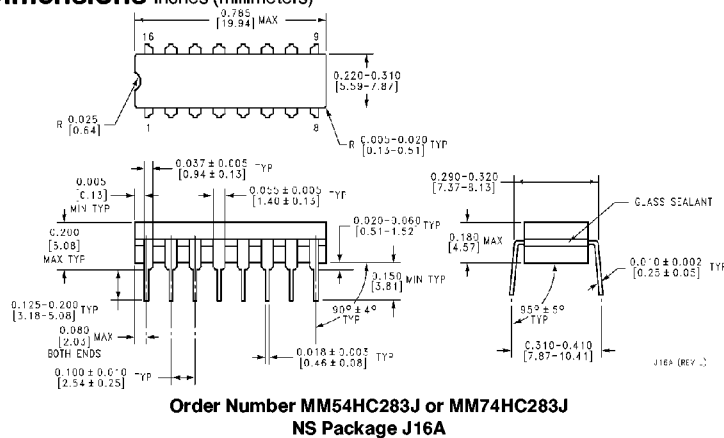
# Logic Diagram

'HC283



TL/F/5332-2

**Physical Dimensions** inches (millimeters)



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