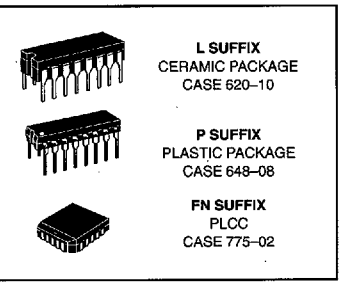
Quad Exclusive OR Gate

MC10113

The MC10113 is a quad Exclusive OR gate, with an enable common to all four gates. The outputs may be wire–ORed together to perform a 4–bit comparison function (A = B). The enable is active low.

P_D = 175 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ
t_r, t_f = 2.0 ns typ (20% to 80%)

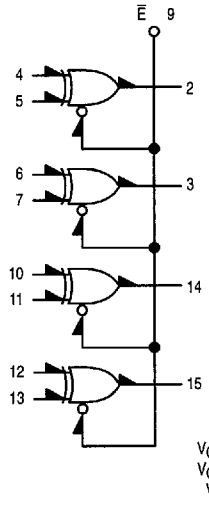


L SUFFIX
CERAMIC PACKAGE
CASE 620–10

P SUFFIX
PLASTIC PACKAGE
CASE 648–08

FN SUFFIX
PLCC
CASE 775–02

LOGIC DIAGRAM

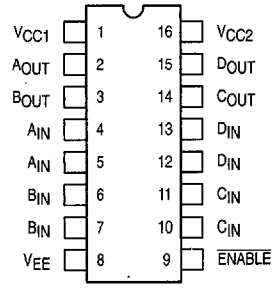


V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

TRUTH TABLE

IN		$\overline{E}$	OUTPUT
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
X	X	H	L

DIP
PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 6–11.

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			−30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		46			42		46	mAdc
Input Current	I_{inH}	4,7,10,13		425			265		265	µAdc
		5,6,11,12		350			220		220	
		9		870			545		545	
	I_{inL}	*	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	2	−1.060	−0.890	−0.960		−0.810	−0.890	−0.700	Vdc
		3	−1.060	−0.890	−0.960		−0.810	−0.890	−0.700	
		14	−1.060	−0.890	−0.960		−0.810	−0.890	−0.700	
		15	−1.060	−0.890	−0.960		−0.810	−0.890	−0.700	
Output Voltage Logic 0	V_{OL}	2	−1.890	−1.675	−1.850		−1.650	−1.825	−1.615	Vdc
		3	−1.890	−1.675	−1.850		−1.650	−1.825	−1.615	
		14	−1.890	−1.675	−1.850		−1.650	−1.825	−1.615	
		15	−1.890	−1.675	−1.850		−1.650	−1.825	−1.615	
Threshold Voltage Logic 1	V_{OHA}	2	−1.080		−0.980			−0.910		Vdc
		3	−1.080		−0.980			−0.910		
		14	−1.080		−0.980			−0.910		
		15	−1.080		−0.980			−0.910		
Threshold Voltage Logic 0	V_{OLA}	2		−1.655			−1.630		−1.595	Vdc
		3		−1.655			−1.630		−1.595	
		14		−1.655			−1.630		−1.595	
		15		−1.655			−1.630		−1.595	
Switching Times (50Ω Load)					Min	Typ	Max			ns
Propagation Delay	t_{4+2+}	2	1.1	4.7	1.3	2.6	4.5	1.3	5.0	
	t_{4-2-}	2	1.1	4.7	1.3	2.6	4.5	1.3	5.0	
	t_{9+2-}	2	1.3	5.2	1.5	3.4	5.0	1.5	5.5	
	t_{9-2+}	2	1.3	5.2	1.5	3.4	5.0	1.5	5.5	
Rise Time (20 to 80%)	t_{2+}	2	1.1	4.2	1.1	2.5	3.9	1.1	4.4	
Fall Time (20 to 80%)	t_{2-}	2	1.1	4.2	1.1	2.5	3.9	1.1	4.4	

* Individually test each input applying V_{IH} or V_{IL} to input under test.

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ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	4,7,10,13	*				8	1, 16
			5,6,11,12	*				8	1, 16
			9	9				8	1, 16
		I_{inL}	*		*			8	1, 16
Output Voltage	Logic 1	V_{OH}	2	4				8	1, 16
			3	7				8	1, 16
			14	11				8	1, 16
			15	13				8	1, 16
Output Voltage	Logic 0	V_{OL}	2		4			8	1, 16
			3		7			8	1, 16
			14		11			8	1, 16
			15		13			8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	2			4		8	1, 16
			3			6		8	1, 16
			14			10		8	1, 16
			15			12		8	1, 16
Threshold Voltage	Logic 0	V_{OLA}	2				5	8	1, 16
			3				7	8	1, 16
			14				11	8	1, 16
			15				13	8	1, 16
Switching Times	(50Ω Load)			+1.11V		Pulse In	Pulse Out	–3.2 V	+2.0 V
Propagation Delay		t_{4+2+}	2			4	2	8	1, 16
		t_{4-2-}	2			4	2	8	1, 16
		t_{9+2-}	2	4		9	2	8	1, 16
		t_{9-2+}	2	4		9	2	8	1, 16
Rise Time	(20 to 80%)	t_{2+}	2			4	2	8	1, 16
Fall Time	(20 to 80%)	t_{2-}	2			4	2	8	1, 16

* Individually test each input applying V_{IH} or V_{IL} to input under test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

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