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A TDK Group Company

SSI 32C9003
PC-AT Combo Controller
80 Mbit/s, Dual Bit NRZ Interface

Preliminary Data

January 1994

DESCRIPTION

The SSI 32C9003 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build an ATA disk drive. The 32C9003 has a dual bit NRZ interface to allow interfacing with channel ICs supporting this interface. The circuitry of the SSI 32C9003 includes a complete ATA interface, an advanced buffer manager, a high performance disk formatter and an 88 bit Reed-Solomon ECC with fast "on-the-fly" hardware correction. The SSI 32C9003 provides maximum performance while minimizing micro controller intervention.

The SSI 32C9003 is capable of transfers of up to 80 megabits per second on the disk interface and 6 megawords per second across the ATA bus. In addition, on-the-fly error corrections and microcontroller accesses to the buffer memory can occur during transfers.

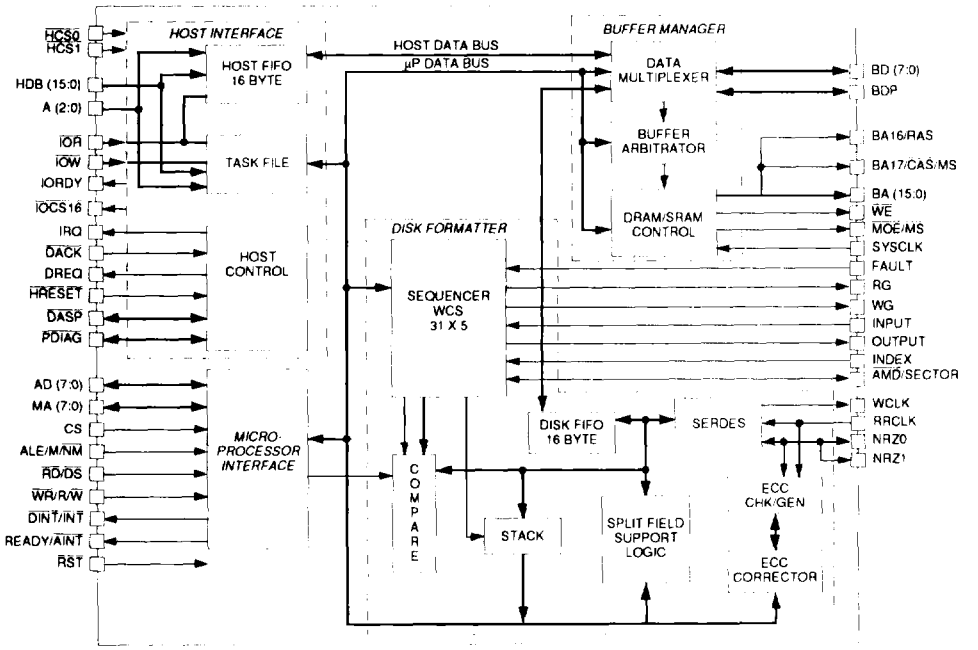
(continued)

FEATURES

- **ATA Interface**
  - **Single chip PC AT controller**
  - **Full ANSI ATA compliance**
  - **Direct PC bus connection with on board 24 mA drivers**
  - **PC transfers to 6.7 megawords per second**
  - **Supports PIO, DMA and Multiword DMA (EISA Class B Demand DMA)**
  - **Logic for daisy chaining 2 drives**
  - **Operate as master, slave or both**
  - **Hardware support for write-multiple and read-multiple commands**
  - **Automatic command decoding of Write, Write Long, Write DMA, Write Multiple, Write Buffer and Format commands**

(continued)

BLOCK DIAGRAM



SSI 32C9003
PC-AT Combo Controller
80 Mbit/s, Dual Bit NRZ Interface

DESCRIPTION (continued)

The SSI 32C9003 is one of a family of Silicon Systems' single chip disk controllers which support a wide range of device interfaces. The 32C9301 and 32C9302 are both 3.3/5 volt dual voltage ATA controllers with a dual bit and single bit NRZ disk formatter interface. The SSI 32C9001 is a 5 volt only version of the 32C9301 which is 100% firmware and pinout compatible. The SSI 32C9020, SSI 32C9022 and SSI 32C9023 family members are SCSI disk controllers providing many of the same features as the SSI 323C9003. The SSI 32C9340 disk controller completes the family providing PCMCIA/ATA compliant interfaces. All members are based on a common architecture allowing major portions of firmware to be reused. The Silicon Systems' chip family is illustrated in hierarchy chart shown in Figure 1.

The high level of integration within the SSI 32C9003 represents a major reduction in parts count. When the SSI 32C9003 ATA Controller is combined with the SSI 32R2010 Read/Write device, the SSI 32P3000 Pulse Detector, the SSI 32D4040 Dual Bit Data Synchronizer with 1,7 ENDEC, the SSI 32H4631 Servo and Motor Speed Controller, an appropriate micro controller and memory a complete, cost efficient, high performance intelligent drive solution is created.

FEATURES (continued)

- **ATA Interface** (continued)
  - **Automatic updates of the host task file registers in both Cyl/Hd/Sec and LBA modes**
  - **Automatic Multi-Sector data transfers without microprocessor intervention**
  - **Automatic Host Interrupt and Busy for multiple sector transfers integrated with buffer streaming logic**
  - **16 byte FIFO to improve performance**
  - **Power management, including power down at I/O pins**
- **Buffer Manager**
  - **Direct support of DRAM or SRAM**
    - **SRAM: up to 256k bytes of memory with throughput to 20 megabytes per second**
    - **DRAM: up to 1 megabyte of memory with throughput to 17.78 megabytes per second**
  - **Programmable memory timing**
  - **Buffer RAM segmentation with flexible segment sizes from 256 bytes to 1 megabyte**
  - **Dedicated host, disk and microprocessor address pointers**
  - **Buffer Streaming with internal buffer protection circuit providing buffer integrity**
- **Disk Formatter**
  - **Dual Bit NRZ interface supporting data rates to 80 megabits per second**
  - **Automatic multi-sector transfer**
  - **Header or microprocessor based split data field support**
  - **Advanced sequencer organized in 31 x 5 bytes**
  - **88-bit Reed Solomon ECC with "on-the-fly" fast hardware correction circuitry**
  - **Capable of correcting up to four 10-bit symbols in error**
  - **Guaranteed to correct one 31-bit burst or two 11-bit bursts**
  - **Hardware on-the-fly correction of an 11-bit single burst error within a one half sector time**
  - **Detects up to one 51-bit burst or three 11-bit bursts**
- **Microprocessor Interface**
  - **Supports both multiplexed or non-multiplexed microprocessors**
  - **Separate or combined host and disk interrupts**
- **Other Features**
  - **Internal power down modes**
  - **Available in 120 and 128-Lead TQFP, and 128 QFP packages**

FUNCTIONAL DESCRIPTION

The SSI 32C9003 contains the following four major functional blocks:

Microprocessor Interface
ATA Interface
Disk Formatter
Buffer Manager

The Microprocessor Interface allows the local microprocessor access to all of the SSI 32C9003 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers, can control all activities of the SSI 32C9003. The microprocessor can elect to perform host and/or disk operations directly, or it can enable the advanced features of the SSI 32C9003 which can perform these operations automatically.

The ATA Interface block handles all PC AT bus activities. The ATA interface includes 24 mA drivers allowing for direct connection of the SSI 32C9003 to the PC AT bus. The ATA interface block is highly automated, capable of performing multiple block transfers without micro controller involvement. The ATA block interfaces directly with the Buffer Manager via an internal speed matching FIFO.

The Disk Formatter performs the serialization and deserialization of data. If provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the Disk Formatter is an advanced programmable sequencer. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The disk interface can be configured through a wide range of capabilities. This allows the SSI 32C9003 to interface with nearly any read/write channel and allows the user of the SSI 32C9003 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9003 controller and the SSI 32D4040 Data Synchronizer with 1,7 ENDEC, you are guaranteed a problem free interface.

Within the Disk Formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check an enhanced 16 bit CRC for headers and an 88 bit Reed Solomon code for data. If the checker detects an error using the 88 bit Reed Solomon code, the syndrome information is transferred into the corrector. The corrector then performs the necessary operations to determine if the

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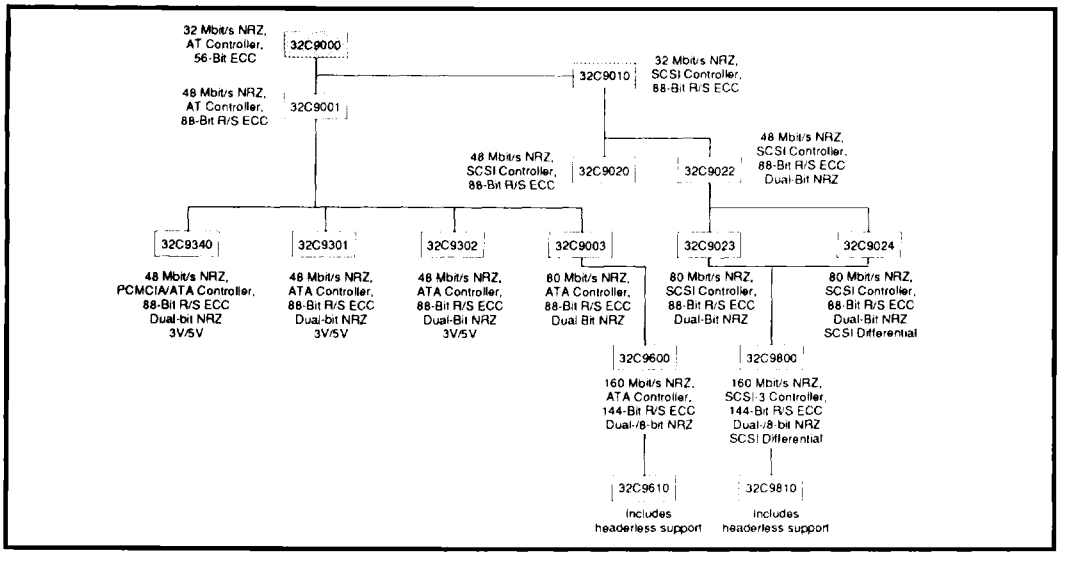

FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy

FUNCTIONAL DESCRIPTION (continued)

error was correctable and, if it was correctable, the corrector interfaces directly with the buffer controller and performs the correction automatically. The corrector performs its correction within one half of a sector. This guarantees that the corrector will always be available to correct the next sector if necessary.

The Buffer Manager can support either SRAM or DRAM. When configured to operate with DRAM, the Buffer Manager automatically performs necessary refresh cycles. The buffer manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. Besides interfacing with the buffer memory, the Buffer Manager interfaces with the ATA Interface block, the Disk Formatter block, the ECC corrector and the microprocessor. If more than one of these devices requires access to the buffer memory, the Buffer Manager arbitrates the requests automatically.

PIN DESCRIPTION

The following convention is used in the pin description:

- (I) denotes an input
- (O) denotes an output
- (I/O) denotes a bidirectional signal
- (Z) denotes a tri-state output
- (OD) denotes an open drain output

Active low signals are denoted by a bar on top of the signal name and dual function pins are denoted with a slash between the two signals — $\overline{AMD}$/SECTOR

GENERAL

NAME	TYPE	DESCRIPTION
VDD		POWER SUPPLY PIN
GND		GROUND

HOST INTERFACE

A(2:0)	I	HOST ADDRESS LINES. The Host Address lines A(2:0) are used to access the various PC/AT control/status, and data registers.
$\overline{HCS1}$	I	HOST CHIP SELECT 1. This pin selects access to the control block task file registers.
$\overline{HCS0}$	I	HOST CHIP SELECT 0. This pin selects access to the command block task file registers.
$\overline{IOCS16}$	OD	16 BIT DATA TRANSFER. An open drain active low output that indicates that a 16-bit buffer transfer is active.
IRQ	O,Z	HOST INTERRUPT. Asserted active high to indicate to the Host that the controller needs attention.
IORDY	O,Z	I/O CHANNEL READY. This signal is asserted low to extend host transfer cycles when the controller is not ready to respond. This pin will be tristated when a read or write is not in progress.

HOST INTERFACE (continued)

NAME	TYPE	DESCRIPTION
DREQ	O,Z	DMA REQUEST. The active high DMA Request signal is used during DMA transfer between the Host and the controller.
$\overline{\text{DACK}}$	I	DMA ACKNOWLEDGE. This active low signal is used during DMA to complete the DMA handshake for data transfer between the host and the controller.
$\overline{\text{IOR}}$	I	I/O READ. This active low pin is asserted by the Host during a Host read operation. When asserted with $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$, or $\overline{\text{DACK}}$, data from the device is enabled onto the host data bus.
$\overline{\text{IOW}}$	I	I/O WRITE. Asserted active low by the HOST during a HOST write operation. When asserted with $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$, or $\overline{\text{DACK}}$, data from the host data bus is strobed into the device.
$\overline{\text{HRESET}}$	I	HOST RESET. This active low signal stops all commands in progress and initializes the control/status registers — This signal can also "wake up" the device while it is in power down mode.
HDB(15:0)	I/O	HOST DATA BUS. These bits are used for word transfers between the Buffer Memory and the Host; bits (7:0) are used for status, commands, or ECC byte transfers.
$\overline{\text{DASP}}$	I,OD	DRIVE ACTIVE/DRIVE 1 PRESENT. This is a time-multiplexed signal which indicates that a drive is active, or that Drive 1 is present.
$\overline{\text{PDIAG}}$	I,OD	PASSED DIAGNOSTICS. This signal is an output when configured as Drive 1 and an input when configured as Drive 0.

DISK INTERFACE

INDEX	I	INDEX. This input is a pulse that occurs once per revolution and defines the start of first sector.
OUTPUT	O	DISK SEQUENCER OUTPUT. This pin is controlled by bit 2 of the control field of the disk sequencer.
INPUT	I	INPUT. This signal is used to synchronize the disk sequencer to an external event.
$\overline{\text{AMD}}$/ SECTOR	I	ADDRESS MARK DETECT/SECTOR. This pin is configured to operate in Hard or Soft Sector mode by initializing the Disk Formatter Mode Control Register: 4FH, bit 1. In the hard sector mode it is used as the sector input — a pulse on this pin indicates a sector mark is found. In the soft sector mode, an active low input indicates an address mark was detected. The device powers up in soft sector mode.
RG	O	READ GATE. This active high output enables the reading of the disk. It is asserted at the beginning of the PLO for header and data field by the sequencer — sequencer Control Field bits 5 and 6. It is automatically deasserted at the end of the CRC or ECC.

PIN DESCRIPTION (continued)

DISK INTERFACE

NAME	TYPE	DESCRIPTION
WG	O	WRITE GATE. This active high output enables writing onto the disk. It is asserted and deasserted by the sequencer Control Field bits 5 and 6.
RRCLK	I	READ REFERENCE CLOCK. This pin is used in conjunction with the NRZs pin to clock data in. It is also used as a clock for the disk sequencer and is used to generate WCLK.
WCLK	O	WRITECLOCK. This signal clocks the NRZ data out.
NRZ0, 1	I/O	NON RETURN TO ZERO. These signals are the read data input 0 and 1 from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. NRZ1 is the most significant bit.
FAULT	I	Fault: Asserting this pin causes the disk sequencer to stop immediately.

MICROPROCESSOR INTERFACE

$\overline{RST}$	I	RESET. An asserted active low input generates a component reset that holds the internal registers of the controller at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals and Host outputs are set to the high-Z state.
ALE	I	ADDRESS LATCH ENABLE/Multiplexed or Non-multiplexed address select: If this input is constantly low, the microprocessor interface is configured with non-multiplexed address and data busses. If this input is ever high, the microprocessor interface is configured with a multiplexed address and data bus. In this case, this pin functions as the address latch enable, and the latched address is output on the MA(7:0) pins.
CS	I	CHIP SELECT. This signal must be asserted high for all microprocessor accesses to the registers of this chip.
$\overline{WR}$/R/$\overline{W}$	I	WRITE STROBE/READ/WRITE. When the Intel bus control interface is selected, this signal acts as the $\overline{WR}$ signal. When the Write strobe signal is asserted low and the CS signal is asserted high, the data on the AD lines will be written to the register. When the Motorola bus control interface is selected, this signal acts as the R/$\overline{W}$ signal. A high on this input along with the $\overline{RD}$/$\overline{DS}$ signal asserted and the CS signal asserted high indicates a read operation. A low on this input along with the $\overline{RD}$/$\overline{DS}$ signal asserted and the CS signal asserted high indicates a write operation.

MICROPROCESSOR INTERFACE (continued)

NAME	TYPE	DESCRIPTION
$\overline{RD}/\overline{DS}$	I	READ STROBE/DATA STROBE. When the Intel bus control interface is selected, this signal acts as the $\overline{RD}$ signal. When the read strobe signal is asserted low and the CS signal is asserted high, the data from the specified register will be driven onto the AD signals. When the Motorola bus control interface is selected, this signal acts as the $\overline{DS}$ signal. A high on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a read operation. A low on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a write operation.
$\overline{DINT}/\overline{INT}$	O, OD	DISK INTERRUPT. This signal is an interrupt line to the microprocessor. It is the combined interrupt line of the disk side and host side interrupts when pin RDY/$\overline{HINT}$ is programmed as Ready; otherwise, it only signals the occurrence of disk side interrupt events. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state.
AD(7:0)	I/O	ADDRESS/DATA BUS. When configured in the Multiplexed mode, these lines are multiplexed, bidirectional data path to the microprocessor. During the beginning of the memory cycle the bus captures the low order byte of the microprocessor address. These lines provide communication with the controller device's internal registers and the buffer memory. When configured in the Non-multiplexed mode, these lines are bidirectional data lines.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS: This 8-bit output bus is the AD(7:0) bus latched by the ALE pin during the low order address phase of a Multiplexed type microprocessor cycle. These signals are non-multiplexed address input when used with a Non-multiplexed microprocessor.
READY/$\overline{AINT}$	O, OD	READY/HOST SIDE INTERRUPT: When programmed as the Ready function, this signal is deasserted low for the microprocessor to insert wait states to allow time for the chip to respond to the access. When programmed as the host side interrupt, this pin interrupts the microprocessor when there is a host related interrupt event. The interrupt signal is programmable for either a push-pull or open-drain output circuit. This signal powers up as the 'Ready' function.

PIN DESCRIPTION (continued)

BUFFER MANAGER INTERFACE

NAME	TYPE	DESCRIPTION
BA(15:0)	O	BUFFER MEMORY ADDRESS LINES 15 through 0. These sixteen outputs provide address lines for the dynamic memory or static memory chips used to implement the buffer memory.
BA16/$\overline{RAS}$	O	BUFFER MEMORY ADDRESS 16: In SRAM mode, this pin generates the address: A16 for direct connection to a Static RAM address line 16. BUFFER ROW ADDRESS STROBE: This active low output signal is generated to strobe the row — high order — address into the dynamic RAMs. It is intended to be directly tied to the RAMs input control pin.
BA17/$\overline{CAS}$/$\overline{MS}$	O	BUFFER MEMORY ADDRESS 17/COLUMN ADDRESS STROBE/ MEMORY SELECT: This signal is used for addressing the buffer memory in SRAM mode or as the column address strobe in DRAM mode. When configured as $\overline{MS}$ this signal is active during both buffer memory reads and buffer memory writes. After $\overline{RST}$ is asserted, this signal will be high.
BD(7:0)	I/O	BUFFER MEMORY DATA BUS. 7 through 0. The bidirectional Data Bus connects directly to the buffer memory. This bus is designed for high speed data transfer.
BDP	I/O	BUFFER MEMORY PARITY: This bit is the parity value for BD(7:0).
$\overline{MOE}$/$\overline{MS}$	O	MEMORY OUTPUT ENABLE/MEMORY SELECT. When configured as $\overline{MOE}$, this signal is active during buffer memory reads. When configured as $\overline{MS}$, this signal is active during both buffer memory reads and buffer memory writes, The timing of the $\overline{MS}$ signal follows that of the address pins.
$\overline{WE}$	O	WRITE ENABLE. This active low output signal is used to strobe the data into the RAMs from the Data bus. For both buffer memory applications, this line is tied directly to the SRAM or DRAM control pin.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address lines, write enable WE, and memory output enable MOE. In power down mode, this signal is shut off from the internal logic and hence buffer memory access is inhibited.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

PARAMETER	RATING
Power Supply Voltage, VCC	7V
Ambient Temperature	0 to 70°C
Storage Temperature	-65 to 150°C
Power Dissipation	750 mW
Input, Output pins	-0.5 to VCC+0.5V

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VDD Power Supply Voltage		4.5		5.5	V
IDD Supply Current				50	mA
IDDS Standby Current	Note 1			250	µA
VIL Input Low Voltage		-0.5		0.8	V
VIH Input High Voltage	Except $\overline{RST}$ pin	2.0		VCC+0.5	V
VIH Input High Voltage	$\overline{RST}$ pin	3.9		VCC+0.5	V
VOL Output Low Voltage	Note 2			0.4	V
VOL Output Low Voltage	Note 3			0.5	V
VOH Output High Voltage IOH = -400 µA		2.4			V
IL Input Leakage Current 0 < VIN < VCC		-10		10	µA
CIN Input Capacitance				10	pF
COUT Output Capacitance				10	pF

Note: (1) Synchronization and Clock Control Register, 7FH: bits 3 and 4 set. RRCLK and SYSCLK internally inhibited.

(2) All interface pins except Host Interface pins. IOL= 2 mA.

(3) Host Interface pins, IOL = 24 mA.

MICROPROCESSOR INTERFACE TIMING PARAMETERS

Multiplexed Bus Interface Timings (Figures 2, 3, 4, 5)

Ta	ALE Width		20			ns
Tma	Address valid to MA (7:0) valid				30	ns
Tr	$\overline{RD}$ Width		80			ns
As	Address valid to ALE ↓		5			ns
Ah	ALE ↓ to address invalid		10			ns
Cs	CS valid to $\overline{RD}$ ↓ or $\overline{DS}$ ↓		20			ns
Ch	$\overline{RD}$ ↑ or $\overline{DS}$ ↑ to CS ↓		0			ns
Tda	$\overline{RD}$ ↓ or $\overline{DS}$ ↓ to read data valid	Except Read of WCS			30	ns
Tda	$\overline{RD}$ ↓ or $\overline{DS}$ ↓ to read data valid	Read of WCS			50	ns
Tds	$\overline{DS}$ width		80			ns
Tdh	$\overline{RD}$ ↑ to or $\overline{DS}$ ↑ read data invalid		0		25	ns
Tsrw	R/$\overline{W}$ valid to $\overline{DS}$ ↓		20			ns
Thrw	$\overline{DS}$ ↑ to R/W invalid		20			ns
Tdrdy	$\overline{RD}$ ↓ to READY ↓ (Intel) or $\overline{DS}$ ↓ to READY ↓ (Motorola)				30	ns
Wds	Write data valid to $\overline{WR}$ ↑ or $\overline{DS}$ ↑		40			ns
Wdh	$\overline{WR}$ ↑ or $\overline{DS}$ ↑ to write data invalid		10			ns

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ELECTRICAL SPECIFICATIONS (continued)

Non-Multiplexed Bus Interface Timings (Figure 6)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Tmas	MA (7:0) valid to $\overline{DS}$ ↓		5			ns
Tmah	$\overline{DS}$ ↑ to MA (7:0) invalid		5			ns
Cs	CS valid to $\overline{DS}$ ↓		20			ns
Ch	$\overline{DS}$ ↑ to CS ↓		0			ns
Tda	$\overline{DS}$ ↑ to read data valid	Except Read of WCS			30	ns
Tda	RD ↓ or $\overline{DS}$ ↑ to read data valid	Read of WCS			50	ns
Tds	DS width		80			ns
Tdh	DS ↑ to read data invalid		0		25	ns
Tsrw	$\overline{R/W}$ valid to $\overline{DS}$ ↓		20			ns
Thrw	$\overline{DS}$ ↑ to $\overline{R/W}$ invalid		20			ns
Tdrdy	$\overline{DS}$ ↓ to READY ↓ (Motorola)				30	ns
Wds	Write data valid to $\overline{WR}$ ↑ or $\overline{DS}$ ↑		40			ns
Wdh	$\overline{WR}$ ↑ or $\overline{DS}$ ↑ to write data invalid		10			ns

Note: (1) Loading capacitor = 30 pF
(2) ↑ indicates rising edge ↓ indicates falling edge

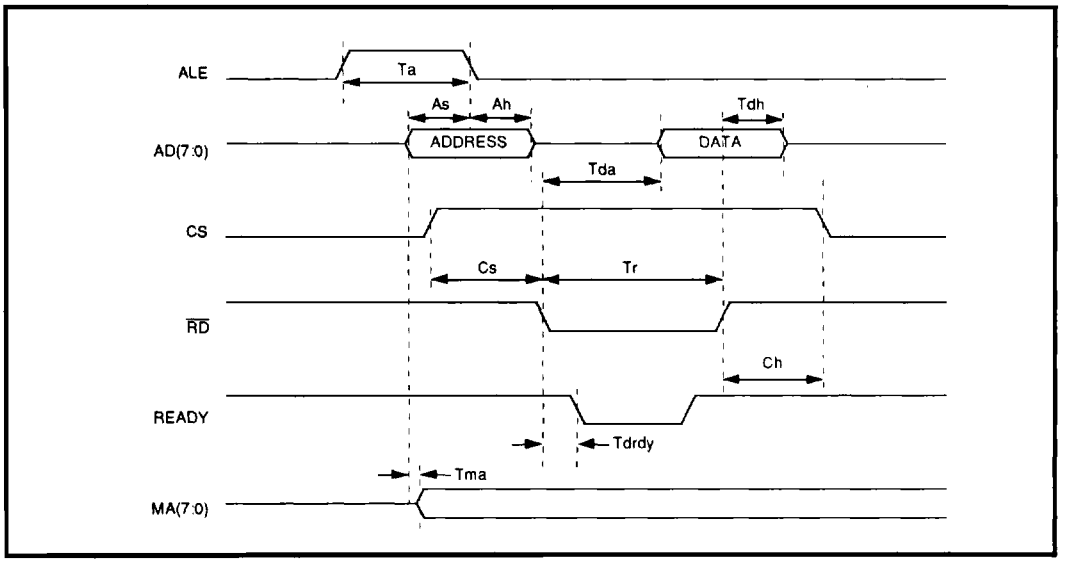

FIGURE 2: Intel Register Multiplexed Read Timing

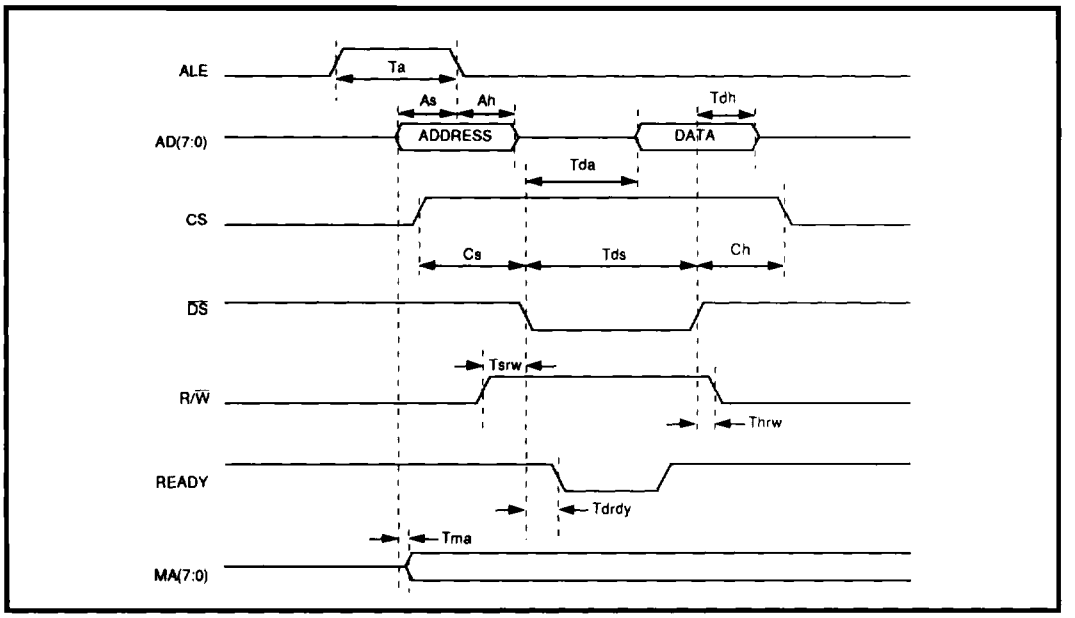

FIGURE 3: Motorola Register Multiplexed Read Timing

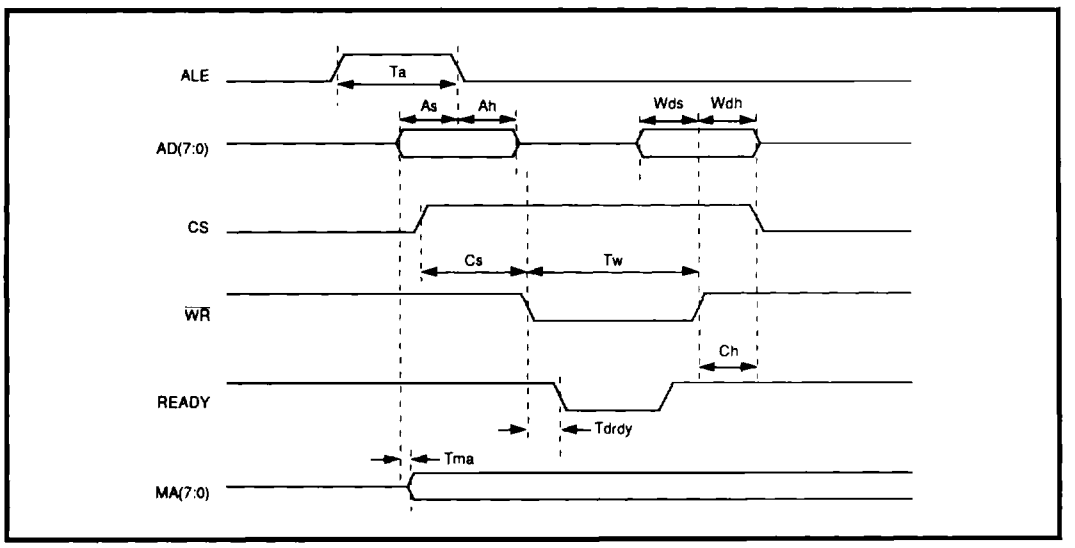

FIGURE 4: Intel Register Multiplexed Write Timing

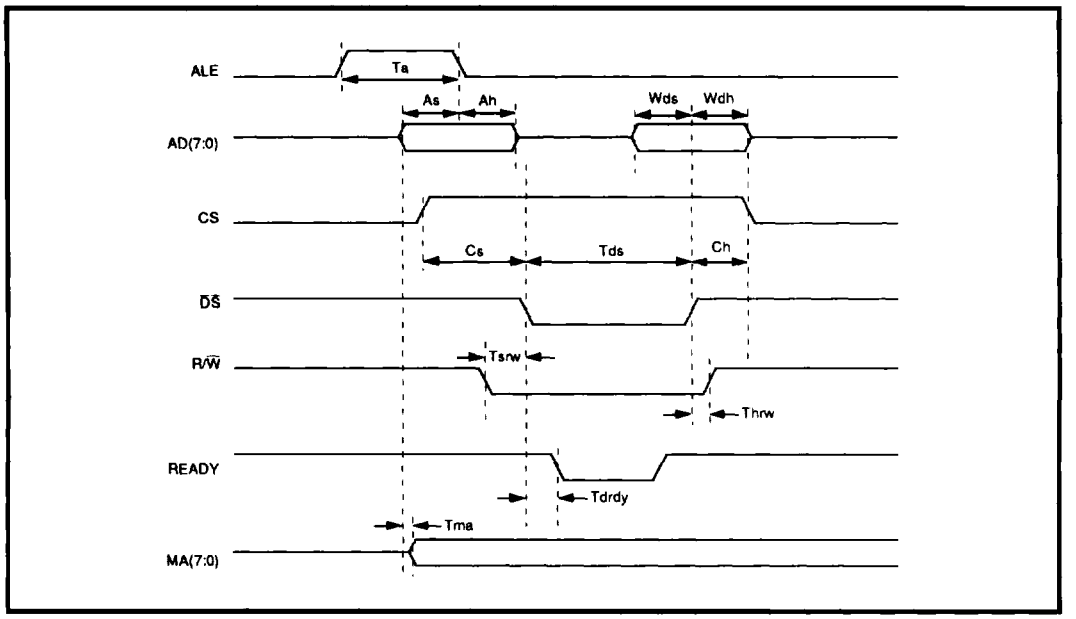

FIGURE 5: Motorola Register Multiplexed Write Timing

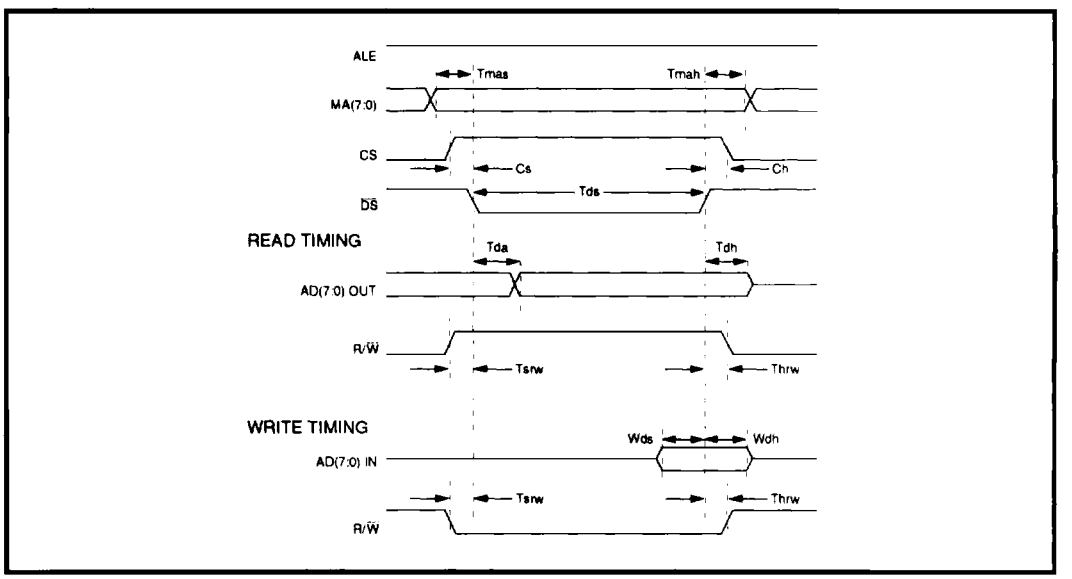

FIGURE 6: Non-Multiplexed Bus Timing Diagrams

ELECTRICAL SPECIFICATIONS (continued)

Disk Read/Write Timing (Figure 7)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Trrc	RRCLK period (dual bit)		27.8			ns
Trrc	RRCLK period (single bit)		20.8			ns
Trrcl	RRCLK low time (dual bit)		11.1			ns
Trrcl	RRCLK low time (single bit)		8.5			ns
Trrch	RRCLK high time (dual bit)		11.1			ns
Trrch	RRCLK high time (single bit)		8.5			ns
Dis	NRZ in valid to RRCLK high		3			ns
Dih	RRCLK high to NRZ in invalid		3			ns
As	$\overline{AMD}$ valid to RRCLK high (soft sector only)		3			ns
Dv	RRCLK high to NRZ1, NRZ0 out valid				18	ns
Dvw	WCLK low to NRZ1, NRZ0 out valid		-3		+3	ns
Trwl	RRCLK high to WCLK low				18	ns
Trwh	RRCLK low to WCLK high				18	ns
Twckh	WCLK high time (dual bit)		8.3			ns
Twckh	WCLK high time (single bit)		6.3			ns
Twckl	WCLK low time (dual bit)		8.3			ns
Twckl	WCLK low time (single bit)		6.3			ns

Note: Loading capacitance = 10 pF

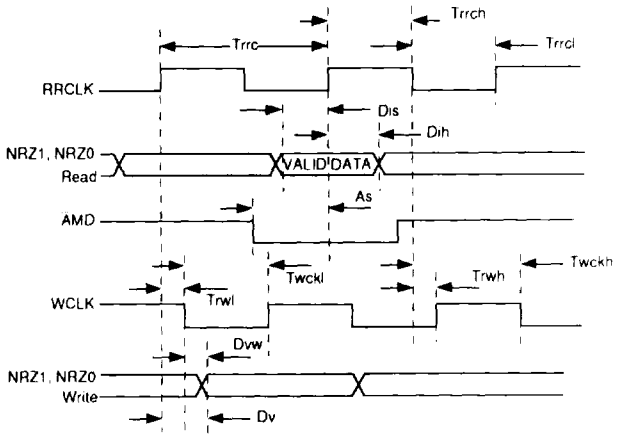

FIGURE 7: Disk Interface Timing

ELECTRICAL SPECIFICATIONS (continued)

BUFFER MEMORY READ/WRITE TIMING PARAMETERS (Figures 8 through 14)

PARAMETER		MIN	NOM	MAX	UNIT
T	SYSCLK period	25			ns
T/2	SYSCLK high/low time	10			ns
Tav	SYSCLK ↑ to address valid (Note 1)			18	ns
Tmsv	SYSCLK ↑ to $\overline{MS}$ ↓ (Notes 1, 6)			18	ns
Tmsh	SYSCLK ↑ to $\overline{MS}$ ↓ (Note 1)			18	ns
Tmv	SYSCLK ↑ to $\overline{MOE}$ ↓ (Note 1)			18	ns
Tmh	SYSCLK ↑ to $\overline{MOE}$ ↓ (Note 1)			18	ns
Twv	SYSCLK ↑ to $\overline{WE}$ ↓ (Note 1)			18	ns
Twh	SYSCLK ↑ to $\overline{WE}$ ↓ (Note 1)			18	ns
Tdov	SYSCLK ↑ to data out valid (Note 1)			18	ns
Tdoh	SYSCLK ↑ to data out invalid (Note 1)			18	ns
Tdis	Data in valid to $\overline{MOE}$ ↑ (SRAM) Data in valid to $\overline{CAS}$ ↑ (DRAM)	5			ns
Tdih	$\overline{MOE}$ ↑ to data in valid (SRAM) $\overline{CAS}$ ↑ to data in valid (DRAM)	0			ns
Trv	SYSCLK ↑ to $\overline{RAS}$ ↓ (Note 1)			18	ns
Trh	SYSCLK ↑ to $\overline{RAS}$ ↑ (Note 1)			18	ns
Trav	SYSCLK ↑ to row address valid (Note 1)			18	ns
Trah	SYSCLK ↑ to row address invalid (Note 1)			18	ns
Tcv	SYSCLK ↑ to $\overline{CAS}$ ↓ (Note 1)			18	ns
Tch	SYSCLK ↑ to $\overline{CAS}$ ↑ (Note 1)			18	ns
Tcav	SYSCLK ↑ to column address valid (Note 1)			18	ns
Tcah	SYSCLK ↑ to column address invalid	0			ns

BUFFER MEMORY READ/WRITE FUNCTIONAL PARAMETERS (Figures 8 through 14) (continued)

PARAMETER		CONDITIONS	TYPICAL	UNIT
Trwl	$\overline{RAS}\downarrow$ to $\overline{RAS}\uparrow$	Notes 2, 3	(RWL + 3)•T	ns
Trwh	$\overline{RAS}\uparrow$ to $\overline{RAS}\downarrow$	Notes 2, 4	(RWH + 1)•T	ns
Tcwl	$\overline{CAS}\downarrow$ to $\overline{CAS}\uparrow$	Note 2	(CWL + 1)•T	ns
Tcwh	$\overline{CAS}\uparrow$ to $\overline{CAS}\downarrow$	Notes 2, 5	(CWL + 1)•T	ns

Notes: Loading capacitance = 30 pF

Note 1: The measured delay for any of the signal indicated by this note will not vary from the measured delay of any other signal indicated by this note by more than ±2 ns.

Note 2: RWL, RWH, CWL and CWH are fields in the Buffer Manager Timing Control Register (54H). Each is a two bit field which can contain a value of 0, 1, 2, or 3. These values determine the minimum number of SYSCLK periods (T) for the associated signal width.

Note 3: The minimum width value of Trwl will be generated for refresh cycles and for any buffer memory access cycle except when multiple page mode accesses are performed. When multiple page mode accesses are performed, the width of the $\overline{RAS}$ low pulse is extended until the end of the last $\overline{CAS}$ low cycle.

Note 4: The minumum value of Trwh will be generated whenever the Buffer Manager determines that a buffer request is pending at the completion of the current memory cycle and a page mode access can not be used because the needed location is not within the current page, or a new memory request is being processed.

Note 5: The minumum value of Tcwh will be generated only between consecutive page mode accesses.

Note 6: $\overline{MS}$ will rise only if the Buffer Manager determines that no additional requests for buffer access are pending. If the Buffer Manager determines that another access is to be made, $\overline{MS}$ is kept low between the accesses for improved speed.

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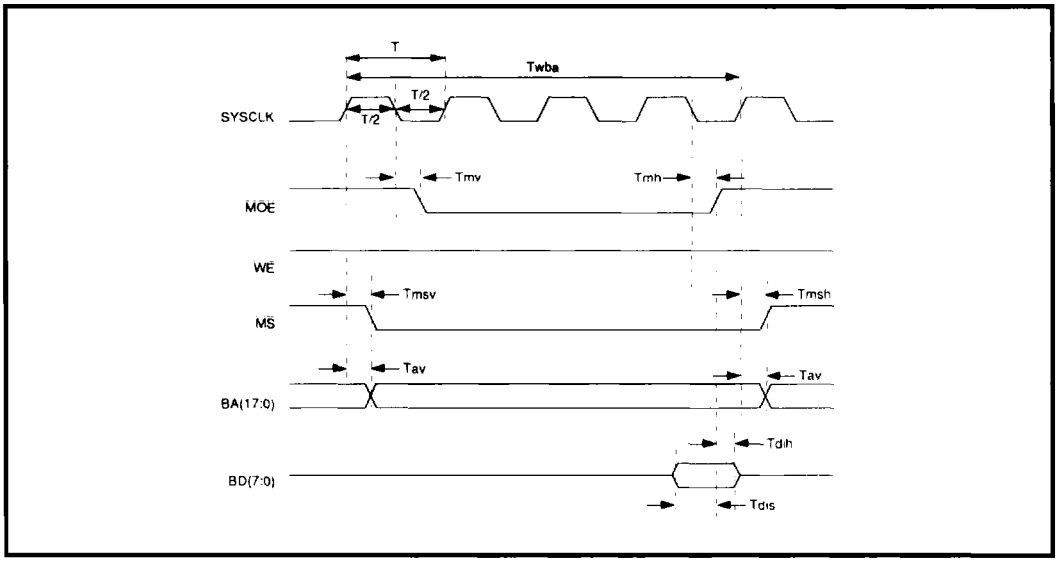

Note: Twba is a functional parameter that gives the duration of one RAM data buffer access cycle in SYSCLK periods. The value is programmed in bits 1-0 of register 54H. These examples show Twba = 4T.

FIGURE 8: SRAM Read Timing

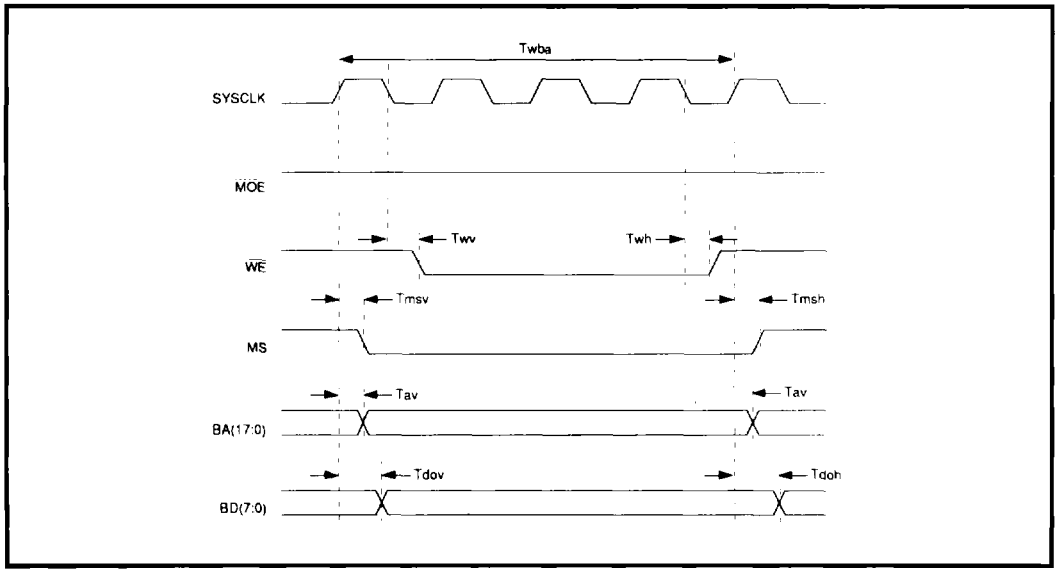

FIGURE 9: SRAM Write Timing

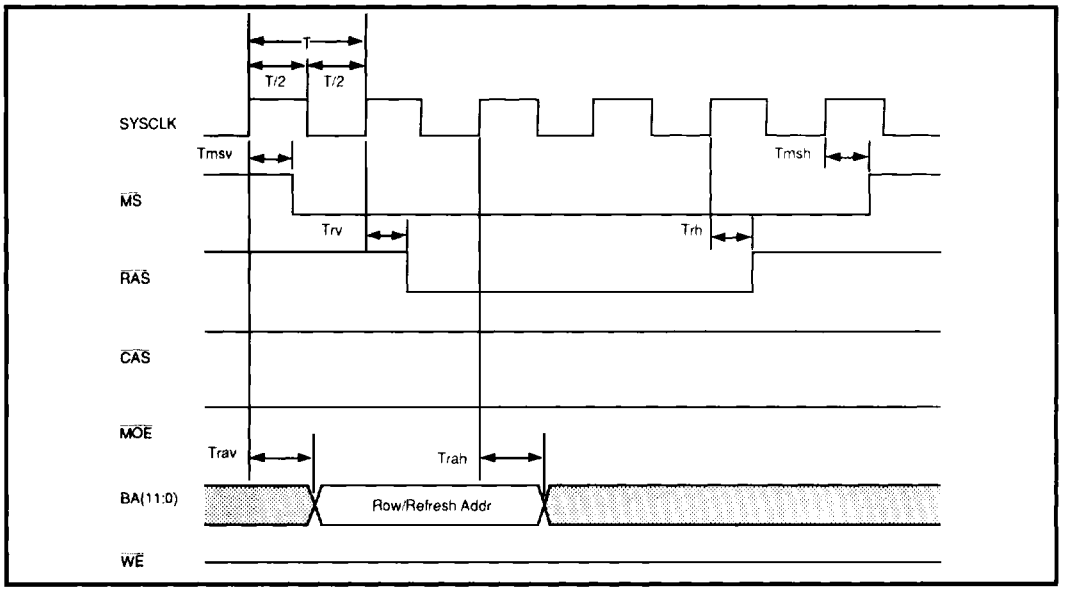

FIGURE 10: DRAM Timing, Refresh Cycle (Shown with WRL = 0)

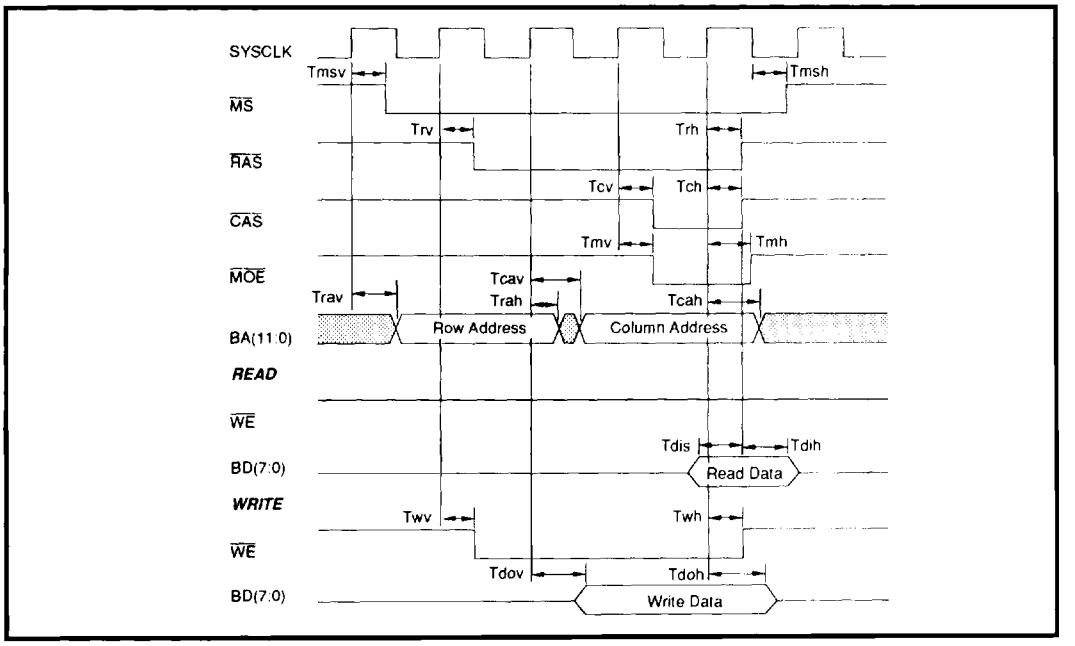

FIGURE 11: DRAM Timing, Standard Cycle (Shown with RWL = 0 and CWL = 0)

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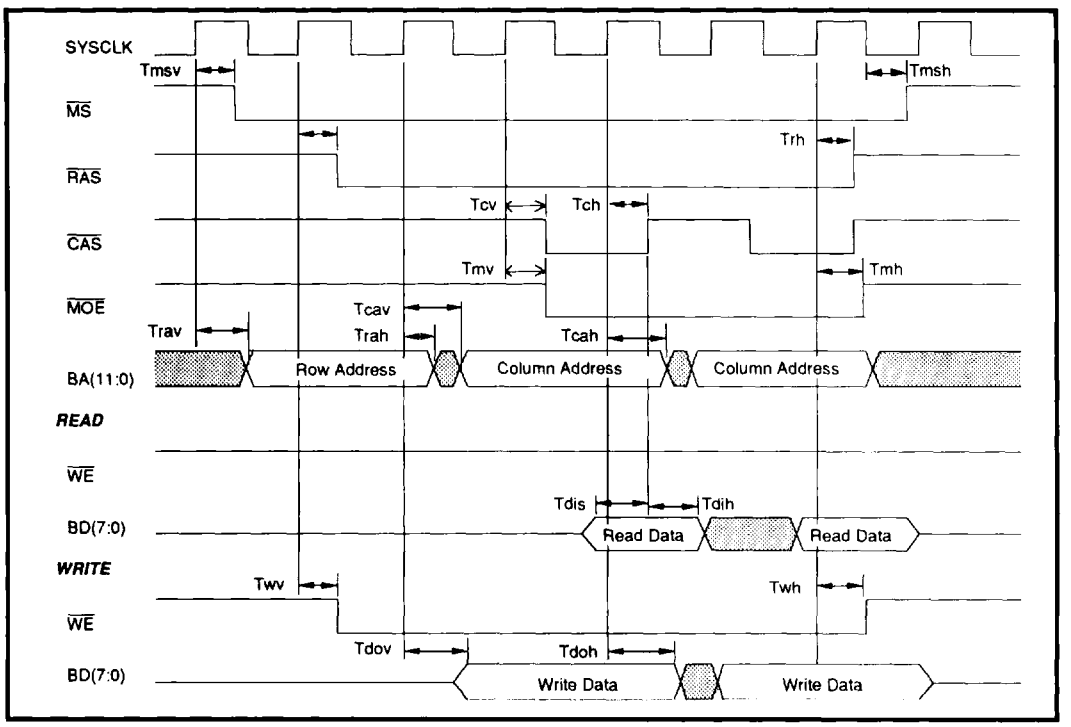

FIGURE 12: DRAM Timing, Fast Page Cycles (Shown with RWL = 0, RWH = 0, CWL = 0 and CWH = 0)

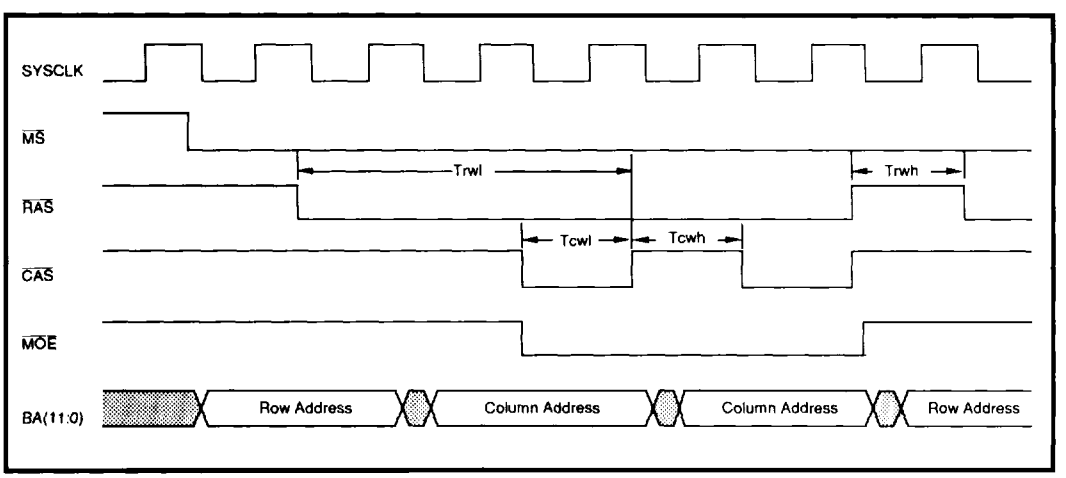

FIGURE 13: DRAM Timing (Showing the Relationship of RWL, RWH, CWL and CWH to overall timing)

ELECTRICAL SPECIFICATIONS (continued)

AT Host Interface Timing Parameters

PARAMETER		MIN	NOM	MAX	UNIT
DREQL	$\overline{DACK}$ ↓ to DREQ ↓			40	ns
DREQD	$\overline{IOR}$ ↓ or $\overline{IOW}$ ↓ to DREQ ↓			40	ns
RDTA	$\overline{IOR}$ ↓ to HD(15:0) valid			50	ns
DMASET	$\overline{DACK}$ ↓ to $\overline{IOW}$ ↓ or $\overline{IOR}$ ↓	0			ns
DMAHLD	$\overline{IOR}$ ↑ or $\overline{IOW}$ ↑ to $\overline{DACK}$ ↑	0			ns
RDHLD	$\overline{IOR}$ ↑ to HD (15:0) hi-Z	2		20	ns
WDS	HD(15:0) setup to $\overline{IOW}$ ↑	30			ns
WDHLD	HD(15:0) hold from $\overline{IOW}$ ↑	10			ns
RWPULSE	$\overline{IOR}$ or $\overline{IOW}$ low pulse width	80			ns
RWH	$\overline{IOR}$ or $\overline{IOW}$ high pulse width	50			ns
CS16L	$\overline{HCS0}$ ↓, A(2:0) ↓, A9 ↓ or $\overline{HCS1}$ ↑ to $\overline{IOCS16}$ ↓			20	ns
IOCHL	$\overline{IOR}$ or $\overline{IOW}$ ↓ to $\overline{IOCHRDY}$ ↓			25	ns
ADRSET	$\overline{HCS0}$, A(2:0), A9/$\overline{HCS1}$ setup to $\overline{IOR}$ ↓ or $\overline{IOW}$ ↓	25			ns
ADRHLD	$\overline{HCS0}$, A(2:0), A9/$\overline{HCS1}$ hold from $\overline{IOR}$ ↑ or $\overline{IOW}$ ↑	5			ns
Note: Loading capacitance = 30 pF					

Functional Specification

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
IOCHTW	$\overline{IOCHRDY}$ pulse width		0		5xBCLK	ns

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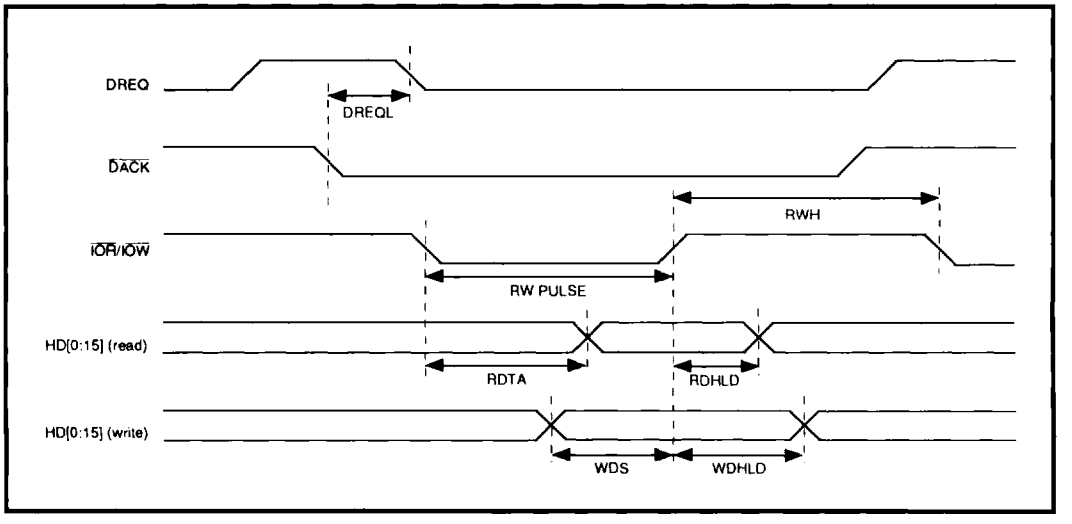


FIGURE 14: Host DMA 8-16 Bit Interface Timing (Non-demand mode)

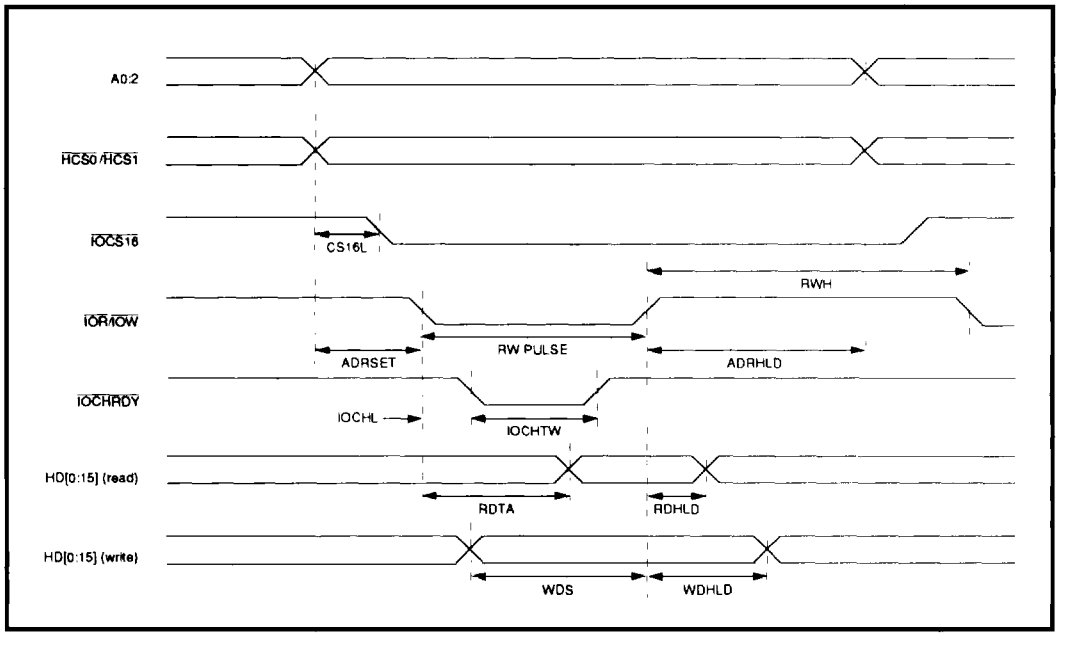


FIGURE 15: Host Programmed I/O 8-16 Bit Timing

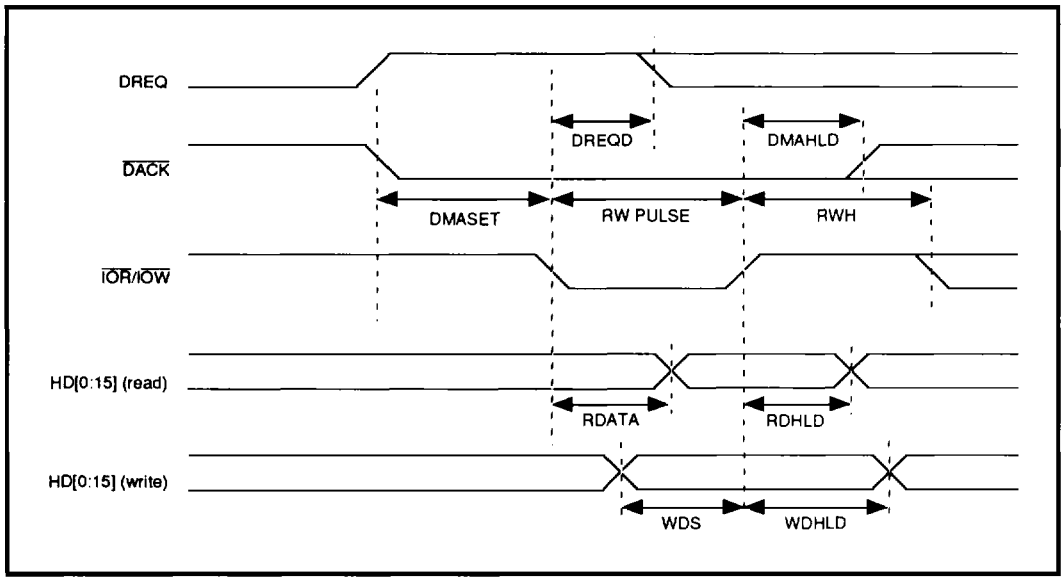


FIGURE 16: Host DMA 8/16-Bit Interface Timing (Demand Mode)

ELECTRICAL SPECIFICATIONS (continued)

RESET Assertion Timing Parameters (Figure 17)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Trpwl	$\overline{RST}$ pulse width low	NOT Power On Reset	500			ns
		Power On Reset	7.5			µs

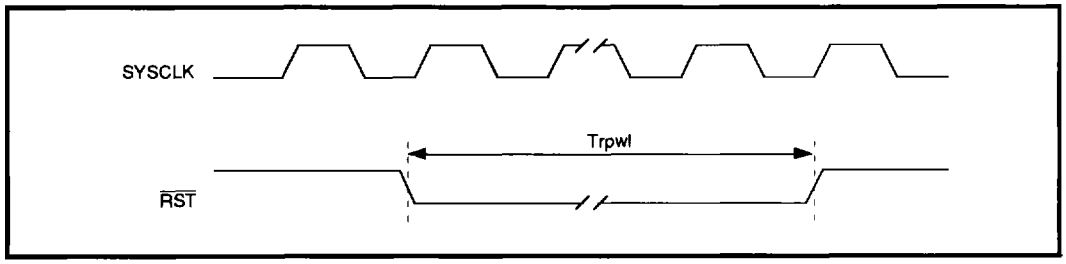
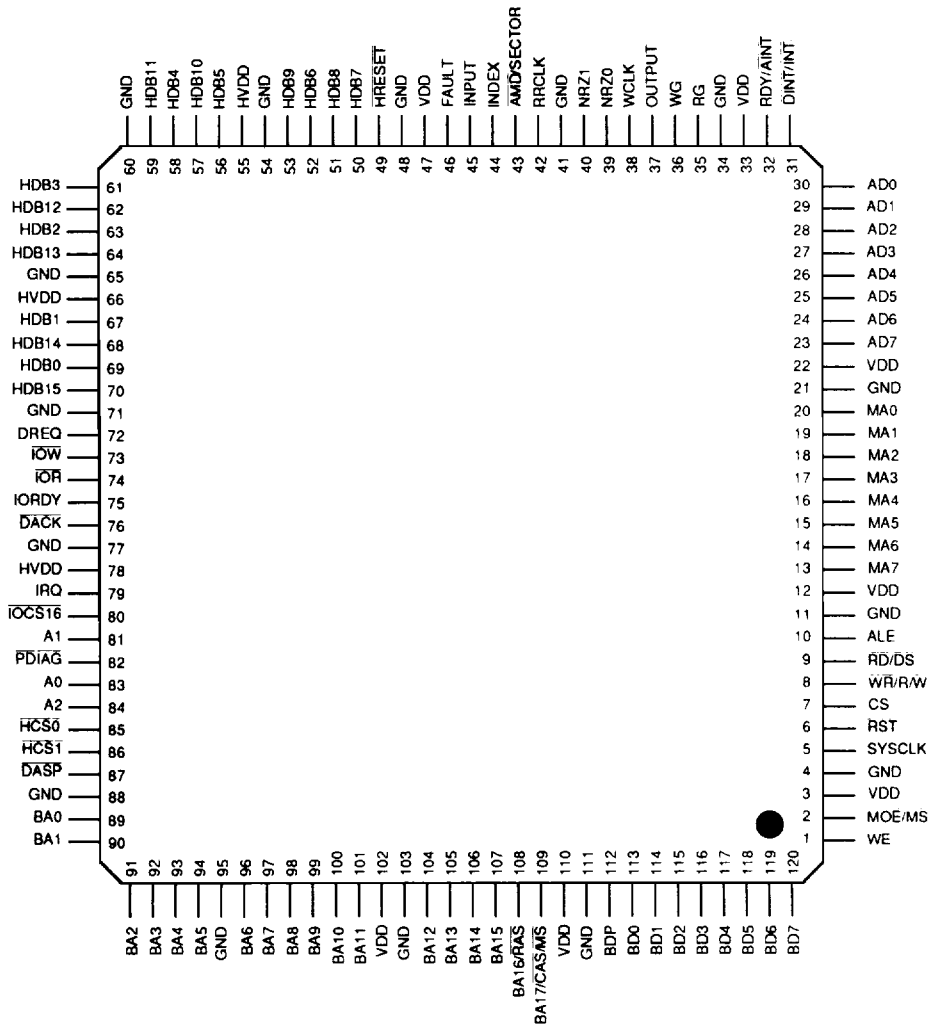


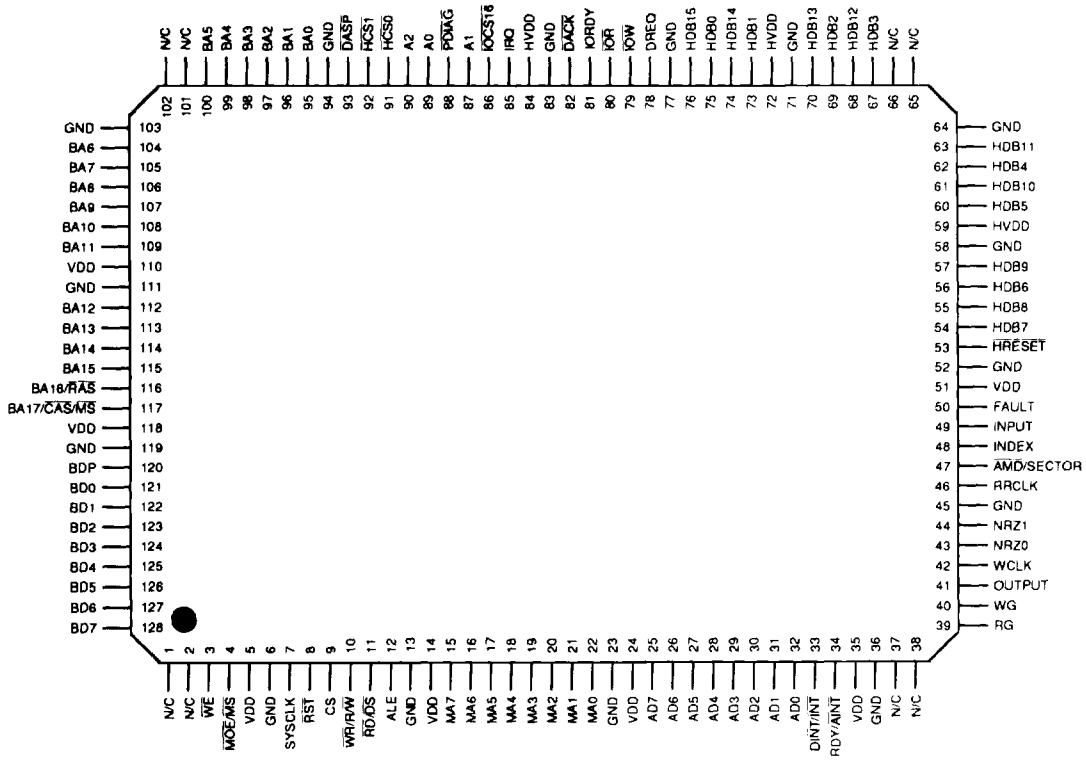
FIGURE 17: RESET Assertion Timing

SSI 32C9003
PC-AT Combo Controller
80 Mbit/s, Dual Bit NRZ Interface



120-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.



CAUTION: Use handling procedures necessary for a static sensitive component.

128-Lead QFP, TQFP

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ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
120-Lead TQFP	SSI 32C9003-CGT2	SSI 32C9003-CGT2
128-Lead TQFP	SSI 32C9003-CGT	SSI 32C9003-CGT
128-Lead QFP	SSI 32C9003-CG	SSI 32C9003-CG

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

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