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Memory Products	

# 82HS195 82HS195A 82HS195B

## 16K-bit TTL bipolar PROM

### DESCRIPTION

The 82HS195, 82HS195A and 82HS195B are field-programmable, which means that custom patterns are immediately available by following the Signetics Generic II fusing procedure. The 82HS195 devices are supplied with all outputs at logical High. Outputs are programmed to a logic Low level at any specified address by fusing a programmable matrix.

These devices include on-chip decoding and 2 Chip Enable inputs for memory expansion. They feature 3-State outputs for optimization of word expansion in bus-based organizations.

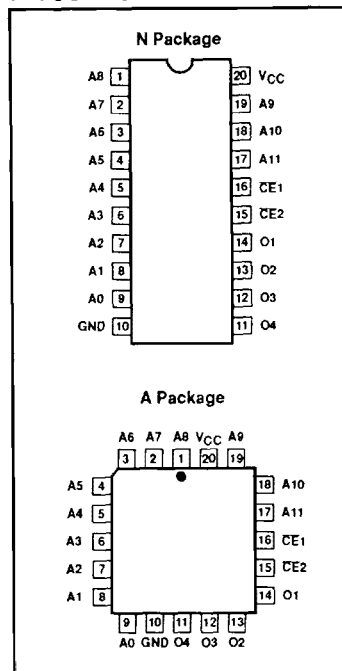
Ordering information can be found on the following page.

These devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Handbook.

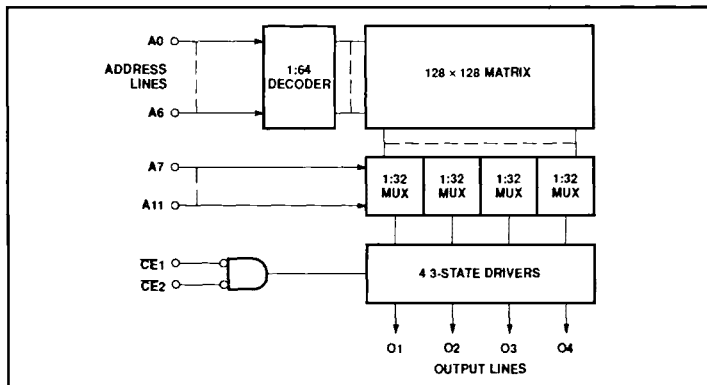
### FEATURES

- Low power dissipation: 35μW/bit typ
- Address access time:
  - N82HS195: 45ns max
  - N82HS195A: 35ns max
  - N82HS195B: 25ns max
- Input loading: -250μA max
- Two Chip Enable inputs
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are High level
- Fully TTL compatible
- Outputs: 3-State
- SMD packaging 20-Pin PLCC

### PIN CONFIGURATIONS



### BLOCK DIAGRAM



# 16K-bit TTL bipolar PROM (4096 × 4)

## 82HS195 / 82HS195A / 82HS195B

### ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Plastic Dual-In-Line 300mil-wide	N82HS195 N, N82HS191A N, N82HS195B N
20-Pin Plastic Leaded Chip Carrier 350mil-square	N82HS195 A, N82HS195A A, N82HS195B A

### ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	+7.0	$V_{DC}$
$V_{IN}$	Input voltage	+5.5	$V_{DC}$
$V_O$	Output voltage Off-State	+5.5	$V_{DC}$
$T_{amb}$	Operating temperature range	0 to +75	°C
$T_{stg}$	Storage temperature range	-65 to +150	°C

### DC ELECTRICAL CHARACTERISTICS

 $0^{\circ}\text{C} \leq T_{amb} \leq +75^{\circ}\text{C}, 4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$ 

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1,2</sup>	LIMITS			UNIT
			Min	Typ <sup>3</sup>	Max	
<b>Input voltage</b>						
$V_{IL}$	Low <sup>4</sup>	$I_{IN} = -12\text{mA}$	2.0		0.8	V
$V_{IH}$	High <sup>4</sup>					
$V_{IC}$	Clamp					
<b>Output voltage</b>						
$V_{OL}$	Low	$\overline{CE}1 \text{ \& \ } \overline{CE}2 = \text{Low}$	2.4		0.45	V
$V_{OH}$	High	$I_{OUT} = 16\text{mA}$ $I_{OUT} = -2.0\text{mA}$				
<b>Input current</b>						
$I_{IL}$	Low	$V_{IN} = 0.45\text{V}$			-250	$\mu\text{A}$
$I_{IH}$	High	$V_{IN} = 5.25\text{V}$				
<b>Output current</b>						
$I_{OZ}$	Hi-Z state	$\overline{CE}1 \text{ \& \ } \overline{CE}2 = \text{High}, V_{OUT} = 0.5\text{V}$	-15		-40	$\mu\text{A}$
$I_{OS}$	Short circuit <sup>5</sup>	$\overline{CE}1 \text{ \& \ } \overline{CE}2 = \text{High}, V_{OUT} = 5.5\text{V}$				
		$\overline{CE}1 \text{ \& \ } \overline{CE}2 = \text{Low}, V_{OUT} = 0\text{V}, \text{High stored}$				
<b>Supply current<sup>6</sup></b>						
$I_{CC}$		$V_{CC} = 5.25\text{V}$		120	145	mA
<b>Capacitance</b>						
$C_{IN}$	Input	$\overline{CE}1 \text{ \& \ } \overline{CE}2 = \text{High}, V_{CC} = 5.0\text{V}$			5	pF
$C_{OUT}$	Output	$V_{IN} = 2.0\text{V}$ $V_{OUT} = 2.0\text{V}$				

#### NOTES:

- All voltage values are with respect to network ground terminal.
- Positive current is defined as into the terminal referenced.
- Typical values are at  $V_{CC} = 5\text{V}$ ,  $T_{amb} = +25^{\circ}\text{C}$ .
- Measured with one output switching from a Logic "1" to a Logic "0".
- Duration of the short circuit should not exceed 1 second.
- Measured with all inputs grounded and all outputs open.

# 16K-bit TTL bipolar PROM (4096 × 4)

## 82HS195 / 82HS195A / 82HS195B

### AC ELECTRICAL CHARACTERISTICS

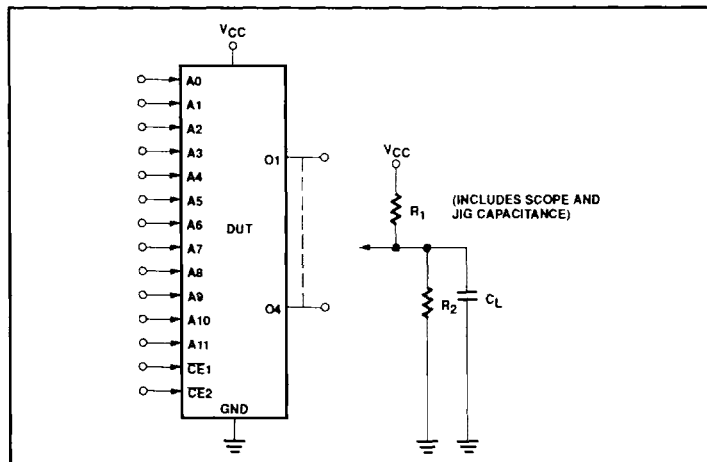
$R_1 = 470\Omega$ ,  $R_2 = 1k\Omega$ ,  $C_L = 30pF$ ,  $0^\circ C \leq T_{amb} \leq +75^\circ C$ ,  $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	82HS195			82HS195A			82HS195B			UNIT
				Min	Typ <sup>1</sup>	Max	Min	Typ <sup>1</sup>	Max	Min	Typ <sup>1</sup>	Max	
<b>Access time<sup>2</sup></b>													
$t_{AA}$		Output	Address		35	45		25	35		20	25	ns
$t_{CE}$		Output	Chip Enable		20	25		15	20		10	15	ns
<b>Disable time<sup>3</sup></b>													
$t_{CD}$		Output	Chip Disable		20	25		15	20		10	15	ns

**NOTES:**

1. Typical values are  $V_{CC} = 5V$ ,  $T_{amb} = +25^\circ C$ .
2. Tested at an address cycle time of  $1\mu s$ .
3. Measured at a delta of 0.5V from Logic Level with  $R_1 = 750\Omega$ ,  $R_2 = 750\Omega$  and  $C_L = 5pF$ .

### TEST LOAD CIRCUIT



### VOLTAGE WAVEFORM

