FUJITSU

1M x 8 DRAM MODULE

MB85231-10
MB85231-12

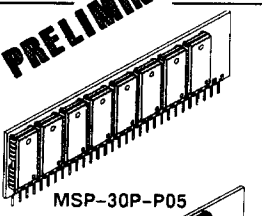
July 1988
Edition 1.0

1,048,576 x 8 BIT DYNAMIC RANDOM ACCESS MEMORY MODULE

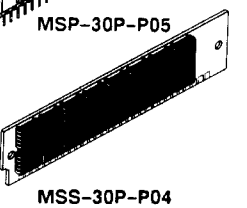
The Fujitsu MB85231 is a fully decoded, dynamic CMOS random access memory module with eight MB81C1001, in 26-pin SOJ packages, and eight .22μF decoupling capacitor under the each memory, mounted on a 30-pin SIP or a 30-pad SIMM module. Organized as 1,048,576 x 8-bit words, the MB85231 PCB module is optimized for those applications requiring high density and large memory storage capability. The operation and electrical characteristics of the MB85231 are the same as the MB81C1001 devices which feature a Nibble mode operation.

- 1,048,576 x 8 DRAM, 30-pin SIP and SIMM
- RAS access time (t_{RAC}):
  100 ns max. (MB85231-10)
  120 ns max. (MB85231-12)
- Cycle time (t_{RC}):
  180 ns min. (MB85231-10)
  210 ns max. (MB85231-12)
- Column access time (t_{CAC}):
  30 ns max. (MB85231-10)
  35 ns max. (MB85231-12)
- Nibble mode cycle time (t_{NC}):
  50 ns max. (MB85231-10)
  55 ns max. (MB85231-12)
- Dual +5V supply, ±10% tolerance
- Low power:
  Active = 2640 mWmax. (MB85231-10)
  2200mW max. (MB85231-12)
  Standby = 44 mWmax. (CMOS level)
- Refresh:
  - 8.2 ms / 512 refresh cycle
  - "$\overline{RAS}$-only", "$\overline{CAS}$-before-$\overline{RAS}$" and "Hidden" refresh capability
- Nibble Mode Read and Write capability
- Leaded and Leadless type are available.
- JEDEC standard (30 pin SIP) pin assignment

PRELIMINARY



MSP-30P-P05



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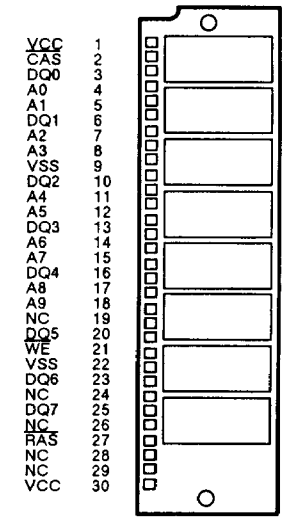
PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7	V
Storage temperature	T_{STG}	-55 to 125	°C
Power dissipation	P_D	8.0	W
Short circuit output current	—	50	mA

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 – BLOCK DIAGRAM

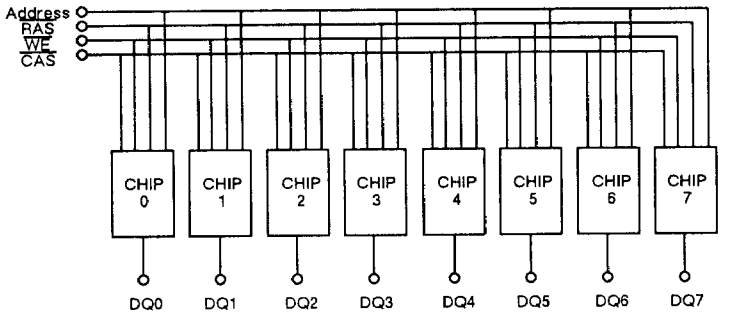
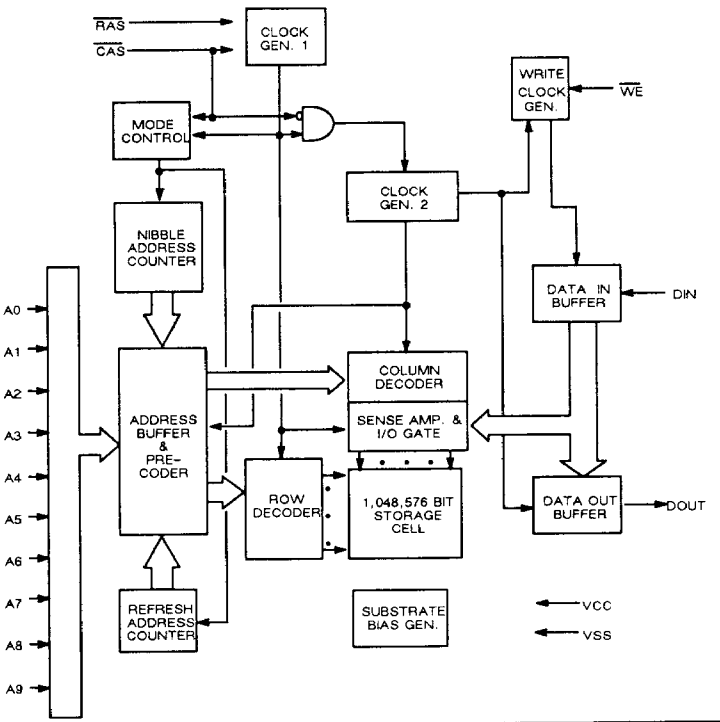


Fig. 2 – BLOCK DIAGRAM FOR EACH CHIP



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CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9	C_{IN1}	—	56	pF
Input Capacitance, $\overline{RAS}$	C_{IN2}	—	47	pF
Input Capacitance, $\overline{CAS}$	C_{IN3}	—	49	pF
Input Capacitance, $\overline{WE}$	C_{IN4}	—	46	pF
I/O Capacitance, DQ0 to DQ7	C_{DQ}		14	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to Vss)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V
Input High Leve, all Inputs	V_{IH}	2.4		6.5	V
Input Low Level, all inputs all DQs	V_{IL1} V_{IL2}	-2.0 -1.0*1		0.8 0.8	V V
Operating Temperature Range	T_A	0	25	70*2	°C

Note: *1 The device will withstand undershoots to the -2.0V level with a maximum pulse width of 20ns at the -1.5V level.
*2 Maximum ambient temperature is permissible under certain conditions.

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DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC}=min.)	MB85231-10	I_{CC1}			480	mA
	MB85231-12				400	
STANDBY CURRENT Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	TTL level	I_{CC2}			16	mA
	CMOS level				8	
REFRESH CURRENT 1 Average Power Supply Current ($\overline{CAS}$=V_{IH}; $\overline{RAS}$=min cycling)	MB85231-10	I_{CC3}			440	mA
	MB85231-12				360	
NIBBLE MODE CURRENT Average Power Supply Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$=min cycling)	MB85231-10	I_{CC4}			320	mA
	MB85231-12				264	
REFRESH CURRENT 2 Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC}=min)	MB85231-10	I_{CC5}			440	mA
	MB85231-12				360	
INPUT LEAKAGE CURRENT		I_{IL}	-30		30	µA
OUTPUT LEAKAGE CURRENT		I_{OL}	-10		10	µA
OUTPUT HIGH LEVEL (I_{OH}=-5mA)		V_{OH}	2.4			V
OUTPUT LOW LEVEL (I_{OL}=4.2mA)		V_{OL}			0.4	V

Note: * I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

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AC CHARACTERISTICS

(At recommended operating conditions otherwise noted.) Notes 1, 2, 3

Parameter	NOTES	Symbol	MB85231-10		MB85231-12		Unit
			Min.	Max.	Min.	Max.	
Time Between Refresh		t_{REF}		8.2		8.2	ms
Random Read/Write Cycle Time	4	t_{RC}	180		210		ns
Access Time from $\overline{RAS}$	5,8	t_{RAC}		100		120	ns
Access Time from $\overline{CAS}$	6,8	t_{CAC}		30		35	ns
Access Time from Column Address	7,8	t_{AA}		50		60	ns
Output Data Hold Time		t_{OH}	10		10		ns
Output Buffer Turn On Delay Time		t_{ON}	5		5		ns
Output Buffer Turn Off Delay Time	9	t_{OFF}		25		25	ns
Input Transition Time		t_T	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	70		80		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	100	100000	120	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	30		35		ns
$\overline{CAS}$ to RAS Precharge Time		t_{CRP}	0		0		ns
$\overline{RAS}$ to CAS Delay Time	10,11	t_{RCD}	20	70	20	85	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	30		35		ns
$\overline{CAS}$ Hold Time		t_{CSH}	100		120		ns
Row Address Setup Time		t_{ASR}	0		0		ns
Row Address Hold Time		t_{RAH}	15		15		ns
Column Address Setup Time		t_{ASC}	0		0		ns
Column Address Setup Time		t_{CAH}	15		20		ns
$\overline{RAS}$ to Column Address Delay Time	12	t_{RAD}	20	50	20	60	ns
Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	50		60		ns
Read Command Setup Time		t_{RCS}	0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	13	t_{RRH}	0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	13	t_{RCH}	0		0		ns
Write Command Setup Time	14	t_{WCS}	0		0		ns
Write Command Hold Time		t_{WCH}	15		20		ns
$\overline{WE}$ Pulse Width		t_{WP}	15		20		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	25		30		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	20		25		ns
DIN Setup Time		t_{DS}	0		0		ns
DIN Hold Time		t_{DH}	15		20		ns
Nibble Mode Read/Write Cycle Time		t_{NC}	50		55		ns
Access Time from $\overline{CAS}$ Precharge	8,15	t_{CPA}		60		55	ns
Nibble Mode $\overline{CAS}$ Precharge Time		t_{NCP}	15		15		ns

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AC CHARACTERISTICS (Continued)

(At recommended operating conditions otherwise noted.) Notes 1, 2, 3

Parameter / NOTES	Symbol	MB85230-10		MB85230-12		Unit
		Min.	Max.	Min.	Max.	
$\overline{CAS}$ Precharge Time($\overline{CAS}$-before $\overline{RAS}$ refresh)	t_{CPN}	15		15		ns
$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)	t_{RPC}	0		0		ns
$\overline{CAS}$ Setup Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{CSR}	0		0		ns
$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{CHR}	15		20		ns

NOTES;

1. An initial pause ($\overline{RAS}$=$\overline{CAS}$=V_{IH}) of 200 µs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T=5ns
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. The minimum cycle time depends upon the ambient temperature and cooling condition. See Fig. 3.
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 4 and 5.
6. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA}-t_{CAS}-t_T$, access time is t_{CAC}.
7. If $t_{RAD} \geq t_{RAD}$ (max), $t_{ASC} \geq t_{AA}-t_{CAS}-t_T$, access time is t_{AA}.
8. Measured with a load equivalent to two TTL loads and 100 pF.
9. t_{OFF} is specified that output buffer changes to high impedance state.
10. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RAC} (max) is specifies as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAS} or t_{AA}.
11. t_{RCD} (min) = t_{RAH} (min) +2t_T + t_{ASC} (min).
12. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. t_{WCS} is specified as a reference point only. If tWCS(min),the DQn pins will maintain impedance(High-Z) state throughout the entire cycle.
15. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from V_{IL} to V_{IH}.). Therefore, If t_{CP} is short, t_{CAC} is longer than t_{CAC} (max).

Fig. 3 - MB85230 DERATING CURVE (Normal Cycle)

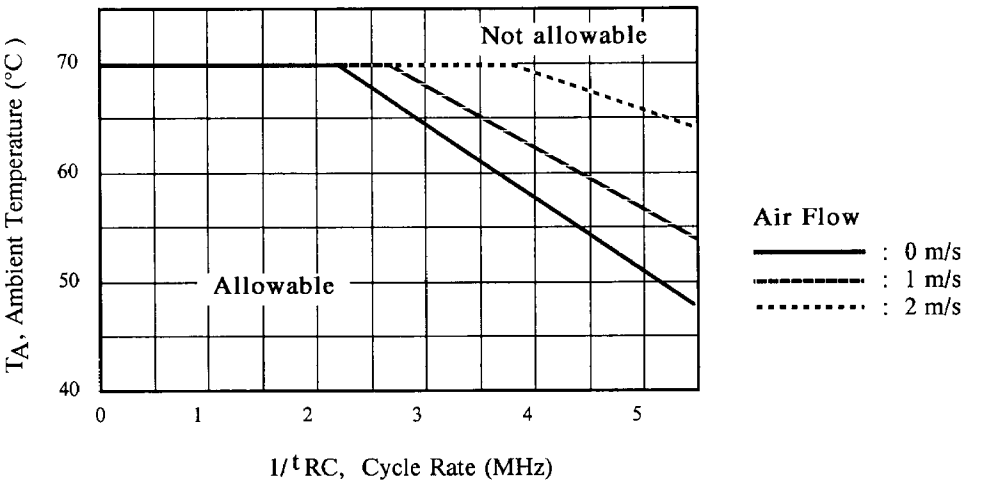


Fig. 4 - tRAC vs tRCD

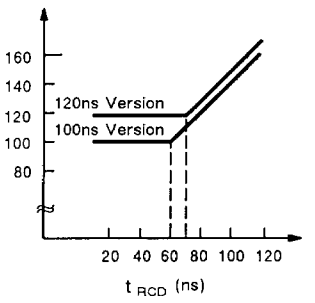
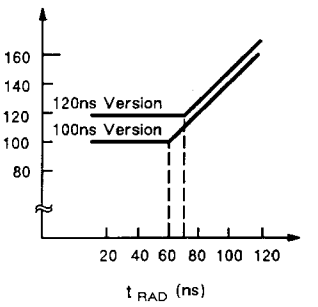


Fig. 5 - tRAC vs tRAD



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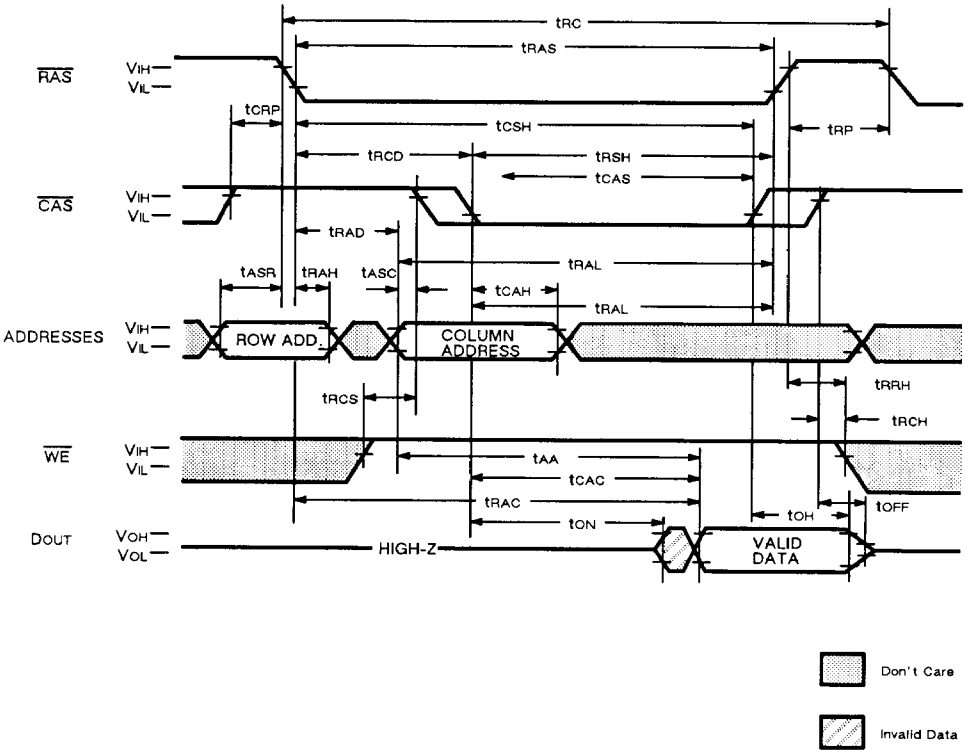
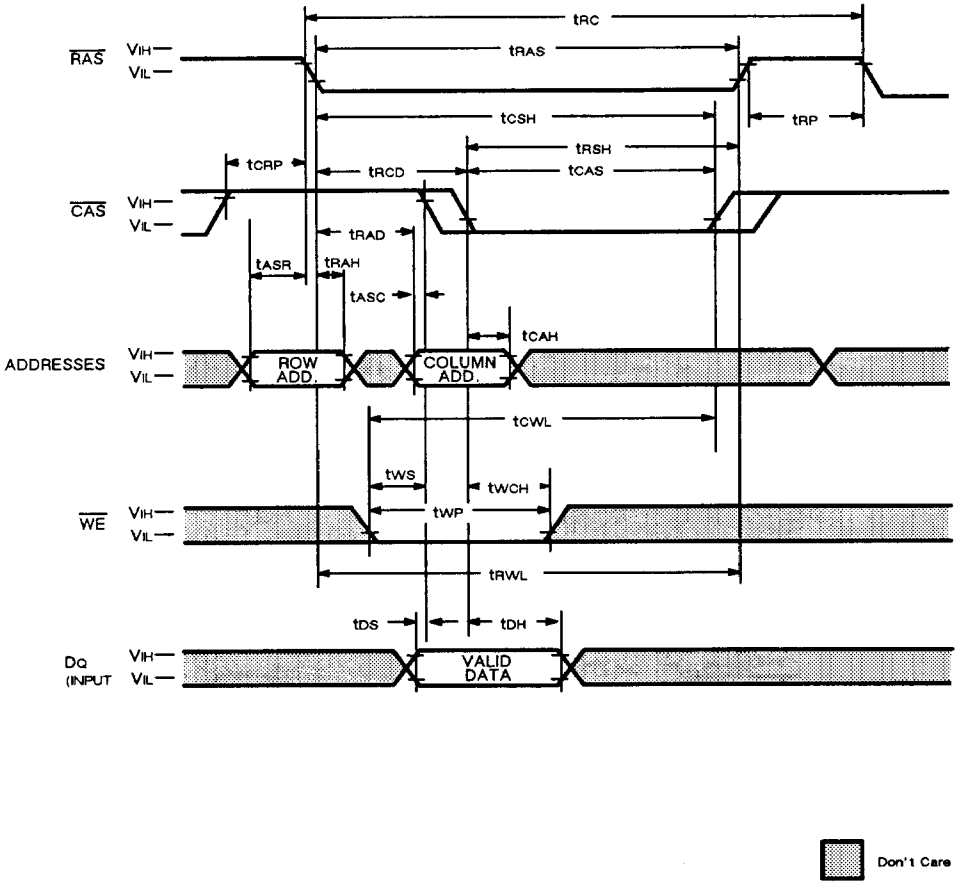
READ CYCLE


tRC
tRAS
RAS
VIH
VIL
tCRP
tCSH
tRP
tRCD
tRSH
tCAS
CAS
tRAD
tASR
tRAH
tASC
tRAL
tCAH
ADDRESSES
ROW ADD.
COLUMN ADDRESS
tRCS
tRRH
tRCH
WE
tAA
tCAC
tRAC
tON
tOH
tOFF
DOUT
VOH
VOL
HIGH-Z
VALID DATA
Don't Care
Invalid Data

WRITE CYCLE (Early Write)



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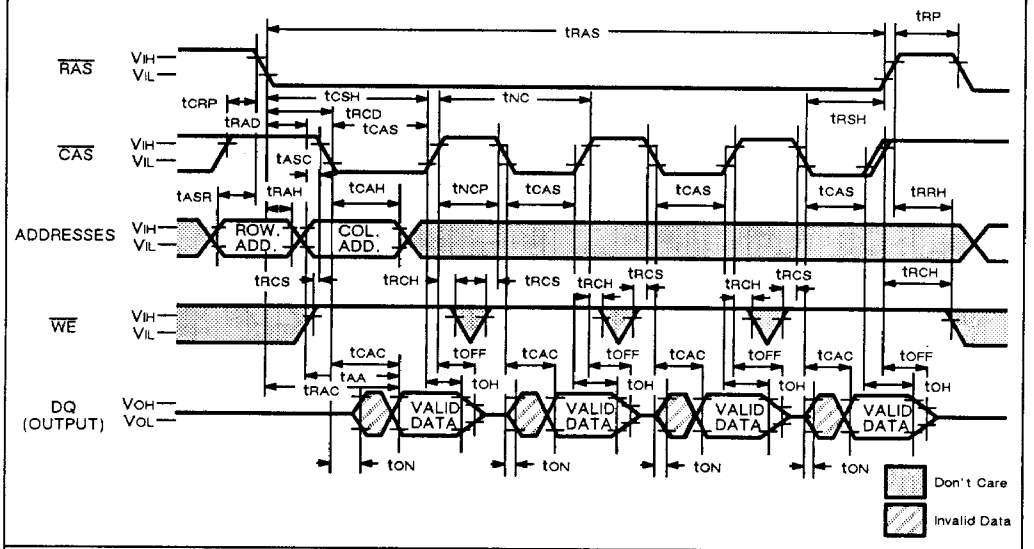
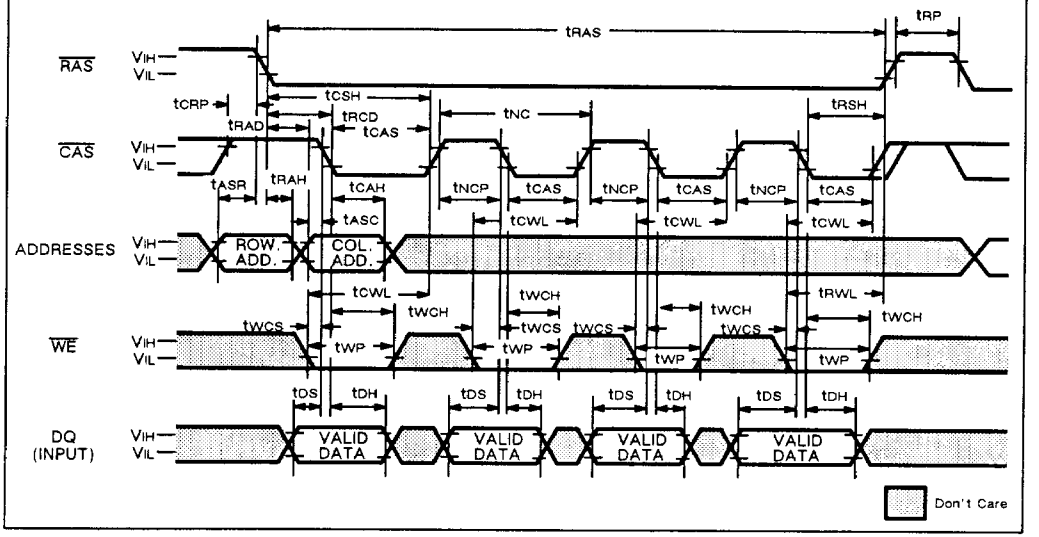
NIBBLE MODE READ CYCLE



NIBBLE MODE WRITE CYCLE



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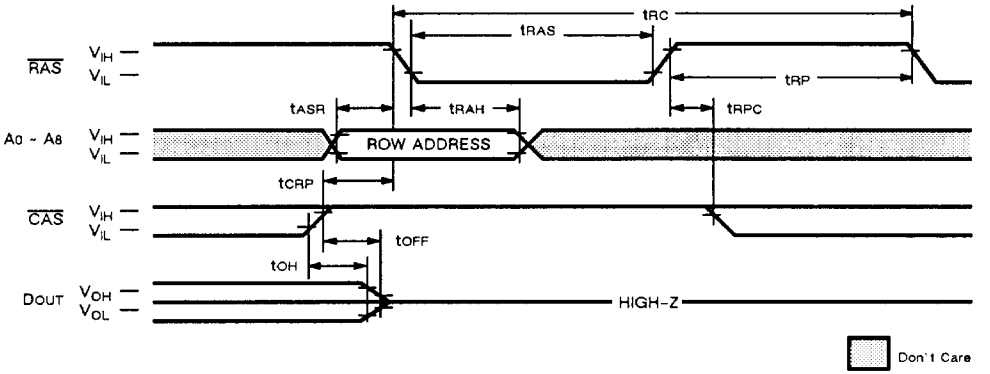
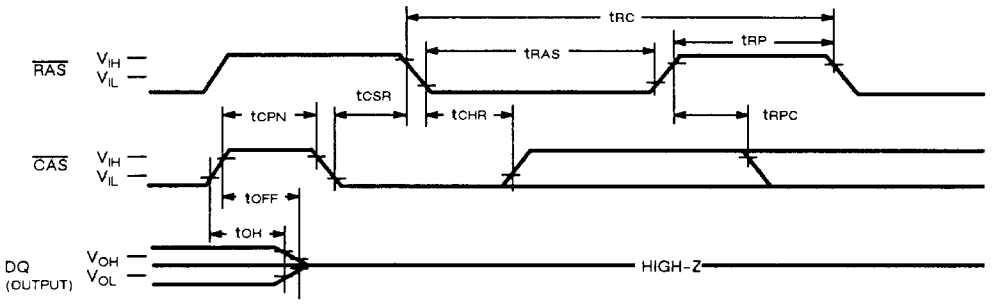
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{WE}$, DQ (Input) = Don't Care, A9=VIH or VIL



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: ADDRESS, $\overline{WE}$, DQ (Input) = Don't Care



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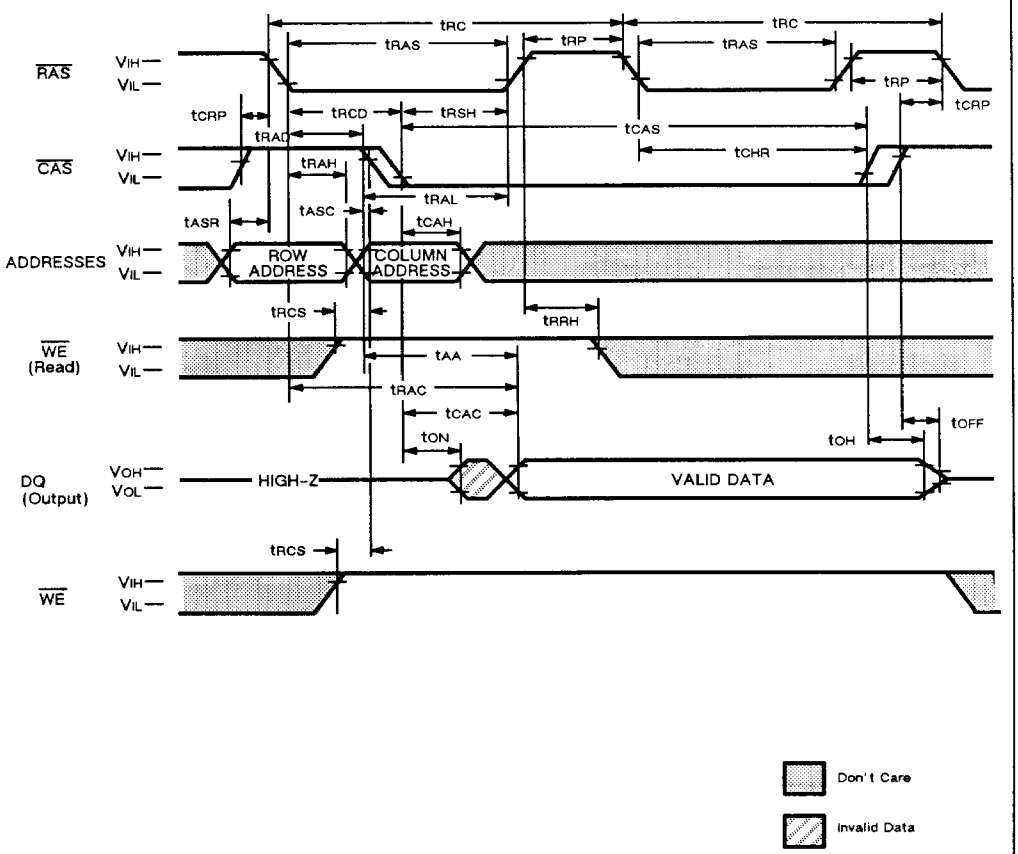
HIDDEN REFRESH CYCLE



DESCRIPTION

Block Analysis:
As shown in Fig. 1 and Fig. 2, the MB85231 is composed of eight MB81C1001, and the memory selection of the each MB81C1001 consists of a 1024-by-1024 cell matrix.
Operational modes of this module are specified below.

Address Inputs:
A total of twenty binary input address bits are required to decde any 8-bit of the 8,388,608 storage cells within the MB85231. Ten row address bits are established on the address input pins (A_0 to A_9) and latched with the Row Address Strobe, $\overline{RAS}$. The ten column address bits are established on the address input pins(A_0 to A_9) and latched with the Column Address Strobe, $\overline{CAS}$. All row and column addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. Since the flow through type address latches are used, address information at address pins are automatically latched as column address after t_{RAH} (min)+ t_T. If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{CAC} or t_{AA} whichever occurs later.

Write Enable:
Read or Write mode is selected with the $\overline{WE}$ inputs. A high on $\overline{WE}$ selects read cycle and low selects write mode.

Data Input/Output:

1. Data Input;
   In write cycle, the 8-bit data is written into the MB85231 during write cycle through each DQ pins. Each input data is strobed and latched by falling edge of $\overline{CAS}$, and $\overline{WE}$ must be brought to V_{IL} before falling edge of $\overline{CAS}$, data input strobed by $\overline{CAS}$, and setup and hold times are referenced to $\overline{CAS}$.

2. Data Output;
   The output buffers on each chip are three state TTL compatible with a fan out of 2 TTL loads. Output data has the same porality as input data. The outputs are in high impedance state until $\overline{CAS}$ is brought low. In a read cycle, the output becomes valid within t_{CAC} or t_{AA} whichever occurs later after falling edge of $\overline{CAS}$. The data output remans valid until $\overline{CAS}$ returns to high.

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Read Cycle:
The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$=V_{IL} and keeping $\overline{WE}$=V_{IH} throughout the cycle. The row and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The output data is remain valid with $\overline{CAS}$=V_{IL}, i.e., if $\overline{CAS}$ goes V_{IH}, the data becomes invalid with t_{OH}. The access time is determined by $\overline{RAS}$ (t_{RAC}), $\overline{CAS}$(t_{CAC}), or Column address input (t_{AA}). If t_{RCD}($\overline{RAS}$ to $\overline{CAS}$ delay time) is greater than the specification, the access time is t_{CAC}. If t_{RAD} is greater than the specification, the access time is t_{AA}.

Write Cycle:
The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$. The 8-bit data on DQ pins are latched with the falling edge of $\overline{CAS}$ and written into memory. In addition, during write cycle, t_{RWL}, t_{CWL}, and t_{RAL} must be satisfied the specifications.

Nibble Mode:
The nibble mode is a 4-bit serial access mode allows high speed addressing with $\overline{CAS}$ during read or write cycle. The each cell accessed dring nibble mode are determined by the combination of row and column address on A9(RA9 and CA9). The two address are used to select one of four bits for initial access. After the first bits is accessed by normal read or write mode, the remaining nibble bits can be accessed by toggling $\overline{CAS}$, high to row level. Toggling $\overline{CAS}$ causes RA9 and CA9 to be increased internally while all other address bits are held constant and makes the next nibble bit available for access.
Refer to Table 1 for nibble mode address sequence.
If more than four bits are accessed during nibble mode, the address sequence will begin to repeat.

1. Nibble Mode Read Cycle:
   The nibble mode write cycle is also executed after normal cycle with holding $\overline{RAS}$=V_{IL}, applying column address and $\overline{CAS}$, and keeping $\overline{WE}$=V_{IH}. Since all address during nibble mode cycle is latched by normal cycle, the read operation is simplified.

2. Nibble Mode Read Cycle:
   The nibble mode write cycle is also executed by the same manner as nibble mode read cycle except for the state of $\overline{WE}$. The data on each DQ is latched with the falling edge of $\overline{CAS}$ and written into the memory.

DESCRIPTION (Continued)

Refresh:

The refresh of DRAM is executed by normal read and write cycle, i.e., the cells on each one row line, A_0 through A_8 except for A_9, are refreshed by one of two cycles. Each 512 row address must be refreshed every 8.2ms period. During the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and re-write to the cell. The MB85230 also has three types of refresh modes, $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, and Hidden refresh.

1. **$\overline{RAS}$-only Refresh;**
   The $\overline{RAS}$-only refresh is executed by keeping $\overline{RAS}$=V_{IL} and keeping $\overline{CAS}$=V_{IH} through the cycle. The row address to be refreshed is latched with the falling edge of $\overline{RAS}$. During this refresh, the DQ pins are kept high impedance state.

2. **$\overline{CAS}$-before-$\overline{RAS}$ Refresh;**
   The $\overline{CAS}$-before-$\overline{RAS}$ refresh is executed by bringing $\overline{CAS}$=V_{IL} before $\overline{RAS}$. By this combination, the MB85231 executes $\overline{CAS}$-before-$\overline{RAS}$ refresh. The row address input is not necessary because it is generated internally.

3. **Hidden Refresh;**
   The hidden refresh is execute dby keeping $\overline{CAS}$=V_{IL} to next cycle during read mode, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{CAS}$ is kept V_{IL} continuously from previous cycle, followed refresh cycle should be $\overline{CAS}$-before-$\overline{RAS}$ refresh.

Table 1 — NIBBLE MODE ADDRESS SEQUENCE

Sequence	Nibble bit	Row address	RA9	Column address	CA9	
$\overline{RAS}$/$\overline{CAS}$ (normal mode)	1	101010101	0	101010101	0	Input address
Toggling $\overline{CAS}$ (nibble mode)	2	101010101	1	101010101	0	Generated
Toggling $\overline{CAS}$ (nibble mode)	3	101010101	0	101010101	1	internally
Toggling $\overline{CAS}$ (nibble mode)	4	101010101	1	101010101	1	
Toggling $\overline{CAS}$ (nibble mode)	1	101010101	0	101010101	0	Sequence repeats

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FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data I/O	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column		
Standby	V_{IH}	V_{IH}	X	X	X	High-Z	Cells are not refreshed.
Read (Normal)	V_{IL}	V_{IL}	V_{IH}	Valid	Valid	Output Valid	$t_{RCS} \geq t_{RCS}$ (min)
Read (Fast Page)	V_{IL}	V_{IL}	V_{IH}	Valid	Valid	Output Valid	$t_{RCS} \geq t_{RCS}$ (min) Cells are not refreshed.
Write (Normal)	V_{IL}	V_{IL}	V_{IL}	Valid	Valid	Input Valid	$t_{WCS} \geq t_{WCS}$ (min)
Write (Fast Page)	V_{IL}	V_{IL}	V_{IL}	Valid	Valid	Input Valid	$t_{WCS} \geq t_{WCS}$ (min) Cells are not refreshed.
$\overline{RAS}$-only Refresh	V_{IL}	V_{IH}	X	Valid	X	High-Z	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh	V_{IL}	V_{IL}	X	X	X	High-Z	$t_{CRS} \geq t_{CRS}$ (min)
Hidden Refresh	V_{IL} *	V_{IL}	V_{IH}	X	X	Output Valid	Previous data is kept.

Note: X: Don't Care
*: $\overline{RAS}$ puts V_{IH} at once.

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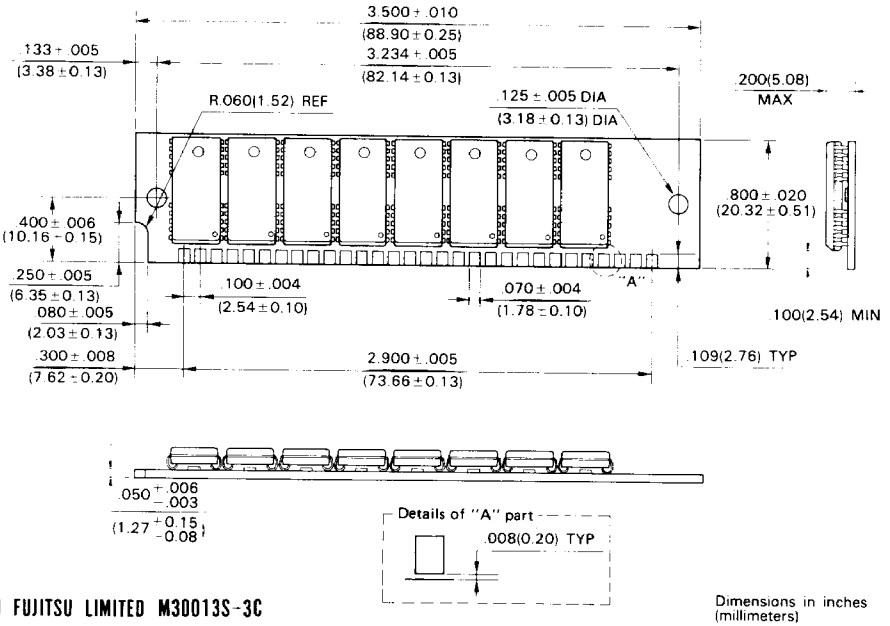
PACKAGE DIMENSIONS

(Suffix: PJPB)

30-LEAD PLASTIC MODULE (SOCKET TYPE)

(Case No. : MSS-30P-P04)



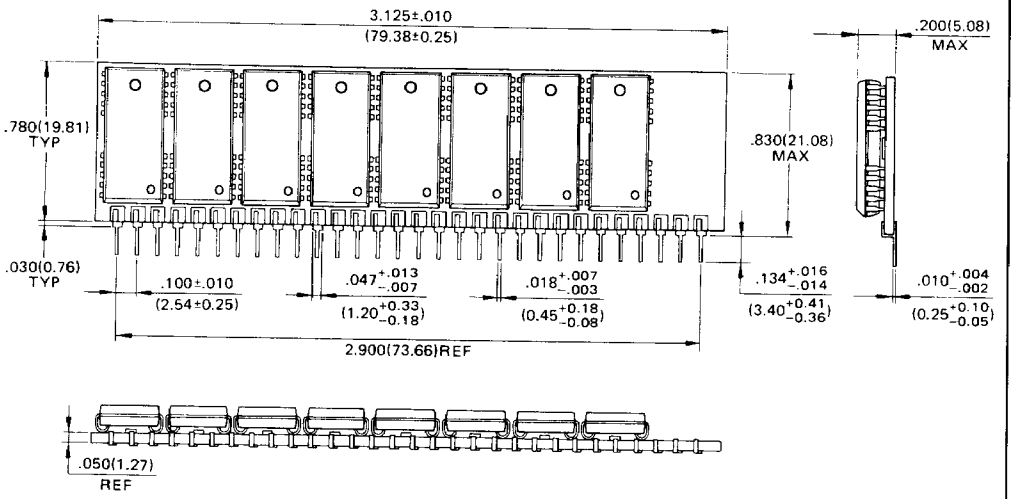
Dimensions in inches
(millimeters)

5

PACKAGE DIMENSIONS (Continued)

(Suffix: PJPS)

30-LEAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSP-30P-P05)



Dimension in inches (millimeters)

5