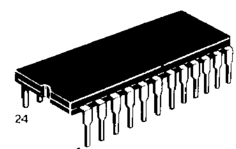
MC10315L
MC10317L

MOTOROLA

Advance Information

HIGH SPEED 7-BIT ANALOG-TO-DIGITAL FLASH CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 623-05

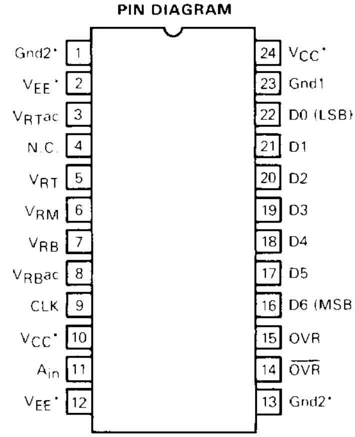
SEVEN-BIT PARALLEL HIGH SPEED A/D CONVERTER (WITH OVERRANGE)

The MC10315L/MC10317L is a 7-bit high speed parallel A/D converter which employs ECL processing. The device consists of 128 parallel latched comparators across a high quality input reference network. The 128 comparator outputs are then fed to a 128-to-7 encoder and latched to the outputs which are ECL compatible. An overrange bit is provided to allow overrange sensing, or to facilitate the connection of an MC10315L and MC10317L in parallel to produce an 8-bit A/D converter. The MC10315L and MC10317L are identical devices except for the method of overranging used, which simplifies the utilization of two 7-bit converters to produce an 8-bit conversion. (See ordering information and technical description.)

Applications include video display and radar signal processing, high speed instrumentation, and TV broadcast video encoding.

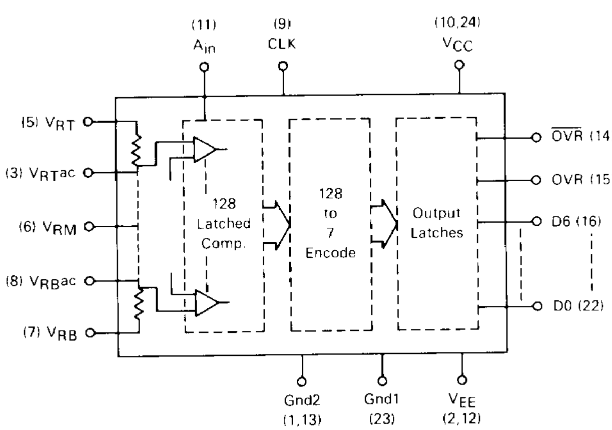
- 7-Bit Resolution/8-Bit Accuracy Plus Overrange
- Direct Interconnection for 8-Bit Conversion
- 15 MHz Sampling Rate
- Wide Range of Input Voltage: ±2.0 Volts
- Low Input Capacitance: ≤70 pF
- 1.2 Watt Power Dissipation
- No Sample and Hold Required for Video Bandwidth Signals
- Standard 24-Pin Package

PIN DIAGRAM



*V_{CC}, V_{EE} and Gnd2 are each available on two pins. Interconnections for the respective function are made on chip. To minimize I•R drops on chip and in the bonding wires, utilization of both pins for each function is recommended.

MC10315L/MC10317L DEVICE/APPLICATION CONFIGURATION



ORDERING INFORMATION**			
	Overrange Function		
	Analog Input	Logic Levels	
Device	Condition	OVR Bit	D0-D6 Bits
MC10315L	Overranged	High	High
MC10317L	Overranged	High	Low

**For information regarding an evaluation board, contact Linear Marketing.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted (Note 1))

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	+7.0 -8.0	Vdc Vdc
Ground 1	Gnd1	-0.8, +3.0	Volts
Clock Input Voltage	V_{CLK}	0 to V_{EE}	Volts
Analog Inputs: A_{in}, V_{RT}, V_{RB} $\lvert V_{RT} - V_{RB} \rvert$		 +2.5 2.5	Volts
Digital Output Source Current (per Output)	I_{source}	30	mA
Power Dissipation Free Air Convection Air Flow ≥ 500 Lfpm	$P_{D(max)}$	 2.8 4.0	W
Operating Temperature	T_A	0 to +70	°C
Junction Temperature	T_J	165	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Air Free Air Convection Air Flow ≥ 500 Lfpm	$R_{\theta JA}$	 50 35	°C/W

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ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -5.2 Vdc, T_A = 25°C unless otherwise noted (Note 1))

Characteristic	Symbol	MC10315L/MC10317L Min	Typ	Max	Unit
Resolution 0°C ≤ T_A ≤ 70°C		–	–	7	Bits
Non-Linearity fs ≤ 15 MHz, V_{RT}-V_{RB} = 2.0 V	NL	–	±0.16	–	%
Differential Non-Linearity fs ≤ 15 MHz, V_{RT}-V_{RB} = 2.0 V	DNL	–	±0.10	–	%
Offset Error V_{RT}-V_{RB} = 2.0 V Top Bottom	 V_{OSRT} V_{OSRB}	 – –	 +7.0 ±7.0	 – –	mV
Maximum Sampling Frequency 0°C ≤ T_A ≤ 70°C V_{RT}-V_{RB} = 2.0 V, No Missing Codes	fs		15	–	MHz
Aperture Delay Time	t_{ad}	–	3.0	–	ns
Aperture Uncertainty		–	80	–	ps
Data Valid Delay Time 0°C ≤ T_A ≤ +70°C	t_{vd}	–	43	–	ns
Comparator Track Delay Time 0°C ≤ T_A ≤ +70°C	t_{cd}	–	25	–	ns
Differential Phase Differential Gain fs = 14.3 MHz Unlocked NTSC or PAL Ramp Modulated with 40 IRE Color Subcarrier		– –	1.0 1.5	– –	Deg. %
Maximum Analog Input Slew Rate	SR	–	35	–	V/μs
Analog Input Bias Current V_{in} ≥ V_{RT}, 0°C ≤ T_A ≤ +70°C	I_{IB}	–	300	400	μA
Equivalent Analog Input Resistance V_{RT}-V_{RB} = 2.0 V, 0°C ≤ T_A ≤ +70°C	R_{in}	5.0	–	–	KΩ
Analog Input Capacitance V_{in} ≥ V_{RT}	C_{in}	–	70	–	pF
Reference Ladder Current V_{RT}-V_{RB} = 2.0 V	I_{ref}	24	31	47	mA
Reference Ladder Resistance (Total Resistance)	R_{ref}	–	64	–	Ω

ELECTRICAL CHARACTERISTICS (V_{CC} +5.0 Vdc, V_{EE} 5.2 Vdc, T_A 25°C unless otherwise noted (Note 1)) continued

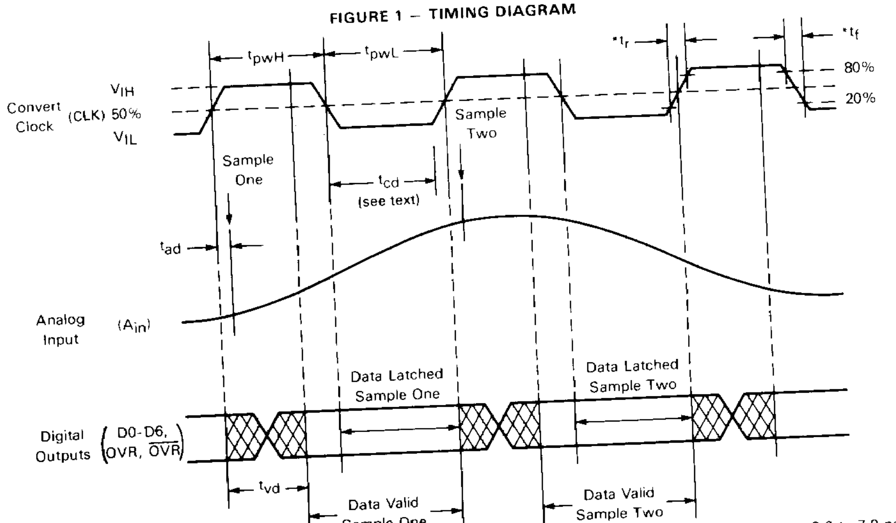
Characteristic	Symbol	MC10315L/MC10317L Min	Typ	Max	Unit
Reference Ladder Resistance Temperature Coefficient $0°C \leq T_A \leq +70°C$	T_{CR}		0.37	—	%/°C
Clock Input Logic Levels, $0°C \leq T_A \leq +70°C$ High Logic State / Low Logic State Note 2	V_{IH} / V_{IL}	−1.145	–	— / −1.455	V
Clock Input Current High Logic State / Low Logic State	I_{IH} / I_{IL}	–	150 / 100	–	µA
Digital Output Logic Levels High Logic State / Low Logic State $0°C \leq T_A \leq +70°C$ Note 2	V_{OH} / V_{OL}	1.020	– / –	– / −1.605	V
Power Supply Current, $0°C \leq T_A \leq +70°C$ $4.75\ V \leq V_{CC} \leq 5.25\ V$ $-4.94\ V \geq V_{EE} \geq -5.46\ V$	I_{CC} / I_{EE}		118 / −110	150 / −140	mA

RECOMMENDED OPERATING CONDITIONS (Note 1)

Characteristic	Symbol	MC10315L/MC10317L Min	NOMINAL	Max	Unit
Power Supply Voltages	V_{CC} / V_{EE}	4.75 / 5.46	5.0 / 5.2	5.25 / 4.94	Vdc
Ground 1	Gnd1	0.3	0	+1.0	V
Reference Input, Top	V_{RT}	1.0	0	+2.0	V
Reference Input, Bottom	V_{RB}	2.0	0	+1.0	V
Reference Input Voltage Range (V_{RT} V_{RB})	V_{RR}	1.0		2.0	V
Convert Clock Pulse Width, High / Convert Clock Pulse Width, Low	t_{pwH} / t_{pwL}	44 / 25			ns
Digital Output Current	I_{OH}		10		mA
Operating Temperature Range	T_A	0		70	°C

Notes:
1. All voltage levels referenced to Ground 2 (Gnd2) unless otherwise noted.
2. MECL 10K logic levels are designed to meet the dc specifications after thermal equilibrium has been established with a transverse airflow greater than 500 Linear fpm and $V_{EE} = -5.2\ V \pm 0.010\ V$. All outputs are specified driving 50Ω to −2.0 V.

FIGURE 1 — TIMING DIAGRAM



*Recommended range of rise (t_r) and fall (t_f) times are 2.0 to 7.0 ns.

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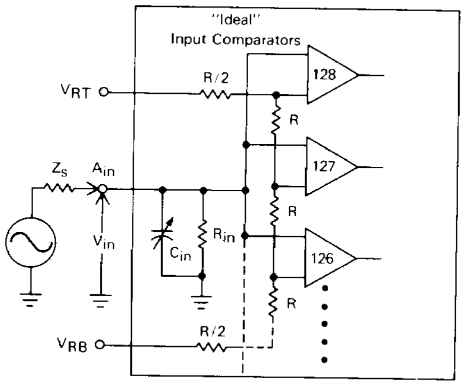
FIGURE 2 — EQUIVALENT R_{in} AND C_{in} OF THE ANALOG INPUT



$$R_{in} \approx \frac{|V_{RT}-V_{RB}|}{400\ \mu A}$$

$$^{*}C_{in} \approx \frac{30pF}{|V_{RT}-V_{RB}|}\,|V_{in}-V_{RB}| + 40\ pF$$

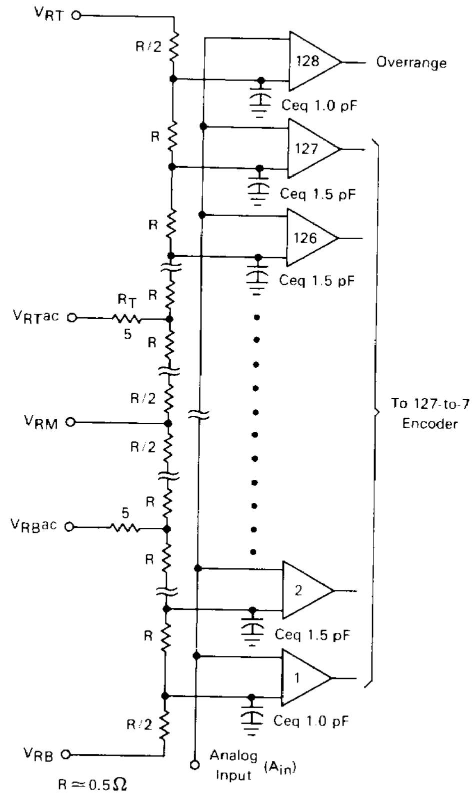
*Valid for $V_{RT} \geqslant V_{in} \geqslant V_{RB}$

$R \approx 0.5\,\Omega$

R_{in} – Effective input resistance representing the cumulative bias currents of the 128 input comparators.

C_{in} – Equivalent input capacitance variable as a function of V_{in}.

FIGURE 3 — EQUIVALENT CIRCUIT OF REFERENCE RESISTOR LADDER NETWORK



$R \approx 0.5\,\Omega$

Ceq – The lumped equivalent value of capacitance representing the distributed capacitance for each resistor (R) and the input capacitance for each comparator.

FIGURE 4 — CLOCK INPUT IS STANDARD MECL INPUT WITH EMITTER FOLLOWER

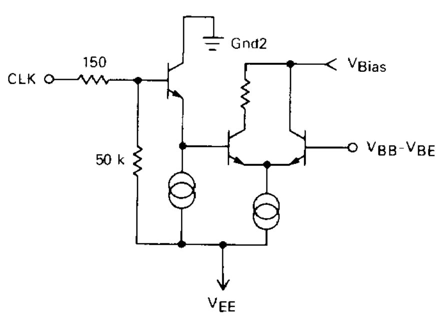
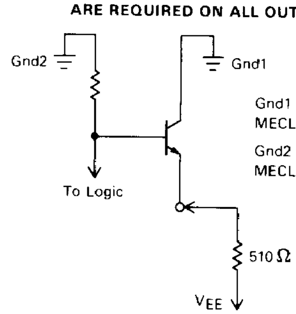


FIGURE 5 — DIGITAL OUTPUTS ARE STANDARD MECL 10K WITH EMITTER FOLLOWERS CAPABLE OF SOURCING 25 mA. EXTERNAL PULL-DOWN RESISTORS ARE REQUIRED ON ALL OUTPUTS.



*Recommended value of external pull-down resistors for all outputs.

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FIGURE 6 — OUTPUT CODING FOR THE MC10315L/MC10317L DEVICES*

Comparator Step	Analog Input Range (15.6 mV per LSB)			MC10315L Data Bits (D0-D6)	MC10317L Data Bits (D0-D6)	Overrange Bit (OVR)	$\overline{\text{Overrange}}$ Bit ($\overline{\text{OVR}}$)
	−2.0 V to 0 V	0 V to 2.0 V	±1.0 V				
000	2.0000 V	+ 0.0000 V	- 1.0000 V	0000000	0000000	0	1
001	− 1.9922 V	+ 0.0078 V	0.9922 V	0000001	0000001	0	1
•	•	•	•	•	•	↓	↓
•	•	•	•	•	•		
•	•	•	•	•	•		
063	- 1.0234 V	+ 0.9766 V	0.0234 V	0111111	0111111		
064	1.0078 V	+ 0.9922 V	0.0078 V	1000000	1000000		
065	0.9922 V	+ 1.0078 V	+ 0.0078 V	1000001	1000001		
•	•	•	•	•	•		
•	•	•	•	•	•		
•	•	•	•	•	•		
126	0.0391 V	+ 1.9609 V	+ 0.9609 V	1111110	1111110		
127	0.0234 V	+ 1.9766 V	+ 0.9766 V	1111111	1111111	↓	↓
128	0.0078 V	+ 1.9922 V	+ 0.9922 V	1111111	0000000	1	0

*The MC10315L and MC10317L differ only in output coding at comparator step 128 where the device is overranged.

CIRCUIT DESCRIPTION

Conversion Timing

The MC10315L/MC10317L performs a conversion and outputs data within a single clock cycle. Referring to Figure 1 will indicate that the clock input is sensitive to the rising and falling clock edges. All significant operations are referenced to the edges. A rising clock edge holds the analog input by latching the (128) input comparators. The output latches are also released to toggle and update to the new digital value. The falling edge of the clock will latch the data outputs. Clock timing must be considered to ensure a valid conversion. With the rising edge of the clock, there will be an aperture delay (t_{ad}) which is the time from the threshold of the (50%) edge to the actual time the input comparators latch in the analog value of A_{in}. The data valid delay time (t_{vd}) is the time interval for valid data to appear at the outputs. t_{vd} is 43 ns from the rising clock edge. After this time, the clock can go low to latch the valid data at the outputs. The clock must remain low a minimum time before another rising edge in order for the input comparators to unlatch and begin to track. This comparator tracking delay time (t_{cd}) is 25 ns. After this minimum time, the conversion clock cycle is repeated, latching in a new analog input value.

The minimum recommended clock pulse width high time (t_{pwH}) is 44 ns and pulse width low time (t_{pwL}) is 25 ns for maximum recommended sample frequency (fs).

Rise (t_r) and fall (t_f) time of the clock edges should be in the range from 2.0 to 7.0 ns to minimize the chance of clocking errors or uncertainty.

Analog Input (A_{in})

The dc current drive required by the analog input (A_{in}) is a function of the input voltage (V_{in}) and is directly attributable to the accumulation of input bias currents for each of the 128 comparators. When $V_{in} \leq V_{RB}$, the dc current is zero and when $V_{in} \geq V_{RT}$ the current is a maximum of 400 μA. Looking at this current as a function of V_{in} on a large signal basis, it will appear as a straight line approximation.

This input current loading on a driving source impedance can produce a dc gain error. Cancellation of this error is accomplished by utilizing an adjustable voltage reference at V_{RT}. If V_{RT} is tied to a fixed reference or grounded, the driving amplifiers offset can be adjusted. However, a zero error will now occur which can be cancelled by adjusting V_{RB}. Another method of reducing dc gain error due to analog input current is to use a driving amplifier with sufficiently low output impedance (Z_S). This can be determined by:

$$Z_S \leq \frac{\text{maximum gain error (V)}}{400\ \mu A}$$

i.e., with a 1.0 volt analog input range ($V_{RT}-V_{RB}$ = 1.0 V), a 1/2 LSB of gain error = 3.9 mV

$$Z_S \leq \frac{3.9\ mV}{400\ \mu A} \leq 9.76\ \Omega$$

Analog Input (A_{in}) (Continued)

The input capacitance (C_{in}) is also a function of input voltage (V_{in}). For $V_{in} \leq V_{RB}$, $C_{in} \simeq 40$ pF; $V_{in} \geq V_{RT}$, $C_{in} \simeq 70$ pF. The input capacitance on a large signal basis over the analog input range is a linear function. C_{in} can limit the analog input bandwidth if the driving source impedance is too great. This can introduce an ac gain error if the corner frequency f_c is not sufficiently extended from maximum input frequency (f_{in}).

For example, to keep the ac gain error to within 1/2 LSB of 7-bits, the corner frequency (f_c) of the effective single pole, low-pass filter created by the driving source impedance (Z_s) and the input capacitance (C_{in}) should be: $fc \geq 11.3 f_{in}$

C_{in} - analog input capacitance.
f_{in} - maximum input frequency of A_{in}
f_c - corner frequency determined by C_{in} and Z_s
n - number of bits
Z_s - driving source impedance of the analog input

For single Pole Filter: $$\frac{fc}{f_{in}} \geq \frac{1}{\sqrt{\dfrac{1}{\left(\dfrac{2^{n+1}-1}{2^{n+1}}\right)^2} - 1}}$$

If measures have already been taken to keep dc gain error to within 3.9 mV (1/2 LSB for 1.0 V full scale) by providing a low Z_s as described earlier, the calculated $Z_s \leq 9.76\ \Omega$ will sufficiently extend the corner frequency of the input pole to $\simeq 233$ MHz.

Figure 2 illustrates the equivalent analog input in terms of an effective variable C_{in} and R_{in}.

Reference Inputs

As shown in Figure 3, a resistive (divider) ladder comprised of 128 matched resistors with a nominal value of 0.5 Ω each, provides a reference voltage to each of the 128 comparator inputs. Recommended range of reference voltage applied across the resistive ladder (V_{RT} to V_{RB}) is 1.0 volt to 2.0 volts. V_{RT} must be kept more positive than V_{RB}. V_{RT} must not exceed +2.5 volts above Gnd2 and V_{RB} must not become more negative than −2.5 volts below Gnd2. With 2.0 volts across the reference ladder (V_{RT}-V_{RB}=2.0 V), the ladder network has a common-mode range capability about Gnd2, permitting analog input (A_{in}) ranging options such as ± 1.0 volt, 0 to - 2.0 volts and 0 to 2.0 volts. A minimum of 1.0 volt should be maintained across the ladder network to ensure linearity to 7-bits. Less than 1.0 volt will degrade linearity due to comparator offsets becoming a significant factor.

Additional taps on the reference ladder are pinned out, providing access to the middle (V_{RM}), 1/4 (V_{RB}ac) and 3/4 (V_{RT}ac) scale points. V_{RM} can be left open, but if ladder linearity adjustment is required, an appropriate reference voltage can be applied. The V_{RB}ac and V_{RT}ac pins are intended for ac bypassing if ladder noise presents a problem. Reference voltages can be applied to these pins if tighter ladder linearity is desired. If the reference ladder voltage is to be varied dynamically such as in an AGC application, ac bypassing of any of the reference taps would likely yield undesirable results.

Calibration is accomplished by adjusting V_{RB} and V_{RT} to set the first and 127th comparator thresholds to the desired voltages. If a 0 to −1.0 V input (A_{in}) range is desired, continuously strobe the convertor with −0.9961 V on the analog input, adjust V_{RB} for output toggling between codes 0000000 and 0000001. Then apply A_{in} = −0.0117 V and adjust V_{RT} for toggling between 1111110 and 1111111 (thresholds 126th and 127th). Rather than adjusting V_{RT}, it may be more convenient to connect V_{RT} to Gnd2 and adjust the driving amplifier offset control. V_{RB} can again be used as a gain adjust point to cancel the effects of using the offset control technique.

Application Information

8-bits of resolution and accuracy can be obtained by stacking two 7-bit converters and wire ORing the data outputs. Shown in Figure 7 is an MC10315L and MC10317L in an 8-bit A/D configuration. The circuit is quite straightforward with the analog input (A_{in}) for each converter tied together, forming a common input. The analog input range is negative unipolar with V_{RT} of the MC10315L grounded (Gnd2) or referenced very near ground. V_{RB} of the MC10315L is connected to V_{RT} of the MC10317L and referenced to $V_{REF}/2$ to ensure this node is midscale. Unit to unit variations in Reference Ladder Resistance of each device can shift this point if a reference is not used, causing linearity errors. Care should be taken when interconnecting V_{RB} and V_{RT} of the MC10315L and MC10317L respectively. Reference ladder current flowing through resistance of printed circuit board runs, sockets and even device pins and bonding wires can establish significant IR drops of several millivolts causing differential non-linearity errors at midscale. A negative reference of -2.000 V is applied to V_{RB} of the MC10317L. The remaining pins V_{RT}ac, V_{RB}ac and V_{RM} for both devices can be left open or be connected to additional external references if linearity improvements are required. V_{RT}ac and V_{RB}ac can also be used as ac decoupling points for the resistor ladders to reduce any transients which may exist due to current noise.

The clock (CLK) inputs are driven by a common clock. Depending on the input frequency to be encoded, it may be necessary to skew the rising clock edges to one of the devices to compensate for a slight difference in aperture delay time (t_{ad}) which may occur between the two devices.

Application Information (Continued)

The digital outputs, D0 through D6 are wire ORed. The overrange (OVR) bit of the MC10317L becomes the MSB for the 8-bit word in Binary coding.

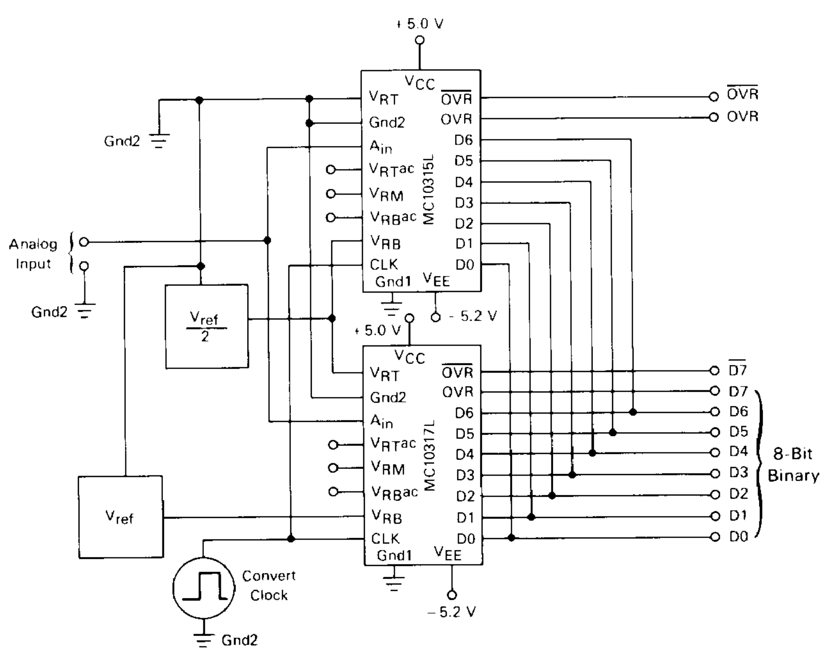
The MC10315L and MC10317L differ only in the method of overranging (see Figure 6, output coding truth table). When the MC10317L input (A_{in}) is overranged, the overrange (OVR) bit goes high, all other bits (D0-D6) go low. This enables direct wire ORing of additional A/D outputs to expand to ≥8-bits. When the MC10315L is overranged, OVR goes high and the data bits (D0-D6) remain high. This device provides a true termination of a digital word when the system becomes overranged. Generally the MC10315L will be used in a 7-bit, stand-alone converter scheme, or as the upper scale A/D when stacking two or more devices to expand to ≥7-bits.

Pull-down resistors are required at the digital outputs. A recommended value of 510 Ω will provide proper output fall times in most applications and also hold down device power dissipation. The outputs are capable of sustaining MECL levels when terminated with a 50 Ω (to −2.0 V) characteristic load impedance to minimize reflections. Design rules for MECL 10K should be followed when using these devices.

Care must be taken in PC board ground layout to prevent digital ground currents from flowing through the analog ground. Separate grounds are provided on the MC10315L/MC10317L to help isolate the digital noise from the analog section of a system. Gnd1 is internally connected to only the collectors of the output emitter followers as shown in Figure 5. This provides a separate path for current transients of the switched output loads. All other internal circuitry is referenced to Gnd2.

Low and high frequency power supply bypassing should be provided physically close to the device, with V_{CC} and V_{EE} bypassed to Gnd2.

FIGURE 7 — CIRCUIT CONFIGURATION UTILIZING A MC10315L AND MC10317L A/D TO PERFORM A HIGH SPEED, 8-BIT CONVERSION



Note:
Required pull-down resistors at the digital outputs are not shown. All digital outputs should be treated according to MECL 10K design rules.