CMS88D8MB36 8-MEGABYTE
CMS88D4MB36 4-MEGABYTE
DRAM MEMORY CARDS

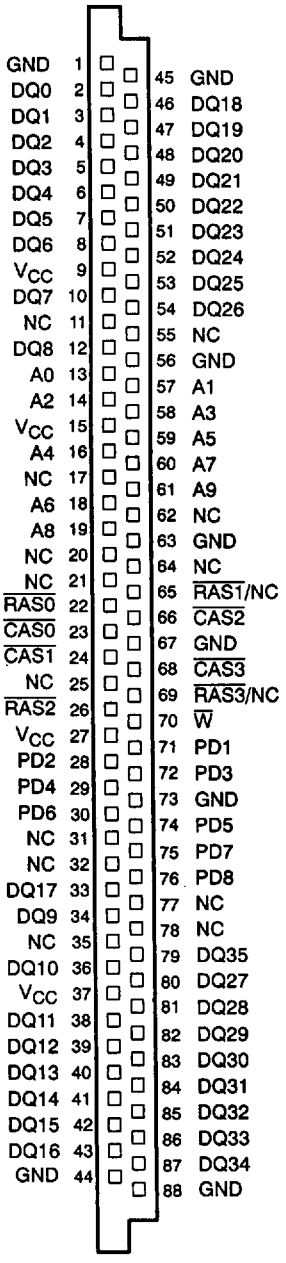
SMNS421B–NOVEMBER 1991–REVISED JANUARY 1993

T-81-27-15

- **Credit Card Size (85.6 mm × 54 mm × 3.4 mm)**
- **Single 5-V Power Supply (±5% Tolerance)**
- **Enhanced Page Mode Operation**
- **CMS88D8MB36 – 2M × 36/4$\overline{RAS}$/4$\overline{CAS}$**
  CMS88D4MB36 – 1M × 36/2$\overline{RAS}$/4$\overline{CAS}$
- **Operating Temperature . . . 0°C to 55°C**
- **Standard 88-Pin Two-Piece Connector**
- **CMOS Buffered Inputs on All Inputs Except $\overline{RAS}$ and DQ**
- **3-State Unlatched Output**
- **Performance Ranges:**

	ACCESS TIME t_{RAC}	ACCESS TIME t_{CAC}	READ OR WRITE CYCLE t_{RC}
CMS88D8MB36–7	70 ns	25 ns	130 ns
CMS88D8MB36–8	80 ns	27 ns	150 ns
CMS88D4MB36–7	70 ns	25 ns	130 ns
CMS88D4MB36–8	80 ns	27 ns	150 ns

88-PIN MEMORY CARD
(CONNECTOR VIEW)



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description

The CMS88D8MB36 and CMS88D4MB36 series are dynamic random-access memory cards designed to be used as internal system memory or as external add-on memory.

These cards have CMOS buffers added to the $\overline{CAS}$, $\overline{W}$, and address inputs to minimize loading caused by the module. $\overline{RAS}$ and data in/out remain compatible with Series 74 TTL.

The cards can operate in enhanced page mode. All address lines and data are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The common I/O features of the CMS88D8MB36 and CMS88D4MB36 dictate the use of early write cycles.

PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ35	Data Inputs/Outputs
PD1–PD8	Presence Detect
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Power Supply
V_{SS}	Ground
$\overline{W}$	Write Enable
NC	No Internal Connection

operation

The CMS88D8MB36 and CMS88D4MB36 cards are divided into separate banks of memory. Each bank is selectable using $\overline{RAS}x$ and $\overline{CAS}x$ as shown in the table below. $\overline{RAS0}$–$\overline{RAS3}$ control which side of the DRAM banks are connected to the memory card DQ pins. Therefore, only two $\overline{RAS}$ signals may be active during any read or write cycle.

Table 1. Memory Bank Definition

DATA BLOCK	$\overline{RAS}x$		$\overline{CAS}x$	
	Side 1	Side 2	Side 1	Side 2
DQ0–DQ8	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$	$\overline{CAS0}$
DQ9–DQ17	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS1}$	$\overline{CAS1}$
DQ18–DQ26	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$	$\overline{CAS2}$
DQ27–DQ35	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$	$\overline{CAS3}$

power up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. The eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

specifications

Refresh period is extended to 16 ms. During this period, each of the 1024 rows must be strobed with $\overline{RAS}$ to retain data.

memory card components

- Meets JEDEC standard
- UL approved materials

Table 2. Pin Definition for Presence Detect

DEVICE	CONFIGURATION					SPEED†			REFRESH CYCLE†	
	PD1(71)	PD2(28)	PD3(72)	PD4(29)	PD5(74)		PD6 (30)	PD7 (75)		PD8 (76)
CMS88D8MB36	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	–70 ns	V_{SS}	NC	SLOW	NC
CMS88D4MB36	V_{SS}	NC	V_{SS}	V_{SS}	NC	–80 ns	NC	V_{SS}	SELF	V_{SS}

† Applies to both CMS88D8MB36 and CMS88D4MB36 devices.

Table 3. Pin Definition

DEVICE	$\overline{RAS1}$/NC (65)	$\overline{RAS3}$/NC (69)
CMS88D8MB36	$\overline{RAS1}$	$\overline{RAS3}$
CMS88D4MB36	NC	NC

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Voltage range on V_{CC} ..... −0.5 V to 6 V
Short circuit output current ..... 50 mA
Power dissipation (CMS8D8MB36) ..... 22 W
Power dissipation (CMS8D4MB36) ..... 11 W
Operating free-air temperature ..... 0°C to 55°C
Storage temperature range ..... −40 °C to 85 °C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	$\overline{CAS}$, $\overline{W}$, address lines	0.7 V_{CC}			V
		$\overline{RAS}$ and DQ lines	2.4		6.5	
V_{IL}	Low-level input voltage (see Note 2)	$\overline{CAS}$, $\overline{W}$, address lines			0.3 V_{CC}	V
		$\overline{RAS}$ and DQ lines	−1		0.8	
T_A	Operating free air temperature		0		55	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA			2.4	V
V_{OL}	Low-level output voltage	I_{IL} = 4.2 mA		0.4		V
I_I	Input current for addresses, $\overline{CASx}$, and $\overline{W}$	V_I = 0 to 5.25 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}			±10	µA
	Input current $\overline{RASx}$ (leakage)	V_I = 0 to 5.25 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}			±50	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.25 V, $\overline{CASx}$ high			±20	µA

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'88D8MB36-7		'88D8MB36-8		UNIT
			MIN	MAX	MIN	MAX	
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle (see Note 3)		961		861	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, all other signals stable, V_{CC} = 5.25 V (see Note 3)		21		21	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR)	Minimum cycle, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle, $\overline{RAS}$ active, $\overline{CAS}$ high (see Note 3)		1850		1650	mA
I_{CC4}	Average page current	t_{PC} = minimum, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling (see Note 3)		961		861	mA

NOTE 3: $V_{IH} = V_{CC} - 0.2$ V and V_{IL} = 0 V for all operating currents.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		15	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ inputs		35	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ inputs		15	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		15	pF
$C_{i(DQ)}$	Input/output capacitance of DQ pins		14	pF

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electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA			2.4	V
V_{OL}	Low-level output voltage	I_{IL} = 4.2 mA	0.4			V
I_I	Input current for addresses, $\overline{CASx}$, and $\overline{W}$	V_I = 0 to 5.25 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}			±10	µA
	Input current $\overline{RASx}$ (leakage)	V_I = 0 to 5.25 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}			±50	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.25 V, $\overline{CASx}$ high			±10	µA

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'88D4MB36-7		'88D4MB36-8		UNIT
			MIN	MAX	MIN	MAX	
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle (see Note 3)		950		850	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high. All other signals stable, V_{CC} = 5.25 V (see Note 3)		11		11	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR)	Minimum cycle, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle, $\overline{RAS}$ active, $\overline{CAS}$ high (see Note 3)		950		850	mA
I_{CC4}	Average page current	t_{PC} = minimum, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling (see Note 3)		950		850	mA

NOTE 3: $V_{IH} = V_{CC} - 0.2$ V and V_{IL} = 0 V for all operating currents.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		15	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ inputs		35	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ inputs		15	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		15	pF
$C_{i(DQ)}$	Input/output capacitance of DQ pins		7	pF

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'88D8MB36-7 '88D4MB36-7		'88D8MB36-8 '88D4MB36-8		UNIT
		MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$x low		25		27	ns
t_{CAA}	Access time from column-address		42		47	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80	ns
t_{CPA}	Access time from column precharge		47		52	ns
t_{CLZ}	$\overline{CAS}$x low to output in low Z	0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$x high (see Note 4)	0	25	0	27	ns

NOTE 4: t_{OFF} is specified when the output is no longer driven.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'88D8MB36-7 '88D4MB36-7		'88D8MB36-8 '88D4MB36-8		UNIT
		MIN	MAX	MIN	MAX	
t_{RC}	Read cycle time	130		150		ns
t_{WC}	Write cycle time	130		150		ns
t_{PC}	Page mode read or write cycle time (see Note 5)	52		57		ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	25	10 000	27	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high	50		60		ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low	70	10 000	80	10 000	ns
t_{RASP}	Page mode, pulse duration, $\overline{RAS}$ low	70	100 000	80	100 000	ns
t_{wp}	Write pulse duration	22		22		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	0		0		ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	7		7		ns
t_{DS}	Data setup time before $\overline{CAS}$ low	0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		ns
t_{WCS}	$\overline{W}$ low setup before $\overline{CAS}$ low	0		0		ns
t_{CWL}	$\overline{W}$ low setup before $\overline{CAS}$ high	18		20		ns
t_{RWL}	$\overline{W}$ low setup before $\overline{RAS}$ high	25		27		ns
t_{WSR}	$\overline{W}$ high setup ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	17		17		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	15		15		ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	10		12		ns
t_{AR}	Column address hold time after $\overline{RAS}$ low (see note 6)	55		60		ns
t_{CLCH}	Hold time, $\overline{CAS}$ low to $\overline{CAS}$ high	12		12		ns
t_{DH}	Data hold time after $\overline{CAS}$ low	15		15		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low	55		60		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 7)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 7)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 6)	55		60		ns
t_{WHR}	$\overline{W}$ high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	70		80		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	7		7		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	25		27		ns

NOTES: 5. To assure t_{PC} min, t_{ASC} should be greater than or equal to 5 ns.
6. The minimum value is measured when t_{RCD} is set to t_{RCD}(min) as a reference.
7. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

PARAMETER		'88D8MB36-7 '88D4MB36-7		'88D8MB36-8 '88D4MB36-8		UNIT
		MIN	MAX	MIN	MAX	
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 8)	20	47	22	53	ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 8)	15	28	17	33	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	42		47		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	35		40		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 9)	15		20		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 9)	17		17		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 9)	0		0		ns
t_{REF}	Refresh time interval		16		16	ms
t_T	Transition time (see Note 10)	3	50	3	50	ns

NOTES: 8. Maximum values specified to assure access times.
9. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
10. All cycle times assume t_T = 5 ns.

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