

# HB66A76816CA-25

1,572,864Word×8bit / 786,432Word×16bit  
High Density CMOS Static RAM Card

Rev.0  
sep.10,1992



The HB66A76816CA-25 is a high density 1.5MWord×8bit or 768kWord×16bit static RAM Card, mounted of 12pieces 1M static RAM sealed in TSOP package.  
An outline of the HB66A76816CA-25 is 68-pin two piece connector package.  
Therefore, the HB66A76816CA-25 makes high density and it is possible to expand easily for memory system.

## ■ Features

- Type HB66A76816CA-25
- Memory capacity 1.5MWord×8bit  
768kWord×16bit
- Attribute Memory 512Word×8bit
- Power supply +5V(±5%)
- Memory backup battery CR2025 1pcs. (replaceable)
- Memory retention period 1.5year (Ta=+20°C)
- Interface Parallel I/O interface
- Standard weight 30g
- Operating temperature 0 to +55°C, 95%RH or less
- Product code To be stamped on the product
- High speed 250ns(max.)
- Compatibility JEIDA 4.1 / PCMCIA 2.0

## ■ Ordering information

| Part no.        | Access time | Package                 |
|-----------------|-------------|-------------------------|
| HB66A76816CA-25 | 250ns       | 68-pin 2piece connector |

MIZTOSI

■ Pin out

|          |         |     |         |          |
|----------|---------|-----|---------|----------|
| Pin Name | Pin No. |     | Pin No. | Pin Name |
| GND      | 1       | ○ ○ | 35      | GND      |
| D3       | 2       | ○ ○ | 36      | /CD1     |
| D4       | 3       | ○ ○ | 37      | D11      |
| D5       | 4       | ○ ○ | 38      | D12      |
| D6       | 5       | ○ ○ | 39      | D13      |
| D7       | 6       | ○ ○ | 40      | D14      |
| /CE1     | 7       | ○ ○ | 41      | D15      |
| A10      | 8       | ○ ○ | 42      | /CE2     |
| /OE      | 9       | ○ ○ | 43      | NC       |
| A11      | 10      | ○ ○ | 44      | NC       |
| A9       | 11      | ○ ○ | 45      | NC       |
| A8       | 12      | ○ ○ | 46      | A17      |
| A13      | 13      | ○ ○ | 47      | A18      |
| A14      | 14      | ○ ○ | 48      | A19      |
| /WE      | 15      | ○ ○ | 49      | A20      |
| RFU      | 16      | ○ ○ | 50      | NC       |
| Vcc      | 17      | ○ ○ | 51      | Vcc      |
| RFU      | 18      | ○ ○ | 52      | NC       |
| A16      | 19      | ○ ○ | 53      | NC       |
| A15      | 20      | ○ ○ | 54      | NC       |
| A12      | 21      | ○ ○ | 55      | NC       |
| A7       | 22      | ○ ○ | 56      | NC       |
| A6       | 23      | ○ ○ | 57      | NC       |
| A5       | 24      | ○ ○ | 58      | NC       |
| A4       | 25      | ○ ○ | 59      | NC       |
| A3       | 26      | ○ ○ | 60      | NC       |
| A2       | 27      | ○ ○ | 61      | /REG     |
| A1       | 28      | ○ ○ | 62      | BVD2     |
| A0       | 29      | ○ ○ | 63      | BVD1     |
| D0       | 30      | ○ ○ | 64      | D8       |
| D1       | 31      | ○ ○ | 65      | D9       |
| D2       | 32      | ○ ○ | 66      | D10      |
| WP       | 33      | ○ ○ | 67      | /CD2     |
| GND      | 34      | ○ ○ | 68      | GND      |

■ Pin Description

| Pin Name   | Function                |
|------------|-------------------------|
| /WE        | Write Enable            |
| /OE        | Output Enable           |
| A0 to A20  | Address Input           |
| D0 to D15  | Data-input/output       |
| /CE1, /CE2 | Chip Enable             |
| /CD1, /CD2 | Card Detect             |
| Vcc        | +5V Supply              |
| GND        | Ground                  |
| WP         | Write Protect           |
| REG        | Attribute memory select |
| BVD1, BVD2 | Battery Voltage Detect  |
| NC         | No connect              |

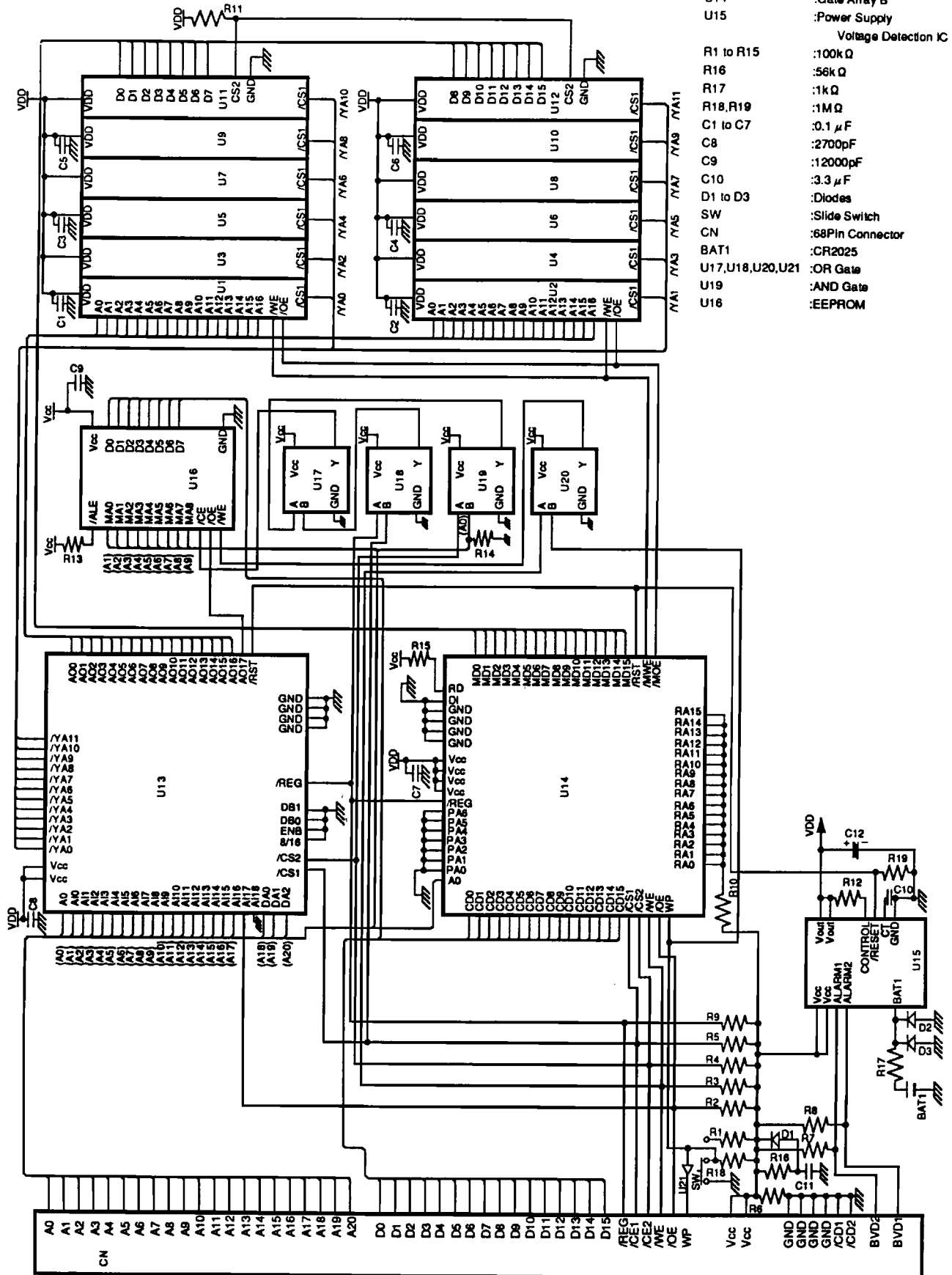
Note)

1. NC pins are open. Be sure to keep this terminal open on the system side. The terminals indicated below may be used on the system side because their functions are already specified.
  - #18:Vpp1(Supply voltage for program (even bytes))
  - #52:Vpp2(Supply voltage for program (odd bytes))
  - #50:A21, #53:A22, #54:A23, #55:A24, #56:A25
2. When one or both of the /CE1, and /CE2 signals are supplied high, set all input signals high or low. The same may be with input/output signals which are in the input state (to avoid the high impedance state).

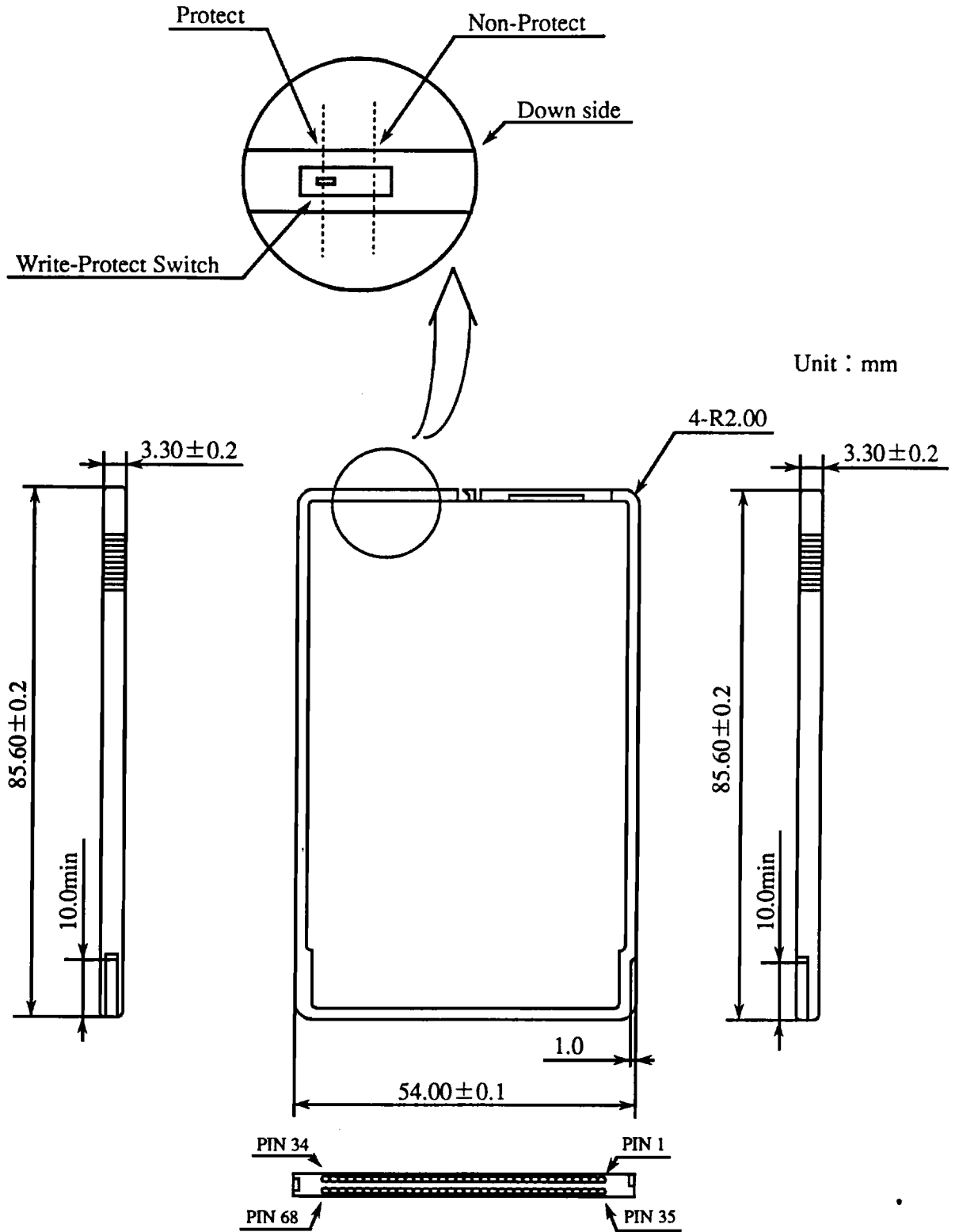
Block Diagram

Note :

- U1 to U12 :1Mbit SRAM
- U13 :Gate Array A
- U14 :Gate Array B
- U15 :Power Supply
- U16 :Voltage Detection IC
- R1 to R15 :100k $\Omega$
- R16 :56k $\Omega$
- R17 :1k $\Omega$
- R18,R19 :1M $\Omega$
- C1 to C7 :0.1 $\mu$ F
- C8 :2700pF
- C9 :12000pF
- C10 :3.3 $\mu$ F
- D1 to D3 :Diodes
- SW :Slide Switch
- CN :68Pin Connector
- BAT1 :CR2025
- U17,U18,U20,U21 :OR Gate
- U19 :AND Gate
- U16 :EEPROM



Physical Outline



## Function Table

| /CE1 | /CE2 | A0 | /WE | /OE | /REG | Mode           | D0~D7     | D8~D15   | Status   |
|------|------|----|-----|-----|------|----------------|-----------|----------|----------|
| H    | H    | ×  | ×   | ×   | H    | Not select     | High-Z    | High-Z   | Stand by |
| L    | H    | L  | H   | L   | H    | Read (×8)      | Do(Even)  | High-Z   | Active   |
| L    | H    | H  | H   | L   | H    | Read (×8)      | Do(Odd)   | High-Z   | Active   |
| L    | H    | L  | L   | ×   | H    | Write (×8)     | Di (Even) | High-Z   | Active   |
| L    | H    | H  | L   | ×   | H    | Write (×8)     | Di (Odd)  | High-Z   | Active   |
| H    | L    | ×  | L   | ×   | H    | Write (×8)     | High-Z    | Di (odd) | Active   |
| H    | L    | ×  | H   | L   | H    | Read (×8)      | High-Z    | Do(odd)  | Active   |
| L    | L    | ×  | H   | L   | H    | Read (×16)     | Do(Even)  | Do(odd)  | Active   |
| L    | L    | ×  | L   | ×   | H    | Write (×16)    | Di (Even) | Di (odd) | Active   |
| ×    | L    | ×  | H   | H   | H    | Output disable | High-Z    | High-Z   | Active   |
| L    | H    | ×  | H   | H   | H    | Output disable | High-Z    | High-Z   | Active   |

H:High level      L:Low level      ×:Either "H"or "L"  
 Di:Input data      Do:Output data

Note)

1. When the write protect switch is turned to the protect side, no data can be written and the WP signal goes high.
2. Attribute memory addresses are from A0 to A9. A10 and more addresses are not used.

## Absolute Maximum Ratings

| Parameter            | Symbol          | Min. | Typ. | Max.                            | Unit |
|----------------------|-----------------|------|------|---------------------------------|------|
| Power supply voltage | V <sub>cc</sub> | -0.5 | 5.0  | 7.0                             | V    |
| Input/Output voltage | V <sub>I</sub>  | -0.5 | -    | V <sub>cc</sub> +0.5 (max. 7.0) | V    |

## Recommended DC Operating Conditions (Ta=0 to +55°C)

| Parameter          | Symbol          | Min.                 | Typ. | Max.                 | Unit |
|--------------------|-----------------|----------------------|------|----------------------|------|
| Supply voltage     | V <sub>cc</sub> | 4.75                 | 5.0  | 5.25                 | V    |
|                    | V <sub>ss</sub> | 0                    | 0    | 0                    | V    |
| Input high voltage | V <sub>iH</sub> | V <sub>cc</sub> ×0.3 | -    | V <sub>cc</sub> +0.3 | V    |
| Input low voltage  | V <sub>iL</sub> | -0.3                 | -    | 0.8                  | V    |

■ DC Characteristics ( $V_{cc}=5V \pm 5\%$ ,  $T_a=0$  to  $+55^\circ\text{C}$ )

| Parameter                      | Symbol                       | Min.         | Typ. | Max. | Unit | Test Conditions       |                     |
|--------------------------------|------------------------------|--------------|------|------|------|-----------------------|---------------------|
| Standby power supply current   | $I_{SB1}$                    | -            | -    | 2.0  | mA   | *Note1)-2             |                     |
| Operating power supply current | $I_{CC1}$                    | -            | -    | 200  | mA   |                       |                     |
| Input current                  | A0 to A20<br>D0 to D15       | $I_{I1}$     | -10  | -    | 10   | $\mu\text{A}$         | $V_I=V_{CC}$ or GND |
|                                | /CE1, /CE2, /OE<br>/WE, /REG | $I_{I2}$     | -70  | -    | 70   | $\mu\text{A}$         | $V_I=V_{CC}$ or GND |
| Output voltage *Note1)-1       | $V_{OH}$                     | $V_{CC}-0.4$ | -    | -    | V    | $I_{OH}=-12\text{mA}$ |                     |
|                                | $V_{OL}$                     | -            | -    | 0.4  | V    | $I_{OL}=12\text{mA}$  |                     |

Note1)

1. Except WP signal, /CD1 signal, /CD2 signal, BVD1 signal, BVD2 signal.
2. Set the power supply voltage for the memory card to 5.0V. Set the /CE1, /CE2, /OE, /WE, and /REG signal to the high level ( $V_{IH} \geq V_{CC}-0.2\text{V}$ ) and the A0 signal to the low level ( $V_{IL} \leq 0.2\text{V}$ ). Then measure the current. (The output signal is open.)
3. Set the power supply voltage for the memory card to 5.0V. Measure the current when the memory card is accessed. (The access time is 250ns.)

■ Capacitance ( $T_a=+25^\circ\text{C}$ ,  $f=1\text{MHz}$ )

| Parameter                | Symbol   | Typ. | Max. | Unit | Test Conditions         |
|--------------------------|----------|------|------|------|-------------------------|
| Input capacitance        | $C_{in}$ | -    | 10   | pF   | $V_{CC}=V_I=\text{GND}$ |
| Input/Output capacitance | CI/O     | -    | 35   | pF   | $V_{CC}=V_I=\text{GND}$ |

Note2)

Input capacitance of A0 signal, /CE1 signal, /CE2 signal, /OE signal and /REG signal are 20pF Max.

### ■ AC Characteristics (Ta=0 to +55°C, Vcc=5V ± 5%)

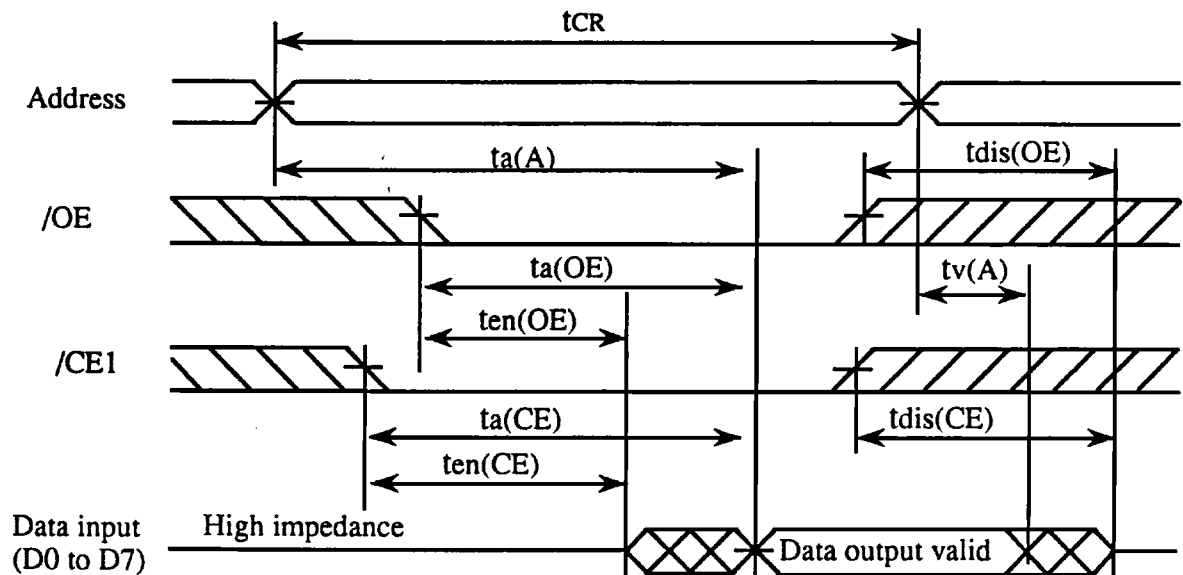
AC Test condition

- Input pulse level : 0.8 to 3.5V
- Input pulse rise and fall time : 10ns
- Input and output timing reference level : 1.5V
- Output load : 1TTL Gate and CL=100pF  
(Including scope and jig capacitance)

### ● Read Cycle

| Parameter                           | Symbol   | Standard |      | Unit |
|-------------------------------------|----------|----------|------|------|
|                                     |          | Min.     | Max. |      |
| Read cycle time                     | tCR      | 250      | -    | ns   |
| Address access time                 | ta(A)    | -        | 250  | ns   |
| Card enable access time             | ta(CE)   | -        | 250  | ns   |
| Output enable time                  | ta(OE)   | -        | 125  | ns   |
| Output disable time from /CE1, /CE2 | tdis(CE) | -        | 100  | ns   |
| Output disable time from /OE        | tdis(OE) | -        | 100  | ns   |
| Output enable time from /CE1, /CE2  | ten(CE)  | 5        | -    | ns   |
| Output enable time                  | ten(OE)  | 5        | -    | ns   |
| Data valid from address change      | tv(A)    | 0        | -    | ns   |

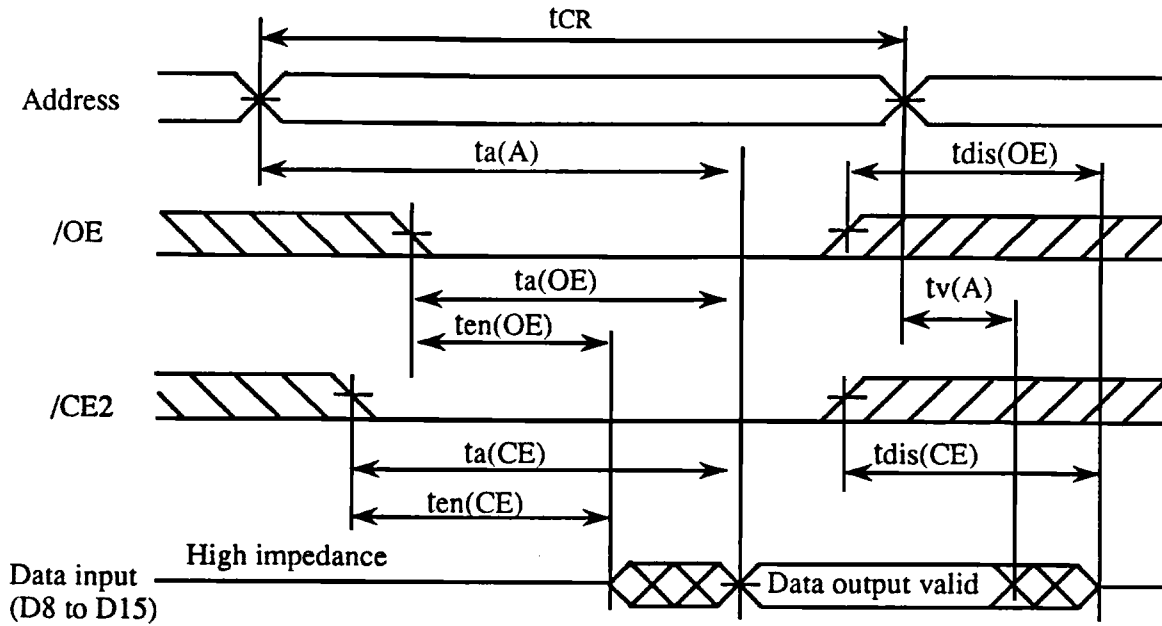
### ● Read Cycle Timing (1) (/CE2=V<sub>IH</sub> fixing) 8bits output



Note3)

1. During the read cycle, set the /WE signal high.
2. The hatched part may be either high or low.

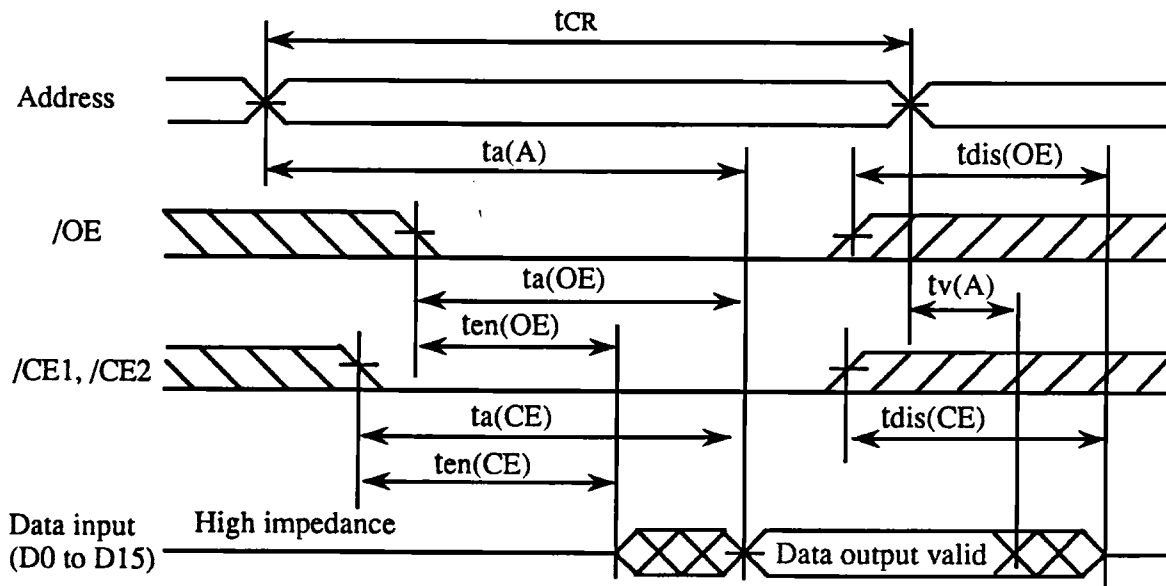
● Read Cycle Timing (2) (/CE1=VIH fixing) 8bits output



Note4)

1. During the read cycle, set the /WE signal high.
2. The hatched part may be either high or low.

● Read Cycle Timing (3) 16bits output



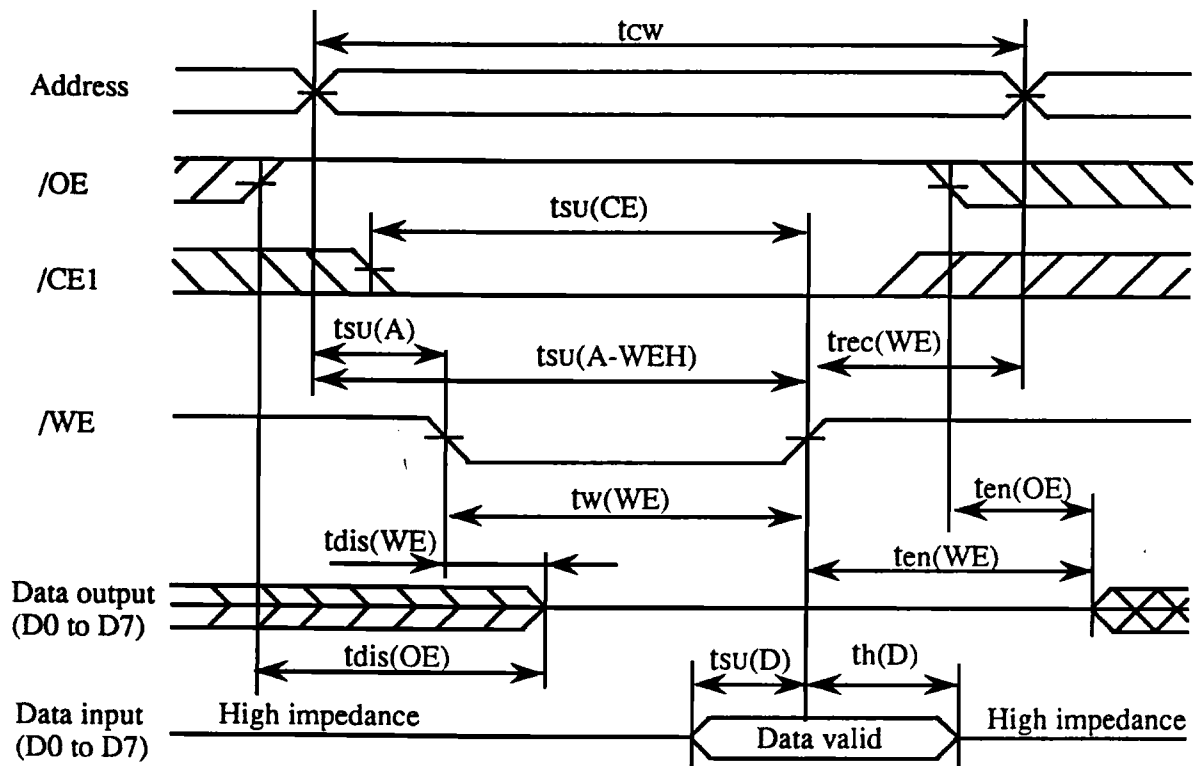
Note5)

1. During the read cycle, set the /WE signal high.
2. The hatched part may be either high or low.
3. Change the /CE1 signal and the /CE2 signal simultaneously.

## ● Write Cycle

| Parameter                      | Symbol          | Standard |      | Unit |
|--------------------------------|-----------------|----------|------|------|
|                                |                 | Min.     | Max. |      |
| Write cycle time               | $t_{CW}$        | 250      | -    | ns   |
| Write pulse width              | $t_{W(WE)}$     | 150      | -    | ns   |
| Address setup time             | $t_{SU(A)}$     | 30       | -    | ns   |
| Address setup time for /WE     | $t_{SU(A-WEH)}$ | 180      | -    | ns   |
| Card enable setup time for /WE | $t_{SU(CE)}$    | 180      | -    | ns   |
| Data setup time for /WE        | $t_{SU(D)}$     | 80       | -    | ns   |
| Data hold time                 | $t_{h(D)}$      | 30       | -    | ns   |
| Write recover time             | $t_{rec(WE)}$   | 30       | -    | ns   |
| Output disable time from /WE   | $t_{dis(WE)}$   | -        | 100  | ns   |
| Output disable time from /OE   | $t_{dis(OE)}$   | -        | 100  | ns   |
| Output enable time from /WE    | $t_{en(WE)}$    | 5        | -    | ns   |
| Output enable time from /OE    | $t_{en(OE)}$    | 5        | -    | ns   |

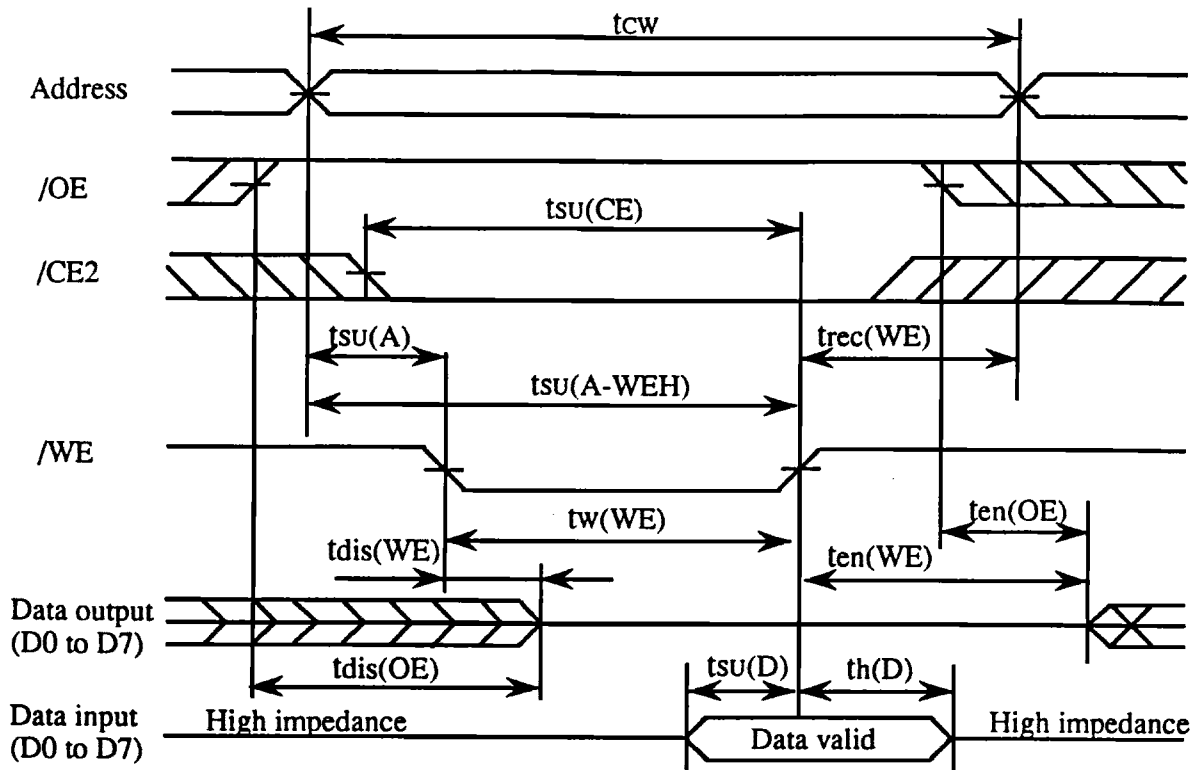
## ● Write Cycle Timing (1) (/CE2=V<sub>IH</sub> fixing) 8bits output (/WEcontrol)



### Note6)

1. Data is written when the /CE1 signal is low and the /WE signal is low and overlapped ( $t_{W(WE)}$ ).
2. When a data signal is in the output state, do not apply an input signal in a reverse phase to the output.
3. The hatched part may be either high or low.

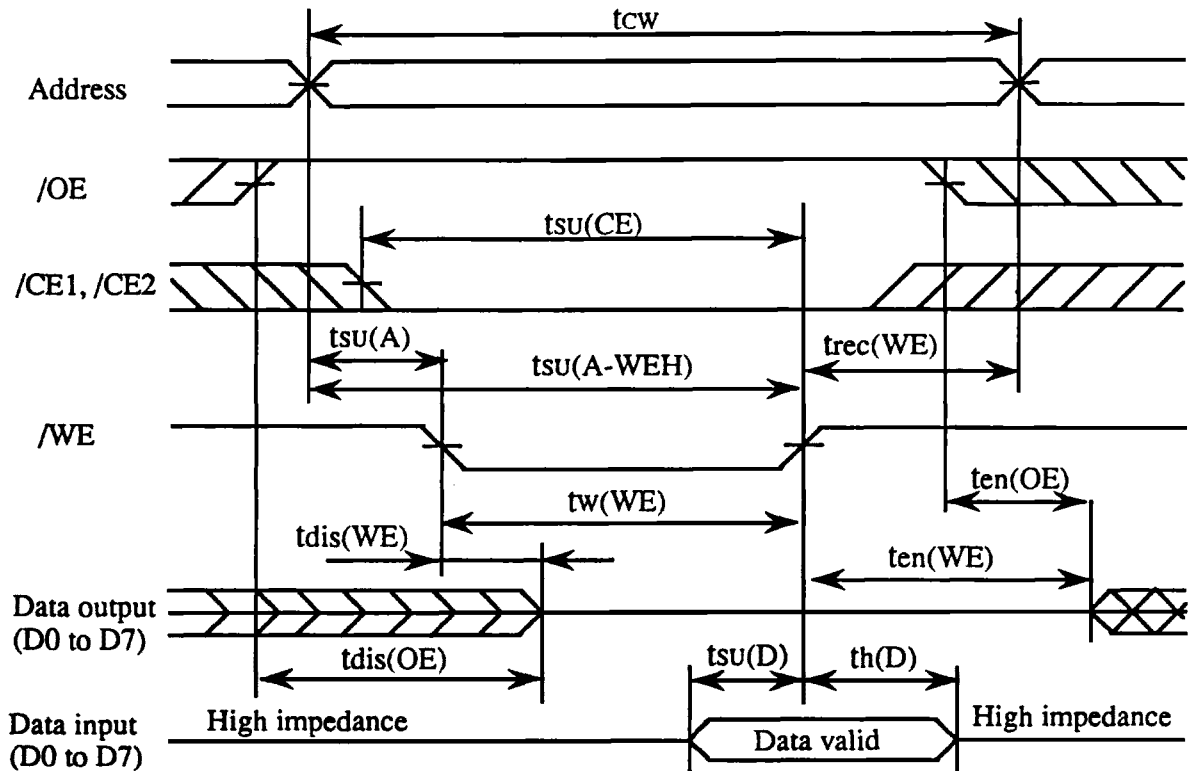
● Write Cycle Timing (2) (/CE1=VIH fixing) 8bits output (/WE control)



Note7)

1. Data is written when the /CE2 signal is low and the /WE signal is low and overlapped ( $t_w(WE)$ ).
2. When a data signal is in the output state, do not apply an input signal in a reverse phase to the output.
3. The hatched part may be either high or low.

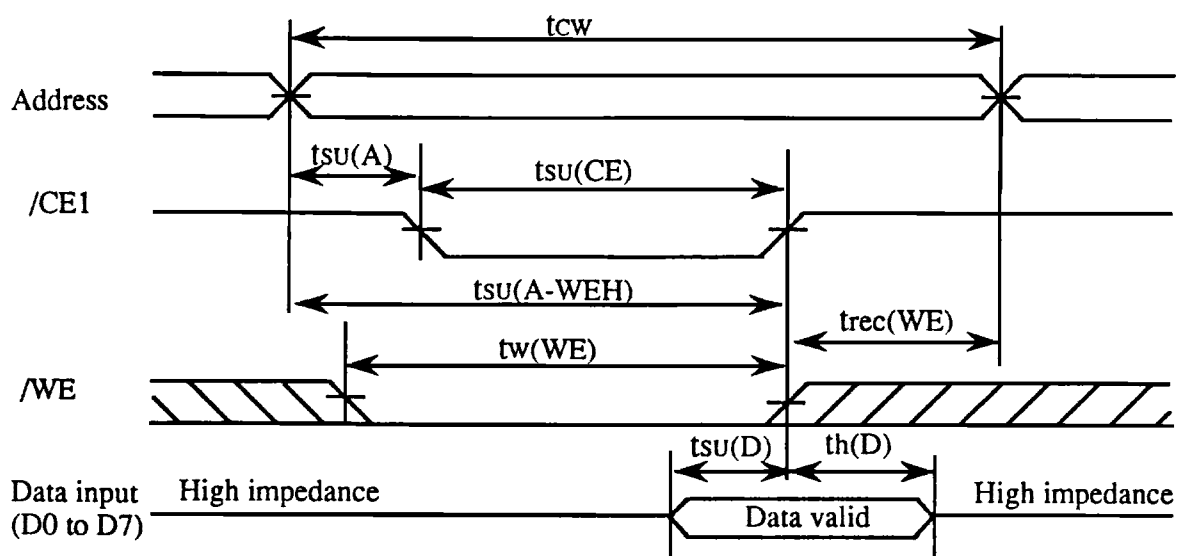
● Write Cycle Timing (3) 16bits output (/WE control)



Note8)

1. Data is written when the /CE1 and /CE2 signal is low and the /WE signal is low and overlapped ( $t_w(WE)$ ).
2. When a data signal is in the output state, do not apply an input signal in a reverse phase to the output.
3. The hatched part may be either high or low.
4. Change the /CE1 signal and the /CE2 signal simultaneously.

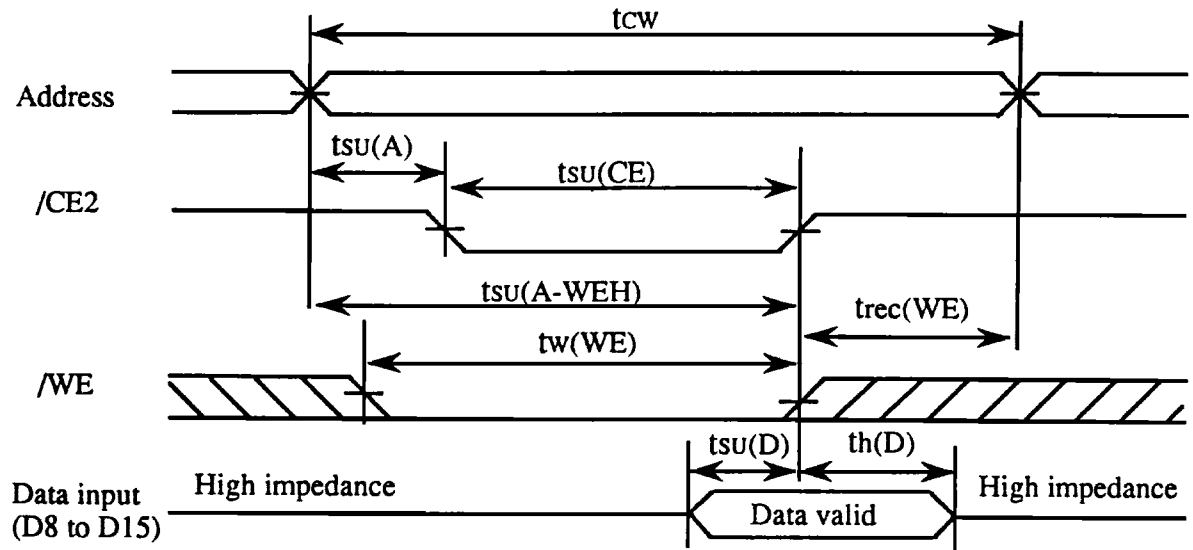
● Write Cycle Timing (4) ( $/CE2=VIH$  fixing) 8bits output ( $/CE1$  control)



Note9)

1. Data is written when the  $/CE1$  signal is low and  $/WE$  signal is low and overlapped ( $t_{SU}(CE)$ ).
2. When a data signal is in the output state, do not apply an input signal in a reverse phase to the output.
3. The hatched part may be either high or low.
4. To keep the output buffer of a data signal in the high impedance state, falling the  $/CE1$  signal simultaneously with or later than falling of the  $/WE$  signal, and rising the  $/CE1$  signal simultaneously with or earlier than rising of the  $/WE$  signal.

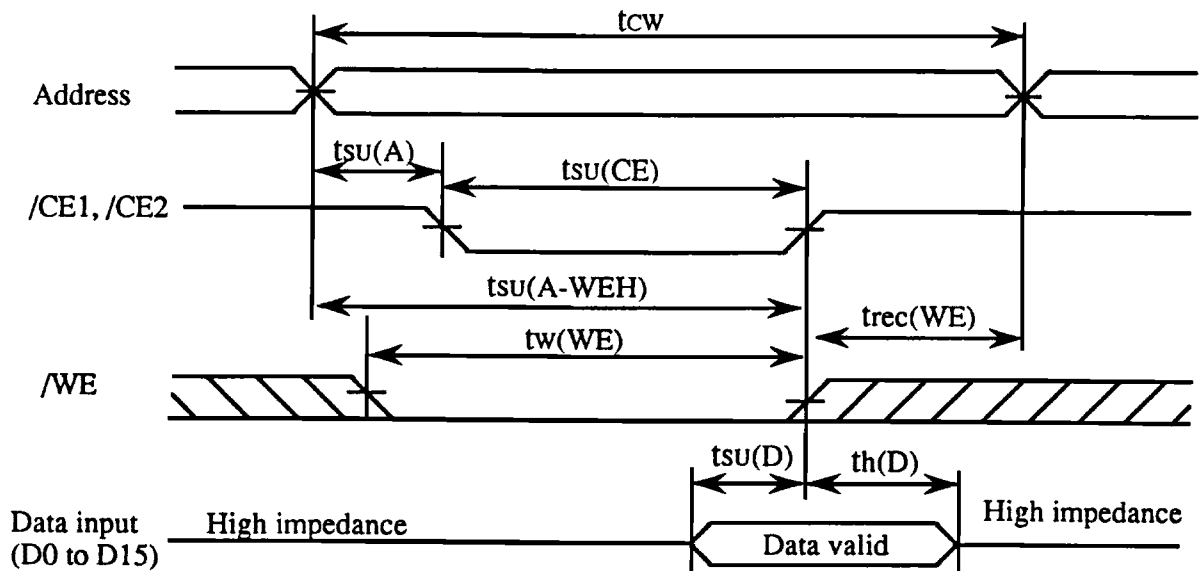
● Write Cycle Timing (5) (/CE1=VIH fixing) 8bits output (/CE2 control)



Note10)

1. Data is written when the /CE1 signal is low and /WE signal is and overlapped ( $t_{su}(CE)$ ).
2. When a data signal is in the output state, do not apply an input signal in a reverse phase to the output.
3. The hatched part may be either high or low.
4. To keep the output buffer of a data signal in the high impedance state, falling the /CE2 signal simultaneously with or later than falling of the /WE signal, and rising the /CE2 signal simultaneously with or earlier than rising of the /WE signal.

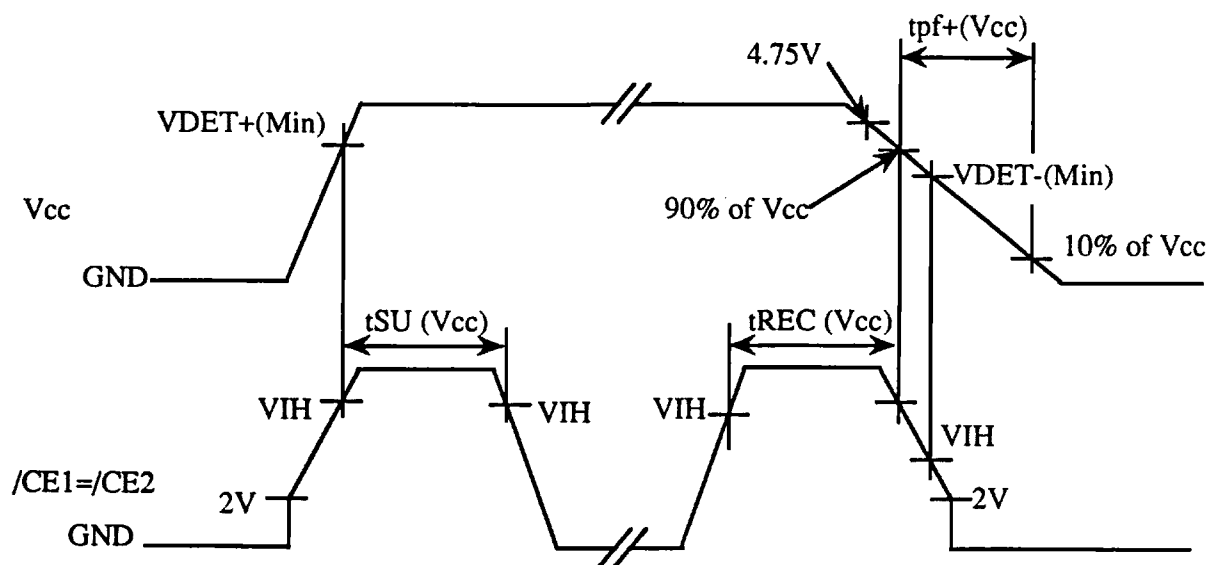
● Write Cycle Timing (6) 16bits output (/CE1, /CE2 control)



Note 11)

1. Data is written when the /CE1 and /CE2 signal is low and /WE signal is low and overlapped ( $t_{SU}(CE)$ ).
2. When a data signal is in the output state, do not apply an input signal in a reverse phase to the output.
3. The hatched part may be either high or low.
4. Change the /CE1 signal and the /CE2 signal simultaneously.
5. To keep the output buffer of a data signal in the high impedance state, falling the /CE1 signal and the /CE2 signal simultaneously with or later than falling of the /WE signal, and rising the /CE1 signal and the /CE2 signal simultaneously with or earlier than rising of the /WE signal.

### Power up / Power down Timing (Ta=+20°C)



$$(0.7 \times V_{cc} \leq V_{IH} \leq V_{cc} + 0.3)$$

| Symbol   | Parameter                         | Min. | Max. | Unit      |
|----------|-----------------------------------|------|------|-----------|
| VDET+    | Operation start detection voltage | 4.15 | 4.45 | V         |
| VDET-    | Operation stop detection voltage  | 4.05 | 4.35 | V         |
| VSU(CE)  | /CE setup time                    | 4.0  | -    | msec      |
| tREC(CE) | /CE recover time                  | 1.0  | -    | $\mu$ sec |
| Vpf(Vcc) | Vcc falling time                  | 3.0  | 300  | msec      |

#### Note12)

When inserting or removing the memory card with  $V_{cc}$  ( $5V \pm 5\%$ ) applied, keep the /CE1 and /CE2 signals in the high impedance state. Simultaneously, also keep other signals in the high impedance state. During the /CE setup time (4msec min.) after the memory card is inserted, do not access the memory card. (In this period, do not set both or one of the /CE1 and /CE2 signals low.)

■ Battery voltage detect

When the memory card is applied with  $V_{cc}$  ( $5V \pm 5\%$ ), the voltage of the battery mounted on the memory card is outputted as a digital signal.

| Period | BVD1(#63) | BVD2(#62) | Comment   |
|--------|-----------|-----------|---|
| 1*     | H         | H         | The battery voltage is normal.                          |
| 2      | H         | L         | In this period, exchange the battery.                   |
| 3      | L         | L         | The battery voltage is abnormal.(Data cannot be stored) |

Note) 1. Exchange the battery during period 1, if possible, according to the memory retention period.


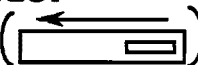
| Item           | Min. | Max. | Unit | Measurement conditions |
|----------------|------|------|------|------------------------|
| $V_{OL}$ (BVD) | 0.4  | —    | V    | $I_{OL}=5mA$           |
| $V_{OH}$ (BVD) | —    | 4.5  | V    | $I_{OH}= -4mA$         |

■ Attribute memory

The attribute memory is for storing the card attribute information. The card is not provided with attribute memory. Consequently, when address 0 is read in the same way as main memory after setting the /REG signal to the "L" level, FF(H) is output to D0-D7. The access time at this time is a maximum 300ns.

■ Write-protect switch

To protect the memory card from being written on, set the write-protect switch on the side of the memory card to PROTECT.

| Write-protect switch   | WP signal (pin 33) | Description  |
|--|--------------------|--|
| Protection mode<br>PROTECT<br>side      | H                  | Neither attribute memory nor main memory can be written on.<br>However, both attribute memory and main memory can be read. |
| Non-Protection mode<br>PROTECT<br>side  | L                  | Both attribute memory and main memory can be written on and read.  |

## Document

■ Attribute memory AC Characteristics ( $T_a=0$  to  $+55^\circ\text{C}$ ,  $V_{cc}=5\text{V} \pm 5\%$ )

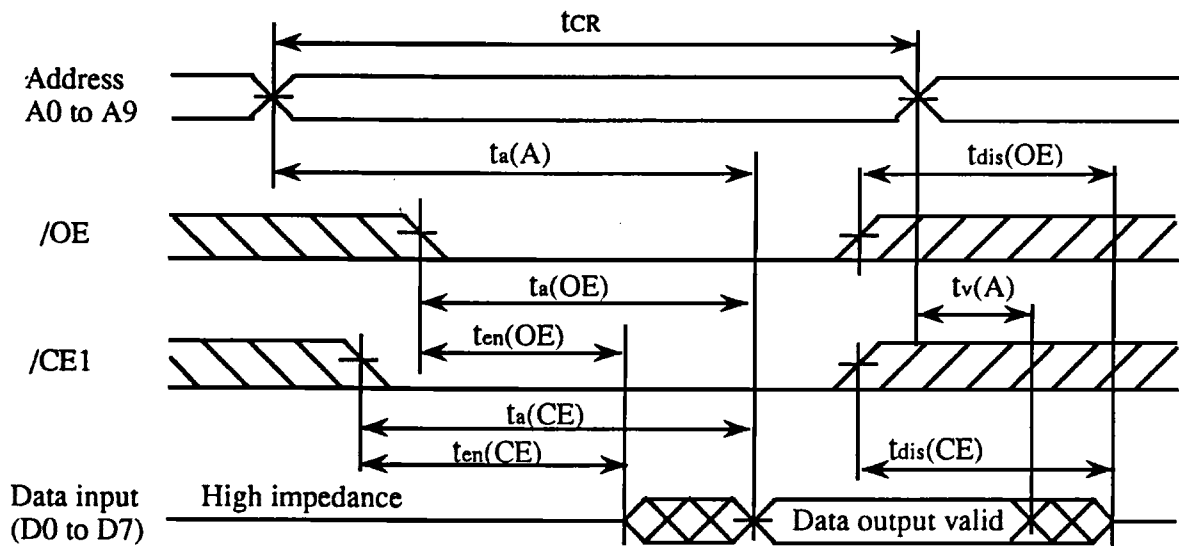
● AC Characteristics measurement Condition

- Input pulse level : 0.8 to 3.5V
- Input pulse rise and fall time : 10 ns
- Input and output timing reference level : 1.5V
- Output load : 1TTL+ $C_L$ (100pF)  
(Including scope and jig capacitance)

● Attribute memory read cycle

| Parameter                           | Symbol        | Standard |      | Unit |
|-------------------------------------|---------------|----------|------|------|
|                                     |               | Min.     | Max. |      |
| Read cycle time                     | $t_{CR}$      | 300      | —    | ns   |
| Address access time                 | $t_a(A)$      | —        | 300  | ns   |
| Card enable access time             | $t_a(CE)$     | —        | 300  | ns   |
| Output enable time                  | $t_a(OE)$     | —        | 150  | ns   |
| Output disable time from /CE1, /CE2 | $t_{dis}(CE)$ | —        | 100  | ns   |
| Output disable time from /OE        | $t_{dis}(OE)$ | —        | 100  | ns   |
| Output enable time from /CE1, /CE2  | $t_{en}(CE)$  | 5        | —    | ns   |
| Output enable time                  | $t_{en}(OE)$  | 5        | —    | ns   |
| Data valid from address change      | $t_v(A)$      | 0        | —    | ns   |

● Attribute memory read cycle waveform



Note)

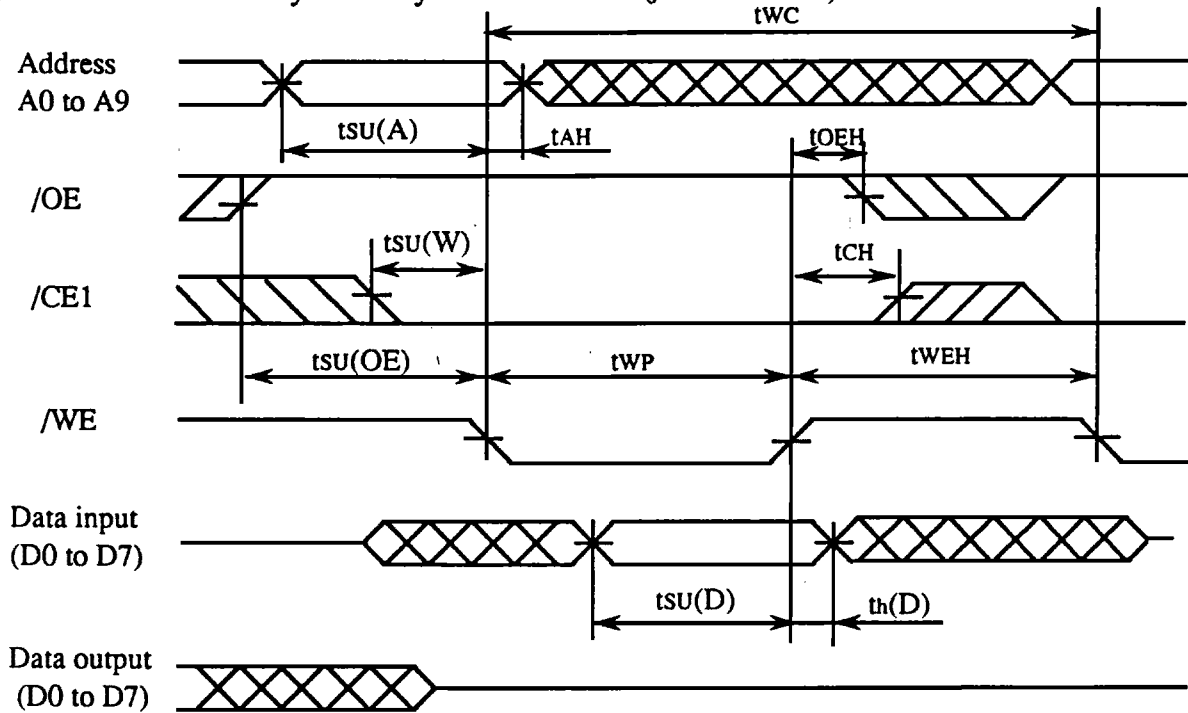
Set the /REG signal to the "L" level and the /WE signal to the "H" level when attribute memory is read, and set either the /CE2 signal to the "L" level or the /CE2 signal to the "H" level and the A0 signal to "L" level

Document

● Attribute memory write cycle

| Parameter                     | Symbol  | Standard |      | Unit |
|-------------------------------|---------|----------|------|------|
|                               |         | Min.     | Max. |      |
| Write cycle time              | tWC     | 10       | —    | ms   |
| Write pulse width             | tWP     | 180      | —    | ns   |
| Address setup time            | tSU(A)  | 10       | —    | ns   |
| Data setup time               | tSU(D)  | 100      | —    | ns   |
| Write setup time              | tSU(W)  | 0        | —    | ns   |
| Output enable setup time      | tSU(OE) | 45       | —    | ns   |
| Address retention time        | tAH     | 260      | —    | ns   |
| Write retention time          | tCH     | 0        | —    | ns   |
| Guard enable pulse width      | tCW     | 210      | —    | ns   |
| Output enable retention time  | tOEH    | 70       | —    | ns   |
| /WE high level retention time | tWEH    | 9.9      | —    | ms   |
| /CE high level retention time | tCEH    | 9.9      | —    | ms   |
| Data retention time           | tH(D)   | 80       | —    | ns   |

● Attribute memory write cycle waveform (/WE control)

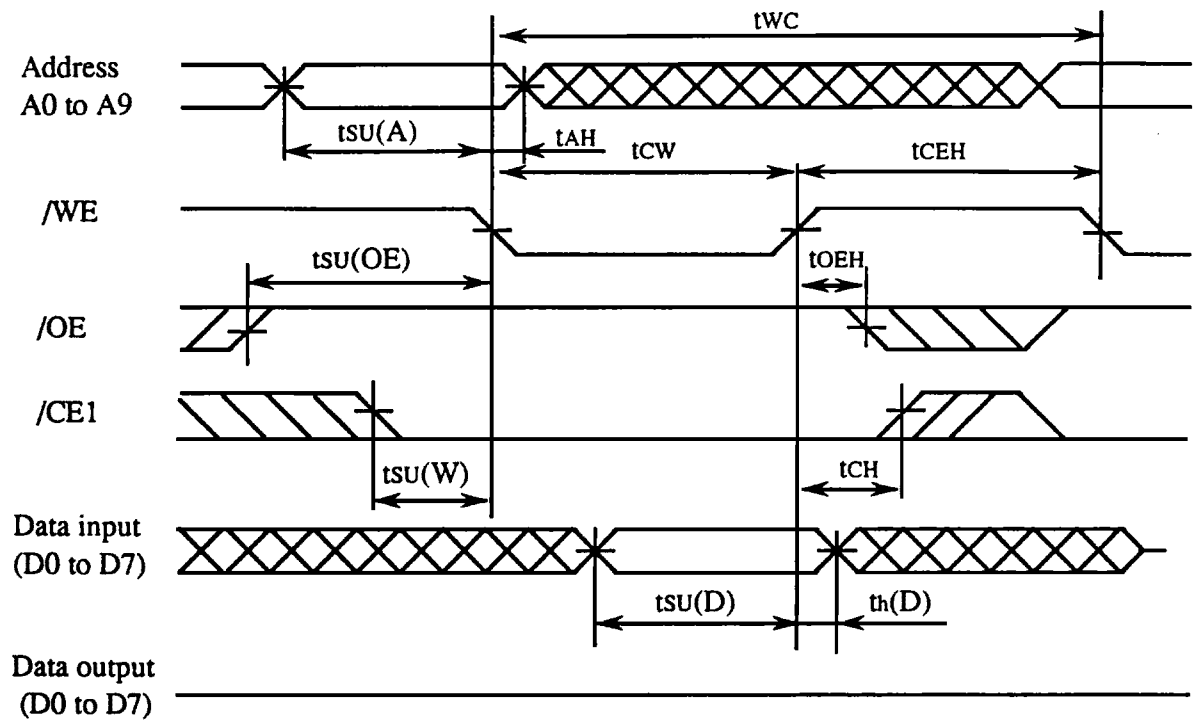


Note)

Set the /REG signal to the "L" level when attribute memory is write, and set either the /CE2 signal to the "L" level or the /CE2 signal to the "H" level and the A0 signal to the "L" level.

## Document

## ● Attribute memory write cycle waveform (/CE control)



## Note)

Set the  $\overline{\text{REG}}$  signal to the "L" level when attribute memory is write, and set either the  $\overline{\text{CE2}}$  signal to the "L" level or the  $\overline{\text{CE2}}$  signal to the "H" level and the A0 signal to the "L" level.

■ Revision Record

| Revision | Date       | Content Modification | Drawn by         | Approved by        |
|----------|------------|----------------------|------------------|--------------------|
| 0        | Sep.10.'92 | Initial issue        | <i>T. Sugano</i> | <i>K. Yamazaki</i> |