



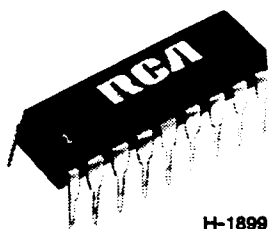
RCA Solid State

NOW
PART OF THE
NEW HARRIS SEMICONDUCTOR
HARRIS

CA3261

Linear Integrated Circuits

Advance Information



H-1899

18-Lead Dual-In-Line
Plastic Package
E Suffix

AFC/Horizontal Oscillator Signal Processor With Sync Separator and AGC

Features:

- Horizontal oscillator with AFC
- Sync separator with noise immunity
- Strobed AGC system
- IF AGC output
- Delayed outputs for forward or reverse AGC tuners
- Internal noise threshold
- High-impedance video input
- Choice of dual external time constants for sync separator noise immunity
- RF AGC delay externally controlled
- Output short-circuit protection
- LC on crystal oscillator control
- Independent horizontal AFC sync input

The RCA-CA3261* is a monolithic integrated circuit TV signal processor designed for use in color or monochrome receivers. Circuit functions include a horizontal oscillator with AFC, a sync separator, and a key AGC system. The AGC system provides output signals for IF (reverse) and tuner (forward and/or reverse). The wide frequency-range horizontal oscillator has high stability at 503.5 kHz.

Applications:

- TV Receiver-Horizontal/AFC/SYNC/AGC
- TV/CATV Sync Processor
- CRT/Monitor Systems Sync Processor
- High Line Rate Horizontal Deflection Processor
- High Stability LC Oscillator Sweep Circuits

*Formerly RCA Developmental Type No. TA11996.

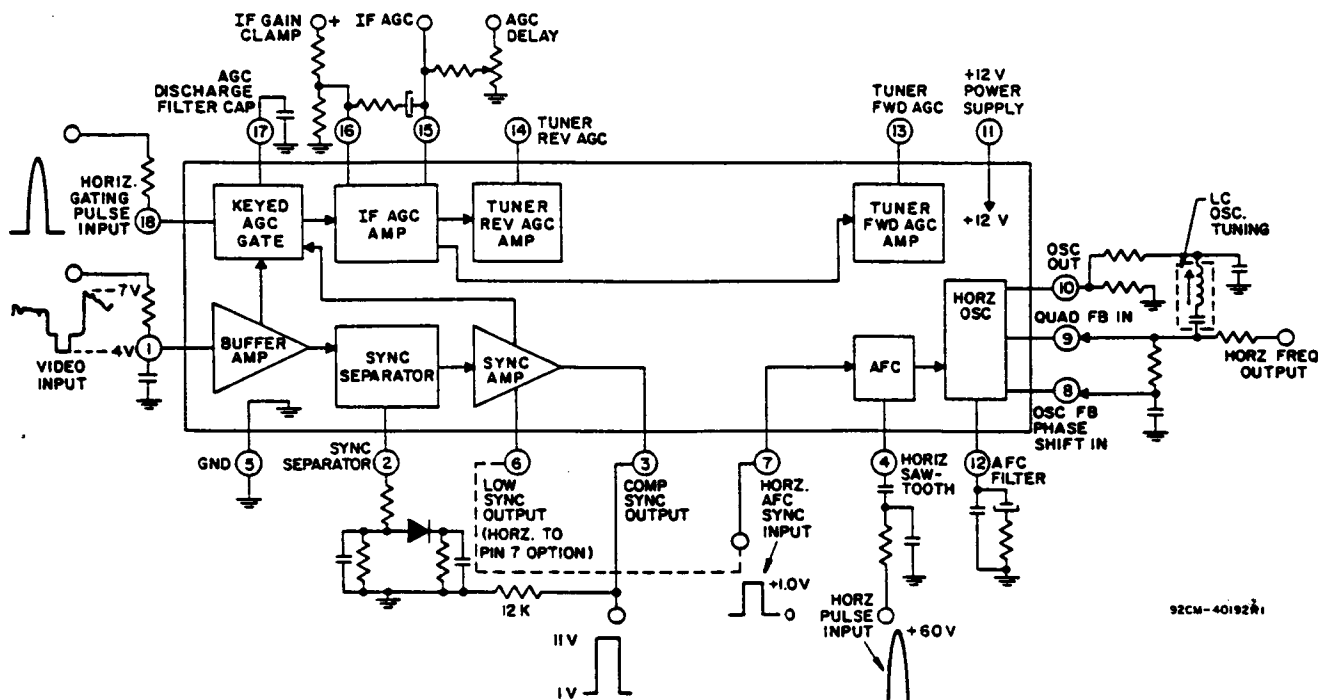


Fig. 1 - Functional block diagram of the CA3261.

Trademark(s) Registered
Marca(s) Registrada(s)

Printed in USA/5-87

Information furnished by RCA Corporation ("RCA"), a wholly owned subsidiary of General Electric Company ("GE") is believed to be accurate and reliable. However, no responsibility is assumed by RCA or GE for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of RCA or GE.

This document contains information on a product under development. RCA reserves the right to change or discontinue this product without notice.

File Number 1833

When the CA3261 is used in conjunction with the CA3202 horizontal/vertical countdown circuit, the need for horizontal and vertical hold controls is eliminated.

The CA3261 is supplied in a 16-lead dual-in-line plastic package (E suffix).

Refer to Data Sheets CA3154 (File No. 1183), CA3202* (File No. 1348) and Application Note ICAN-6802* for complete application information.

*CA3154G - CA3154E
CA3157G - CA3202E

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY VOLTAGE	15 V
DEVICE DISSIPATION:	
Up to $T_A = 55^\circ\text{C}$	750 mW
Above $T_A = 55^\circ\text{C}$	Derate linearly 7.9 mW/ $^\circ\text{C}$
AMBIENT-TEMPERATURE RANGE:	
Operating	-40 to +85 $^\circ\text{C}$
Storage	-65 to +150 $^\circ\text{C}$
LEAD TEMPERATURE (During soldering):	
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max.	+265 $^\circ\text{C}$

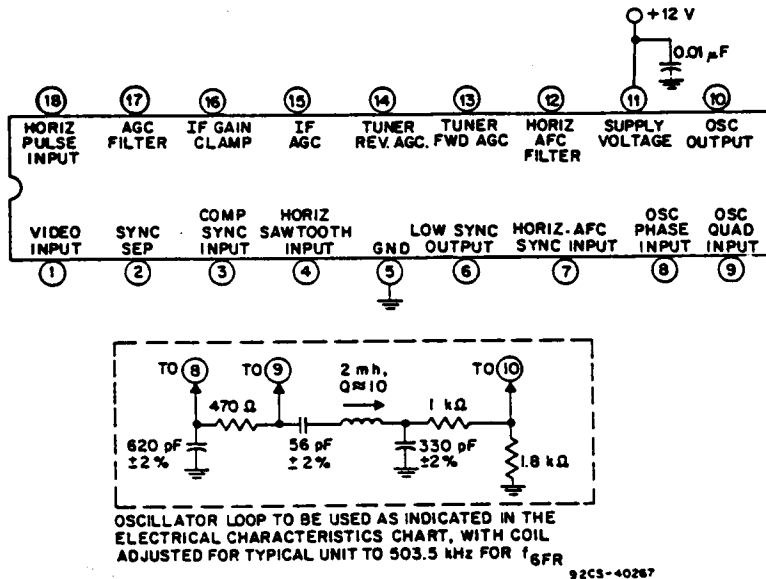


Fig. 2 - Electrical characteristics test circuit.

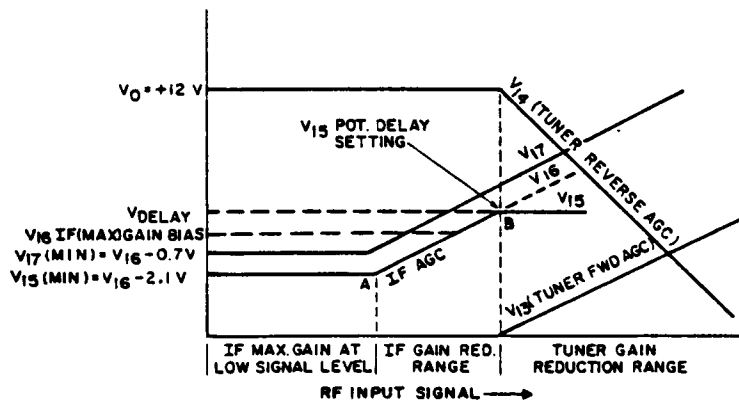


Fig. 3 - Typical operation of AGC circuits using the CA3261.

ELECTRICAL CHARACTERISTICS, at $T_A = 25^\circ\text{C}$, connect Terminal 5 to Gnd, Pin 6 to Pin 7, and Terminal 11 to +12 V unless otherwise specified.

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
	Terminals Connected As Shown Below	Min.	Typ.	Max.	
Power Supply Current, I_{11}	Measure (11) to +4V	10	—	22	mA
Video Inverter Voltage, V_2	(1) to +4V, (2) 12 k Ω to Gnd, (3) 27 k Ω to Gnd, Measure (2)	5.2	—	6.4	V
Sync Separator High Output Voltage, V_{3H}	Same as above	10.7	—	—	V
Sync Separator Low Output Voltage, V_{3L}	(1) to +4V, (3) 27 k Ω to Gnd, Measure (3)	—	—	1.3	V
Video Noise Clamp Voltage, V_3 Clamp	(1) to +3.1V, (3) 27 k Ω to Gnd, Measure (3)	10.7	—	—	V
AGC Discharge Current, I_{17} Discharge	(1) to +4.4V, (2) 10 k Ω to Gnd, (17) 470 Ω to +6V, (18) 27 k Ω to 12V, Measure (17)	0.6	—	1.4	mA
AGC Charge Current, I_{17} Charge	(1) to +3.45V, otherwise same as above	-2.1	—	-4.8	mA
AGC Comparator Leakage, I_{17} Leakage	(1) to +3.45V, (2) 10 k Ω to Gnd, (17) 4.7 k Ω to +6V, Measure (17)	-20	—	+20	μA
AGC Threshold Voltage, V_{17H}	Adj. (1) for $I_{15} = 0 \pm 0.1$ mA, (2) 10 k Ω to Gnd, (17) 4.7 k Ω to +6V, (18) 27 k Ω to +12V, Measure (1)	3.8	4	4.3	V
Minimum IF AGC, V_{15L}	(13) 10 k Ω to Gnd, (14) 10 k Ω to +12V, (15) 22 k Ω to +5V, (16) 1 k Ω to +2.95V, (18) 1 k Ω to +2.2V, Measure (15)	0.75	—	1.25	V
Forward Tuner AGC Leakage Current, I_{13} Leakage	(13) 10 k Ω to Gnd, (14) 10 k Ω to 12V, (15) 2.2 k Ω to +5V, (16) 1 k Ω to +2.95V, (17) 1 k Ω to +5.3V, Measure (13)	-20	—	+20	μA
Reverse Tuner AGC Leakage, I_{14} Leakage	Same as above, but Measure (14)	-10	—	+10	μA
IF AGC High Voltage, V_{15H}	Same as above, but Measure (15)	3.65	—	4.15	V
Forward Tuner AGC Low Voltage, V_{13L}	(13) 3.6 k Ω to Gnd, (14) 3.16 k Ω to +12V, (15) 2.2 k Ω to +5V, (16) 1 k Ω to +2.95V, (17) 1 k Ω to +7.9V, Measure (13)	0.8	—	3.2	V
Reverse Tuner AGC Low Voltage, V_{14L}	Same as above, but Measure (14)	1.65	—	3.25	V
Maximum IF AGC Voltage, V_{15H}	(13) 10 k Ω to Gnd, (14) 10 k Ω to +12V, (15) 2.2 k Ω to +5V, (16) 1 k Ω to +2.95V, (17) 1 k Ω to +7.9V, Measure (15)	4.85	—	5.2	V
Phase Detector Leakage Current, I_{12L}	(2) 10 k Ω to Gnd, (3) to Gnd, (4) 5 k Ω to +3.8 V, (12) 10 k Ω to +6V, Limit Gnd at (3) to 10 sec., Measure (12)	-5	—	+5	μA
Phase Detector Bias Voltage, V_4		2.65	—	3.1	V
Oscillator Output Voltage, V_6	Connect osc-loop shown in test circuit to (8), (7), (9); (10) to Gnd for 10 sec. max., Measure (8)	0.6	—	1.6	V_{p-p}
Oscillator Free-Running Frequency f_{FR}	Same as above	475	—	535	kHz
Oscillator Frequency High, f_{BH}	Connect osc-CKT shown in test CKT to (12), (9), (10); (2) 10 k Ω to Gnd, (4) 5 k Ω to +18V, Measure (8)	520	—	—	kHz
Oscillator Frequency Low, f_{BL}	Same as above except (4) 5 k Ω to +3.8V	—	—	485	kHz
Sync Separator Short Circuit, I_3 Max.	(3) 10 Ω to Gnd for 10 sec. max.	—	—	40	mA
Oscillator Output Short Circuit, I_{10} Max.	(10) 10 Ω to Gnd for 10 sec. max. (3) 10 Ω to Gnd for 10 sec. max.	—	—	130	mA

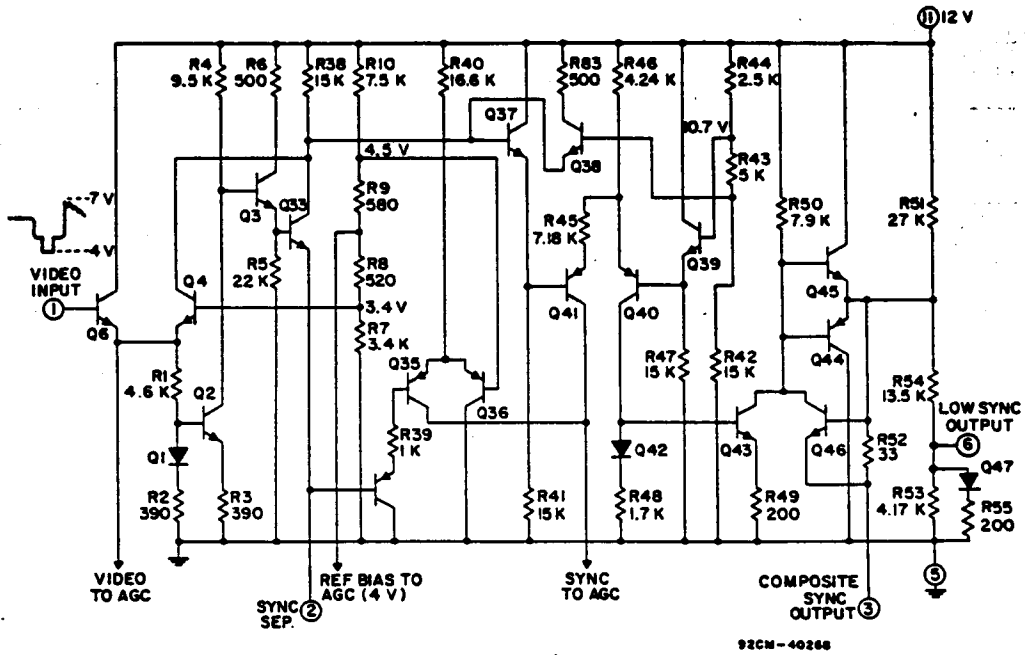


Fig. 4 - Schematic of sync separator section of the CA3261.

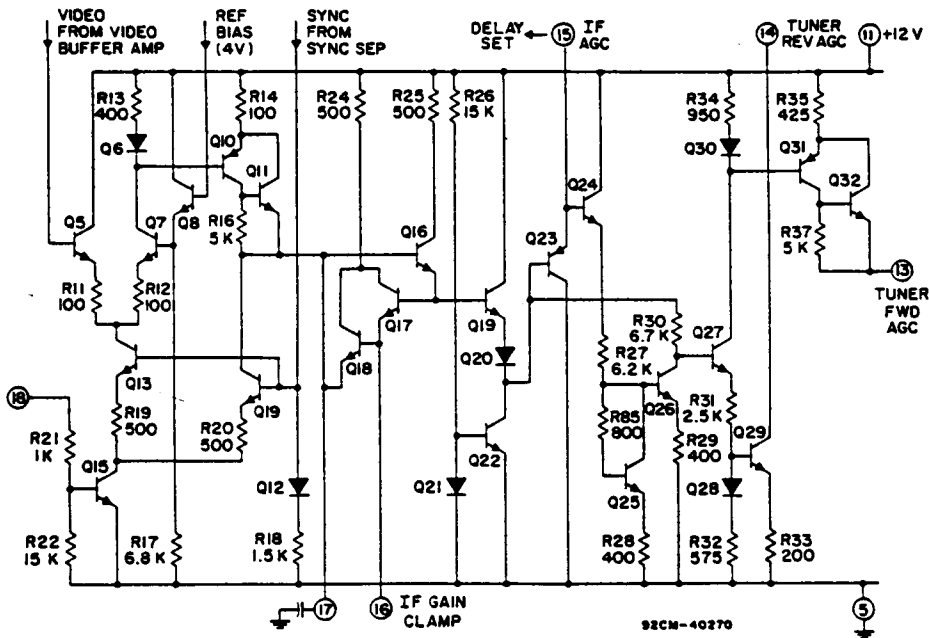


Fig. 5 - Schematic of AGC section of the CA3261.

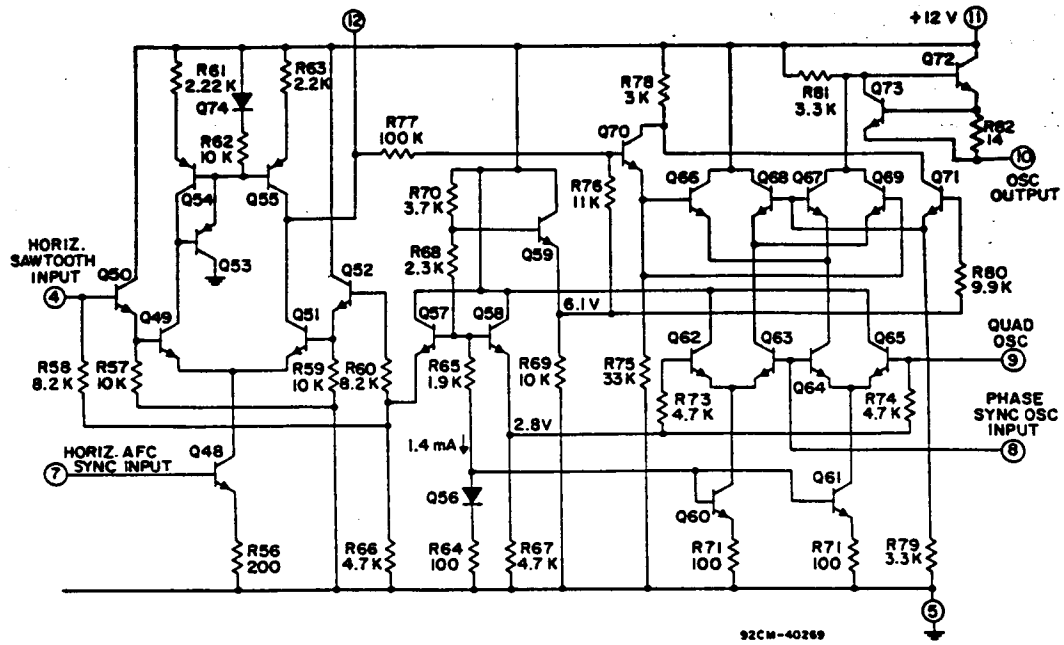


Fig. 6 - Schematic of AFC-oscillator section of the CA3261.

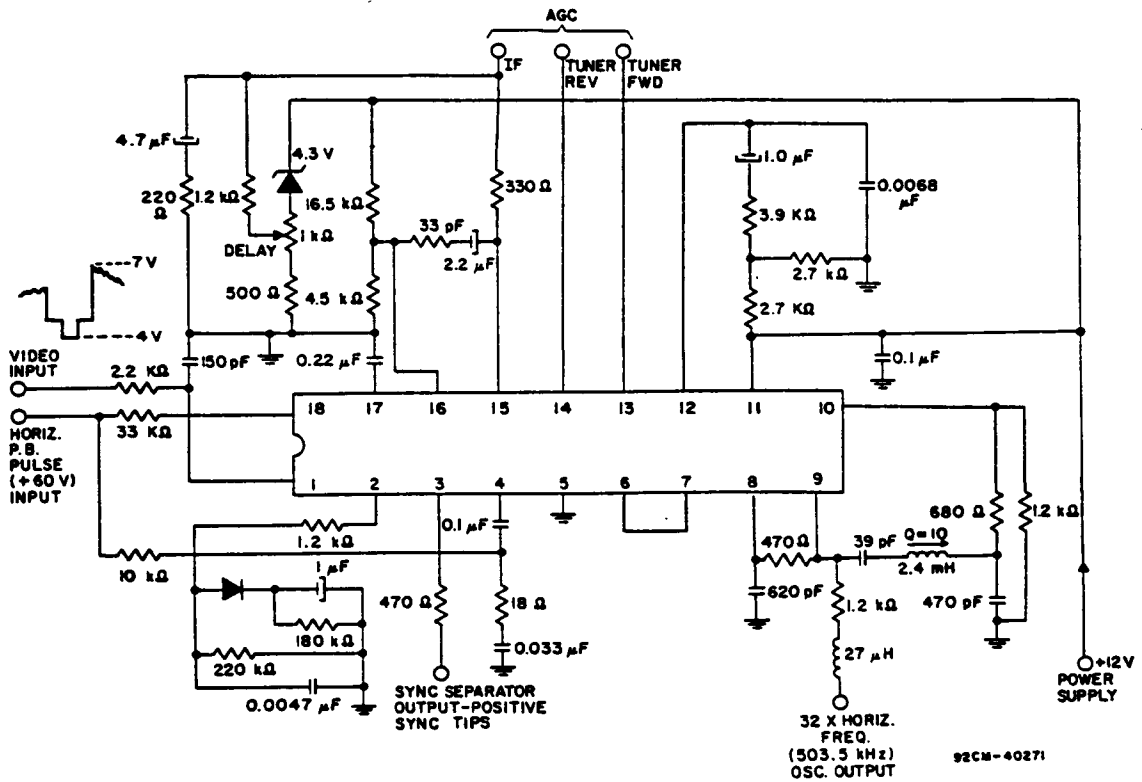


Fig. 7 - Typical application of the CA3261.

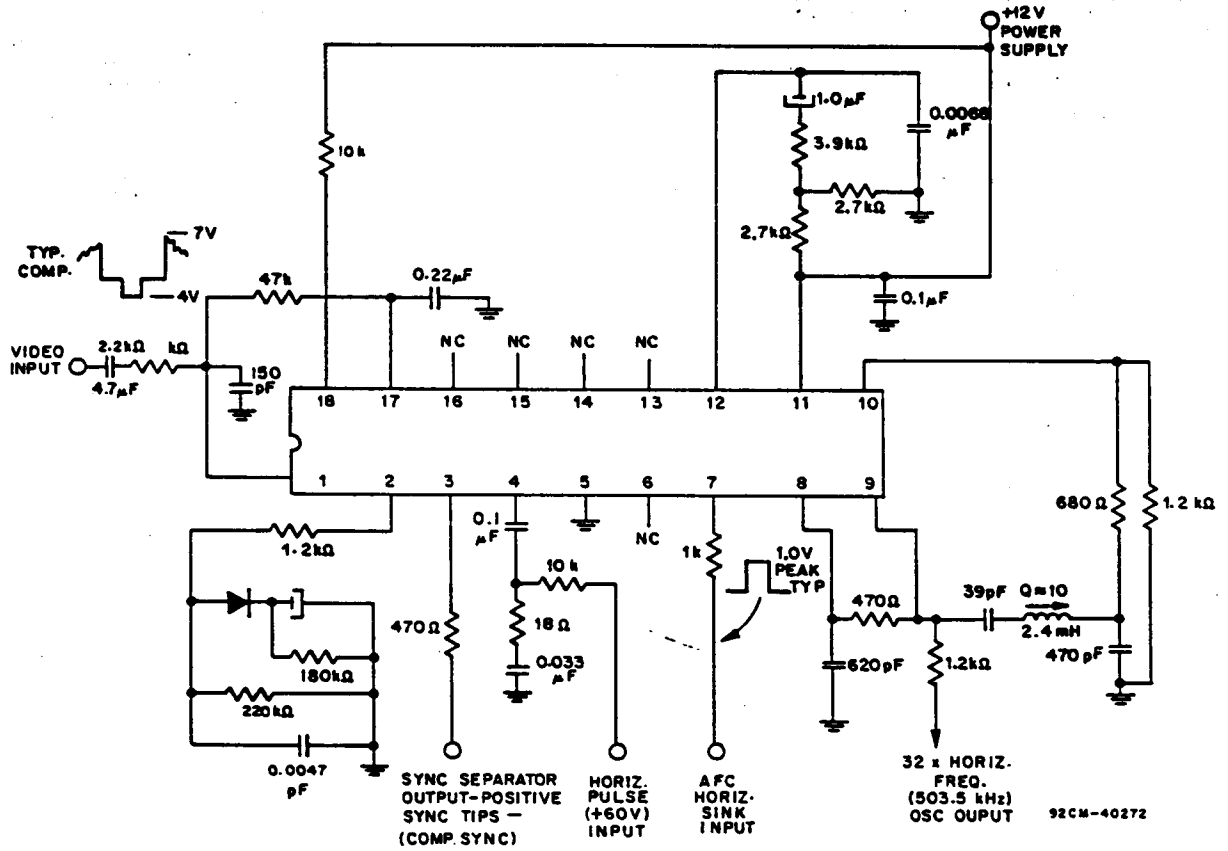
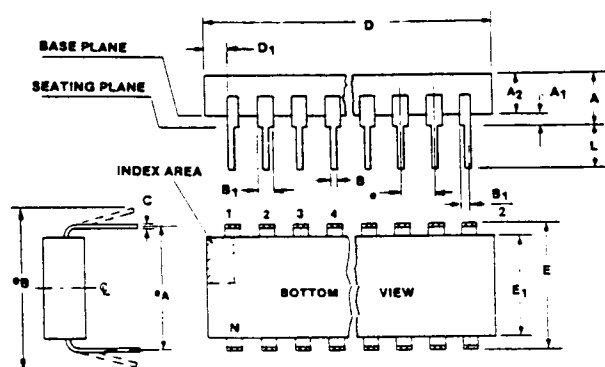


Fig. 8 - CA3261 horizontal oscillator, AFC and sync separator using the AGC for a sync tip clamp.

DIMENSIONAL OUTLINE

(E) Suffix (JEDEC MS-001-AD)
18-Lead Dual-in-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A ₁	0.015	—	0.39	—	9
A ₂	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B ₁	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.845	0.925	21.47	23.49	4
D ₁	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E ₁	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e _A	0.300 BSC		7.62 BSC		9
e _B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	18		18		11

Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions

$$1, N, \frac{N}{2}, \frac{N}{2} + 1.$$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E₁ does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.

92CS-39996

9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D₁ at the left end of the package must equal dimension D₁ at the right end of the package within 0.030 in. (0.76 mm).
13. Pointed or rounded lead tips are preferred to ease insertion.
14. For automatic insertion, any raised irregularity on the top surface (step, mess, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.