HN62438N Series — Preliminary

T-46-13-15

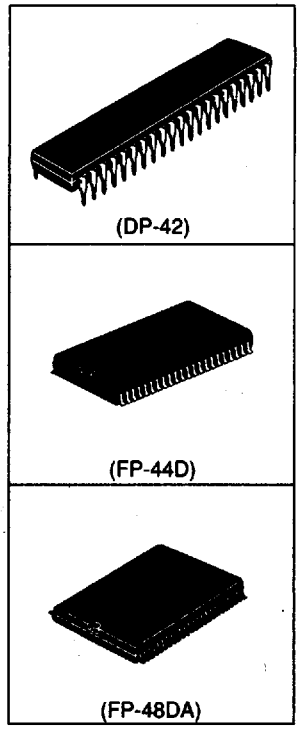
8M (512K x 16-bit) and (1M x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN62438N Series is an 8-Megabit CMOS Mask Programmable Read Only Memory organized either as 524,288 x 16-bit or as 1,048,576 x 8-bit.

The high density and high speed Nibble Access provide enough capacity and high performance to be used in a system using a high speed 16-bit or 32-bit microcomputer. In addition the low power consumption of this device makes it ideal for battery powered, portable systems.

Hitachi's HN62438N is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP and 44-lead Plastic SOP packages. The HN62438N is also packaged in a 44-lead Plastic TSOP and a 48-lead Plastic SOP.



■ FEATURES

- Single Power Supply
  V_{CC} = 5 V ± 10%
- Fast Access Times:
  120 ns/150 ns (max)
- Nibble Access Times:
  60 ns/70 ns (max)
- Low Power Consumption:
  Active Current: 100 mW (typ)
  Standby Current: 5 µW (typ)
- User Selectable Organization:
  512K x 16-bit (Word-Wide)
  1M x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
  42-pin Plastic DIP
  44-lead Plastic SOP
  44-lead Plastic TSOP (Type II)
  48-lead Plastic SOP

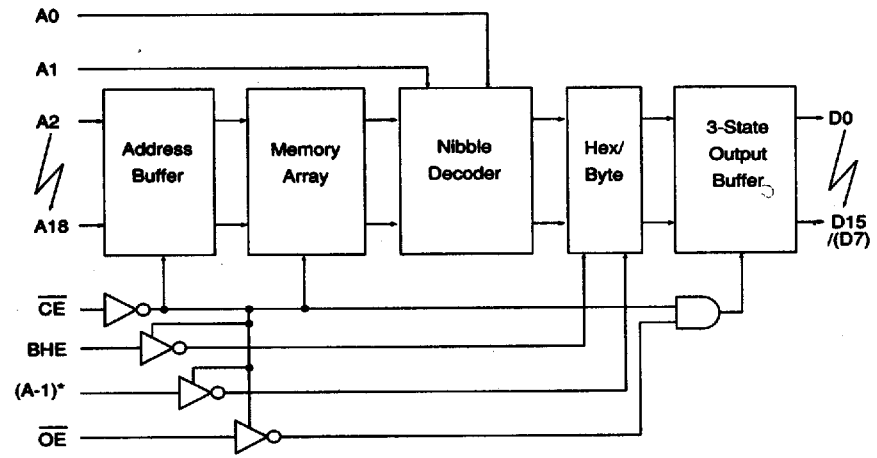
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62438PN-12	120 ns	42-pin Plastic DIP
HN62438PN-15	150 ns	(DP-42)
HN62438FBN-12	120 ns	44-lead Plastic SOP
HN62438FBN-15	150 ns	(FP-44D)
HN62438TTN-12	120 ns	44-lead Plastic TSOP
HN62438TTN-15	150 ns	(TTP-44D)
HN62438FN-12	120 ns	48-lead Plastic SOP
HN62438FN-15	150 ns	(FP-48DA)

PIN DESCRIPTION

Pin Name	Function
A_0 - A_{18}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



(BD.HN62438N)

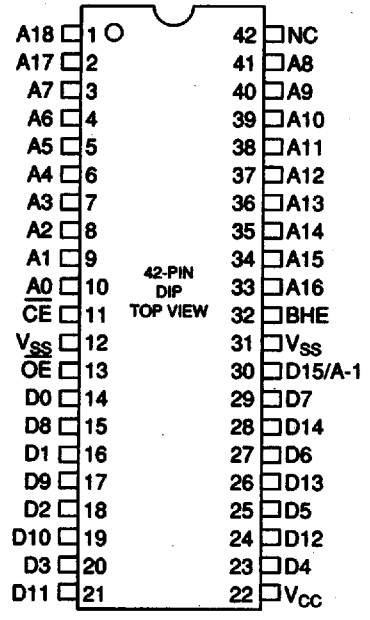
Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

5

■ PIN ARRANGEMENT

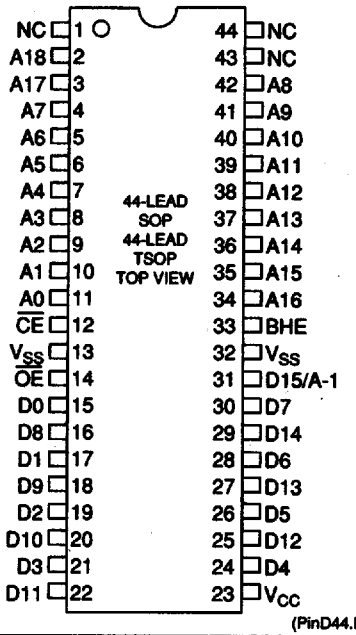
T-46-13-15

HN62438PN Series



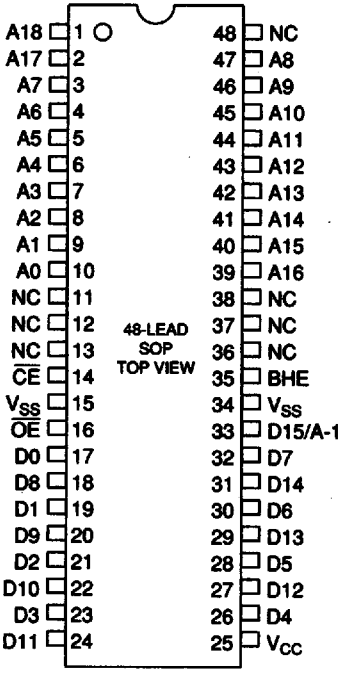
(PinD42.HN62438N)

HN62438FBN Series
HN62438TTN Series



(PinD44.HN62438N)

HN62438FN Series



Note:
Pins 11, 12, 13, 36, 37 and 38 are connected to the inner lead frame.

(PinT248.HN62438N)

HITACHI/ LOGIC/ARRAYS/MEM

T-46-13-15

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	15	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min.
Standby V_{CC} Current	I_{SB}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
Input Voltage	V_{IH}	2.4	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.45	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 1.6 mA

5

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Test Conditions

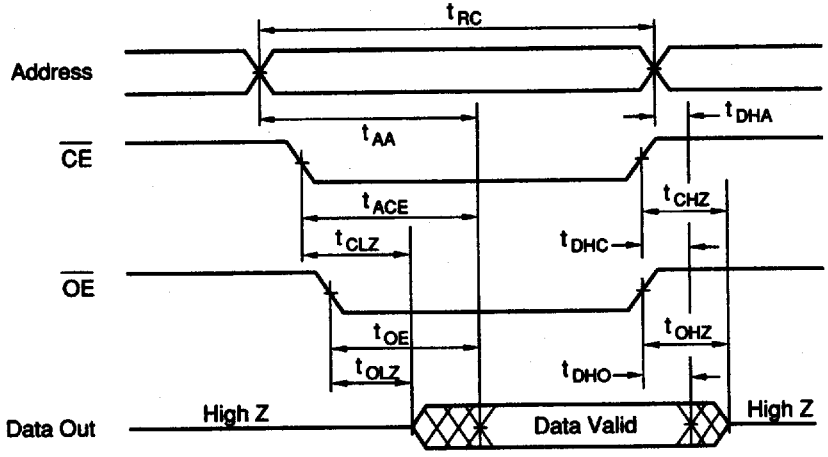
- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

		HN62438N-12		HN62438N-15		
Item	Symbol	Min.	Max.	Min.	Max.	Unit
Read Cycle Time	t_{RC}	120	-	120	-	ns
Nibble Read Cycle Time	t_{NC}	60	-	70	-	ns
Address Access Time	t_{AA}	-	120	-	150	ns
Nibble Address Access Time	t_{NA}	-	60	-	70	ns
$\overline{CE}$ Access Time	t_{ACE}	-	120	-	150	ns
$\overline{OE}$ Access Time	t_{OE}	-	60	-	70	ns
BHE Access Time	t_{BHE}	-	120	-	150	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	-	0	-	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	-	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	0	-	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}[1]	-	60	-	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}[1]	-	60	-	70	ns
BHE to Output in High Z	t_{BHZ}[1]	-	60	-	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	-	10	-	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	-	10	-	ns
BHE to Output in Low Z	t_{BLZ}	10	-	10	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, and t_{BHZ} define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM

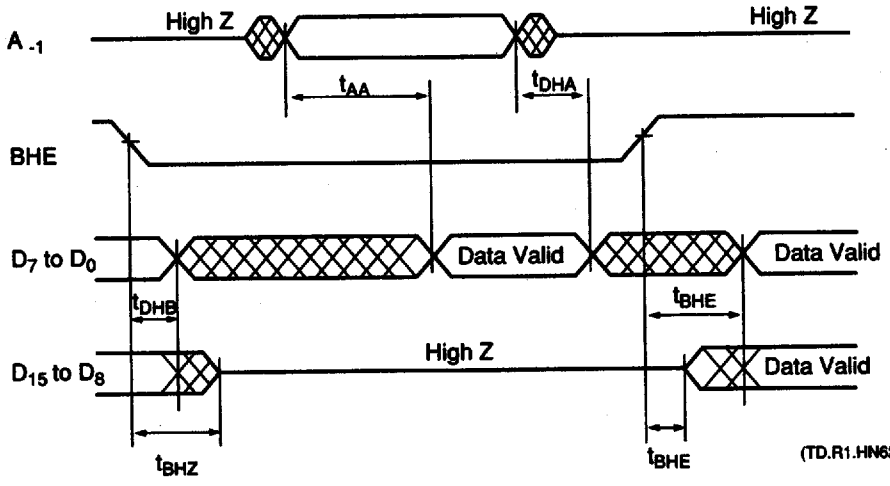
Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})



(TD.R.HN62438N)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

Word Mode/Byte Mode Switch

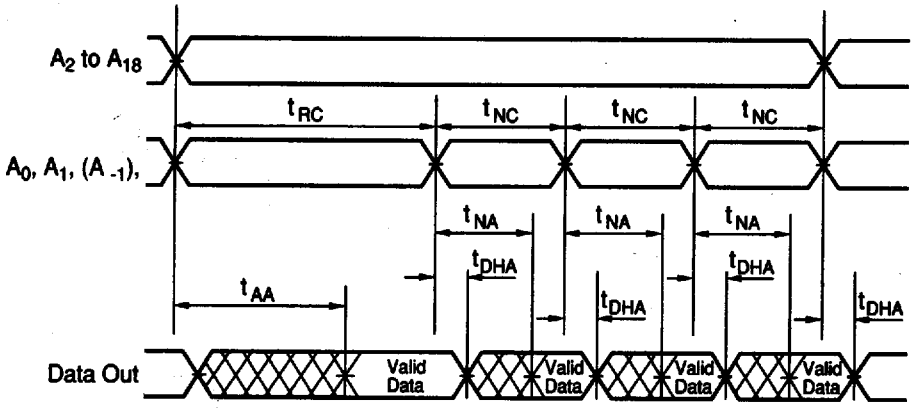


(TD.R1.HN62438N)

Note: 1. $\overline{CE}$ and $\overline{OE}$ are of select status. A_{18} to A_0 are fixed.
2. D_{15}/A_{-1} terminal is of output state when BHE = V_{IH}, $\overline{CE}$ and $\overline{OE}$ are of selected state. At this time, an input signal that is of the inverse phase to the output should not be impressed.

5

Nibble Mode



(TD.RN.HN62438N)

Note: $\overline{CE}$ and $\overline{OE}$ are enable.