# Digital video encoder, GENLOCK-capable — SAA7199B

## 1. FEATURES

- Monolithic integrated CMOS video encoder circuit
- Standard MPU (12 lines) and I²C-bus interfaces for controls
- Three 8-bit signal inputs PD(7-0) for RGB respectively YUV or indexed colour signals (Tables 10 to 17)
- Square pixel and CCIR input data rates
- Band-limited composite sync pulses
- Three 256X8 colour look-up tables (CLUTs) e. g. for gamma-correction
- External subcarrier from a digital decoder (SAA7151B or SAA7191B)
- Multi-purpose key for real-time format switching
- Autonomous internal blanking
- Optional GENLOCK operation with adjustable horizontal sync timing and adjustable subcarrier phase
- Stable GENLOCK operation in VCR standard playback mode
- Optional still video capture extension
- Three suitable video 9-bit digital-to-analog converters
- Composite analog output signals CVBS, Y and C for PAL/NTSC
- "Line 21" data insertion possible

## 2. GENERAL DESCRIPTION

The SAA7199B encodes digital base-band colour/video data into analog Y, C and CVBS signals (S-Video included). Pixel clock and data are line-locked to the horizontal scanning frequency of the video signal. The circuit can be used in a square pixel or in a consumer TV application. Flexibility is provided by programming facilities via MPU-bus (parallel) or I²C-bus (serial).

## 3. QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DDD}$ | digital supply voltage range (pins 2, 21 and 41) | 4.5 | 5.0 | 5.5 | V |
| $V_{DDA}$ | analog supply voltage range (pins 64, 66, 70 and 72) | 4.75 | 5.0 | 5.25 | V |
| $I_P$ | total supply current | - | - | 200 | mA |
| $V_I$ | input signal levels | TTL-compatible | | | |
| $V_o$ | analog output signals Y, C and CVBS without load (peak-to-peak value) | - | 2 | - | V |
| $R_L$ | output load resistance | 90 | - | - | Ω |
| ILE | LF integral linearity error in output signal (9-bit DAC) | - | - | ±1 | LSB |
| DLE | LF differential linearity error in output signal (9-bit DAC) | - | - | ±0.5 | LSB |
| $T_{amb}$ | operating ambient temperature range | 0 | - | 70 | °C |

## 4. ORDERING INFORMATION

| EXTENDED TYPE NUMBER | PACKAGE | | | |
|---|---|---|---|---|
| | PINS | PIN POSITION | MATERIAL | CODE |
| SAA7199B | 84 | PLCC | plastic | SOT189CG |

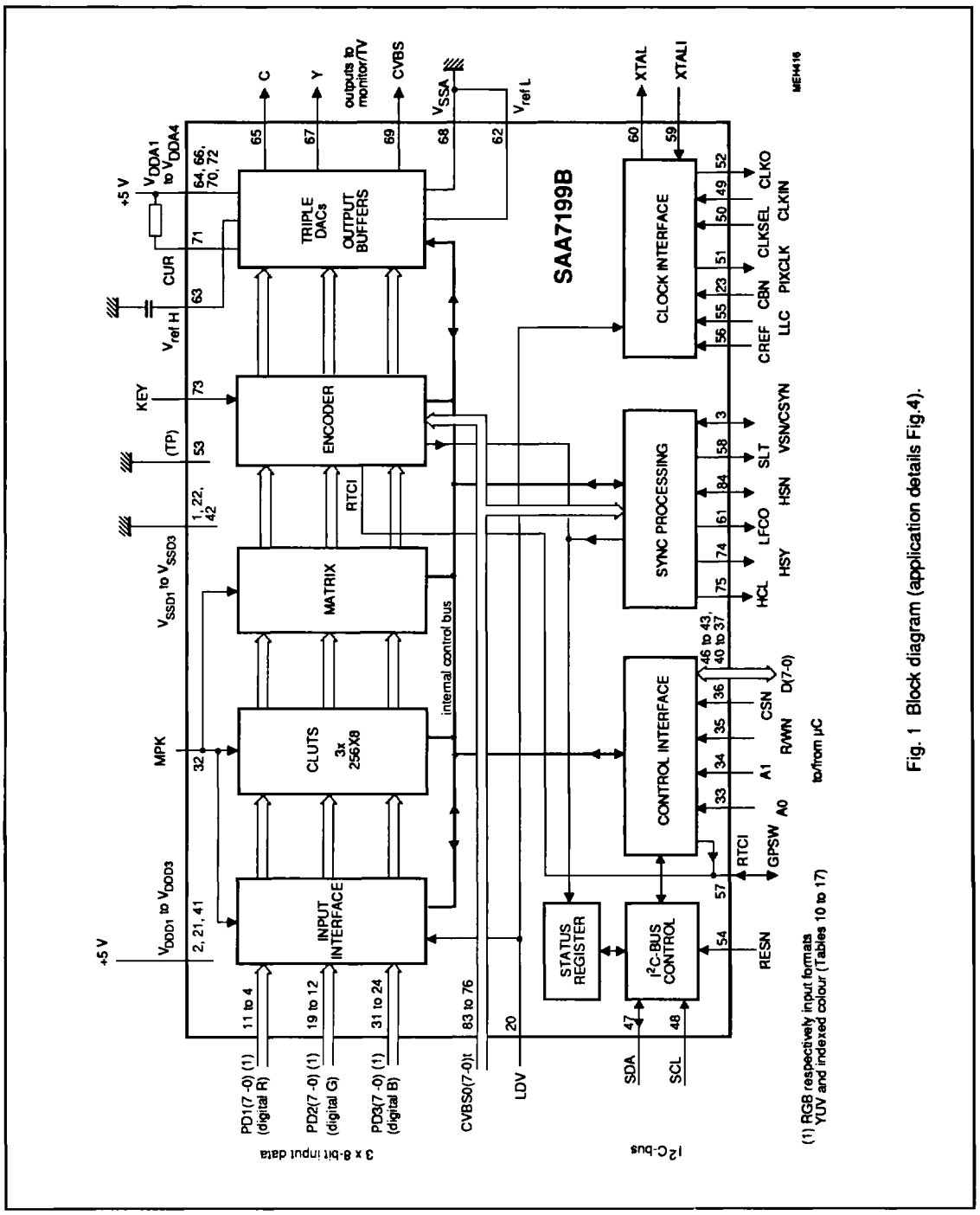



Fig. 1 Block diagram (application details Fig.4).

## PINNING

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| $V_{SSD1}$ | 1 | digital ground 1 (0 V) |
| $V_{DDD1}$ | 2 | +5 V digital supply 1 |
| VSN | 3 | vertical sync output (3-state), conditionally composite sync output; active LOW or active HIGH |
| PD1(0) | 4 | data 1 input: digital signal R (red) respectively V signal (formats in Table 6) |
| PD1(1) | 5 | |
| PD1(2) | 6 | |
| PD1(3) | 7 | |
| PD1(4) | 8 | |
| PD1(5) | 9 | |
| PD1(6) | 10 | |
| PD1(7) | 11 | |
| PD2(0) | 12 | data 2 input: digital signal G (green) respectively Y signal or indexed colour data (formats in Table 6) |
| PD2(1) | 13 | |
| PD2(2) | 14 | |
| PD2(3) | 15 | |
| PD2(4) | 16 | |
| PD2(5) | 17 | |
| PD2(6) | 18 | |
| PD2(7) | 19 | |
| LDV | 20 | load data clock input signal to input interface (samples PDn(7-0), CBN, MPK, KEY and RTCI) |
| $V_{DDD2}$ | 21 | +5 digital supply 2 |
| $V_{SSD2}$ | 22 | digital ground 2 (0 V) |
| CBN | 23 | composite blanking input; active LOW |
| PD3(0) | 24 | data 3 input: digital signal B (blue) respectively U signal (formats in Table 6) |
| PD3(1) | 25 | |
| PD3(2) | 26 | |
| PD3(3) | 27 | |
| PD3(4) | 28 | |
| PD3(5) | 29 | |
| PD3(6) | 30 | |
| PD3(7) | 31 | |
| MPK | 32 | multi-purpose key; active HIGH |
| A0 | 33 | subaddress bit A0 for microcomputer access (Table 3) |
| A1 | 34 | subaddress bit A1 for microcomputer access (Table 3) |

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| R/WN | 35 | read/ write not input signal from microcontroller |
| CSN | 36 | chip select input for parallel interface; active LOW |
| D0 | 37 | bidirectional port from/to microcontroller (bits D3 to D0) |
| D1 | 38 | |
| D2 | 39 | |
| D3 | 40 | |
| $V_{DDD3}$ | 41 | +5 V digital supply 3 |
| $V_{SSD3}$ | 42 | digital ground 3 |
| D4 | 43 | bidirectional port from/to microcontroller (bits D7 to D4) |
| D5 | 44 | |
| D6 | 45 | |
| D7 | 46 | |
| SDA | 47 | $I^2C$-bus data line |
| SCL | 48 | $I^2C$-bus clock line |
| CLKIN | 49 | external clock signal input (maximum 60 MHz) |
| CLKSEL | 50 | clock source select input |
| PIXCLK | 51 | CLKO/2 or conditionally CLKO output signal |
| CLKO | 52 | selected clock output signal (LLC or CLKIN) |
| TP | 53 | connect to ground (test pin) |
| RESN | 54 | reset input; active LOW |
| LLC | 55 | line-locked clock input signal from external CGC |
| CREF | 56 | clock qualifier of external CGC |
| GPSW / RTCI | 57 | general purpose switch output (set via $I^2C$-bus or MPU-bus); real-time control input, defined by $I^2C$ or MPU programming |
| SLT | 58 | GENLOCK flag (3-state): HIGH = sync lost in GENLOCK mode; LOW = otherwise |
| XTALI | 59 | crystal oscillator input (26.8 or 24.576 MHz) |
| XTAL | 60 | crystal oscillator output |
| LFCO | 61 | line frequency control output signal for external CGC |
| $V_{ref\,L}$ | 62 | reference LOW voltage of DACs (resistor chains) |
| $V_{ref\,H}$ | 63 | reference HIGH voltage of DACs (resistor chains) |
| $V_{DDA4}$ | 64 | +5 V analog supply 4 for resistor chains of the DACs |
| C | 65 | chrominance analog output signal C |
| $V_{DDA1}$ | 66 | +5 V analog supply 1 for output buffer amplifier of DAC1 |
| Y | 67 | luminance analog output signal Y |
| $V_{SSA}$ | 68 | analog ground (0 V) |

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| CVBS | 69 | CVBS analog output signal |
| $V_{DDA2}$ | 70 | +5 V analog supply 2 for output buffer amplifier of DAC2 |
| CUR | 71 | current input for analog output buffers |
| $V_{DDA3}$ | 72 | +5 V analog supply 3 for output buffer amplifier of DAC3 |
| KEY | 73 | key signal to insert CVBS input signal into encoded CVBS output signal; active HIGH |
| HSY | 74 | horizontal sync indicator output signal; active HIGH (3-state output to ADC) |
| HCL | 75 | horizontal clamping output; active HIGH (3-state output) |
| CVBS0 | 76 | digital CVBS input signal |
| CVBS1 | 77 | |
| CVBS2 | 78 | |
| CVBS3 | 79 | |
| CVBS4 | 80 | |
| CVBS5 | 81 | |
| CVBS6 | 82 | |
| CVBS7 | 83 | |
| HSN | 84 | horizontal sync output; active LOW or active HIGH for 60/66/72 x PIXCLK at 12.27/13.5/14.75 MHz (3-state output) |

## FUNCTIONAL DESCRIPTION

The SAA7199B is a digital video encoder that translates digital RGB, YUV or 8-bit indexed colour signals into the analog PAL/NTSC output signals Y (luminance), C (4.43/3.58 MHz chrominance) and CVBS (composite signal including sync).

Four different modes are selectable (Table 9):

- stand-alone mode (horizontal and vertical timings are generated)
- slaver mode (stand-alone unit that accepts external horizontal and vertical timing), and optional real-time information for subcarrier/clock from a digital colour decoder
- GENLOCK mode (GENLOCK capabilities are achieved in conjunction with determined ICs).
- test mode (only clock signal is required)

The input data rate (pixel sequence) has an integer relationship to the number of horizontal clock cycles (Table 1). A sufficient stable external clock signal ensures correct encoding. The generated clock frequency in the GENLOCK mode may deviate by ±7 % depending on the reference signal which is corresponding to its input sync signal. The clock will be nominal in the GENLOCK mode when the reference signal is absent (nominal with crystal oscillator accuracy for TV time constants, and nominal ±1.4 % for VCR time constants).

The on-chip colour conversion matrix provides CCIR 601 code-compatible transcoding of RGB to YUV data.

RGB data out of bounds, with respect to CCIR 601 specification, can be clipped to prevent over-loading of the colour modulator. RGB data input can be either in linear colour space or in gamma-corrected colour space. YUV data must be gamma-corrected according to CCIR 601. This circuit operates primarily in a 24-bit colour space (3 x 8-bit) but can also accomodate different data formats (4:1:1, 4:2:2 and 4:4:4) as well as 8-bit indexed pseudo-colour space operations (FMT-bits in Table 6).

RGB CLUTs on chip provide gamma-correction and/or other CLUT functions. They consist of programmable tables to be loaded

**Table 1** Pixel relationships

| ACTIVE PIXELS PER LINE | FIELD RATE | MULTIPLES OF LINE FREQUENCY | PIXCLK OUTPUT SIGNAL (MHz) | XTAL (MHz) |
|---|---|---|---|---|
| 640 (square) | 60 Hz | 780 | 12.272727 | 26.8 |
| 720 | 60 Hz | 858 | 13.5 | 24.576 |
| 768 (square) | 50 Hz | 944 | 14.75 | 26.8 |
| 720 | 50 Hz | 864 | 13.5 | 24.576 |

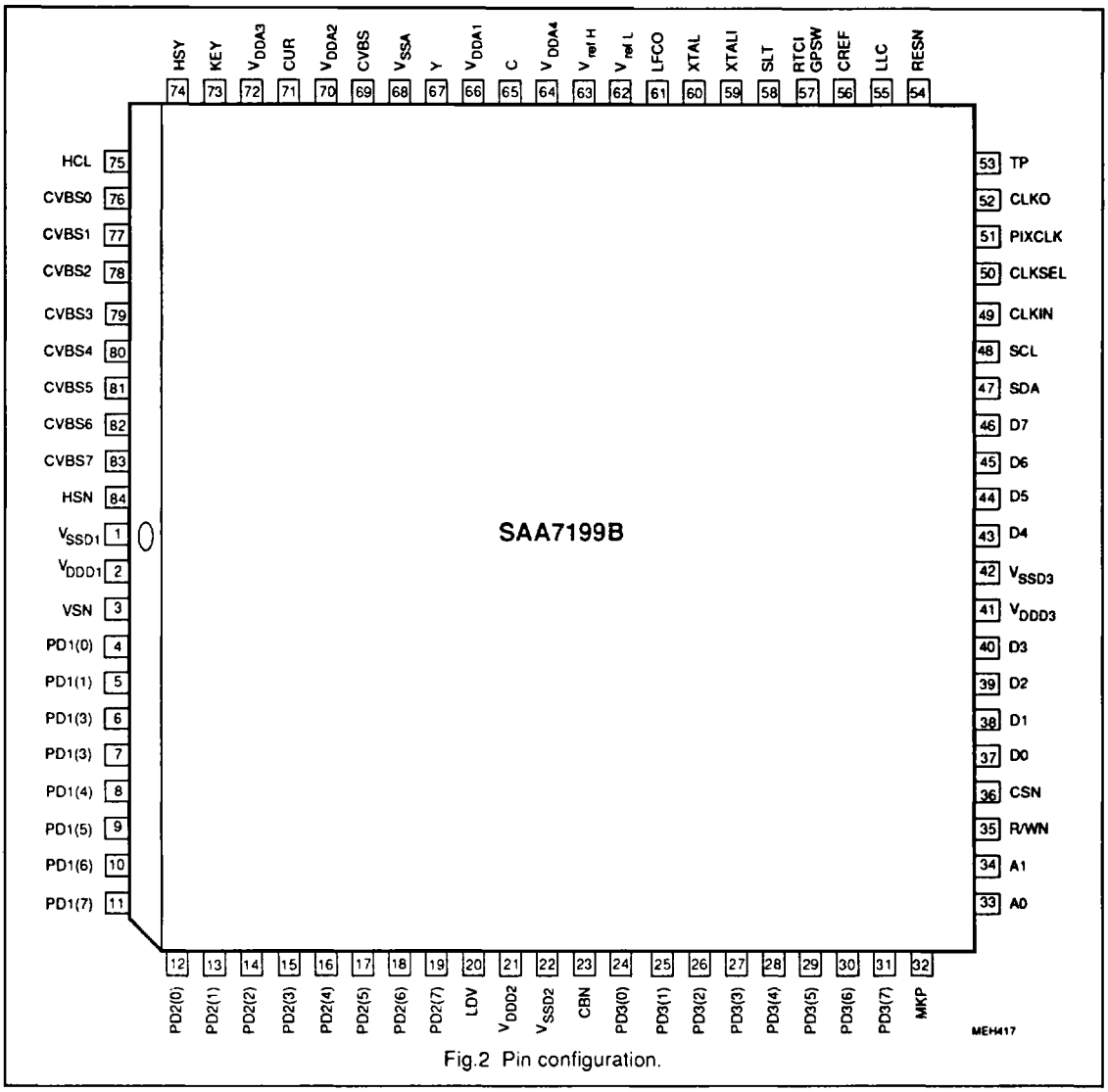



Fig.2 Pin configuration.

independently, and they generate 24-bit gamma-corrected output signals from 24-bit data of one of the input formats or from 8-bit indexed pseudo-colour data.

Required modulation is performed. The digital YUV data is encoded according to standards RS-170A (composite NTSC) and CCIR 624-4 (composite PAL-B/G). S-Video output signal is available (Y/C) as well as some sub-standard output signals (STD-bits in Table 6). A 7.5 IRE set-up level is automatically selected in the 60 Hz mode – there is none in 50 Hz mode.

The analog signal outputs can drive directly into terminated 75 Ω coaxial lines, a passive external filter is recommended (Figures 3 and 13). Analog post-filtering is required (LP in Fig.3).

GENLOCK to an external reference signal is achieved by addition of a video ADC and a clock generator combination. Thus, the system is enabled to lock on a stable video source or to a stable VCR source (normal playback). The SAA7199B, the ADC and the clock generator

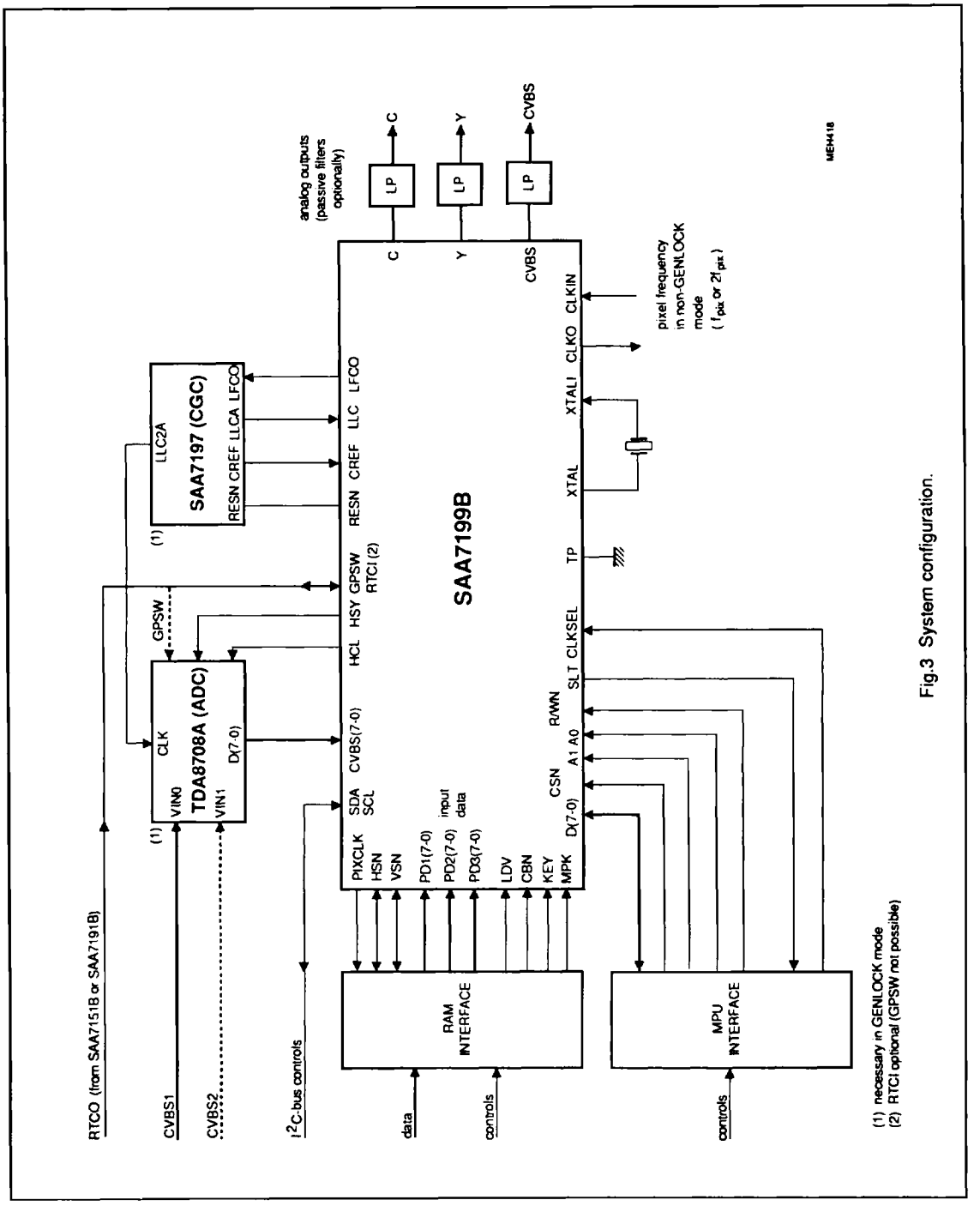



Fig.3 System configuration.

combination (Fig.3) form a control loop achieving a highly stable line-locked clock. The clock has to be generated by a crystal oscillator without this possibility.
The GENLOCK mode is not available in a single device set-up.

**Control interface**

The SAA7199B supports a standard parallel MPU interface as well as the serial I²C-bus interface. The MPU has a direct access to internal control registers and colour tables. Update is possible at any time, excluding coincident internal reading and external writing of the same cell (the current pixel value could be destroyed).
The two interfaces of Table 2 are selected automatically. However, the I²C control is inactive when the MPU interface is selected by CSN = LOW. No simultaneous access must occur. I²C-bus and MPU control complement each other and have access to common registers controlled via a common internal bus. The programmer can use virtually identical programs.
The internal memory space is devided into the look-up table and the control table, each with its own 8-bit address register is used as a pointer for specific location. This address register is provided with auto-incrementation and can be written by only one addressing.

The look-up table contains three banks of 256 bytes. Therefore, each read or write cycle must access to all three banks in a determined order. The support logic is part of the control interface.

Timing (Fig.3).

The reference to generate internal clocks from LLC in GENLOCK operation with SAA7197 is CREF (CREF = LLC/2). In this case input CLKSEL is HIGH and the SRC-bit is 1.

In non-GENLOCK operation the signal from CLKIN is used and LDV is clock reference (input CLKSEL = 0; SCR-bit = CPR-bit = 0).

**Table 2** Access to the contol interface

| SYMBOL | DESCRIPTION |
|---|---|
| SDA (I²C-bus)<br>SCL | serial data line (bi-directional)<br>clock line |
| A1, A0 (MPU-bus)<br>R/WN<br>CSN<br>GPSW<br>RESN | address inputs<br>read/write control<br>chip select; I²C-bus disabled (at LOW)<br>general purpose switch output (bit of control register)<br>reset signal (active-LOW) |

**Table 3** Address assignment

| ADDRESS INPUTS A1 | A0 | I²C-BUS SUBADDRESS | SELECTION |
|---|---|---|---|
| 0 | 0 | 00 | ADR-CLUT (address register of look-up tables) |
| 0 | 1 | 01 | DATA-CLUT |
| 1 | 0 | 02 | ADR-CTRL (index register of control table) |
| 1 | 1 | 03 | DATA-CTRL |

Pins LLC and CLKIN are tied together when no switching between LLC and CLKIN is applied. In Fig.3 it is assumed that LLC and CLKIN are double the pixel clock frequency of CREF respectively LDV.
CREF must be at the same frequency (or constant HIGH or LOW) when LLC is at pixel clock frequency.
CPR-bit = 1 if CLKIN is at pixel clock frequency.
Buffered CLKO signal is always delayed. LLC or CLKIN signals are according to CLKSEL

**Mapping**

Mapping of external control signals onto internal bus. The method is simple. The MPU- bus contains the signals of Table 4 (names in chip-internal nomenclature).

**Bit allocation**

The Bit Allocation Map (BAM) shows the individual control signals, used to control the different operational modes of the circuit. The I²C-bus is normally used for control. The SAA7199B additionally has a MPU-bus interface for direct microprocessor connection. The following BAM resembles the I²C-bus type but can be also used for the parallel bus. The control registers of Table 5 are indexed from 00 to 0F (hex). Auto-incrementation is applied.

**Digital-to-analog converters**

The converters use a combination of resistor chains with low-impedance output buffers. The bottom output voltage is 200 mV to reduce integral non-linearity errors. The analog signal, without load on output pin, is between 0.2 and 2.2 V. Fig.15 shows the application for 1.23 V/ 75 Ω outputs, using the serial 25 Ω + 22 Ω resistors.

Each digital-to-analog converter has its own supply pin for purpose of decoupling. $V_{DDA4}$ is the supply voltage for the resistor chains of the three DACs. The accuracy of this supply voltage influences directly the output amplitudes.
The current CUR into pin 71 is 0.3 mA ($V_{DDA4}$ = 5 V, $R_{64\text{-}71}$ = 20 kΩ); a larger current improves the bandwidth but increases the integral non-linearity.

**Table 4** Signals on the internal bus

| SYMBOL | DESCRIPTION | |
|---|---|---|
| R-WN | Select read/write (read = 1; write = 0) | |
| C-TN | Control table/look-up table (control table = 1; look-up table = 0) | |
| D-AN | Select data/address (data = 1; address = 0) | |
| DI/DO(0-7) | Data bus on port inputs/outputs D7 to D0 | |
| EN | Enable from control interface to synchronize data transfer | |
| **INTERNAL PARALLEL BUS** | **PARALLEL INTERFACE** | **I²C-BUS INTERFACE** |
| R-WN | R/WN (pin 35) | LSB of slave address byte (read = HIGH; write = LOW) |
| C-TN | A1 (pin 34) | X ) |
| A-TN | A0 (pin 33) | X ) 4 subaddresses after decoding |
| DI/DO(0-7) | D7 to D0 | Data bits D7 to D0 for each subaddress |
| EN | CSN and R/WN | Enable by every 9th clock of sample of SCL (control of serial-to-parallel conversion) |

**Table 5** Bit allocation map (I²C-bus access in Table 8)

| INDEX BINARY | HEX | DATA BYTE D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DF** |
|---|---|---|---|---|---|---|---|---|---|---|
| Input processing | | | | | | | | | | |
| 0000 0000 | 00 | VTBY | FMT2 | FMT1 | FMT0 | SCBW | CCIR | MOD1 | MOD0 | 5C |
| 0000 0001 | 01 | TRER7 | TRER6 | TRER5 | TRER4 | TRER3 | TRER2 | TRER1 | TRER0 | XX |
| 0000 0010 | 02 | TREG7 | TREG6 | TREG5 | TREG4 | TREG3 | TREG2 | TREG1 | TREG0 | XX |
| 0000 0011 | 03 | TREB7 | TREB6 | TREB5 | TREB4 | TREB3 | TREB2 | TREB1 | TREB0 | XX |
| Sync processing | | | | | | | | | | |
| 0000 0100 | 04 | SYSEL1 | SYSEL0 | SCEN | VTRC | NINT | HPLL | HLCK* | OEF* | 10 |
| 0000 0101 | 05 | 0 | 0 | GDC5 | GDC4 | GDC3 | GDC2 | GDC1 | GDC0 | 21 |
| 0000 0110 | 06 | IDEL7 | IDEL6 | IDEL5 | IDEL4 | IDEL3 | IDEL2 | IDEL1 | IDEL0 | 52 |
| 0000 0111 | 07 | 0 | 0 | PSO5 | PSO4 | PSO3 | PSO2 | PSO1 | PSO0 | 32 |
| Control, clock and output formatter | | | | | | | | | | |
| 0000 1000 | 08 | DD | KEYE | SRC | CPR | COKI | IM | GPSW | SRSN | 64 |
| 0000 1001 | 09 | 0 | BAME | MPKC1 | MPKC0 | IEPI | RTSC | RTIN | RTCE | 02 |
| 0000 1010+ | 0A+ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| 0000 1011+ | 0B+ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| Encoder control | | | | | | | | | | |
| 0000 1100 | 0C | CHPS7 | CHPS6 | CHPS5 | CHPS4 | CHPS3 | CHPS2 | CHPS1 | CHPS0 | XX++ |
| 0000 1101 | 0D | FSCO7 | FSCO6 | FSCO5 | FSCO4 | FSCO3 | FSCO2 | FSCO1 | FSCO0 | 00 |
| 0000 1110 | 0E | 0 | 0 | 0 | CLCK* | STD3 | STD2 | STD1 | STD0 | 0C |
| 0000 1111+ | 0F+ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

*) read only bits +) reserved ++) adjust as required.

**) DF is the default value for a typical programming example: GENLOCK mode for a VCR; non-gamma-corrected RGB data (realtime keying is possible). SLT will be set if there is no horizontal lock. NTSC-M standard with normal colour bandwidth and 12.2727 MHz pixel rate. CSYN signal will be provided, coming 8 pixel clocks earlier, to compensate pipeline delay in the previous RAM interface. The encoded CVBS is 12 clocks earlier than the CVBS reference on the input of the previous ADC. The CLUTs are bypassed at MPK = HIGH in real-time.

**Table 6** Function of register bits of Table 5

| | | | | |
|---|---|---|---|---|
| Index "00"<br>VTBY | Video look-up table by-pass: | 0 = not bypassed;<br>1 = bypassed (OR connectable with MPK) | | |
| FMT2 to FMT0 | Input formats: | | | |
| | FMT2 | FMT1 | FMT0 | format |
| | 0 | 0 | 0 | YUV 4:1:1 format; DMSD2 compatible |
| | 0 | 0 | 1 | YUV 4:1:1 format; customized |
| | 0 | 1 | 0 | YUV 4:2:2 format; DMSD2 compatible |
| | 0 | 1 | 1 | YUV 4:2:2 format; customized |
| | 1 | 0 | 0 | YUV 4:4:4 format |
| | 1 | 0 | 1 | RGB 4:4:4 format |
| | 1 | 1 | 0 | reserved |
| | 1 | 1 | 1 | 8-bit indexed colour |
| SCBW | Chrominance bandwidth: | 0 = enhanced; 1 = standard | | |
| CCIR | Select level: | 0 = DMSD2 levels; 1 = CCIR levels | | |
| MOD1 to MOD0 | Select mode: | MOD1 | MOD0 | mode |
| | | 0 | 0 | GENLOCK mode |
| | | 0 | 1 | stand-alone mode |
| | | 1 | 0 | slave mode |
| | | 1 | 1 | test mode |
| Index "01"<br>TRER7 to TRER0 | Test register Red (read/write via MPU-bus; write only via I²C-bus) | | | |
| Index "02"<br>TREG7 to TREG0 | Test register Green (read/write via MPU-bus; write only via I²C-bus) | | | |
| Index "03"<br>TREB7 to TREB0 | Test register Blue (read/write via MPU-bus; write only via I²C-bus) | | | |
| Index "04"<br>SYSEL1 to SYSEL0 | Sync select: | SYSEL1 | SYSEL0 | synchronized from |
| | | 0 | 0 | CSYN (active LOW; pin 3) |
| | | 0 | 1 | HSN and VSN (active LOW; pins 84 and 3) |
| | | 1 | 0 | CSYN (active HIGH; pin 3) |
| | | 1 | 1 | HSN and VSN (active HIGH; pins 84 and 3) |
| SCEN | Sync/clamping (HSY/HCL) enable: | 0 = disabled (set to HIGH); 1 = enabled | | |
| VTRC | Select TV/VTR mode: | 0 = 0 TV mode (slow); 1 = VTR mode (fast) | | |
| NINT | Select interlace of encoded signal: | 0 = interlaced (262.5/262.5 or 312.5/312.5)<br>1 = non-interlaced (262/262 or 312/312 in modes 1 and 3 only) | | |

| | |
|---|---|
| HPLL | Select horizontal lock: 0 = lock enabled; 1 = lock disabled (crystal reference) |
| OEF | Status bit field organization (to be read): 0 = even field; 1 = odd field |
| HLCK | Status bit sync indication (to be read): 0 = locked to external sync<br>1 = external sync lost |
| Index "05"<br>GDC5 to GDC0 | GENLOCK delay compensation, note 1: data 00 to 3F equals timing of CVBS output signal is (46 – GDC) pixel clocks = $t_{ofs}$ earlier with respect to reference point $t_{REF1}$.<br>($t_{REF1}$ corresponds to the falling edge of the horizontal sync pulse of CVBS input signal; $t_{ofs}$ is designated for propagation delay of extern GENLOCK source, Fig.10). |
| Index "06"<br>IDEL7 to IDEL0 | Increment delay: update of line-locked clock frequency (Table 5, data "43" hex recommended) |
| Index "07"<br>PSO7 to PSO0 | Phase sync in output signal, note 1: data 00 to 3F equals to active slope of HSN, VSN/CSYN is (58 – PSO) pixel clocks = $t_{Rint}$ earlier with respect to reference point $t_{REF2}$.<br>($t_{REF2}$ corresponds to PSO = 58; $t_{Rint}$ is designated for pipeline delay of the feeding RAM interface, Fig.10). |
| Index "08"<br>DD | Digital video encoder disable: 0 = enabled; 1 = disabled |
| KEYE | Keying enable: 0 = disabled; 1 = enabled (logically AND-connected with KEY) |
| SRC | Clock source: 0 = external system clock; 1 = DTV2 system clock |
| CPR | Clock phase reference: 0 = LDV is (pin 20); 1 = LDV is not |
| COKI | Colour-killer: 0 = colour on; 1 = colour off (subcarrier is switched off) |
| IM | Interrupt mask: 1 = interrupt not masked at sync lost (pin 58)<br>0 = interrupt masked.at sync lost (pin 58) |
| GPSW | General purpose switch at bit RTIN = 1: 0 = pin 57 LOW; 1 = pin 57 HIGH |
| SRSN | Software reset: 0 = no reset; 1 = reset (see reset procedure) |
| Index "09"<br>BAME | Burst amplitude indication: 0..= burst amplitude measurement is overridden; colour lock always assumed<br>1 = burst amplitude is used to control the CLCK status bit, recommended for reference signal without subcarrier burst (pure black and white) in order to avoid PLL hunting. |

<table>
<tr><td>MPKC1 to MPKC0</td><td>Multi-purpose key control: At MKP = LOW (pin 32) are all functions as given by software programming;<br>MKP = HIGH sets in real-time with respect to PDn(7-0).
<table>
<tr><th colspan="2">Set by bits</th><th colspan="4">in function blocks</th></tr>
<tr><th>MPKC1</th><th>MPKC0</th><th>input formatter</th><th>CLUTs</th><th>matrix</th><th>level matching</th></tr>
<tr><td>0</td><td>0</td><td>control via CCIR bit and FMT bits</td><td>bypass</td><td>control via FMT bits</td><td>control via CCIR bit</td></tr>
<tr><td>0</td><td>1</td><td>Format 5 (RGB) CCIR level</td><td>active, no indexed colour</td><td>active</td><td>CCIR level</td></tr>
<tr><td>1</td><td>X</td><td>Format 7 (indexed colour) CCIR level</td><td>active, indexed colour</td><td>active</td><td>CCIR level</td></tr>
</table></td></tr>
<tr><td>IEPI</td><td>Polarity of external PAL-ID signal (H/2 signal) from RTCI input (pin 57):<br>0 = not inverted; 1 = inverted</td></tr>
<tr><td>RTSC</td><td>Real-time select control:<br>0 = Real-time control HPLL increment is selected, that means, information about actual clock frequency from the digital colour decoder is received (SAA7151B or SAA7191B); the corresponding subcarrier frequency is calculated.<br>1 = Real-time control FSC increment with PAL-ID is selected, that means, information about actual subcarrier frequency and PAL-ID from the digital colour decoder is received (SAA7151B or SAA7191B).</td></tr>
<tr><td>RTIN</td><td>Select real-time control input: 0 = pin 57 is input for RTCI signal<br>1 = pin 57 is port output GPSW.</td></tr>
<tr><td>RTCE</td><td>Real-time control enabled: 0 = disabled; 1 = enabled (RTIN = 0)</td></tr>
<tr><td>Index "0C"<br>CHPS7 to CHPS0</td><td>Phase adjustment between chrominance output signal and reference:<br>00 to FF equals 0° to 358.59375° in steps of 1.40625°.</td></tr>
<tr><td>Index "0D"<br>FSC7 to FSC0</td><td>Fine adjustment of subcarrier frequency in non-GENLOCK modes:<br>00 to 7F increasing and FF to 80 decreasing equal approximately ±450 x $10^{-6}$ of the subcarrier frequency in 256 steps.</td></tr>
<tr><td>Index "0E"<br>CLCK</td><td>Lock to external chrominance (to be read): 0 = possible; 1 = not possible.</td></tr>
</table>

| | |
|---|---|
| STD3 to STD0 | Colour encoding standards: |

| STD3 | STD2 | STD1 | STD0 | standard |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | NTSC 4.43; 60 Hz; SQP (12.27 MHz) |
| 0 | 0 | 0 | 1 | NTSC 4.43; 50 Hz; SQP (14.75 MHz) |
| 0 | 0 | 1 | 0 | PAL-B/G 4.43; 50 Hz; SQP (14.75 MHz) |
| 0 | 0 | 1 | 1 | NTSC 4.43; 60 Hz; CCIR (13.5 MHz) |
| 0 | 1 | 0 | 0 | NTSC 4.43; 50 Hz; CCIR (13.5 MHz) |
| 0 | 1 | 0 | 1 | PAL-B/G 4.43; 50 Hz; CCIR (13.5 MHz) |
| 0 | 1 | 1 | 0 | reserved |
| 0 | 1 | 1 | 1 | reserved |
| 1 | 0 | 0 | 0 | PAL-M; 60 Hz; SQP (12.27 MHz) |
| 1 | 0 | 0 | 1 | PAL-M; 60 Hz; CCIR (13.5 MHz) |
| 1 | 0 | 1 | 0 | PAL-N; 50 Hz; CCIR (13.5 MHz) |
| 1 | 0 | 1 | 1 | PAL-N; 50 Hz; SQP (14.75 MHz) |
| 1 | 1 | 0 | 0 | NTSC-M; 60 Hz; SQP (12.27 MHz) |
| 1 | 1 | 0 | 1 | NTSC-M; 60 Hz; CCIR (13.5 MHz) |
| 1 | 1 | 1 | 0 | reserved |
| 1 | 1 | 1 | 1 | reserved |

| | |
|---|---|
| Status bits to be read via I²C-bus: | Table 7 |
| Status bits to be read by microcontroller : | All registers from 00 up to 0F can be read via MPU-bus. Read-only bits are OEF, HCLK (index "04") and CLCK (index "0E") |

**Note to Table 6**

Field blanking (Figures 11 and 12): normally, video to be encoded should not become active after the active edge of VSN or CSYN before line 22.5 at 50 Hz (line 18 at 60 Hz). Total internal field blanking is 11 lines at 50 Hz (13 lines at 60 Hz).

**Colour look-up tables (CLUTs)**

The CLUTs consist of RAM tables. The RAM tables can be loaded – with X = 0 to 255 according to equation 1 – for the signals R, G and B . Gamma-correction (pre-distortion) by following equation:

$$Y = NINT(b + a \times X1^{1/g}); \quad Y(X \leq 16) = 16; \quad Y(X \geq 235) = 235 \quad \text{(equation 1)}$$

with g = 2.2 is

$$a = 219 / (235^{2.2} - 16^{2.2})$$

$$b = 16 - a \times 16^{2.2}$$

The RAM tables are loaded via MPU-bus or via I²C-bus (Table 8).

### I²C-BUS FORMAT

| S | SLAVE ADDRESS | A | SUBADDRESS | A | DATA0 | A | | DATAn | A | P |
|---|---|---|---|---|---|---|---|---|---|---|

S = start condition
SLAVE ADDRESS = **1011 000X**
A = acknowledge, generated by the slave
SUBADDRESS* = subadress byte (Table 8)
DATA = data byte (Table 5)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

**Table 7** I²C-bus status byte (address byte "B1")

| FUNCTION | | STATUS BYTE D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Read status | | 0 | 0 | 0 | 0 | FFOS | OEF | CLCK | HLCK |

Function of the bits:

FFOS — first field of sequence: 0 = false; 1 = first of 4 fields for NTSC (first of 8 fields for PAL). FFOS is not valid for non-interlaced signals.
OEF — field organization: 0 = even field; 1 = odd field
CLCK — possibility of lock to external chrominance: 0 = possible; 1 = not possible
HLCK — sync indication: 0 = locked to external sync; 1 = external sync lost.

**Table 8** I²C-bus write bytes (address byte "B0")

| |
|---|
| **ACCESS TO CONTROL REGISTERS**<br>Address byte "B0" — subaddress byte "02" — index byte (00 to 0F, Table 5) — data bytes (auto-increment) |
| **ACCESS TO CLUTS REGISTERS**<br>Address byte "B0" — subaddress byte "00" — CLUT address bytes (00 to FF) — 3 data bytes for one RGB sequence (auto-increment) |

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

**Table 9** Four different modes

| |
|---|
| **STAND-ALONE MODE** |
| The SAA7199B receives a line-locked clock CLKIN and generates CSYN or HSN/VSN output signals, which trigger the RGB respectively the YUV source signal to provide data and composite blanking CBN. |
| **SLAVE MODE** |
| The SAA7199B receives the line-locked clock CLKIN, CSYN or HSN/VSN, CBN and data from an RGB respectively YUV source. The sync inputs are edge-sensitive; the minimum active length is 1 PIXCLK. Optionally, a real-time control signal RTCI is received from a digital colour decoder. |
| **GENLOCK MODE** |
| Horizontal and vertical sync as well as colour are locked on a received CVBS reference signal. The CVBS reference signal generates also a line-locked clock by the SAA7197 clock generator. Auxiliary signals HCL and HSY as well as CSYN or HSN/VSN are generated to trigger the RGB respectively the YUV source providing data and composite blanking CBN. |
| **TEST MODE** |
| Like stand-alone mode, but data to be encoded are the contents of the test registers TRER, TREGand TREB. VSN/CSYN and HSN outputs are in 3-state condition. |

**Relationship between horizontal frequency and colour subcarrier frequency in non-GENLOCK mode**

a) Internal subcarrier frequency with n = integer:

PAL: $f_{SC} = f_H (n/4 + 1/625)$ respectively $f_H (n/4 + 1/525)$ NTSC: $f_{SC} = f_H (n/2)$

Necessary conditions: Non-GENLOCK mode; RTCE = 0, FSCO = 00h; phase coupling of the two frequencies is given by definite phase reset every 8th fields at PAL (4th fields at NTSC).

FSCO ≠ 00h adjusts the subcarrier frequency, phase reset is disabled and phase between $f_{SC}$ and $f_H$ is not constant.

b) External subcarrier frequency:

$f_{SC}$ is given by RTCI real-time input from a digital colour decoder.

Necessary conditions: Slave mode; RTCE = 1, RTSC = 1. The 8th respectively 4th field reset is enabled at FSCO = 00h (disabled at FSCO ≠ 00h). The subcarrier frequency itself is not influenced by FSCO bits, it is given by real-time increment.

c) External HPLL increment:

$f_{SC}$ is calculated by means of RTCI real-time input signal from a digital colour decoder. The frequency of $f_{SC}$ depends on the absolute crystal frequency value used by the digital colour decoder.

Necessary conditions: Slave mode; RTCE = 1, RTSC = 0. The 8th respectively 4th field reset is enabled at FSCO = 00h (disabled at FSCO ≠ 00). The subcarrier frequency itself is influenced by FSCO bits.

The absolute phase relationship between sync and subcarrier (colour burst out) can be influenced in all three cases by CHPS(7-0) register byte (index "0C").

**Data input formats**

One clock cycle equals 12.27 MHz, 13.5 MHz or 14.75 MHz (Cb = (B-Y) equals U; Cr = (R-Y) equals V; (n) = number of pixel).

**Table 10** Format 0: DMSD2-compatible YUV 4:1:1 format (FMT-bits in index "00"= 000)

| INPUT SIGNAL | CLOCK CYCLE (PIXEL SEQUENCE) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| PD2(7-0) | Y(0) | Y(1) | Y(2) | Y(3) | Y(4) | Y(5) | Y(6) | Y(7) |
| PD3(7) | Cb7(0) | Cb5(0) | Cb3(0) | Cb1(0) | Cb7(4) | Cb5(4) | Cb3(4) | Cb1(4) |
| PD3(6) | Cb6(0) | Cb4(0) | Cb2(0) | Cb0(0) | Cb6(4) | Cb4(4) | Cb2(4) | Cb0(4) |
| PD3(5) | Cr7(0) | Cr5(0) | Cr3(0) | Cr1(0) | Cr7(4) | Cr5(4) | Cr3(4) | Cr1(4) |
| PD3(4) | Cr6(0) | Cr4(0) | Cr2(0) | Cr0(0) | Cr6(4) | Cr4(4) | Cr2(4) | Cr0(4) |
| PD3(3-0) | not used | | | | | | | |
| PD1(7-0) | not used | | | | | | | |

**Table 11** Format 1: Customized YUV 4:1:1 format (FMT-bits in index "00" = 001)

| INPUT SIGNAL | CLOCK CYCLE (PIXEL SEQUENCE) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| PD2(7-0) | Y(0) | Y(1) | Y(2) | Y(3) | Y(4) | Y(5) | Y(6) | Y(7) |
| PD3(7) | Cb7(0) | - | Cr7(0) | - | Cb7(4) | - | Cr7(4) | - |
| PD3(6) | Cb6(0) | - | Cr6(0) | - | Cb6(4) | - | Cr6(4) | - |
| PD3(5) | Cb5(0) | - | Cr5(0) | - | Cb5(4) | - | Cr5(4) | - |
| PD3(4) | Cb4(0) | - | Cr4(0) | - | Cb4(4) | - | Cr4(4) | - |
| PD3(3) | Cb3(0) | - | Cr3(0) | - | Cb3(4) | - | Cr3(4) | - |
| PD3(2) | Cb2(0) | - | Cr2(0) | - | Cb2(4) | - | Cr2(4) | - |
| PD3(1) | Cb1(0) | - | Cr1(0) | - | Cb1(4) | - | Cr1(4) | - |
| PD3(0) | Cb0(0) | - | Cr0(0) | - | Cb0(4) | - | Cr0(4) | - |
| PD1(7-0) | not used | | | | | | | |

**Table 12** Format 2: DMSD2-compatible YUV 4:2:2 format (FMT-bits in index "00" = 010)

| INPUT SIGNAL | CLOCK CYCLE (PIXEL SEQUENCE) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| PD2(7-0) | Y(0) | Y(1) | Y(2) | Y(3) | Y(4) | Y(5) | Y(6) | Y(7) |
| PD3(7) | Cb7(0) | Cr7(0) | Cb7(2) | Cr7(2) | Cb7(4) | Cr7(4) | Cb7(6) | Cr7(6) |
| PD3(6) | Cb6(0) | Cr6(0) | Cb6(2) | Cr6(2) | Cb6(4) | Cr6(4) | Cb6(6) | Cr6(6) |
| PD3(5) | Cb5(0) | Cr5(0) | Cb5(2) | Cr5(2) | Cb5(4) | Cr5(4) | Cb5(6) | Cr5(6) |
| PD3(4) | Cb4(0) | Cr4(0) | Cb4(2) | Cr4(2) | Cb4(4) | Cr4(4) | Cb4(6) | Cr4(6) |
| PD3(3) | Cb3(0) | Cr3(0) | Cb3(2) | Cr3(2) | Cb3(4) | Cr3(4) | Cb3(6) | Cr3(6) |
| PD3(2) | Cb2(0) | Cr2(0) | Cb2(2) | Cr2(2) | Cb2(4) | Cr2(4) | Cb2(6) | Cr2(6) |
| PD3(1) | Cb1(0) | Cr1(0) | Cb1(2) | Cr1(2) | Cb1(4) | Cr1(4) | Cb1(6) | Cr1(6) |
| PD3(0) | Cb0(0) | Cr0(0) | Cb0(2) | Cr0(2) | Cb0(4) | Cr0(4) | Cb0(6) | Cr0(6) |
| PD1(7-0) | not used | | | | | | | |

**Table 13** Format 3: Customized YUV 4:2:2 format (FMT-bits in index "00" = 011)

| INPUT SIGNAL | CLOCK CYCLE (PIXEL SEQUENCE) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| PD2(7-0) | Y(0) | Y(1) | Y(2) | Y(3) | Y(4) | Y(5) | Y(6) | Y(7) |
| PD3(7-0) | Cb (0) | - | Cb (2) | - | Cb (4) | - | Cb (6) | - |
| PD1(7-0) | Cr (0) | - | Cr (2) | - | Cr (4) | - | Cr (6) | - |

**Table 14** Format 4: YUV 4:4:4 format (FMT-bits in index "00" = 100)

| INPUT SIGNAL | CLOCK CYCLE (PIXEL SEQUENCE) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| PD2(7-0) | Y(0) | Y(1) | Y(2) | Y(3) | Y(4) | Y(5) | Y(6) | Y(7) |
| PD3(7-0) | Cb (0) | Cb (1) | Cb (2) | Cb (3) | Cb (4) | Cb (5) | Cb (6) | Cb (7) |
| PD1(7-0) | Cr (0) | Cr (1) | Cr (2) | Cr (3) | Cr (4) | Cr (5) | Cr (6) | Cr (7) |

**Table 15** Format 5: RGB 4:4:4 format (FMT-bits in index "00" = 101)

| INPUT SIGNAL | CLOCK CYCLE (PIXEL SEQUENCE) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| PD1(7-0) | R(0) | R(1) | R(2) | R(3) | R(4) | R(5) | R(6) | R(7) |
| PD2(7-0) | G(0) | G(1) | G(2) | G(3) | G(4) | G(5) | G(6) | G(7) |
| PD3(7-0) | B(0) | B(1) | B(2) | B(3) | B(4) | B(5) | B(6) | B(7) |

**Table 16** Format 7: Indexed colour format (FMT-bits in index "00" = 111). Input codes 0 to 255 are allowed, output code of CLUTs should preferably be the same as given in Format 5

| INPUT SIGNAL | CLOCK CYCLE (PIXEL SEQUENCE) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| PD2(7-0) | INC(0) | INC(1) | INC(2) | INC(3) | INC(4) | INC(5) | INC(6) | INC(7) |

**Table 17** Input data levels for formats 0 to 4 and 5; EBU colour bar: 100 % white equals 100 IRE intensity; 75 % colour saturation for formats 1 to 4, 100 % for format 5

| INPUT CHANNEL | LEVEL | DIGITAL LEVEL | CODE | CCIR-BIT | FORMAT |
|---|---|---|---|---|---|
| Y channel | 0 IRE<br>100 IRE | 12<br>230 | offset binary | 0 | formats 0 to 4 |
| Cb channel | bottom peak<br>colourless<br>top peak | −101<br>0<br>100 | two's complement | 0 | formats 0 to 4 |
| Cr channel | bottom peak<br>colourless<br>top peak | −106<br>0<br>105 | two's complement | 0 | formats 0 to 4 |
| Y channel | 0 IRE<br>100 IRE | 16<br>235 | offset binary | 1 | formats 0 to 4 |
| Cb channel | bottom peak<br>colourless<br>top peak | 44<br>128<br>212 | offset binary | 1 | formats 0 to 4 |
| Cr channel | bottom peak<br>colourless<br>top peak | 44<br>128<br>212 | offset binary | 1 | formats 0 to 4 |
| R, G and B | 0 IRE<br>100 IRE | 16<br>235 | offset binary | 1 | format 5 |

### GENLOCK input data

**Table 18** Format 7: CVBS GENLOCK input data format has 8-bit word length. The input data come from an analog-to-digital converter (TDA8708) with gain-controlled and clamped CVBS or VBS signals

| INPUT SIGNAL | CLOCK CYCLE (PIXEL SEQUENCE) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| CVBS7 to CVBS0 | CVBS(0) | CVBS(1) | CVBS(2) | CVBS(3) | CVBS(4) | CVBS(5) | CVBS(6) | CVBS(7) |

| CONDITIONS OF CVBS INPUT SIGNAL | TWO'S COMPLEMENT REPRESENTATION | |
|---|---|---|
| sync bottom | coresponding to binary code | −128 |
| 0 IRE (black) | coresponding to binary code | −64* |
| 100 IRE (white) | coresponding to binary code | 95 |
| top peak of 75 % colour | coresponding to binary code | 95 |
| bottom peak of 75 % colour | coresponding to binary code | −100 |

* If exactly matched levels are wanted in the internal multiplexer, the value 0 IRE should correspond to −68 and 100 IRE to 82.

**Encoding data levels**

Input data levels are transformed in three stages:

- in the matrix when RGB or indexed colour is applied (formats 5 and 7)
- in the normalizing amplifier depending on 50/60 Hz mode and CCIR-bit (index "00")
- in the modulator

**Table 19(a)** Y and C output levels in **50 Hz** mode (PAL) for RGB input levels (100/100 colour bar)

| SIGNAL | INPUT DATA | | | MATRIX OUTPUT DATA | | | NORMALIZER OUTPUT DATA | | | MODULATOR OUTPUT DATA | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | R | G | B | (R-Y) | Y | (B-Y) | V* | Y | U | Y | C** |
| white | 235 | 235 | 235 | 128 | 235 | 128 | 0 | 421 | 0 | 421 | 0 |
| yellow | 235 | 235 | 16 | 146 | 210 | 16 | 29 | 387 | −132 | 387 | ±135 |
| cyan | 16 | 235 | 235 | 16 | 170 | 166 | −184 | 332 | 44 | 332 | ±189 |
| green | 16 | 235 | 16 | 34 | 145 | 54 | −155 | 297 | −87 | 297 | ±178 |
| magenta | 235 | 16 | 235 | 221 | 107 | 202 | 152 | 245 | 86 | 245 | ±175 |
| red | 235 | 16 | 16 | 240 | 82 | 90 | 183 | 211 | −45 | 211 | ±188 |
| blue | 16 | 16 | 235 | 110 | 41 | 240 | −30 | 154 | 131 | 154 | ±134 |
| black | 16 | 16 | 16 | 128 | 16 | 128 | 0 | 120 | 0 | 120 | 0 |
| blanking | X | X | X | X | X | X | X | X | X | 120 | 0 |
| burst | X | X | X | X | X | X | 45 | X | −45 | X | ±63 |
| top sync | X | X | X | X | X | X | X | X | X | 0 | X |

**Table 19(b)** Y and C output levels in **60 Hz** mode (NTSC) for RGB input levels (100/100 colour bar)

| SIGNAL | INPUT DATA | | | MATRIX OUTPUT DATA | | | NORMALIZER OUTPUT DATA | | | MODULATOR OUTPUT DATA | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | R | G | B | (R-Y) | Y | (B-Y) | V | Y | U | Y | C** |
| white | 235 | 235 | 235 | 128 | 235 | 128 | 0 | 416 | 0 | 416 | 0 |
| yellow | 235 | 235 | 16 | 146 | 210 | 16 | 29 | 385 | −132 | 385 | ±135 |
| cyan | 16 | 235 | 235 | 16 | 170 | 166 | −184 | 335 | 44 | 335 | ±189 |
| green | 16 | 235 | 16 | 34 | 145 | 54 | −155 | 303 | −87 | 303 | ±178 |
| magenta | 235 | 16 | 235 | 221 | 107 | 202 | 152 | 256 | 86 | 256 | ±175 |
| red | 235 | 16 | 16 | 240 | 82 | 90 | 183 | 225 | −45 | 225 | ±188 |
| blue | 16 | 16 | 235 | 110 | 41 | 240 | −30 | 173 | 131 | 173 | ±134 |
| black | 16 | 16 | 16 | 128 | 16 | 128 | 0 | 142 | 0 | 142 | 0 |
| blanking | X | X | X | X | X | X | X | X | X | 120 | 0 |
| burst | X | X | X | X | X | X | 0 | X | −64 | X | ±64 |
| top sync | X | X | X | X | X | X | X | X | X | 0 | X |

X = not defined; * the V component is inverted in the PAL line; ** the ± figures are peak values of the subcarrier signal.

**Chrominance filtering in the encoder**

1. Decimation for 4:4:4 formats input data (Formats 4, 5 and 7; Fig.4).
2. Interpolation for 4:1:1 input data into 4:2:2 data – also suitable to reduce the bandwidth of 4:2:2 data. This filter is controlled by SCBW-bit (SCWB = 1 means active).
3. Interpolation at 13.5 MHz for 4:2:2 input data into 4:4:4 data before modulating baseband signals onto the colour subcarrier. Figures 5, 6 and 7 show the overall transfer characteristics of chrominance in "standard bandwidth condition" (SCBW = 1). Figures 8 and 9 show the overall transfer characteristics of chrominance in "enhanced bandwidth condition" (SCBW = 0), which is not possible for 4:1:1 input data. The transfer curves are slightly different at 12.27 and 14.75 MHz.

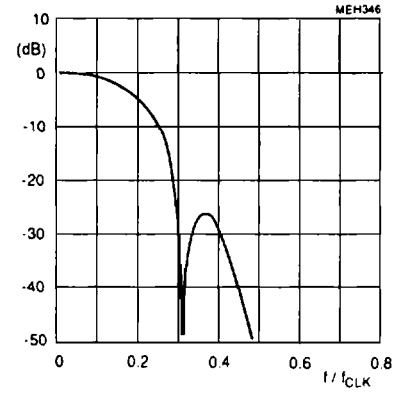



Fig.4 Transfer characteristics of 4:4:4 to 4:2:2 decimator.

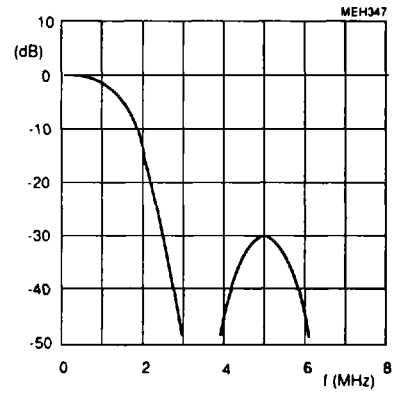



Fig.5 Overall transfer characteristics 4:1:1 input data.

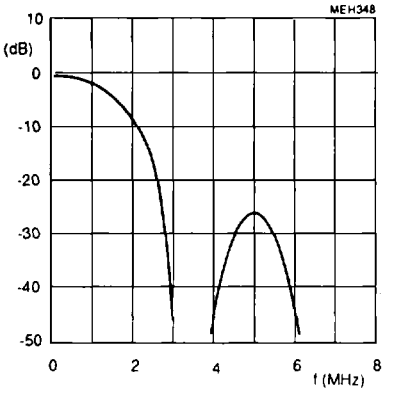



Fig.6 Overall transfer characteristics 4:2:2 input data (SCBW-bit = 1).

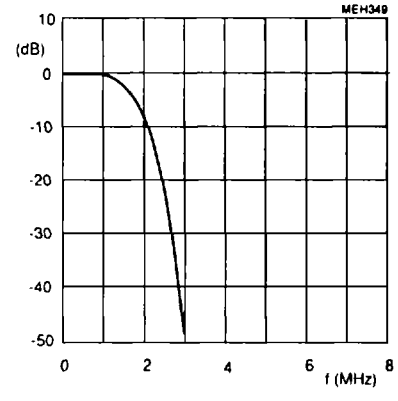



Fig.7 Overall transfer characteristics 4:4:4 input data (SCBW-bit = 1).

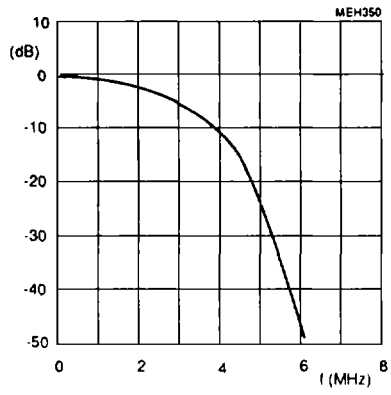



Fig.8 Overall transfer characteristics 4:2:2 input data (SCBW-bit = 0).

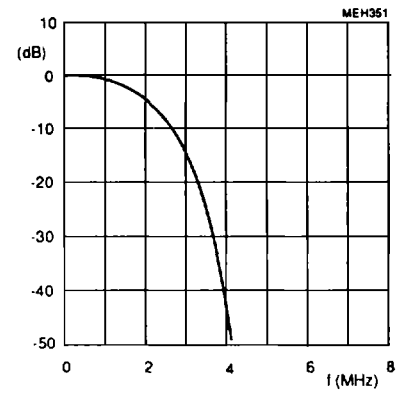



Fig.9 Overall transfer characteristics 4:4:4 input data (SCBW-bit = 0).

**Accuracy of matrix**

Evaluation of quantization errors.

The RGB to YUV matrix is realized according to the following algorithm:

Y = INT ((NINT(R x 2 x 0.299) + NINT(G x 2 x 0.587) +NINT(B x 2 x 0.114)) / 2)

U = NINT ((B-Y) x 0.57722)

V = NINT ((R-Y) x 0.72955)

Errors can occur in the calculation of Y, which in consequence influence the U and V outputs.
The greatest positive error occurs, if in all of the three for Y calculation used ROMs the values are rounded up to 0.5 LSB, and no truncation error of 0.5 LSB is generated after summation:

(3 x 0,5 LSB) / 2 = +0.75 LSB;
with truncation "error": (3 x 0,5 LSB) / 2 – 0.5 LSB = +0.25 LSB.

The greatest negative error occurs at rounding off in all the three ROMs and by consecutive truncation:

3 x (–0,5 LSB) / 2 – 0.5 LSB = –1.25 LSB.

As a result, the matrix error can be ±1 digit, which corresponds to approximately ±0.5% differential non-linearity.

**Estimation of noise by quantization**

The sum of all sqared quantization errors is SS normalized to $220^3$ input combinations (3-dimensional colour scale).

SS = 0.187545 $LSB^2$.

Compared with noise energy for ideal quantization, SSI = 1/12 $LSB^2$ results in a deterioration by the conversion matrix of

D = 10 log (0.187545 x 12) = 3.5 dB (equals 0.5 bit).

If SS is the sum of all sqared quantization errors, normalized to 220 input combinations of a grey-scale (R = G = B), then is

SS = 0.12273 $LSB^2$.

Compared with noise energy for ideal quantization, SSI = 1/12 $LSB^2$ results in a deterioration by the conversion matrix of

D = 10 log (0.12273 x 12) = 1.7 dB (equals 0.25 bit).

**Normalizing amplifiers in luminance channel**

The absolute amplification error for 50 Hz non-set-up signals is 0.375 %; differential non-linearity is −0.333 % (equals −1 LSB).
The absolute amplification error for 60 Hz set-up signals is −1.5 %; differential non-linearity is −0.365 % (equals −1 LSB).

**Normalizing amplifiers in chrominance channel**

The absolute amplification error is approximately ±0.5 % with a truncation error of −0.5 LSB.

The subcarrier amplitude for standards with luminance set-up is the same as for the standards without luminance set-up.

**Modulator**

The absolute amplification error is −0.39 %; there is no truncation error.

**Functional timing**

GENLOCK mode:
The encoded signal can be generated earlier with respect to CVBS(7-0) bits (offset $t_{ofs}$ set by GDC-bits; index "05"). The HSN output signal can be generated early by PSO-bits (index "07") with respect to CBN to compensate for pipelining delay $t_{Rint}$ of the RAM interface (valid also in stand-alone mode).

The horizontal timing is independent of active video at data inputs PDn(7-0). The line blanking period on the outputs is set to approximately 12 µs in 50 Hz standards (11 µs in 60 Hz standards).

Slave mode:
HSN pin is used as an input. The active edge of the input signal is assumed to fit to the incoming CBN signal. Deviations can be compensated in the range of the GCD-bits (index "05").

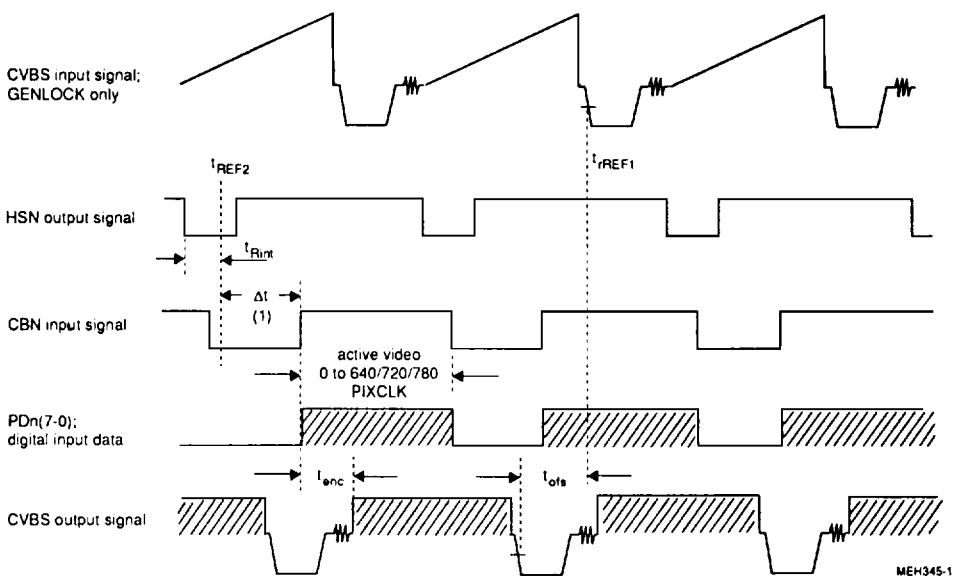



Fig.10 Horizontal timing. $t_{Rint}$ = pipeline delay of RAM interface adjustable from −5 to +58 pixel clocks (PIXCLK); $t_{ofs}$ = propagation delay of external GENLOCK line adjustable from −17 to +46 pixel clocks.

(1) Δt = 125 x PIXCLK at 12.27 MHz
Δt = 163 x PIXCLK at 14.75 MHz
Δt = 134 x PIXCLK at 13.50 MHz / 50 Hz mode
Δt = 122 x PIXCLK at 13.50 MHz / 60 Hz mode

The $t_{enc}$ time is the total delay from data input to analog CVBS output; it is 55 pixel clock periods long (PIXCLK) plus the propagation delay of the LDV input register regardless of mode and colour standard.
The key input signal is delay-compensated with respect to PDn(7-0)data input.
The generated vertical field and burst blanking sequences are shown in Fig.11 (50 Hz PAL) and Fig.12 (60 Hz NTSC).

**Reset**

Prior to a reset all outputs are undefined. RESN = LOW sets the circuit into the slave mode: MOD1 bit = 1; MOD0-bit = 0. All other control register bits are set to zero. The outputs CSYN/VSN, HSN, SLT, HSY and HCL are automatically set to high-impedance state. The $I^2C$-bus interface is set to a slave receiver.
The D(7-0) pins of the MPU interface are inputs during RESN = LOW. As the circuit requires an external clock signal on pin CLKIN in slave mode, the clock select signal CLKSEL (pin 50) must be LOW during RESN = LOW (pin 54). The LOW time of RESN is preliminary at least 50 pixel clock periods long.

**Disable chip**

All analog outputs are set to zero by DD-bit = 1 (index "08"); while the outputs CSYN/VSN, HSN, HCL, HSY and SLT are set to high-impedance state. The internal clock is divided by 4 at DD-bit = 1.
The circuit can be disabled for any reason. It must be disabled when CLKIN exceeds 32 MHz. After setting DD-bit = 1, the CLKIN input signal can be set to a frequency of < 60 MHz (modification of control registers and RAM tables is not ensured).
To enable the circuit again, CLKIN must be set to a frequency < 32 MHz, a reset (hardware) then is required to set DD-bit to zero.

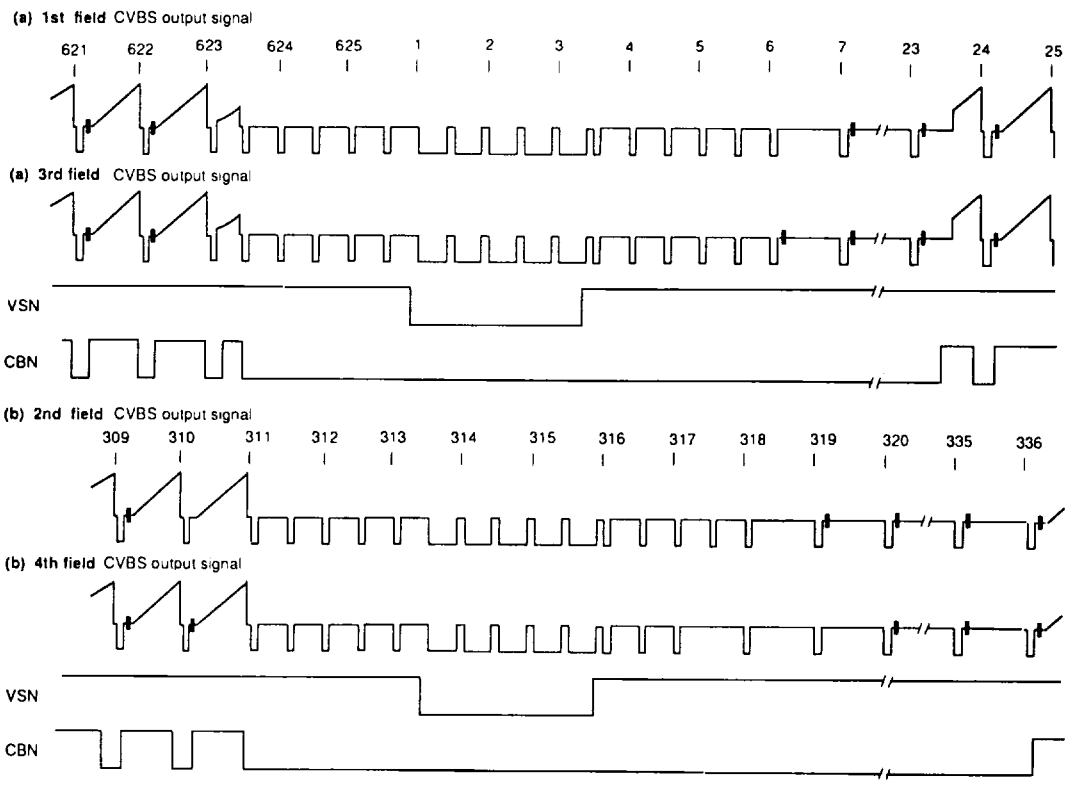



Fig.11 Vertical field and burst blanking sequence for PAL 50 Hz mode.

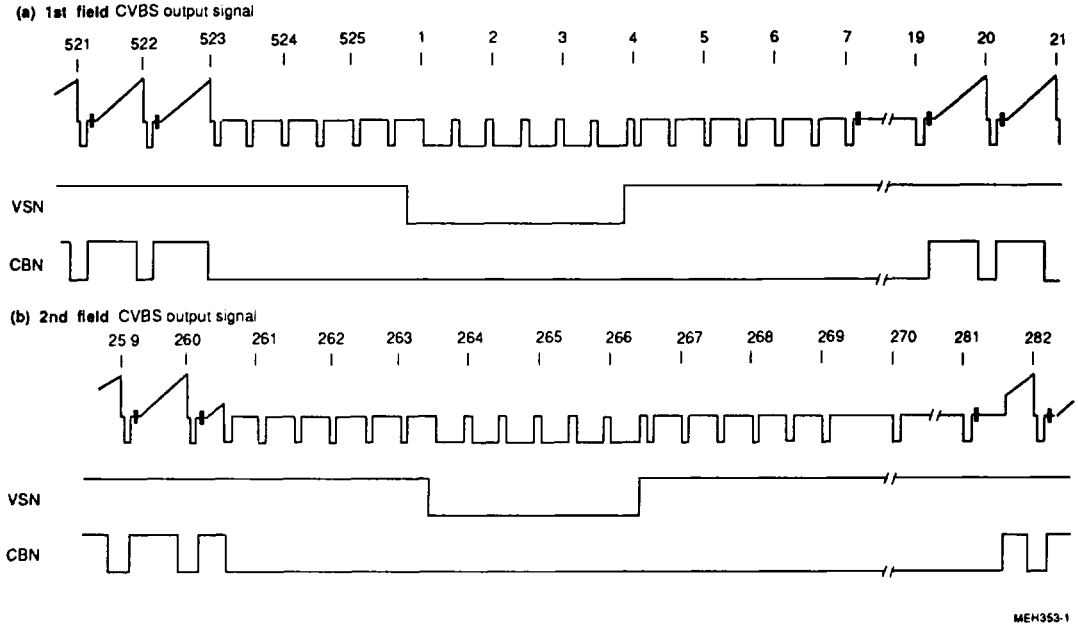



Fig.12 Vertical field and burst blanking sequence for NTSC 60 Hz mode.

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| $V_{DDD1}$ | supply voltage (pin 2) | −0.3 | 7 | V |
| $V_{DDD2}$ | supply voltage (pin 21) | −0.3 | 7 | V |
| $V_{DDD3}$ | supply voltage (pin 41) | −0.3 | 7 | V |
| $V_{DDA1}$ | supply voltage (pin 66) | −0.3 | 7 | V |
| $V_{DDA2}$ | supply voltage (pin 70) | −0.3 | 7 | V |
| $V_{DDA3}$ | supply voltage (pin 72) | −0.3 | 7 | V |
| $V_{DDA4}$ | supply voltage (pin 64) | −0.3 | 7 | V |
| $V_{diff\ GND}$ | difference voltage between digital and analog ground pins ($V_{DDDn} - V_{DDAn}$) | - | ±100 | mV |
| $V_n$ | voltage on all pins, grounds excluded | 0 | $V_P$ | V |
| $P_{tot}$ | total power dissipation | - | 1.1 | W |
| $T_{stg}$ | storage temperature range | −65 | 150 | °C |
| $T_{amb}$ | operating ambient temperature range | 0 | 70 | °C |
| $V_{ESD}$ | electrostatic handling* for all pins | ±2000 | - | V |

* Equivalent to discharging a 100 pF capacitor through an 1.5 kΩ series resistor.

## CHARACTERISTICS

$V_{DDD}$ = 4.5 to 5.5 V; $V_{DDA}$ = 4.75 to 5.25 V; $T_{amb}$ = 0 to 70 °C unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{DDD}$ | digital supply voltage range (pins 2, 21 and 42) | | 4.5 | 5 | 5.5 | V |
| $V_{DDA}$ | analog supply voltage range (pins 66, 70 and 72) | | 4.75 | 5 | 5.25 | V |
| $I_{DDD}$ | digital supply current $I_{DDD1}$ to $I_{DDD3}$ | 40 pF output load | - | - | 140 | mA |
| $I_{DDA}$ | analog supply current $I_{DDA1}$ to $I_{DDA3}$ | 40 pF output load | - | - | 60 | mA |
| **Data and control inputs** (pins 3 to 20, 23 to 40, 43 to 46, 49, 50, 54 to 56, 59, 73 and 76 to 84) | | | | | | |
| $V_{IL}$ | input voltage LOW | note 1 | 0 | - | 0.8 | V |
| $V_{IH}$ | input voltage HIGH | note 1 | 2.0 | - | $V_{DDD}$+ 0.5 | V |
| $I_{LI}$ | input leakage current | | - | - | ±1 | µA |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $C_I$ | input capacitance | data inputs | - | - | 8 | pF |
| | | CLKIN, LLC, LDV | - | - | 10 | pF |
| | | 3-state I/O | - | - | 10 | pF |
| **LFCO output** (pin 61) | | | | | | |
| $V_o$ | output signal (peak-to-peak value) | | 1.4 | - | 2.6 | V |
| $V_{61}$ | output voltage range | | 0 | - | $V_{DDD}$ | V |
| **Data and other control outputs** (pins 3, 51, 52, 57, 58, 60, 74 and 75) | | | | | | |
| $V_{OL}$ | output voltage LOW | note 2 | 0 | - | 0.6 | V |
| $V_{OH}$ | output voltage HIGH | note 2 | 2.4 | - | $V_{DDD}$ | V |
| **C, Y and CVBS analog outputs** (pins 65, 67 and 69) | | | | | | |
| $V_o$ | output signal (peak-to-peak value) | without load; $V_{DDA}$ = 5 V | - | 2 | - | V |
| $V_{65,67,69}$ | minimum output voltage | without load; $V_{DDA}$ = 5 V | - | 0.2 | - | V |
| | maximum output voltage | without load; $V_{DDA}$ = 5 V | - | 2.2 | - | V |
| $R_{65,67,69}$ | internal serial output resistance | not tested | 18 | 25 | 35 | Ω |
| $R_{L\ 65,67,69}$ | output load resistance | recommendation | 90 | - | - | Ω |
| B | output signal bandwidth | -3 dB | 10 | - | - | MHz |
| ILE | LF integral linearity error | 9-bit data | - | - | ±1.0 | LSB |
| DLE | LF differential linearity error | 9-bit data | - | - | ±0.5 | LSB |
| $I_{CUR}$ | input current (pin 71) | Fig.1; $R_{70-71}$ = 20 kΩ | - | 300 | - | μA |
| **I²C-bus SDA and SCL** (pins 47 and 48) | | | | | | |
| $V_{IL}$ | input voltage LOW | | –0.5 | - | 1.5 | V |
| $V_{IH}$ | input voltage HIGH | | 3.0 | - | $V_{DDD}$+0.5 | V |
| $I_I$ | input current | $V_I$ = LOW or HIGH | - | - | ±10 | μA |
| $V_{OL}$ | SDA output voltage (pin 47) | $I_{47}$ = 3 mA | - | - | 0.4 | V |
| $I_{47}$ | output current | during acknowledge | 3 | - | - | mA |
| **Crystal oscillator** | | Fig.14 | | | | |
| $f_n$ | nominal frequency | 3rd harmonic; Table 1 | - | 24.576 | - | MHz |
| | | 3rd harmonic; Table 1 | - | 26.8 | - | MHz |
| $\Delta f / f_n$ | permissible deviation $f_n$ | | - | 50 | - | $10^{-6}$ |
| X1 | crystal specification: | | | | | |
| | temperature range $T_{amb}$ | | 0 | - | 70 | °C |
| | load capacitance $C_L$ | | 8 | - | - | pF |
| | series resonance resistance $R_S$ | | - | 40 | 80 | Ω |
| | motional capacitance $C_1$ | | - | 1.5±20% | - | fF |
| | parallel capacitance $C_0$ | | - | 3.5±20% | - | pF |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **LLC and LDV timing** (pins 55 and 20) | | Fig.16 | | | | |
| $t_{LLC}$ | cycle time | note 3 | 31.5 | - | 44.5 | ns |
| $t_{CH}$ | pulse width | | 40 | 50 | 60 | % |
| $t_r$ | rise time | | - | - | 5 | ns |
| $t_f$ | fall time | | - | - | 6 | ns |
| $t_{LDV}$ | cycle time | | 63 | - | 89 | ns |
| $t_{SUL}$ | LDV set-up time | | 4 | - | - | ns |
| $t_{HDL}$ | LDV hold time | | 10 | - | - | ns |
| **PIXCLK and CLKO timing** (pins 51 and 52) | | Fig.16 | | | | |
| $t_{DCK}$ | PIXCLK and CLKO delay time | | - | - | 25 | ns |
| **PD1(7-0), PD2(7-0), PD3(7-0), CBN, MPK, KEY and RTCI input timing** (pins 4 to 19, 23 to 32, 57 and 73) | | | | | | |
| $t_{SUD}$ | input data set-up time | Fig.16 | 4 | - | - | ns |
| $t_{HDD}$ | input data hold time | | 6 | - | - | ns |
| **CVBS (7-0), VSN/CSYN and HSN timing** (pins 76 to 83, 3 and 84) | | | | | | |
| $t_{SU}$ | input data set-up time | Fig.17 | 10 | - | - | ns |
| $t_{HD}$ | input data hold time | | 5 | - | - | ns |
| **CREF timing** (pin 56) | | Fig.17 | | | | |
| $t_{SUC}$ | input set-up time | | 10 | - | - | ns |
| $t_{HDC}$ | input hold time | | 2 | - | - | ns |
| **MPU timing A1, A0, R/WN, CSN, D(7-0)** (pins 33 to 36, 37 to 40 and 43 to 46); Fig.18 | | | | | | |
| $t_{SA}$ | A1 and A0 address set-up time (pins 33, 34) | | 4 | - | - | ns |
| $t_{HA}$ | A1 and A0 address hold time | | 25 | - | - | ns |
| $t_{SR}$ | R/WN set-up time (pin 35) | | 4 | - | - | ns |
| $t_{HR}$ | R/WN hold time | | 25 | - | - | ns |
| $t_{CL}$ ,$t_{CH}$ | CSN pulse width LOW and HIGH | note 4 | 95 | - | - | ns |
| $t_{SW}$ | data set-up time (D7 to D0) | write | 80 | - | - | ns |
| $t_{HW}$ | data hold time (D7 to D0) | write | 5 | - | - | ns |
| $t_{HDR}$ | data output hold time (D7 to D0) | read | 5 | - | - | ns |
| $t_{ZR}$ | delay to driven ports (D7 to D0) | read | 5 | - | - | ns |
| $t_{DR}$ | delay to ports valid (D7 to D0) | read; note 5 | - | - | 275 | ns |
| $t_{RZ}$ | port outputs disable time (D7 to D0) | read | - | - | 25 | ns |
| **Output timing** (pins 3, 74, 75 and 84) | | Fig.17 | | | | |
| $t_{OD}$ | output delay time | minimum clock period; note 6 | - | 20 | 40 | ns |

**Notes to the characteristics**

1. XTAL, XTALI and TP are not characterized with respect to levels; CLKO is characterized up to 32 MHz and PIXCLK up to 16 MHz
2. Levels are measured with load circuit. LFCO output with 10 kΩ in parallel to 15 pF and other outputs with 1.2 kΩ in parallel to 40 pF at 3V (TTL load).
3. $t_{LLC}$ has to be in the range 63 to 89 ns at CREF = HIGH (pin 56); $t_{LLC}$ = 16.5 ns is allowed only if the multiplexer clock is active.
4. $t_{PIXCLK(min)}$ + 5 ns.
5. 3 x ($t_{PIXCLK(min)}$ + 5 ns).
6. 40 ns at low supply voltage (4 V) and high temperature (70 °C).

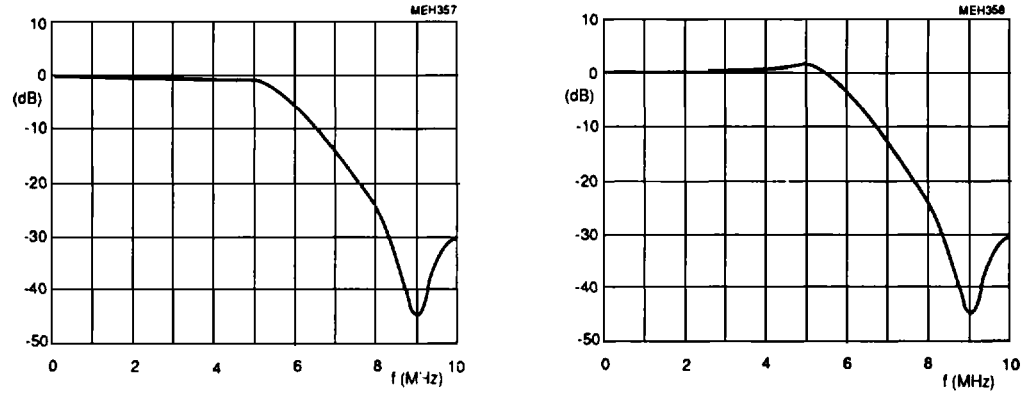



Fig.13 Characteristics of low-pass post-filters. Left: without compensation of DC hold characteristic. Right: with compensation of DC hold characteristic.

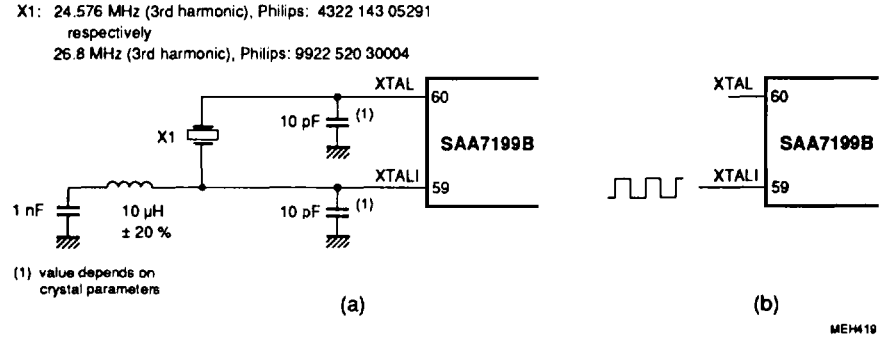
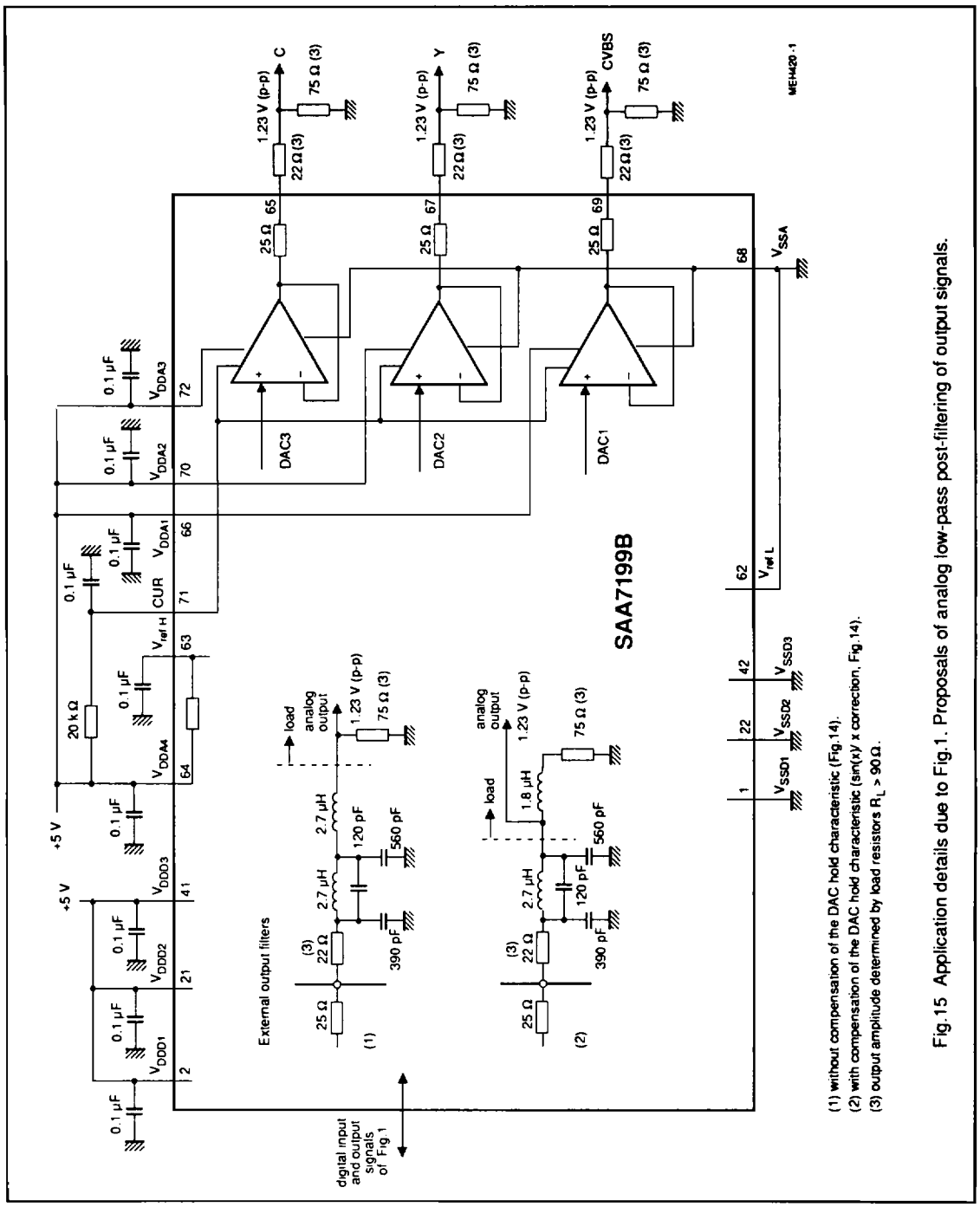



Fig.14 Oscillator application (a) and optional external clock sync (b).




(1) without compensation of the DAC hold characteristic (Fig.14).
(2) with compensation of the DAC hold characteristic (sin(x)/x correction, Fig.14).
(3) output amplitude determined by load resistors $R_L > 90\ \Omega$.

Fig.15 Application details due to Fig.1. Proposals of analog low-pass post-filtering of output signals.

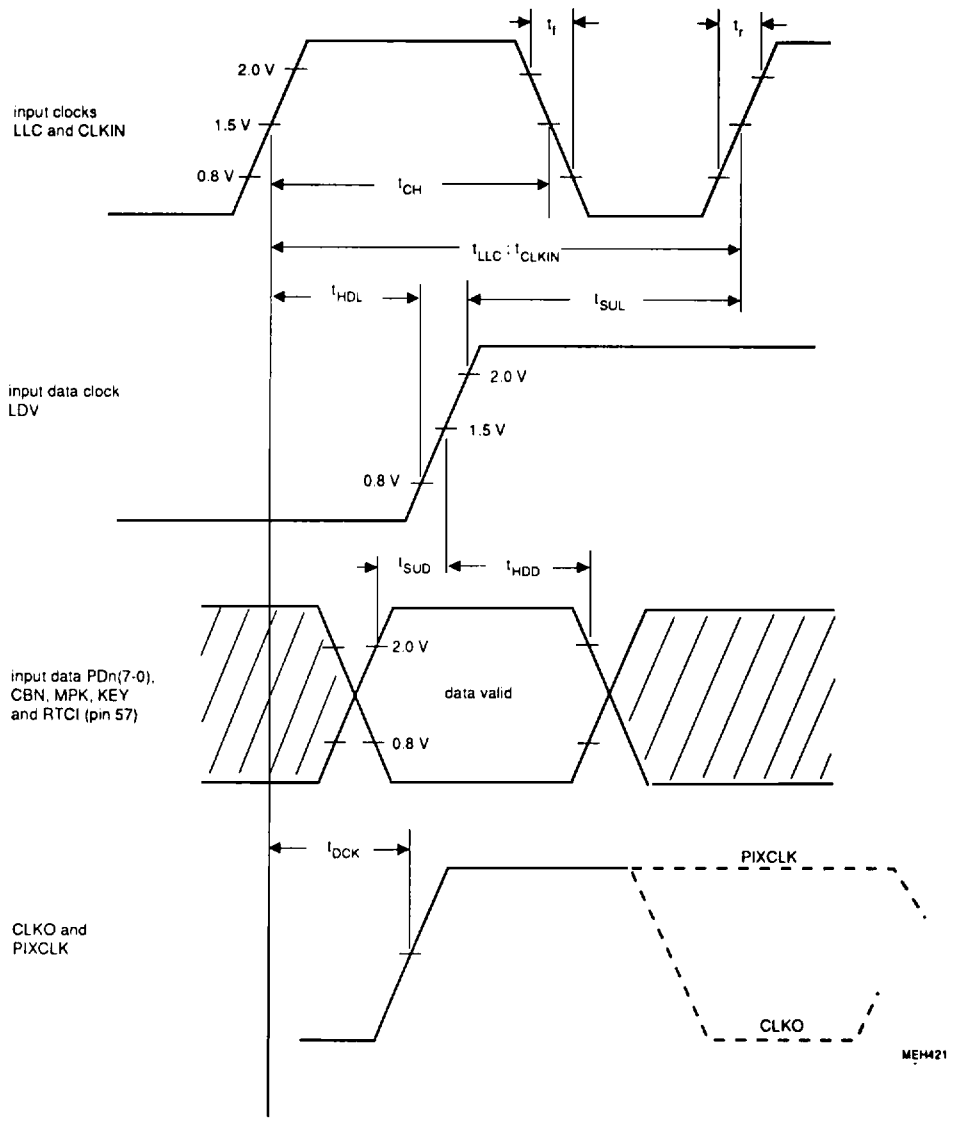



Fig.16 LDV input data timing.

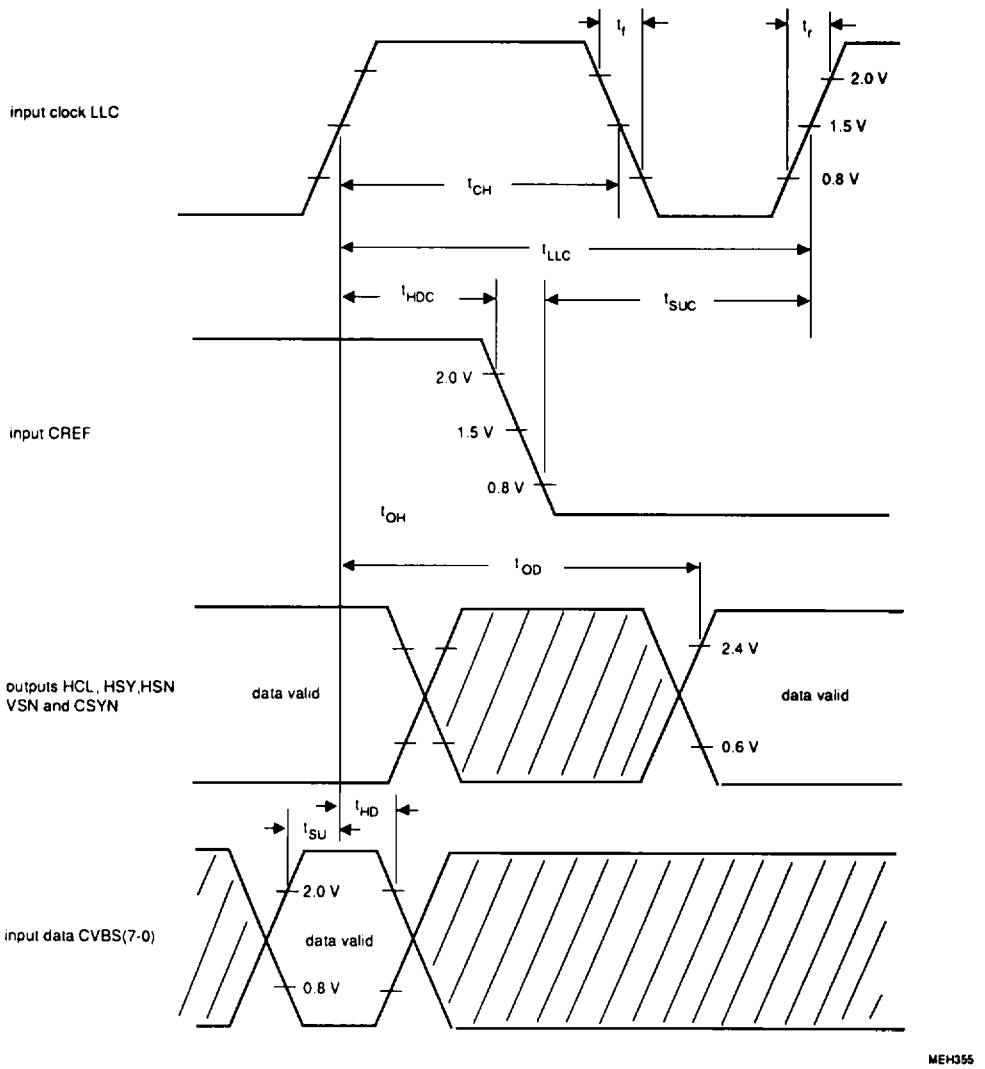



Fig.17 Clock and data timing.

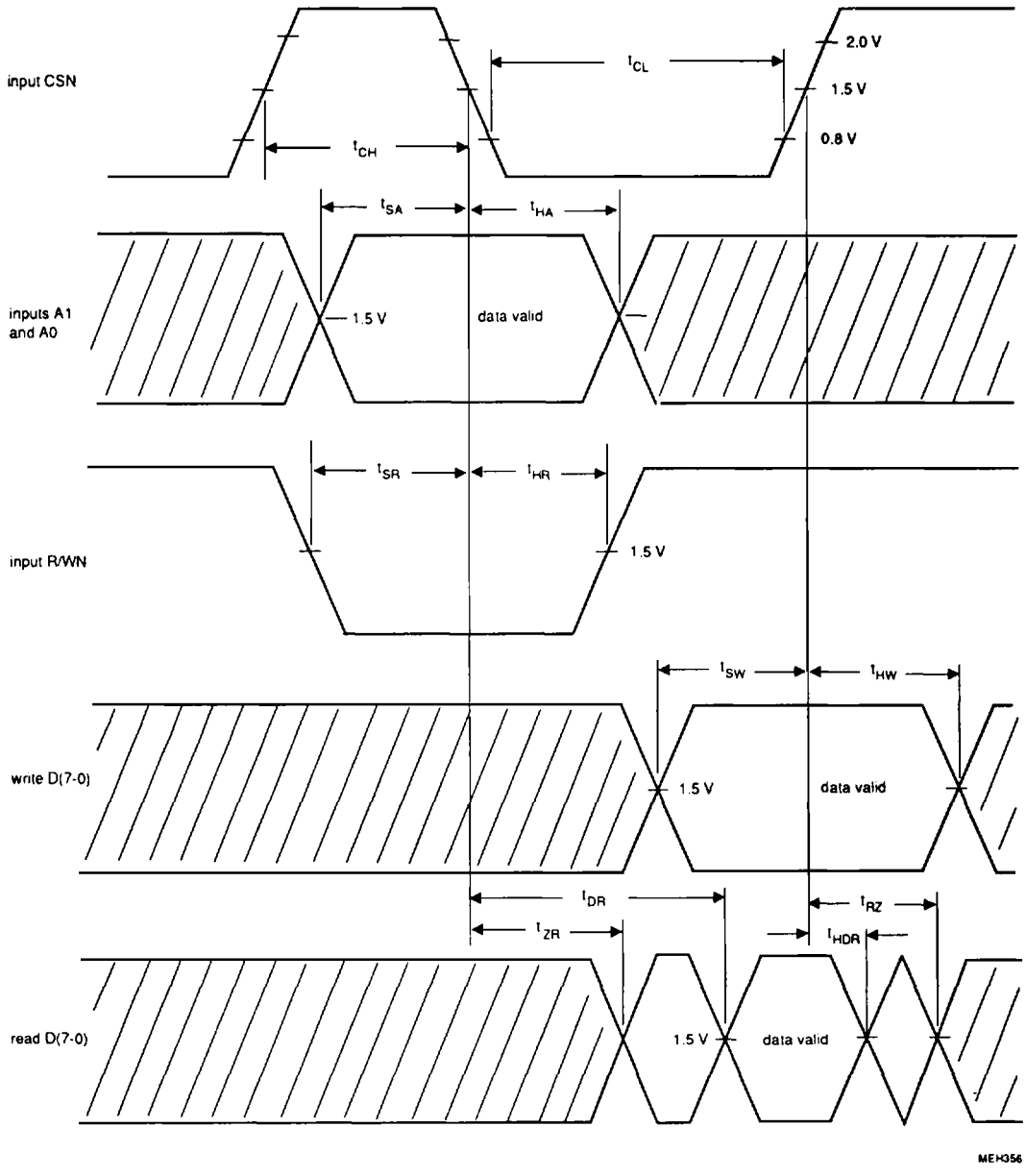



Fig.18 MPU-bus timing.