μPD72068
Floppy-Disk Controller

PRELIMINARY

Description

The μPD72068 FDC is one of NEC's integrated solutions for today's floppy-disk controller designs. An outgrowth of the μPD765A—long established as the industry standard for floppy-disk contol—the μPD72068 maintains complete microcode compatibility and contains the latest enhancements required for multitasking applications. Additionally, the μPD72068 integrates the standard host-interface registers used in IBM PC, PC/XT, PC/AT, and PS/2® designs.

The μPD72068 incorporates a high-performance digital PLL that is impervious to harmonic lock-on, a characteristic of analog counterparts. Being digital, the PLL requires no adjustments and supports all standard data rates as well as 600 kb/s.

The μPD72068 has on-chip clock generation, selectable write precompensation, and all the circuitry necessary for interfacing directly to four floppy-disk drives.

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Features

- Software compatible with μPD765A/765B, μPD7265, μPD72065/65B, μPD72066, and μPD72067
- Compatible with V-Series data/control bus and other standard 8/16-bit CPUs
- IBM and ECMA/ISO formats
- Data transfer rate: 600, 500, 300, 250, 150 kb/s
- High-performance, on-chip digital PLL
- Two system clock generators
- Programmable stepping speed
- Write-compensate circuit (programmable preshift)
- FDD interface
  - — High-current drivers (24-mA sink)
  - — Schmitt receivers
- Direct control of four FDDs
  - — Spindle motor control
  - — Unit select control
- Three selectable modes support:
  - — PC, PC/XT, PC/AT, PS/2 registers
  - — Internal operating mode selection
  - — External operating mode selection

Ordering Information

Part Number	Package
μPD72068GF-3B9	80-pin plastic miniflat
μPD72068L	84-pin PLCC (plastic leaded chip carrier)

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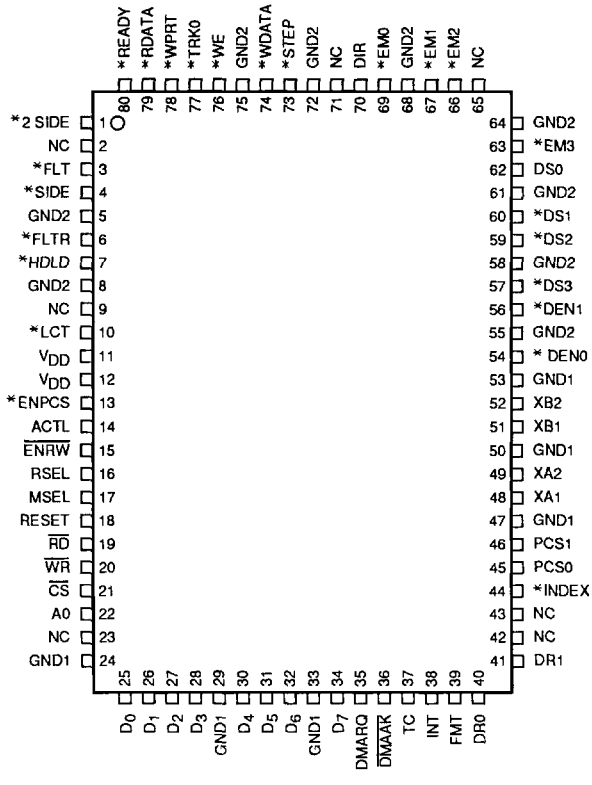
Pin Configurations

80-Pin Plastic Miniflat



* Active level is variable.

Connect GND1 and GND2 to ground with the shortest possible wiring.

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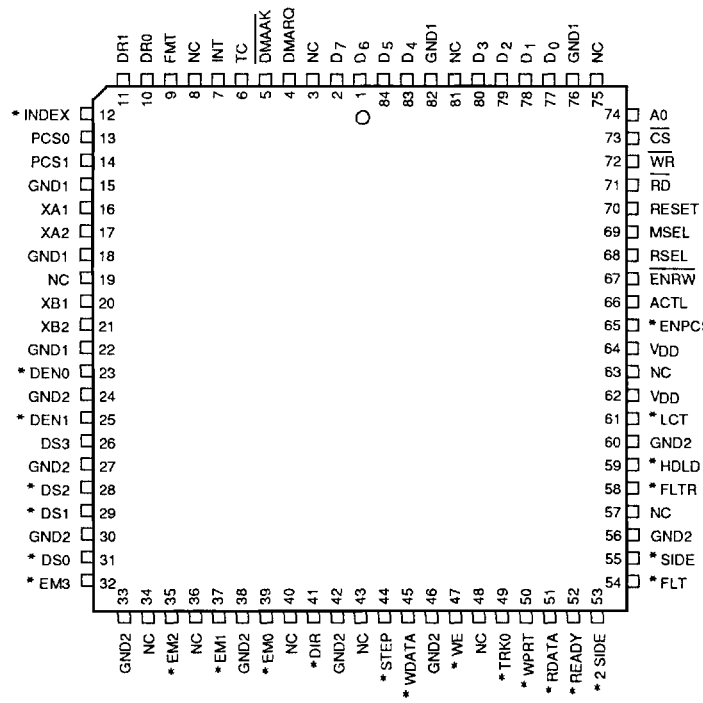
84-Pin PLCC



* Active level is variable.

Connect GND1 and GND2 to ground with the shortest possible wiring.

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Pin Identification

Symbol	I/O	Signal Function
A0	In	Address 0. Selects μPD72068 registers. A0 Registers 0 Status, auxiliary command, digital out 1 Data, control
ACTL	In	Active Level. Sets active level of drive interface signal. ACTL Active Level 0 High 1 Low
$\overline{CS}$	In	Chip Select. Validates $\overline{RD}$ and $\overline{WR}$ signals when MSEL = 0. In Register mode (MSEL = 1), $\overline{CS}$ may be used as address line 1 in a typical PC system.
D_0-D_7	I/O	Data Bus. Bidirectional, three-state data bus.
DEN0, DEN1 (*)	Out	Density. Specifies preset data transfer rate; can be used for FDD data transfer rate control. See table 1.
DIR (*)	Out	Direction. Specifies the seek direction. DIR Seek Direction 0 Centrifugal 1 Centripetal
$\overline{DMAAK}$	In	DMA Acknowledge. Enables DMA cycle.
DMARQ	Out	DMA Request. Requests data transfer in DMA mode.
DR0, DR1	In	Data Rate. Sets data transfer rate in external mode. For internal mode, pull these pins low with high-value resistors.
DS0-DS3 (*)	Out	Drive Select. Selects up to four FDDs.
EM0-EM3 (*)	Out	Enable Motor. Controls spindle motor on/off; also can be used as a general-purpose output port.
ENPCS (*)	In	Enable Precompensation. ACTL ENPCS Preshift Value 0 0 0 ns 0 1 Assigned by mode 1 0 Assigned by mode 1 1 0 ns If the preshift amount is to be varied according to the number of cylinders, the appropriate control signal is input on ENPCS. When applying preshifting to cylinders 43 and above, variable control can be performed automatically by connecting the ENPCS and LCT pins.
$\overline{ENRW}$	In	Enable Read Write. Validate $\overline{RD}$ and $\overline{WR}$ signals when MSEL = 1. When MSEL = 0, this signal is meaningless.
FLT (*)	In	*Fault. Indicates FDD is faulty.*
FLTR (*)	Out	Fault Reset. Releases FDD from fault state.
FMT	In	Format. Selects format in external mode. FMT Format 0 IBM 1 ECMA For internal mode, pull this pin low with a high-value resistor.

Symbol	I/O	Signal Function
HDLD (*)	Out	Head Load. Causes the drive head to contact the diskette.
INDEX (*)	In	Indicates drive head is positioned at physical start point of track on the medium.
INT	Out	Interrupt Request. Requests main system to process transferred data and execution results.
LCT (*)	Out	Low Current. Indicates drive head has selected a cylinder after the 43rd.
MSEL	In	Mode Select. Validates IBM-PC register and on-chip peripheral circuits.
PCS0, PCS1	In	Precompensation. Selects the preshift amount in external or register mode. For internal mode, pull these pins low with high-value resistors.
$\overline{RD}$	In	Read. This control signal causes the main system to read data from the μPD72068 to the data bus.
RDATA (*)	In	Read data (consists of clock and data bits) from FDD.
READY (*)	In	Indicates FDD is ready.
RESET	In	Sets μPD72068 to idle state. FDD interface outputs except for WDATA (undefined) are: ACTL Output 0 All low 1 All high For the main system, INT and DMARQ are set to low and D_0-D_7 are set for input. When MSEL = 0, μPD72068 enters external mode directly after a reset.
RSEL	In	Register Select. When MSEL = 1, used with $\overline{CS}$ and A0 to select registers for IBM-PC (digital out register and control register). Invalid when MSEL = 0
SIDE (*)	Out	Side Select. Selects double-sided drive head. ACTL SIDE Drive Head 0 (Active high) 0 Head 0 0 1 Head 1 1 (Active low) 0 Head 1 1 1 Head 0
STEP (*)	Out	Generates seek pulses.
TC	In	Terminal Count. Terminates data transfer.
TRK0 (*)	In	Indicates drive head is positioned at cylinder 0.
WDATA (*)	Out	Write data (clock and data bits) to FDD.
WE (*)	Out	Requests FDD to write data.
WPRT (*)	In	Indicates medium is write-protected.
$\overline{WR}$	In	Write. Control signal that allows the main system to write data bus data into μPD72068.

Pin Identification (cont)

Symbol	I/O	Signal Function
XA1, XA2	In	Crystal A. For internal oscillator frequency control, a crystal resonator is connected to XA1 and XA2. For external clock input at XA1, XA2 is open. Frequency = 32 MHz To support only 500/250 kb/s data rates, crystal B is not necessary; connect XA2 to XB1.
XB1, XB2	In	Crystal B. For internal oscillator frequency control, a crystal resonator is connected to XB1 and XB2. For external clock input at XB1, XB2 is open. Frequency / Data Rate 38.4 MHz / 600 kb/s 19.2 MHz / All other rates To support only 500/250 kb/s data rates, crystal B is not necessary; connect XA2 to XB1.
2SIDE (*)	In	Indicates a medium with two usable sides has been loaded into the FDD.
NC	—	No Connection.
GND1	—	Digital system ground.
GND2	—	Buffer system ground.
V_{DD}	In	+5-volt power supply

(*) Active high when ACTL = 0; active low when ACTL = 1.

Pin Reset Status

Pin	Reset Status
D_0-D_7	Input
DMARQ, INT	Low
WDATA	Undefined
DIR, DS0-DS3, EM0-EM3, FLTR, HDLD, LCT, SIDE, STEP, WE	Low when ACTL =0; high when ACTL= 1.
DEN0, DEN1	Output depends on the preset data transfer rates. Value set when ACTL = 0 is inverted when ACTL = 1, and vice versa.
Other pins	

Table 1. Data Transfer Rate Settings

Mode	Input Pins DR1	DR0	D1	D0	MFM Data Transfer Rate (kb/s)	Output Pins DEN1	DEN0
Internal/ external (Note 1)	0	0	—	—	250	1	0
	0	1	—	—	500	1	1
	1	0	—	—	150 (300)	1	0
	1	1	—	—	300 (600)	0	0
Register (Note 2)	0	x	0	0	500	1	1
	0	x	0	1	250	1	0
	0	x	1	0	250	1	0
	0	x	1	1	150 (300)	1	0
	1	x	0	0	500	1	1
	1	x	0	1	300 (600)	0	0
	1	x	1	0	250	1	0
	1	x	1	1	150 (300)	1	0

Notes:

(1) In internal mode, DR1 and DR0 are bits of the CONTROL INTERNAL MODE command. In external mode, DR1 and DR0 are input pins.

(2) In register mode, DR0 input pin status is "Don't Care" (x).

(3) Data transfer rates in parentheses are with a 38.4-MHz crystal resonator connected to pins XB1 and XB2 or a 38.4-MHz clock connected to pin XB1.

(4) Data transfer rates are for MFM mode. In FM mode, these rates are halved.

(5) DEN1 and DN0 values are when ACTL = 1 (active low). When ACTL = 0 (active high), values are inverted.

Operation Modes

Since μPD72068 has been developed from μPD72067, the external and internal modes available for μPD72067 are also available for μPD72068 (exept the external VFO mode). In addition, the register mode is available for μPD72068. The register mode is used to operate the IBM-PC registers and special-purpose circuits of μPD72068. Procedures for setting the data transfer rate, precompensation amount, etc., vary depending on the modes. The differences in the procedures are shown in table 2.

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Table 2. Operation Modes

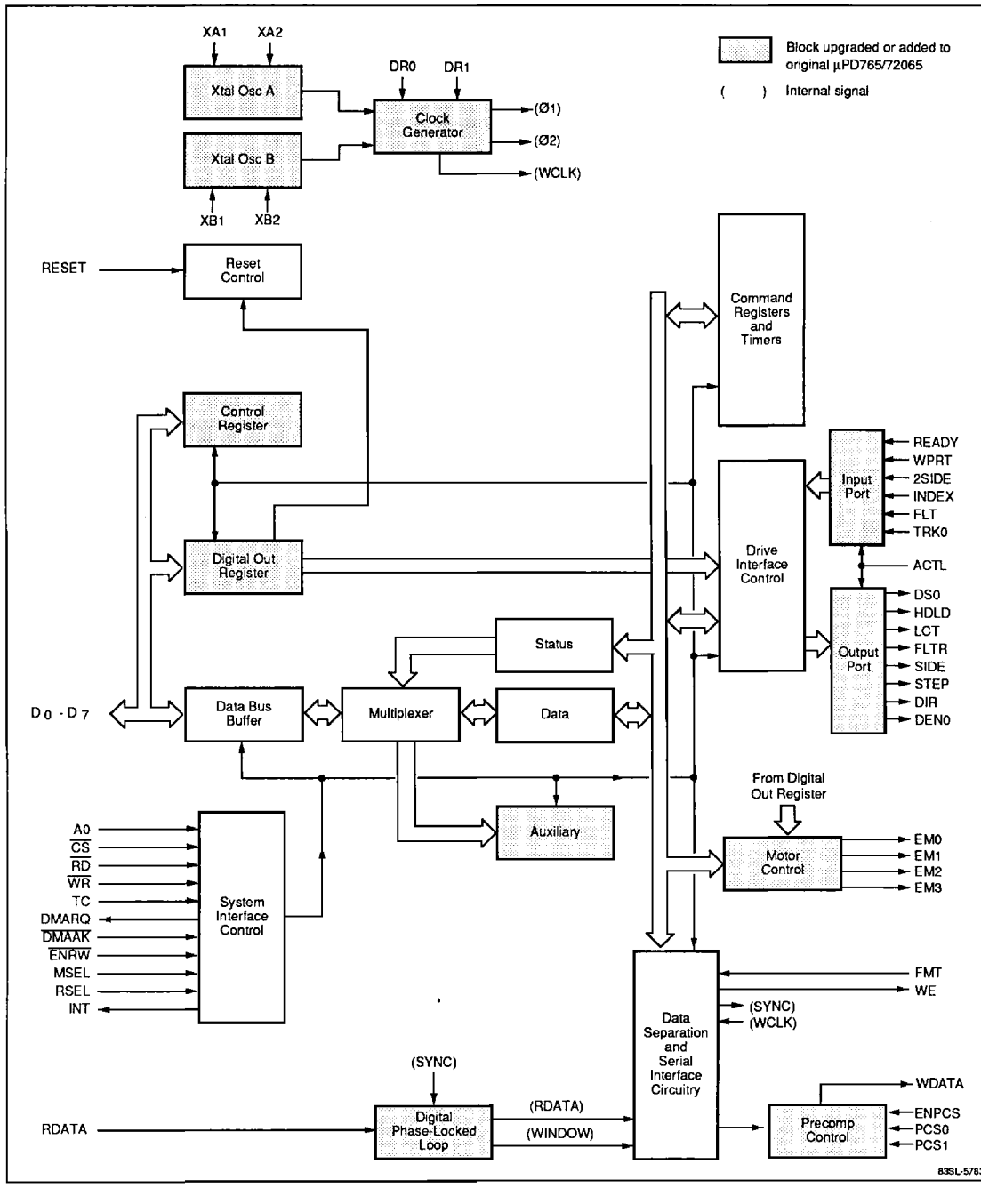
Mode	MSEL Pin	Command	Data Transfer Rate Setting	Drive Select	Precompensation Amount Setting	Format Change	Motor On/Off Control
Register mode	1	None	D0 and D1 bits and DR1 pin of control register	Digital out register	PCS0, PCS1, and DR1 pins	FMT pin	Digital out register
Internal mode	0	Note 1	CONTROL INTERNAL MODE command	US1 and US0 bits in the command	CONTROL INTERNAL MODE command	SELECT FORMAT command	ENABLE MOTORS command
External mode	0	Note 2	DR1 and DR0 pins		PCS1, PCS0, and DR1 pins	FMT pin	

Notes:

(1) CONTROL INTERNAL MODE command

(2) ENABLE EXTERNAL MODE command

μPD72068 Block Diagram



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Absolute Maximum Ratings

T_A = +25°C

Supply voltage, V_{DD}	−0.5 to +7.0 V
Voltage on any pin (except V_{DD})	−0.5 to +7 V
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to 150°C

Capacitance

T_A = +25°C; V_{DD} = 0 V; f = 1 MHz

Parameter	Symbol	Min	Max	Unit	Conditions
Clock capacitance	C_ϕ		20	pF	Unmeasured pins returned to 0 V.
Input capacitance	C_{IN}		20	pF	
Output capacitance	C_{OUT}		20	pF	

Oscillator Specifications

T_A = −10 to +70°C; V_{DD} = +5 V ±10%; see figures 1, 2, and 3.

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Crystal Resonator Source						
Oscillator stabilization time (Note 1)	t_{KS}			10	ms	
External Clock, Direct Input						
Low-level input voltage	V_{IL}	−0.5		0.2 V_{DD}	V	Pins XA1, XB1
High-level input voltage	V_{IH}	0.8 V_{DD}		V_{DD} + 0.5	V	
Clock cycle	t_{CYA}		31.25		ns	Pin XA1
	t_{CYB}		52.08		ns	19.2-MHz clock input to pin XB1
			26.04		ns	38.4-MHz clock input to pin XB1
Permissible clock cycle error from typical value (Note 2)				±0.5	%	Pins XA1, XB1
Clock high-level width	t_{KKH}	7.0			ns	Pin XA1
		15.0			ns	Pin XB1; t_{CYB} = 52.08 ns
		6.0			ns	Pin XB1; t_{CYB} = 26.04 ns
Clock low-level width	t_{KKL}	7.0			ns	Pin XA1
		15.0			ns	Pin XB1; t_{CYB} = 52.08 ns
		6.0			ns	Pin XB1; t_{CYB} = 26.04 ns
Clock rise time	t_{KR}			5.0	ns	
Clock fall time	t_{KF}			5.0	ns	
External Clock, Capacitor-Coupled Input						
Clock input amplitude	V_{KP-P}	2.0		V_{DD}	V	Pins XA1, XB1
Clock cycle	t_{CYA}		31.25		ns	Pin XA1
	t_{CYB}		52.08		ns	19.2-MHz clock input to pin XB1
			26.04		ns	38.4-MHz clock input to pin XB1
Permissible clock cycle error from typical value (Note 2)				±0.5	%	Pins XA1, XB1
Duty cycle, high-level		40		60	%	

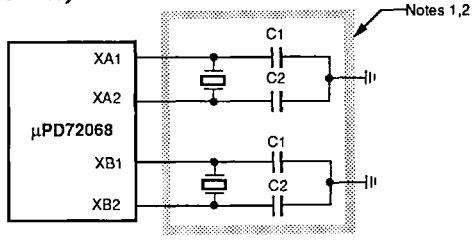
Notes:

(1) Oscillator stabilization time should also be taken as the wait time between the issuance of START CLOCK and RESET STANDBY commands.

(2) Clock cycle error affects DPLL performance.

Figure 1. Recommended External Clock Circuits

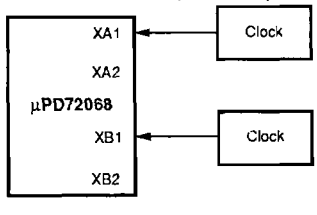
A. Crystal Resonator Source



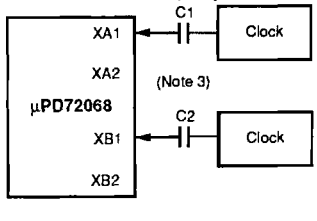
Frequency	*Part No.	C1, C2
32 MHz (pins XA1, XA2)	32 MHz EFD Type	15 pF ±20%
	TQC-254A-6R	10 pF ±20%
	TQC-254A-8R	
19.2 MHz (pins XB1, XB2)	TQC-253A-6R	16 pF ±20%
	TQC-253A-8R	

* Toyo Communication Equipment Co., Ltd.

B. External Clock, Direct Input



C. External Clock, Capacitor-Coupled



Notes:

(1) Oscillator circuit should be as close as possible to pins XA1, XA2, XB1, and XB2.

(2) No other signal lines should pass through shaded box.

(3) C1 and C2 = 110 to 10,000 pf.

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Figure 2. External Clock Waveform

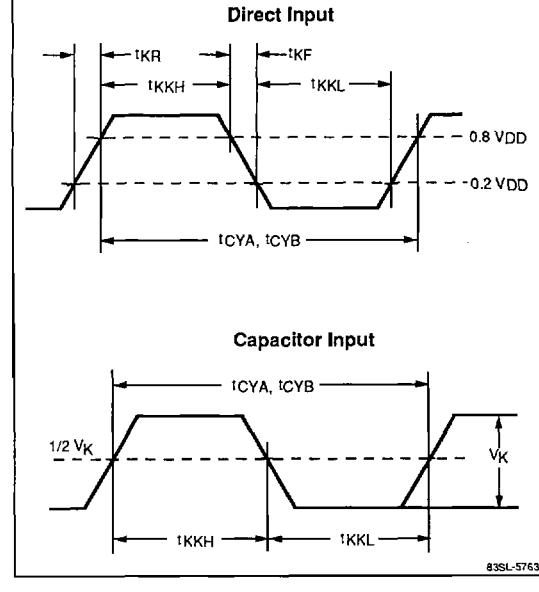
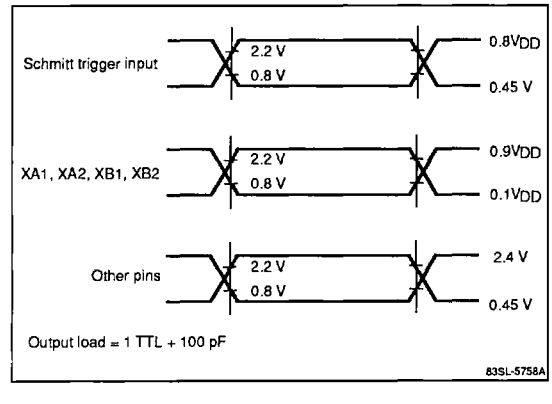


Figure 3. Voltage Thresholds for Timing Measurements



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DC Characteristics

T_A = −10 to +70°C; V_{DD} = +5 V ±10%

Parameter	Symbol	Pin Groups	Min	Max	Unit	Conditions
Low-level input voltage	V_{IL}	2	−0.5	0.8	V	
	V_{IL1}	1	−0.5	0.2 V_{DD}	V	
High-level input voltage	V_{IH}	2	2.2	V_{DD} + 0.5	V	
	V_{IH1}	1	0.8 V_{DD}	V_{DD} + 0.5	V	
Low-level output voltage	V_{OL}	4, 5		0.45	V	I_{OL} = 2.0 mA
	V_{OL1}	3		0.45	V	I_{OL} = 24.0 mA
High-level output voltage	V_{OH}	4, 5	0.7 V_{DD}	V_{DD}	V	I_{OH} = −200 μA
Low-level input leakage current	I_{LIL}	1, 2		−10	μA	V_{IN} = 0 V
High-level input leakage current	I_{LIH}	1, 2		+10	μA	V_{IN} = V_{DD}
Low-level output leakage current	I_{LOL}	4, 5		−10	μA	V_{OUT} = +0.45 V
	I_{LOL1}	3		−100	μA	
High-level output leakage current	I_{LOH}	4, 5		+10	μA	V_{OUT} = V_{DD}
	I_{LOH1}	3		+100	μA	
V_{DD} supply current	I_{DD}			60	mA	Note 1
Standby current	I_{DD1}			100	μA	Note 2

Notes:

(1) When a 32-MHz crystal is connected to XA1-XA2 and a 19.2-MHz crystal is connected to XB1-XB2.

(2) When an external clock is supplied, the clock should be fixed low during standby.

Pin Groups:

(1) Schmitt-trigger inputs: ENPCS, FLT, INDEX, RDATA, READY, TRK0, WPRT, 2SIDE.

(2) Non-Schmitt-trigger inputs and D_0-D_7; excludes XA1, XA2, XB1, XB2.

(3) Drive-side outputs when ACTL = 1 (active-low mode): DEN0-DEN1, DIR, DS0-DS3, EM0-EM3, FLTR, HDLD, LCT, SIDE, STEP, WDATA, WE.

(4) Drive-side outputs when ACTL = 0 (active-high mode): Same pins as group 3.

(5) Other than drive-side outputs; also D_0-D_7.

AC Characteristics 1; 500 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 500 kb/s; t_{CYA} = 31.25 ns (32 MHz at XA1 pin)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	4	t_{AR}	0			ns	For $\overline{ENRW}$ when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	4	t_{RA}	0			ns	
$\overline{RD}$ pulse width	4	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↓	4	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	4	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	4	t_{RI}			400	ns	Note 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	5	t_{AW}	0			ns	For $\overline{ENRW}$ and RSEL when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	5	t_{WA}	0			ns	
$\overline{WR}$ pulse width	5	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	5	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	5	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	5	t_{WI}			400	ns	Note 1
DMARQ cycle time	6	t_{MCY}	13			μs	t_{CYA} = 31.25 ns
$\overline{DMAAK}$ ↓ response time from DMARQ ↑	6	t_{MA}	200			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	6	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	6	t_{AA}	8.5			t_{CYA}	
$\overline{RD}$ ↓ response time from DMARQ ↑	6	t_{MR}	125			ns	t_{CYA} = 31.25 ns
$\overline{WR}$ ↓ response time from DMARQ ↑	6	t_{MW}	250			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	6	t_{MRW}			12	μs	
TC pulse width	6	t_{TC}	60			ns	
RESET pulse width for crystal resonator connection	7	t_{RST}	60			t_{CYA}	During normal operation
			10			ms	On power-on
			10			ms	After standby release
RESET pulse width for external clock input	7	t_{RST}	60			t_{CYA}	During normal operation
			2			ms	On power-on
			60			t_{CYA}	After standby release
Clock hold time on standby	8	t_{WC}	128			t_{CYA}	When external clock is input to XA1 pin
Clock setup time after standby release	8	t_{CW}	64			t_{CYA}	
START CLOCK command write setup time to RESET STANDBY command write	8	t_{WS}	64			t_{CYA}	
INT response time from DMARQ ↓	9	t_{MI}	240		308	t_{CYA}	
$\overline{DMAAK}$ signal invalid from INT ↑	9	t_{IA}			4	t_{CYA}	

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AC Characteristics 1; 500 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
RDATA high-level width	10	t_{RDD}	40			ns	
WDATA high-level width	10	t_{WDD}		250		ns	
DS0-DS3 setup time to DIR (Note 4)	11	t_{DSD}	12			μs	t_{CYA} = 31.25 ns; Note 2
DIR setup time to STEP	11	t_{DST}	1			μs	
DS0-DS3 hold time from STEP (Note 4)	11	t_{STU}	5			μs	
STEP high-level width	11	t_{STP}	6	7	8	μs	
DS0-DS3 hold time from DIR (Notes 3, 4)	11	t_{DDS}	15			μs	
DIR hold time from STEP	11	t_{STD}	24			μs	
STEP cycle time	11	t_{SC}	33			μs	
FLTR high-level width	12	t_{FR}	8		10	μs	
INDEX high-level width	12	t_{IDX}	16			t_{CYA}	

Notes:

(1) For data transfer in non-DMA mode.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 12 μs is actually 11.950 μs.

(3) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(4) Except in register mode.

(5) See figure 3 for timing measurement voltage thresholds.

AC Characteristics 2; 250 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 250 kb/s; t_{CYA} = 31.25 ns (32 MHz at XA1 pin)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	4	t_{AR}	0			ns	For $\overline{ENRW}$ when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	4	t_{RA}	0			ns	
$\overline{RD}$ pulse width	4	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↓	4	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	4	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	4	t_{RI}			400	ns	Note 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	5	t_{AW}	0			ns	For $\overline{ENRW}$ and RSEL when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	5	t_{WA}	0			ns	
$\overline{WR}$ pulse width	5	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	5	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	5	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	5	t_{WI}			400	ns	Note 1
DMARQ cycle time	6	t_{MCY}	26			μs	t_{CYA} = 31.25 ns
$\overline{DMAAK}$ ↓ response time from DMARQ ↑	6	t_{MA}	400			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	6	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	6	t_{AA}	16.5			t_{CYA}	
$\overline{RD}$ ↓ response time from DMARQ ↑	6	t_{MR}	250			ns	t_{CYA} = 31.25 ns
$\overline{WR}$ ↓ response time from DMARQ ↑	6	t_{MW}	500			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	6	t_{MRW}			24	μs	
TC pulse width	6	t_{TC}	60			ns	
RESET pulse width for crystal resonator connection	7	t_{RST}	60			t_{CYA}	During normal operation
			10			ms	On power-on
			10			ms	After standby release
RESET pulse width for external clock input	7	t_{RST}	60			t_{CYA}	During normal operation
			2			ms	On power-on
			60			t_{CYA}	After standby release
Clock hold time on standby	8	t_{WC}	256			t_{CYA}	When external clock is input to XA1 pin
Clock setup time after standby release	8	t_{CW}	128			t_{CYA}	
START CLOCK command write setup time to RESET STANDBY command write	8	t_{WS}	128			t_{CYA}	
INT response time from DMARQ ↓	9	t_{MI}	480		616	t_{CYA}	
$\overline{DMAAK}$ signal invalid from INT ↑	9	t_{IA}			8	t_{CYA}	

5

AC Characteristics 2; 250 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
RDATA high-level width	10	t_{RDD}	40			ns	
WDATA high-level width	10	t_{WDD}		500		ns	
DS0-DS3 setup time to DIR (Note 4)	11	t_{DSD}	24			μs	t_{CYA} = 31.25 ns; Note 2
DIR setup time to STEP	11	t_{DST}	2			μs	
DS0-DS3 hold time from STEP (Note 4)	11	t_{STU}	10			μs	
STEP high-level width	11	t_{STP}	12	14	16	μs	
DS0-DS3 hold time from DIR (Notes 3, 4)	11	t_{DDS}	30			μs	
DIR hold time from STEP	11	t_{STD}	48			μs	
STEP cycle time	11	t_{SC}	66			μs	
FLTR high-level width	12	t_{FR}	16		20	μs	
INDEX high-level width	12	t_{IDX}	32			t_{CYA}	

Notes:

(1) For data transfer in non-DMA mode.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 24 μs is actually 23.950 μs.

(3) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(4) Except in register mode.

(5) See figure 3 for timing measurement voltage thresholds.

AC Characteristics 3; 300 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 300 kb/s; t_{CYA} = 31.25 ns (32 MHz at XA1 pin); t_{CYB} = 52.08 ns (19.2 MHz at XB1 pin)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	4	t_{AR}	0			ns	For $\overline{ENRW}$ when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	4	t_{RA}	0			ns	
$\overline{RD}$ pulse width	4	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↓	4	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	4	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	4	t_{RI}			400	ns	Note 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	5	t_{AW}	0			ns	For $\overline{ENRW}$ and RSEL when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	5	t_{WA}	0			ns	
$\overline{WR}$ pulse width	5	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	5	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	5	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	5	t_{WI}			400	ns	Note 1
DMARQ cycle time	6	t_{MCY}	21.7			μs	t_{CYB} = 52.08 ns
$\overline{DMAAK}$ ↓ response time from DMARQ ↑	6	t_{MA}	333.3			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	6	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	6	t_{AA}	8.3			t_{CYB}	
$\overline{RD}$ ↓ response time from DMARQ ↑	6	t_{MR}	208.3			ns	t_{CYB} = 52.08 ns
$\overline{WR}$ ↓ response time from DMARQ ↑	6	t_{MW}	416.7			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	6	t_{MRW}			20	μs	
TC pulse width	6	t_{TC}	60			ns	
RESET pulse width for crystal resonator connection	7	t_{RST}	60			t_{CYA}	During normal operation
			10			ms	On power-on
			10			ms	After standby release
RESET pulse width for external clock input	7	t_{RST}	60			t_{CYA}	During normal operation
			2			ms	On power-on
			60			t_{CYA}	After standby release
Clock hold time on standby	8	t_{WC}	128			t_{CYB}	When external clock is input to XB1 pin
Clock setup time after standby release	8	t_{CW}	64			t_{CYB}	
START CLOCK command write setup time to RESET STANDBY command write	8	t_{WS}	64			t_{CYB}	
INT response time from DMARQ ↓	9	t_{MI}	240		308	t_{CYB}	
$\overline{DMAAK}$ signal invalid from INT ↑	9	t_{IA}			4	t_{CYB}	

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AC Characteristics 3; 300 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
RDATA high-level width	10	t_{RDD}	40			ns	
WDATA high-level width	10	t_{WDD}		416.7		ns	
DS0-DS3 setup time to DIR (Note 4)	11	t_{DSD}	20			μs	t_{CYB} = 52.08 ns; Note 2
DIR setup time to STEP	11	t_{DST}	1.7			μs	
DS0-DS3 hold time from STEP (Note 4)	11	t_{STU}	8.3			μs	
STEP high-level width	11	t_{STP}	10	11.7	13.3	μs	
DS0-DS3 hold time from DIR (Notes 3, 4)	11	t_{DDS}	25			μs	
DIR hold time from STEP	11	t_{STD}	40			μs	
STEP cycle time	11	t_{SC}	55			μs	
FLTR high-level width	12	t_{FR}	13.3		16.7	μs	
INDEX high-level width	12	t_{IDX}	16			t_{CYB}	

Notes:

(1) For data transfer in non-DMA mode.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 20 μs is actually 19.950 μs.

(3) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(4) Except in register mode.

(5) See figure 3 for timing measurement voltage thresholds.

AC Characteristics 4; 150 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 150 kb/s; t_{CYA} = 31.25 ns (32 MHz at XA1 pin); t_{CYB} = 52.08 ns (19.2 MHz at XB1 pin)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	4	t_{AR}	0			ns	For $\overline{ENRW}$ when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	4	t_{RA}	0			ns	
$\overline{RD}$ pulse width	4	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↓	4	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	4	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	4	t_{RI}			400	ns	Note 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	5	t_{AW}	0			ns	For $\overline{ENRW}$ and RSEL when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	5	t_{WA}	0			ns	
$\overline{WR}$ pulse width	5	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	5	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	5	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	5	t_{WI}			400	ns	Note 1
DMARQ cycle time	6	t_{MCY}	43.4			μs	t_{CYB} = 52.08 ns
$\overline{DMAAK}$ ↓ response time from DMARQ ↑	6	t_{MA}	666.6			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	6	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	6	t_{AA}	16.3			t_{CYB}	
$\overline{RD}$ ↓ response time from DMARQ ↑	6	t_{MR}	416.7			ns	t_{CYB} = 52.08 ns
$\overline{WR}$ ↓ response time from DMARQ ↑	6	t_{MW}	833.4			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	6	t_{MRW}			40	μs	
TC pulse width	6	t_{TC}	60			ns	
RESET pulse width for crystal resonator connection	7	t_{RST}	60			t_{CYA}	During normal operation
			10			ms	On power-on
			10			ms	After standby release
RESET pulse width for external clock input	7	t_{RST}	60			t_{CYA}	During normal operation
			2			ms	On power-on
			60			t_{CYA}	After standby release
Clock hold time on standby	8	t_{WC}	256			t_{CYB}	When external clock is input to XB1 pin
Clock setup time after standby release	8	t_{CW}	128			t_{CYB}	
START CLOCK command write setup time to RESET STANDBY command write	8	t_{WS}	128			t_{CYB}	
INT response time from DMARQ ↓	9	t_{MI}	480		616	t_{CYB}	
$\overline{DMAAK}$ signal invalid from INT ↑	9	t_{IA}			8	t_{CYB}	

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AC Characteristics 4; 150 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
RDATA high-level width	10	t_{RDD}	40			ns	
WDATA high-level width	10	t_{WDD}		833.4		ns	
DS0-DS3 setup time to DIR (Note 4)	11	t_{DSD}	40			μs	t_{CYB} = 52.08 ns; Note 2
DIR setup time to STEP	11	t_{DST}	3.4			μs	
DS0-DS3 hold time from STEP (Note 4)	11	t_{STU}	16.6			μs	
STEP high-level width	11	t_{STP}	20	23.4	26.6	μs	
DS0-DS3 hold time from DIR (Notes 3, 4)	11	t_{DDS}	50			μs	
DIR hold time from STEP	11	t_{STD}	80			μs	
STEP cycle time	11	t_{SC}	110			μs	
FLTR high-level width	12	t_{FR}	26.6		33.4	μs	
INDEX high-level width	12	t_{IDX}	32			t_{CYB}	

Notes:

(1) For data transfer in non-DMA mode.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 40 μs is actually 39.950 μs.

(3) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(4) Except in register mode.

(5) See figure 3 for timing measurement voltage thresholds.

AC Characteristics 5; 600 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 600 kb/s; t_{CYA} = 31.25 ns (32 MHz at XA1 pin); t_{CYB} = 26.04 ns (38.4 MHz at XB1 pin)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	4	t_{AR}	0			ns	For $\overline{ENRW}$ when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	4	t_{RA}	0			ns	
$\overline{RD}$ pulse width	4	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↓	4	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	4	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	4	t_{RI}			400	ns	Note 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	5	t_{AW}	0			ns	For $\overline{ENRW}$ and RSEL when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	5	t_{WA}	0			ns	
$\overline{WR}$ pulse width	5	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	5	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	5	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	5	t_{WI}			400	ns	Note 1
DMARQ cycle time	6	t_{MCY}	10.8			μs	t_{CYB} = 26.04 ns
$\overline{DMAAK}$ ↓ response time from DMARQ ↑	6	t_{MA}	166.7			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	6	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	6	t_{AA}	8.6			t_{CYB}	
$\overline{RD}$ ↓ response time from DMARQ ↑	6	t_{MR}	104.2			ns	t_{CYB} = 26.04 ns
$\overline{WR}$ ↓ response time from DMARQ ↑	6	t_{MW}	208.3			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	6	t_{MRW}			12	μs	
TC pulse width	6	t_{TC}	60			ns	
RESET pulse width for crystal resonator connection	7	t_{RST}	60			t_{CYA}	During normal operation
			10			ms	On power-on
			10			ms	After standby release
RESET pulse width for external clock input	7	t_{RST}	60			t_{CYA}	During normal operation
			2			ms	On power-on
			60			t_{CYA}	After standby release
Clock hold time on standby	8	t_{WC}	128			t_{CYB}	When external clock is input to XB1 pin
Clock setup time after standby release	8	t_{CW}	64			t_{CYB}	
START CLOCK command write setup time to RESET STANDBY command write	8	t_{WS}	64			t_{CYB}	
INT response time from DMARQ ↓	9	t_{MI}	240		308	t_{CYB}	
$\overline{DMAAK}$ signal invalid from INT ↑	9	t_{IA}			4	t_{CYB}	

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AC Characteristics 5; 600 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
RDATA high-level width	10	t_{RDD}	40			ns	
WDATA high-level width	10	t_{WDD}		208.3		ns	
DS0-DS3 setup time to DIR (Note 4)	11	t_{DSD}	10			μs	t_{CYB} = 26.04 ns; Note 2
DIR setup time to STEP	11	t_{DST}	0.8			μs	
DS0-DS3 hold time from STEP (Note 4)	11	t_{STU}	4.2			μs	
STEP high-level width	11	t_{STP}	5.0	5.8	6.7	μs	
DS0-DS3 hold time from DIR (Notes 3, 4)	11	t_{DDS}	12.5			μs	
DIR hold time from STEP	11	t_{STD}	20			μs	
STEP cycle time	11	t_{SC}	27.5			μs	
FLTR high-level width	12	t_{FR}	6.7		8.3	μs	
INDEX high-level width	12	t_{IDX}	16			t_{CYB}	

Notes:

(1) For data transfer in non-DMA mode.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 10 μs is actually 9.950 μs.

(3) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(4) Except in register mode.

(5) See figure 3 for timing measurement voltage thresholds.

AC Characteristics 6; 300 kb/s

T_A = −10 to +70°C; V_{DD} = +5 V ±10%;
MFM data transfer rate = 300 kb/s; t_{CYA} = 31.25 ns (32 MHz at XA1 pin); t_{CYB} = 26.04 ns (38.4 MHz at XB1 pin)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Main System Side							
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ setup time to $\overline{RD}$	4	t_{AR}	0			ns	For $\overline{ENRW}$ when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$ hold time from $\overline{RD}$	4	t_{RA}	0			ns	
$\overline{RD}$ pulse width	4	t_{RR}	200			ns	
Data access time from $\overline{RD}$ ↓	4	t_{RD}			140	ns	
Data float delay time from $\overline{RD}$ ↑	4	t_{DF}	10		85	ns	
INT delay time from $\overline{RD}$ ↑	4	t_{RI}			400	ns	Note 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL setup time to $\overline{WR}$	5	t_{AW}	0			ns	For $\overline{ENRW}$ and RSEL when MSEL = 1
A0, $\overline{CS}$, $\overline{DMAAK}$, $\overline{ENRW}$, RSEL hold time from $\overline{WR}$	5	t_{WA}	0			ns	
$\overline{WR}$ pulse width	5	t_{WW}	200			ns	
Data setup time to $\overline{WR}$	5	t_{DW}	100			ns	
Data hold time from $\overline{WR}$	5	t_{WD}	0			ns	
INT delay time from $\overline{WR}$ ↑	5	t_{WI}			400	ns	Note 1
DMARQ cycle time	6	t_{MCY}	21.7			μs	t_{CYB} = 26.04 ns
$\overline{DMAAK}$ ↓ response time from DMARQ ↑	6	t_{MA}	333.3			ns	
DMARQ delay time from $\overline{DMAAK}$ ↓	6	t_{AM}			140	ns	
$\overline{DMAAK}$ pulse width	6	t_{AA}	16.6			t_{CYB}	
$\overline{RD}$ ↓ response time from DMARQ ↑	6	t_{MR}	208.3			ns	t_{CYB} = 26.04 ns
$\overline{WR}$ ↓ response time from DMARQ ↑	6	t_{MW}	416.7			ns	
$\overline{WR}$/$\overline{RD}$ response time from DMARQ ↑	6	t_{MRW}			24	μs	
TC pulse width	6	t_{TC}	60			ns	
RESET pulse width for crystal resonator connection	7	t_{RST}	60			t_{CYA}	During normal operation
			10			ms	On power-on
			10			ms	After standby release
RESET pulse width for external clock input	7	t_{RST}	60			t_{CYA}	During normal operation
			2			ms	On power-on
			60			t_{CYA}	After standby release
Clock hold time on standby	8	t_{WC}	256			t_{CYB}	When external clock is input to XB1 pin
Clock setup time after standby release	8	t_{CW}	128			t_{CYB}	
START CLOCK command write setup time to RESET STANDBY command write	8	t_{WS}	128			t_{CYB}	
INT response time from DMARQ ↓	9	t_{MI}	480		616	t_{CYB}	
$\overline{DMAAK}$ signal invalid from INT ↑	9	t_{IA}			8	t_{CYB}	

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AC Characteristics 6; 300 kb/s (cont)

Parameter	Figure	Symbol	Min	Typ	Max	Unit	Conditions
Drive Side							
RDATA high-level width	10	t_{RDD}	40			ns	
WDATA high-level width	10	t_{WDD}		416.7		ns	
DS0-DS3 setup time to DIR (Note 4)	11	t_{DSD}	20			μs	t_{CYB} = 26.04 ns; Note 2
DIR setup time to STEP	11	t_{DST}	1.7			μs	
DS0-DS3 hold time from STEP (Note 4)	11	t_{STU}	8.3			μs	
STEP high-level width	11	t_{STP}	10	11.7	13.3	μs	
DS0-DS3 hold time from DIR (Notes 3, 4)	11	t_{DDS}	25			μs	
DIR hold time from STEP	11	t_{STD}	40			μs	
STEP cycle time	11	t_{SC}	55			μs	
FLTR high-level width	12	t_{FR}	13.3		16.7	μs	
INDEX high-level width	12	t_{IDX}	32			t_{CYB}	

Notes:

(1) For data transfer in non-DMA mode.

(2) The minimum value for drive-side parameters is 50 ns less than the value expressed in μs. For example, 20 μs is actually 19.950 μs.

(3) While the unit under test is performing a seek operation, the SENSE DEVICE STATUS command is being executed for the other devices.

(4) Except in register mode.

(5) See figure 3 for timing measurement voltage thresholds.

Figure 4. Read Operation

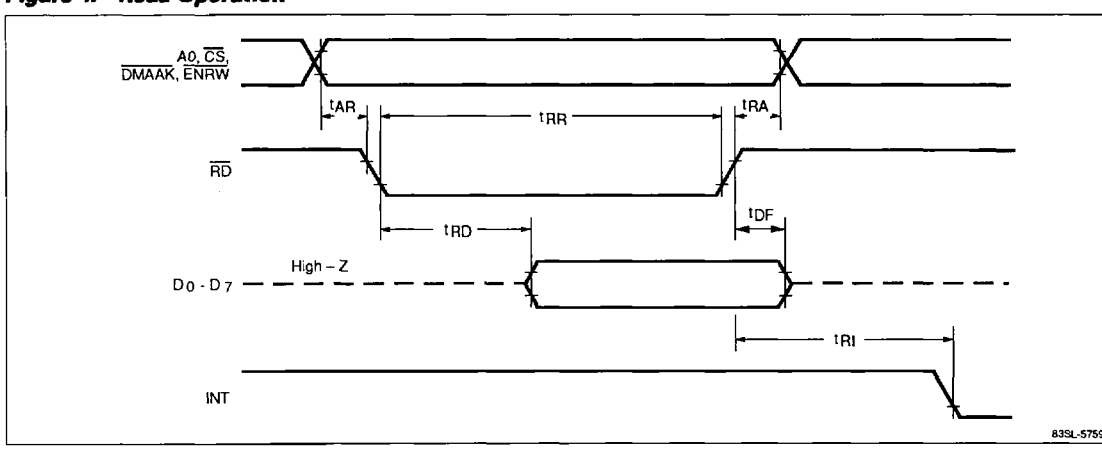

Figure 5. Write Operation

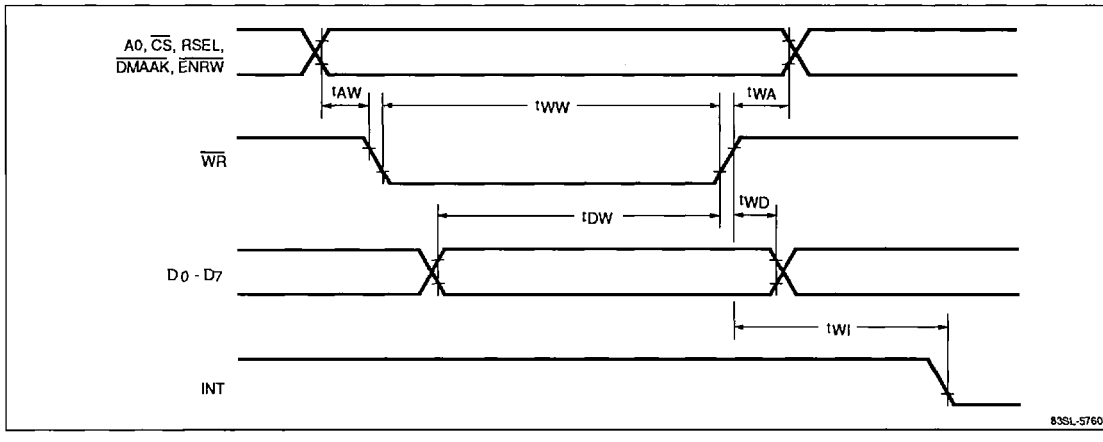

Figure. 6 DMA Operation

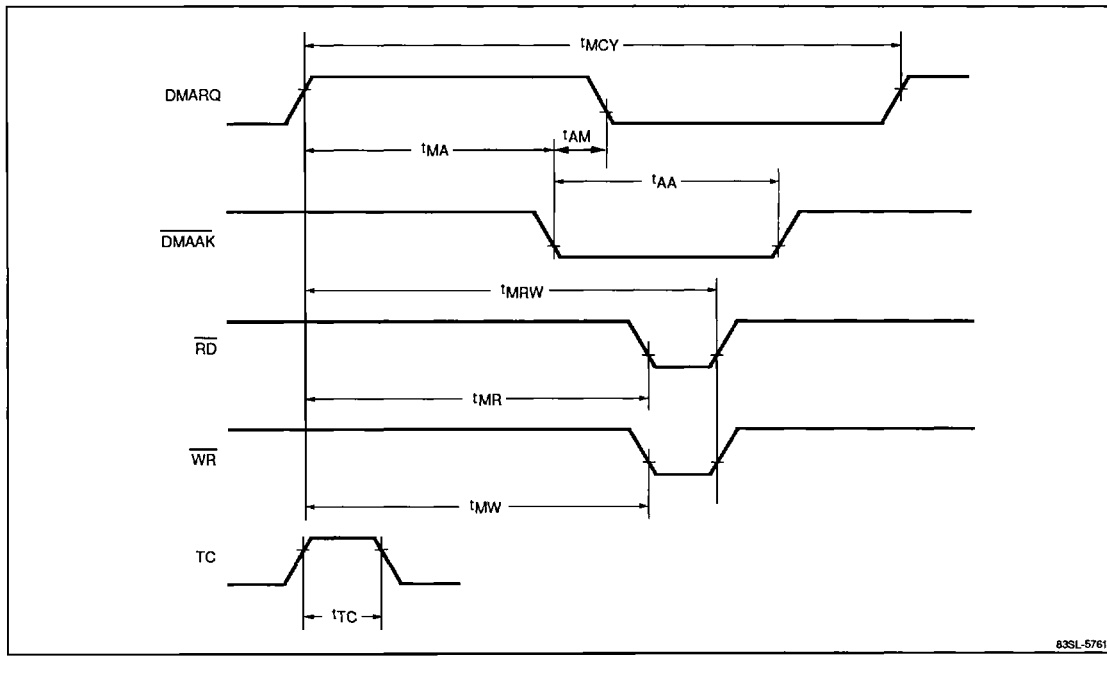

Figure 7. RESET Waveform

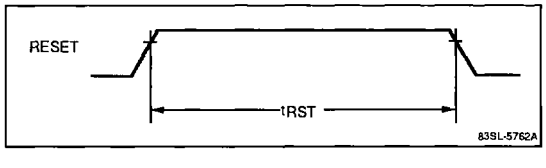

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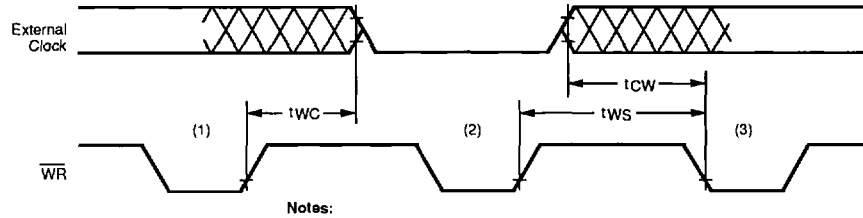
Figure 8. Standby Operation (With External Clock Input)



Notes:

(1) SET STANDBY command write.

(2) START CLOCK command write.

(3) RESET STANDBY command write.

(4) When in standby mode the external clock should be fixed low. The standby current specifications cannot be met unless this is done.

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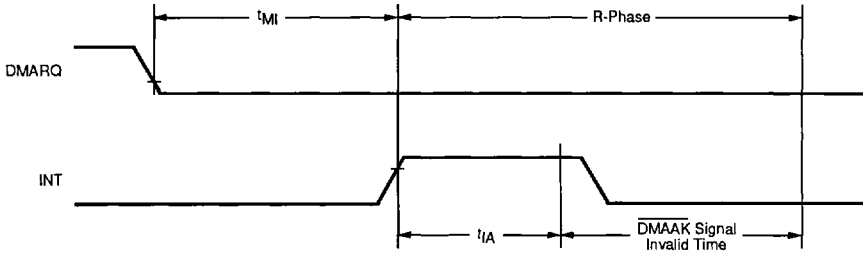
Figure. 9 Operation in Case of Overrun



INT generation on completion of command

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Figure 10. RDATA and WDATA Waveforms

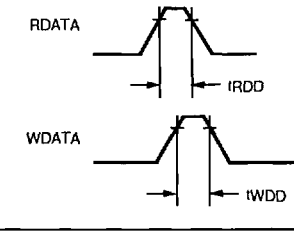

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Figure 11. Seek Operattion

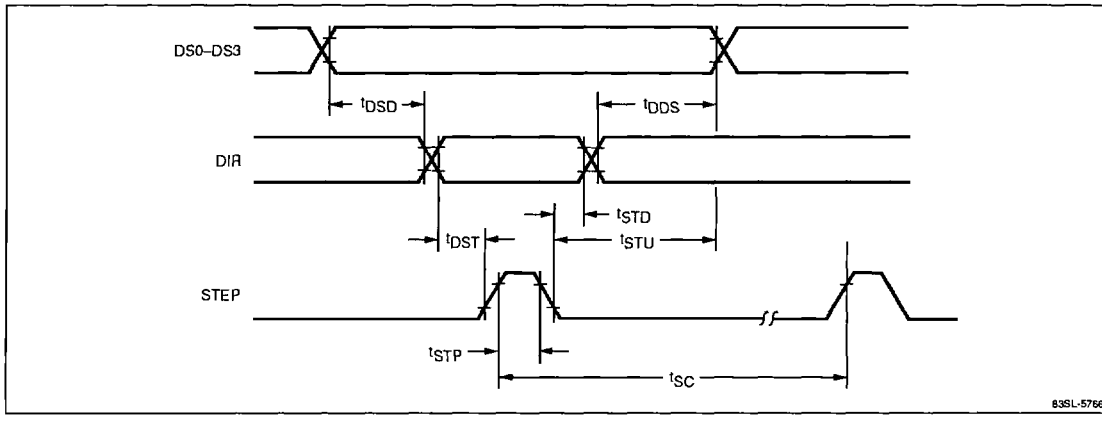
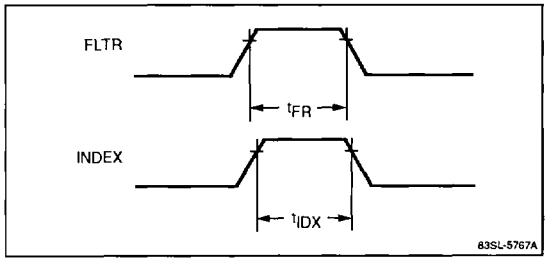


Figure 12. FLTR and INDEX Waveforms



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