2164A FAMILY
65,536 x 1 BIT DYNAMIC RAM

	2164A-15	2164A-20
Maximum Access Time (ns)	150	200
Read, Write Cycle (ns)	260	330
Page Mode Read, Write Cycle (ns)	125	170

- **HMOS-D III technology**
- **Low capacitance, fully TTL compatible inputs and outputs**
- **Single +5V supply, ±10% tolerance**
- **128 refresh cycle/2 ms $\overline{RAS}$ only refresh**
- **Compatible with the 2118**
- **Extended page mode, read-modify-write and hidden refresh operation**
- **Inputs allow a −2.0V negative overshoot**
- **Industry standard 16-pin DIP**
- **Compatible with Intel's microprocessors and DRAM controllers**

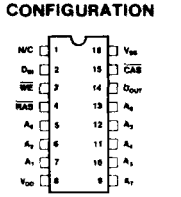
The 2164A is a 65,536 word by 1-bit N-channel MOS dynamic Random Access Memory fabricated with Intel's HMOS-D III technology for high system performance and reliability. The 2164A design incorporates high storage cell capacitance to provide wide internal device margins for reduced noise sensitivities and more reliable system operation. Moreover, high storage cell capacitance results in low soft error rates without the need for a die coat. HMOS-D III process employs the use of redundant elements.

The 2164A is optimized for high speed, high performance applications such as mainframe memory, buffer memory, microprocessor memory, peripheral storage and graphic terminals. For memory intensive microprocessor applications the 2164A is fully compatible with Intel's DRAM controllers and microprocessors to provide a complete DRAM system.

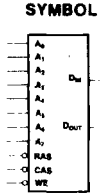
Multiplexing the 16 address bits into the 8 address input pins allows the 2164A to achieve high packing density. The 16 pin DIP provides for high system bit densities, and is compatible with widely available automated testing and insertion equipment. The two 8-bit TTL level address segments are latched into the 2164A by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical timing requirements for the $\overline{RAS}$ and $\overline{CAS}$ clocks allow the use of the address multiplexing technique while maintaining high performance.

The non-latched, three state, TTL compatible data output is controlled by $\overline{CAS}$, independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the data output pin by holding $\overline{CAS}$ low. The data output is returned to a high impedance state, by returning $\overline{CAS}$ to a high state. Hidden refresh capability allows the device to maintain data at the output by holding $\overline{CAS}$ low while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles. Refreshing is accomplished by performing $\overline{RAS}$-only cycles, hidden refresh cycles, or normal read or write cycles on the 128 address combinations of addresses A_0 through A_6, during a 2 ms period.

PIN CONFIGURATION

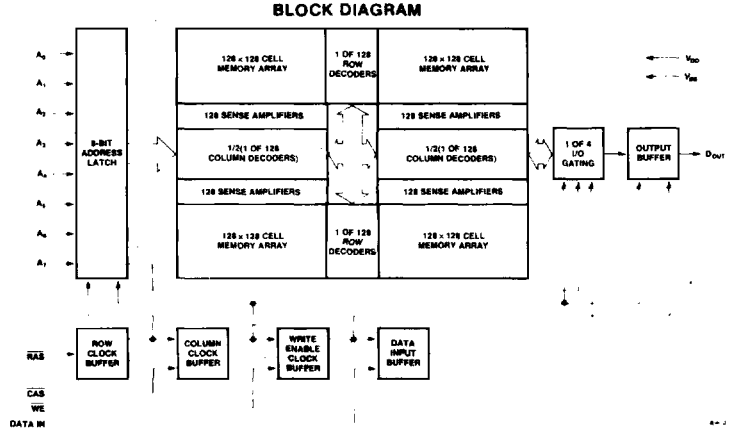


LOGIC SYMBOL



A_0-A_7	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE
$\overline{RAS}$	ROW ADDRESS STROBE
V_{DD}	POWER (+5V)
V_{SS}	GROUND

BLOCK DIAGRAM



April 1982
Order Number: 210425-001

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature.. Cerdip −65°C to +150°C
Plastic −55°C to +125°C
Voltage on Any Pin except V_{DD}
Relative to V_{SS} ..... −2.0V to 7.5V
Voltage on V_{DD} Relative to V_{SS} .... −1.0V to 7.5V
Data Out Current ..... 50 mA
Power Dissipation ..... 1.0 W

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS[1]

$T_A = 0°C$ to $70°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Limits Min.	Typ.[2]	Max.	Unit	Test Conditions	Notes
$\|I_{LI}\|$	Input Load Current (any input)			10	µA	$V_{IN} = V_{SS}$ to V_{DD}	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State			10	µA	Chip Deselected: $\overline{CAS}$ at V_{IH}, D_{OUT} = 0 to 5.5V	
I_{DD1}	V_{DD} Supply Current, Standby		3	5	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}	
I_{DD2}	V_{DD} Supply Current, Operating		42	55	mA	2164A-15, $t_{RC} = t_{RCMIN}$	3
			33	45	mA	2164A-20, $t_{RC} = t_{RCMIN}$	3
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Cycle		30	45	mA	2164A-15, $t_{RC} = t_{RCMIN}$	
			24	40	mA	2164A-20, $t_{RC} = t_{RCMIN}$	
I_{DD5}	V_{DD} Supply Current, Standby Output Enabled			6	mA	$\overline{CAS}$ at V_{IL}, $\overline{RAS}$ at V_{IH}	3
V_{IL}	Input Low Voltage (all inputs)	−1.0		0.8	V		4
V_{IH}	Input High Voltage (all inputs)	2.4		7.0	V		
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2 mA	5
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −5 mA	5

NOTES:
1. All voltages referenced to V_{SS}.
2. Typical values are for $T_A = 25°C$ and nominal supply voltages.
3. I_{DD} is dependent on output loading when the device output is selected. Specified $I_{DD\,MAX}$ is measured with the output open.
4. Specified $V_{IL\,MIN}$ is for steady state operation. During transitions the inputs may overshoot to −2.0V for periods not to exceed 20 ns.
5. Test conditions apply only for D.C. characteristics. A.C. parameters specified with a load equivalent to 2 TTL loads and 100 pF.

CAPACITANCE[1]

$T_A = 25°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Typ.	Max.	Unit
C_{11}	Address, Data In	3	5	pF
C_{12}	$\overline{WE}$, Data Out	3	6	pF
C_{13}	$\overline{RAS}$, $\overline{CAS}$	4	8	pF

NOTES:
1. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:

$$C = \frac{I\Delta t}{\Delta V}$$

with ΔV equal to 3 volts and power supplies at nominal levels.

A.C. CHARACTERISTICS[1,2,3]

$T_A = 0°C$ to $70°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

Symbol	Parameter	2164A-15 Min.	2164A-15 Max.	2164A-20 Min.	2164A-20 Max.	Unit	Notes
t_{RAC}	Access Time From $\overline{RAS}$		150		200	ns	4,5
t_{CAC}	Access Time From $\overline{CAS}$		85		120	ns	5,6
t_{REF}	Time Between Refresh		2		2	ms	
t_{RP}	$\overline{RAS}$ Precharge Time	100		120		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time (non-page cycles)	25		35		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	−20		−20		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	30	65	35	80	ns	7
t_{RSH}	$\overline{RAS}$ Hold Time	85		120		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	150		200		ns	
t_{ASR}	Row Address Set-Up Time	0		0		ns	
t_{RAH}	Row Address Hold Time	20		25		ns	
t_{ASC}	Column Address Set-Up Time	0		0		ns	
t_{CAH}	Column Address Hold Time	25		30		ns	
t_{AR}	Column Address Hold Time to $\overline{RAS}$	90		110		ns	
t_T	Transition time (Rise and Fall)	3	50	3	50	ns	8
t_{OFF}	Output Buffer Turn Off Delay	0	30	0	40	ns	

READ AND REFRESH CYCLES

t_{RC}	Random Read Cycle Time	260		330		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10000	200	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	85	10000	120	10000	ns	
t_{RCS}	Read Command Set-Up Time	0		0		ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CAS}$	5		5		ns	9
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	20		20		ns	9

NOTES:

1. All voltages referenced to V_{SS}.
2. An initial pause of 500 μs is required after power up followed by a minimum of eight (8) initialization cycles (any combination of cycles containing a RAS clock such as RAS-only refresh). 8 initialization cycles are required after extended periods of bias (greater than 2 ms) without clocks.
3. A.C. Characteristics assume $t_T = 5$ ns.
4. Assumes that $t_{RCD} \leq t_{RCD}(max)$. If t_{RCD} is greater than $t_{RCD}(max)$ then t_{RAC} will increase by the amount that t_{RCD} exceeds $t_{RCD}(max)$.
5. Load = 2 TTL loads and 100 pF.
6. Assumes $t_{RCD} \geq t_{RCD}(max)$.
7. $t_{RCD}(max)$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD}(max)$ access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD}(max)$ access time is $t_{RCD} + t_{CAC}$. $t_{RCD}(min) = t_{RAH} + t_{ASC} + t_T + t_T$ ($t_T = 5$ ns).
8. t_T is measured between $V_{IH}(min)$ and $V_{IL}(max)$.
9. Either t_{RCH} or t_{RRH} must be satisfied.

A.C. CHARACTERISTICS (con't.)

WRITE CYCLE

Symbol	Parameter	2164A-15 Min.	2164A-15 Max.	2164A-20 Min.	2164A-20 Max.	Unit	Notes
t_{RC}	Random Write Cycle Time	260		330		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10000	200	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	85	10000	120	10000	ns	
t_{WCS}	Write Command Set-Up Time	−10		−10		ns	10
t_{WCH}	Write Command Hold Time	30		40		ns	
t_{WCR}	Write Command Hold Time to $\overline{RAS}$	95		120		ns	
t_{WP}	Write Command Pulse Width	30		40		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	40		50		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	40		50		ns	
t_{DS}	Data-In Set-Up Time	0		0		ns	
t_{DH}	Data-In Hold Time	30		40		ns	
t_{DHR}	Data-In Hold Time to $\overline{RAS}$	95		120		ns	

READ-MODIFY-WRITE CYCLE

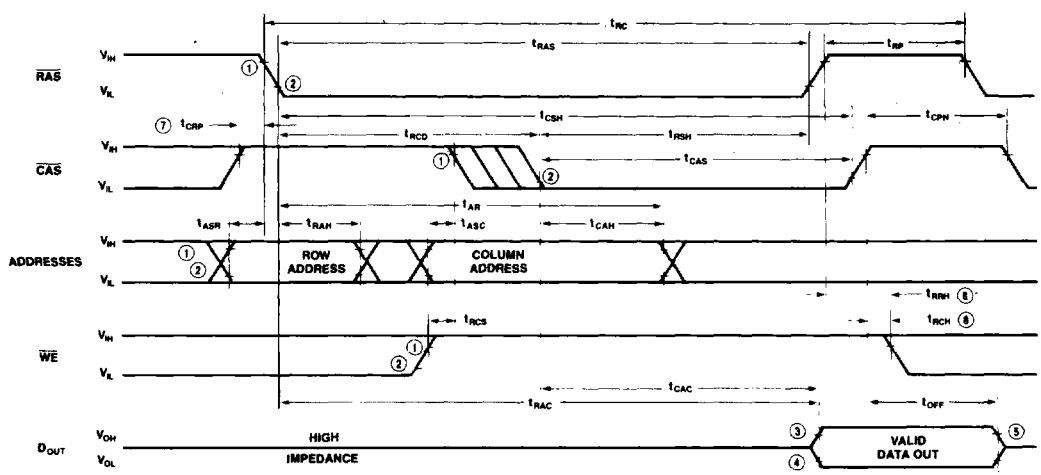
t_{RWC}	Read-Modify-Write Cycle time	280		355		ns	
t_{RRW}	RMW Cycle RAS Pulse Width	170	10000	225	10000	ns	
t_{CRW}	RMW Cycle CAS Pulse Width	105	10000	145	10000	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	125		170		ns	10
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	60		90		ns	10

NOTES:

10. t_{WCS}, t_{CWD} and t_{RWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.

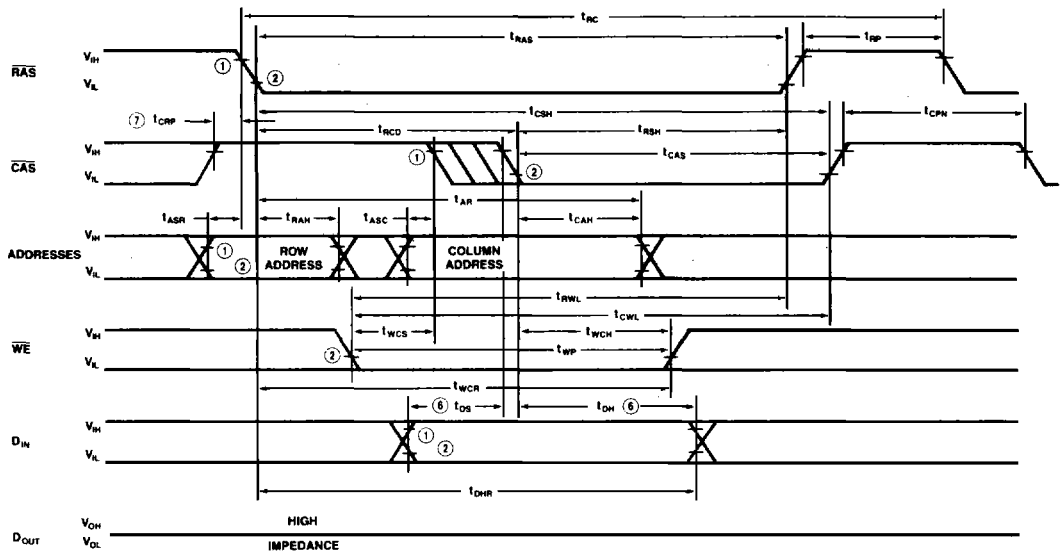
WAVEFORMS

READ CYCLE

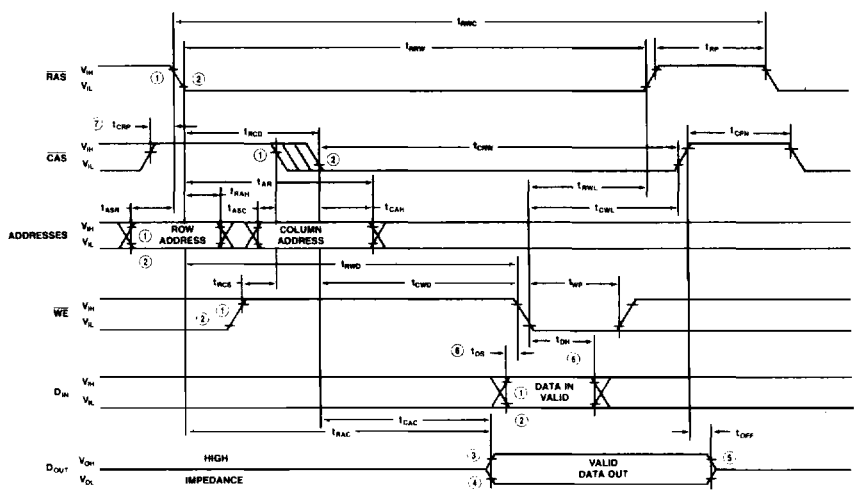


WAVEFORMS

WRITE CYCLE



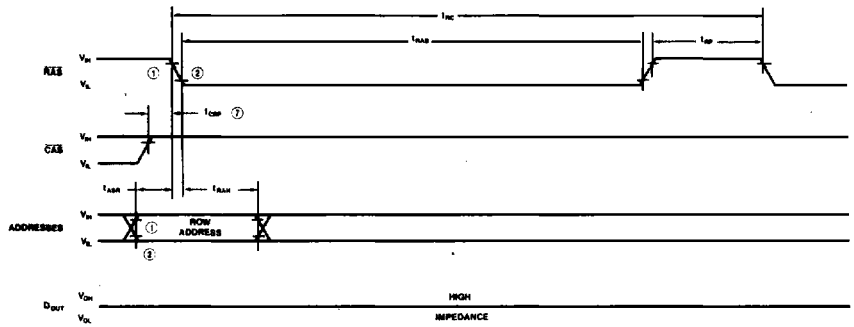
READ-MODIFY-WRITE CYCLE



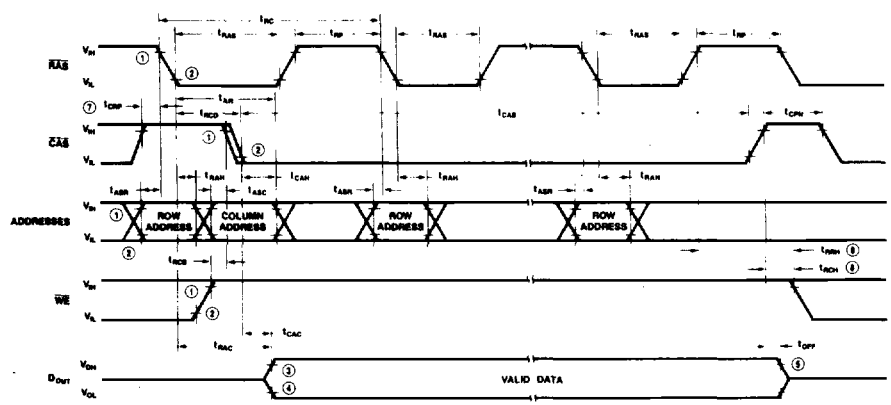
NOTES: 1,2. $V_{IH\ MIN}$ and $V_{IL\ MAX}$ are reference levels for measuring timing of input signals.
3,4. $V_{OH\ MIN}$ and $V_{OL\ MAX}$ are reference levels for measuring timing of D_{OUT}.
5. t_{OFF} is measured to $|I_{OUT}| \leq |I_{LO}|$.
6. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.
7. t_{CRP} requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a $\overline{CAS}$-only cycle (i.e., for systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).
8. Either t_{RCH} or t_{RRH} must be satisfied.

WAVEFORMS

$\overline{RAS}$-ONLY REFRESH CYCLE



HIDDEN REFRESH CYCLE



NOTES: 1,2. $V_{IH\ MIN}$ and $V_{IL\ MAX}$ are reference levels for measuring timing of input signals.
3,4. $V_{OH\ MIN}$ and $V_{OL\ MAX}$ are reference levels for measuring timing of D_{OUT}.
5. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
6. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.
7. t_{CRP} requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a $\overline{CAS}$-only cycle (i.e., for systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).
8. Either t_{RCH} or t_{RRH} must be satisfied.

D.C. AND A.C. CHARACTERISTICS, PAGE MODE [6,7,11]

$T_A = 0°C$ to $70°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

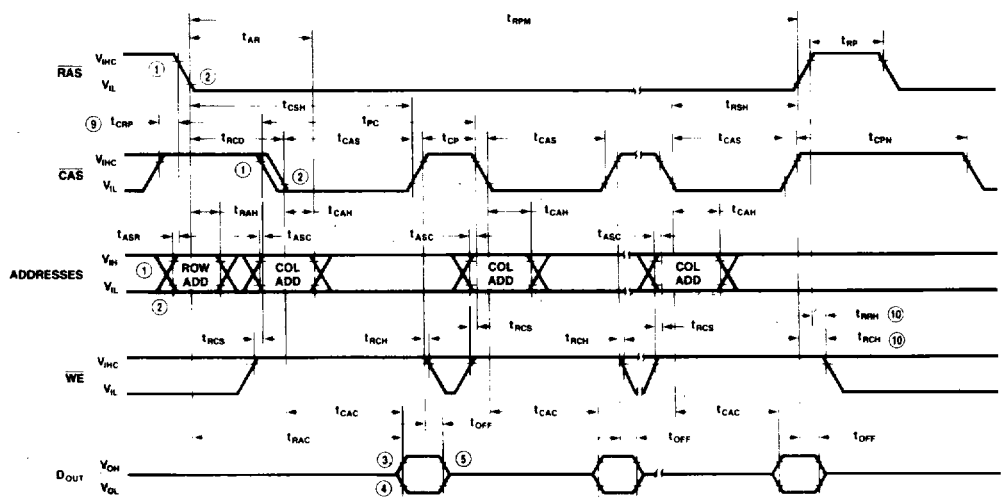
Symbol	Parameter	2164A-15 Min.	2164A-15 Max.	2164A-20 Min.	2164A-20 Max.	Unit	Notes
t_{PC}	Page Mode Read or Write Cycle	125		170		ns	
t_{PCM}	Page Mode Read Modify Write	145		195		ns	
t_{CP}	$\overline{CAS}$ Precharge Time, Page Cycle	30		40		ns	
t_{RPM1}	$\overline{RAS}$ Pulse Width, Page Mode		10000		10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	85	10000	120	10000	ns	
I_{DD4}	V_{DD} Supply Current Page Mode, Minimum t_{PC}, Minimum t_{CAS}		40		35	mA	8

EXTENDED PAGE MODE [11,12]

Symbol	Parameter	2164A-15 S6493 Min.	2164A-15 S6493 Max.	2164A-20 S6494 Min.	2164A-20 S6494 Max.	Unit	Notes
t_{RPM2}	$\overline{RAS}$ Pulse Width, Extended Page Mode		75000		75000	ns	

WAVEFORMS

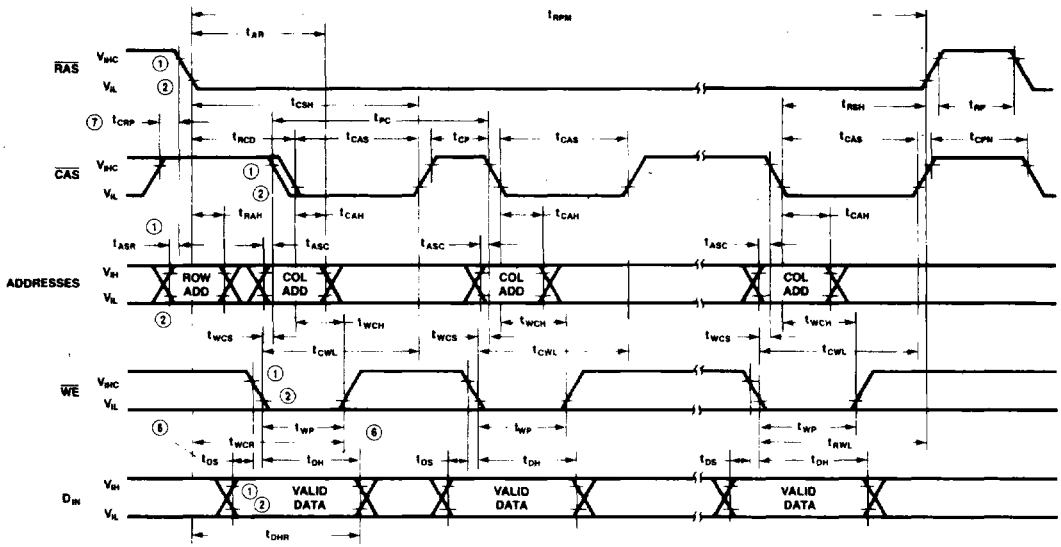
PAGE MODE READ CYCLE



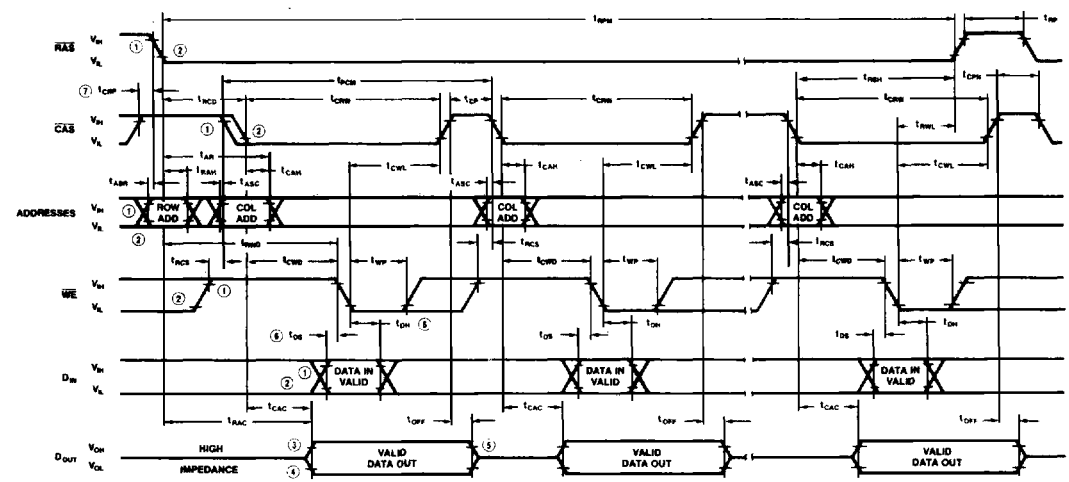
NOTES: 1,2. $V_{IH\ MIN}$ and $V_{IL\ MAX}$ are reference levels for measuring timing of input signals.
3,4. $V_{OH\ MIN}$ and $V_{OL\ MAX}$ are reference levels for measuring timing of D_{OUT}.
5. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
6. All voltages referenced to V_{SS}.
7. A.C. characteristic assume $t_T = 5$ ns.
8. See the typical characteristics section for values of this parameter under alternate conditions.
9. t_{CRP} requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a $\overline{CAS}$-only cycle (i.e., for systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).
10. Either t_{RCH} or t_{RRH} must be satisfied.
11. All previously specified A.C. and D.C. characteristics are applicable.
12. For extended page mode operation, order 2164A-15 S6493, 2164A-20 S6494.

WAVEFORMS

PAGE MODE WRITE CYCLE

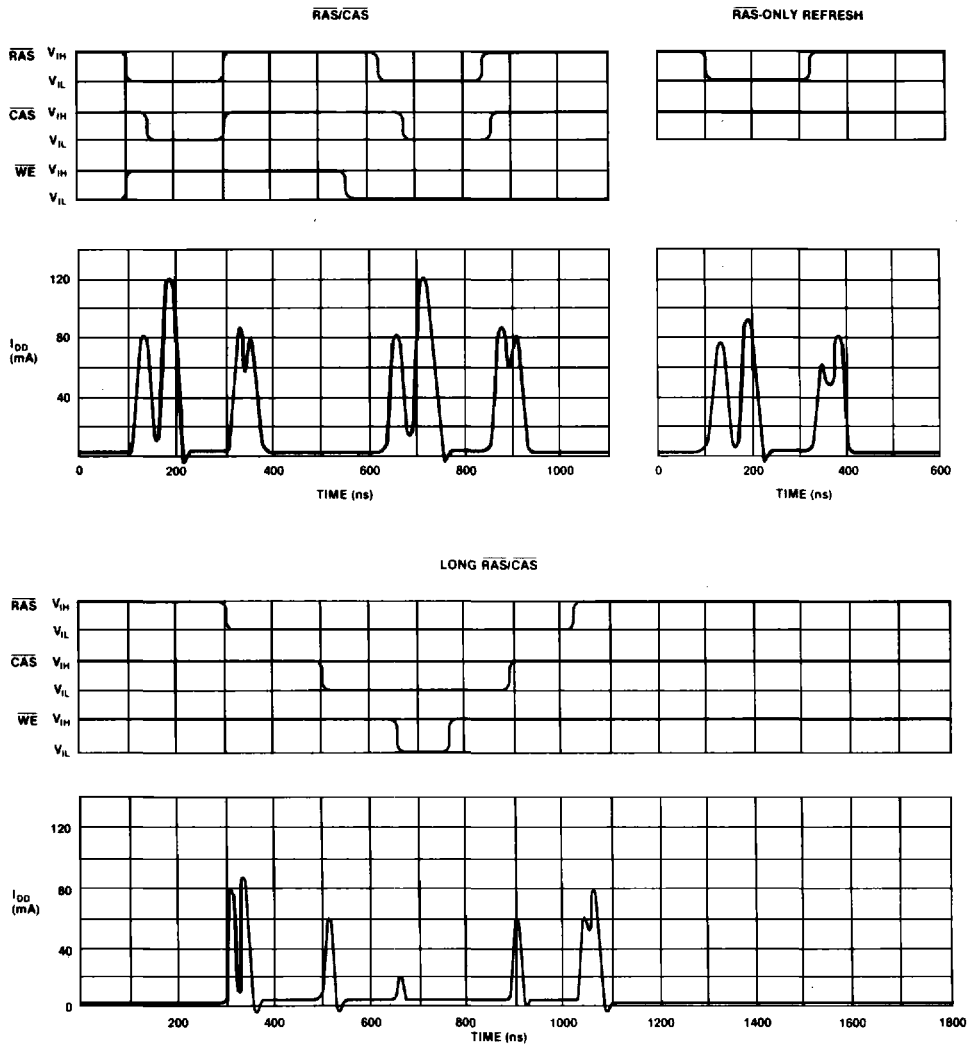


PAGE MODE READ-MODIFY-WRITE CYCLE



NOTES: 1,2. $V_{IH\ MIN}$ and $V_{IL\ MAX}$ are reference levels for measuring timing of input signals.
3,4. $V_{OH\ MIN}$ and $V_{OL\ MAX}$ are reference levels for measuring timing of D_{OUT}.
5. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
6. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.
7. t_{CRP} requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a $\overline{CAS}$-only cycle (i.e., for systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).

TYPICAL SUPPLY CURRENT WAVEFORMS

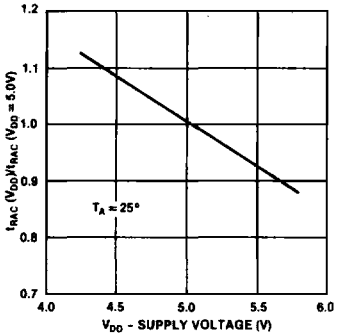


Typical power supply waveforms vs. time are shown for the $\overline{RAS}/\overline{CAS}$ timings of Read/Write, Read/Write (long $\overline{RAS}/\overline{CAS}$), and $\overline{RAS}$-only refresh cycles. I_{DD} current transients at the $\overline{RAS}$ and $\overline{CAS}$ edges require adequate decoupling of these supplies.

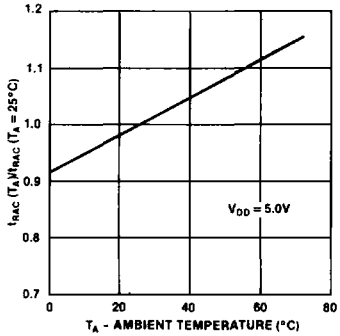
The effects of cycle time, V_{DD} supply voltage and ambient temperature on the I_{DD} current are shown in graphs included in the Typical Characteristics Section. Each family of curves for I_{DD1}, I_{DD2}, and I_{DD3} is related by a common point at $V_{DD} = 5.0V$ and $T_A = 25°C$ for $t_{RAS} = 150$ ns and $t_{RC} = 260$ ns. The typical I_{DD} current for a given condition of cycle time, V_{DD} and T_A, can be determined by combining the effects of the appropriate family of curves.

TYPICAL CHARACTERISTICS

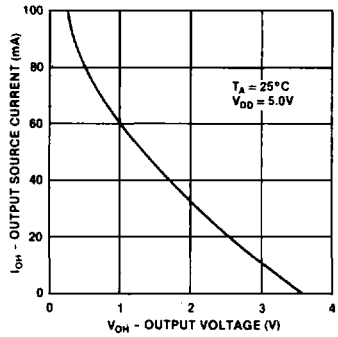
GRAPH 1
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) vs. V_{DD}



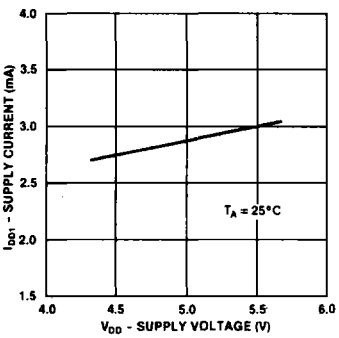
GRAPH 2
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) vs.
AMBIENT TEMPERATURE



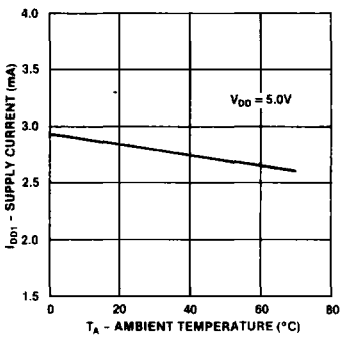
GRAPH 3
TYPICAL OUTPUT
SOURCE CURRENT
I_{OH} vs. OUTPUT VOLTAGE V_{OH}



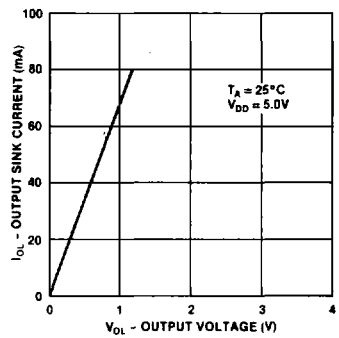
GRAPH 4
TYPICAL STANDBY CURRENT
I_{DD1} vs. V_{DD}



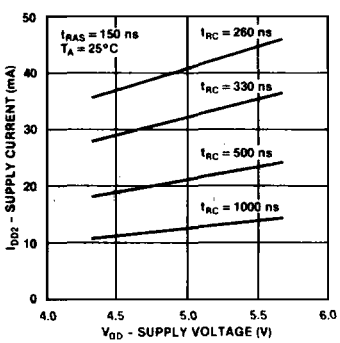
GRAPH 5
TYPICAL STANDBY CURRENT
I_{DD1} vs. AMBIENT TEMPERATURE



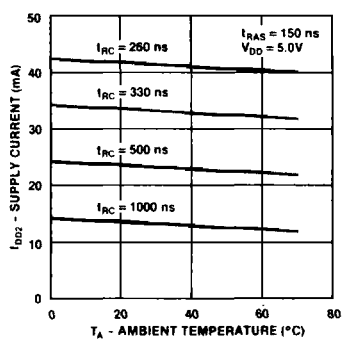
GRAPH 6
TYPICAL OUTPUT
SINK CURRENT
I_{OL} vs. OUTPUT VOLTAGE V_{OL}



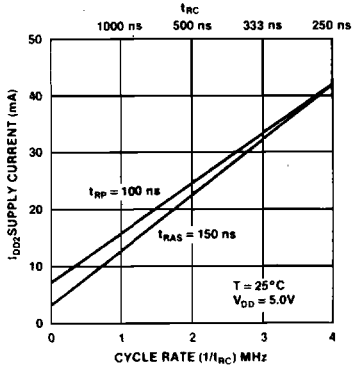
GRAPH 7
TYPICAL OPERATING CURRENT
I_{DD2} vs. V_{DD}



GRAPH 8
TYPICAL OPERATING CURRENT
I_{DD2} vs. AMBIENT TEMPERATURE

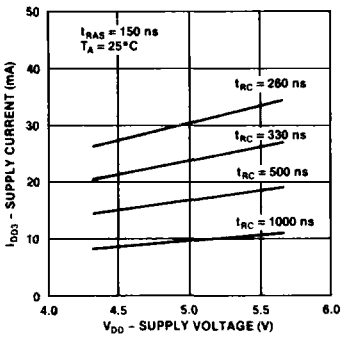


GRAPH 9
TYPICAL OPERATING CURRENT
I_{DD2} vs. 1/t_{RC}

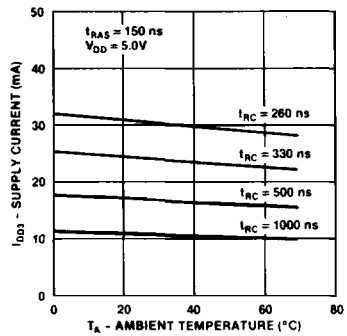


TYPICAL CHARACTERISTICS

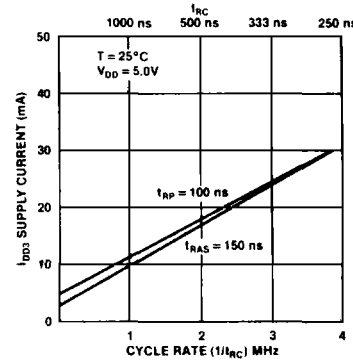
GRAPH 10
TYPICAL $\overline{RAS}$-ONLY
REFRESH CURRENT
I_{DD3} vs. V_{DD}



GRAPH 11
TYPICAL $\overline{RAS}$-ONLY
REFRESH CURRENT
I_{DD3} vs. AMBIENT TEMPERATURE



GRAPH 12
TYPICAL $\overline{RAS}$-ONLY
REFRESH CURRENT
I_{DD3} vs. $1/t_{RC}$



DEVICE DESCRIPTION

The Intel 2164A is produced with HMOS-D III, a high performance MOS technology which incorporates redundant elements. This process, combined with new circuit design concepts, allows the 2164A to operate from a single + 5V power supply, eliminating the + 12V and − 5V requirements. Pin 1 is not connected, which allows P.C.B. layout for future higher density memory generations.

The 2164A is functionally compatible with the 2118, the industry standard 5V-only 16-pin 16K dynamic RAM. This allows simple upgrade from 16K to 64K density merely by adding one additional multiplexed address line.

RAS/CAS Timing

$\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths as defined by t_{RAS} and t_{CAS} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle, once begun by bringing $\overline{RAS}$ and/or $\overline{CAS}$ low, must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle can not begin until the minimum precharge time, t_{RP}, has been met.

Read Cycle

A Read cycle is performed by maintaining Write Enable ($\overline{WE}$) high during a $\overline{RAS}$/$\overline{CAS}$ operation. The output pin of a selected device will remain in a high impedance state until valid data appears at the output at access time.

Write Cycle

A Write cycle is performed by taking $\overline{WE}$ low during a $\overline{RAS}$/$\overline{CAS}$ operation. Data Input (D_{IN} must be valid relative to the negative edge of $\overline{WE}$ or $\overline{CAS}$, whichever transition occurs last.

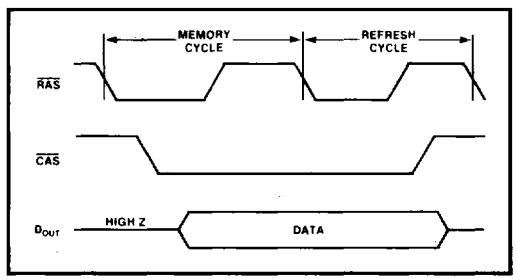
Refresh Cycles

There are 512 sense amplifiers, each controlling 128 storage cells. Thus, the 2164A is refreshed in 128 cycles. Any combination of the seven (7) low order Row Addresses RA_0 through RA_6, will select two rows of data cells (256 cells/row). Row address 7 is not critical during a refresh operation and can be either high or low. Although any cycle, Read, Write, Read-Modify-Write, or $\overline{RAS}$-only, will refresh the memory, the $\overline{RAS}$-only cycle is recommended, since it allows about 20% system power reduction over the other types of cycles.

Hidden Refresh

A standard feature of the 2164A is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and, after a specified precharge period (t_{RP}), executing a

"$\overline{RAS}$-Only" refresh cycle, but with $\overline{CAS}$ held low (see figure below).



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability. The part will be internally refreshed at the row addressed at the time of the second $\overline{RAS}$.

Data Output Operation

The 2164A Data Output (D_{OUT}), which has three-state capability, is controlled by $\overline{CAS}$. During $\overline{CAS}$ high state ($\overline{CAS}$ at V_{IH}), the output is in the high impedance state. The following table summarizes the D_{OUT} state for various types of cycles.

Intel® 2164A Data Output Operation for Various Types of Cycles

Type of Cycle	D_{OUT} State
Read Cycle	Data from Addressed Memory Cell
Early Write Cycle	Hi-Z
$\overline{RAS}$-Only Refresh Cycle	Hi-Z
$\overline{CAS}$-Only Cycle	Hi-Z
Read-Modify-Write Cycle	Data from Addressed Memory Cell
Delayed Write Cycle	Indeterminate

Power On

An initial pause of 500 μs is required after the application of the V_{DD} supply, followed by a minimum of eight (8) initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). 8 initialization cycles are required after extended periods of bias (greater than 2 ms) without clocks. The V_{DD} current (I_{DD}) requirement of the 2164A during power on, is however, dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$ and the rise time of V_{DD} shown in Figure 1.

If $\overline{RAS} = V_{SS}$ during power on, the device may go into an active cycle and I_{DD} would show spikes similar to those shown for the $\overline{RAS}/\overline{CAS}$ timings. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} during power on or be held at a valid V_{IH}.

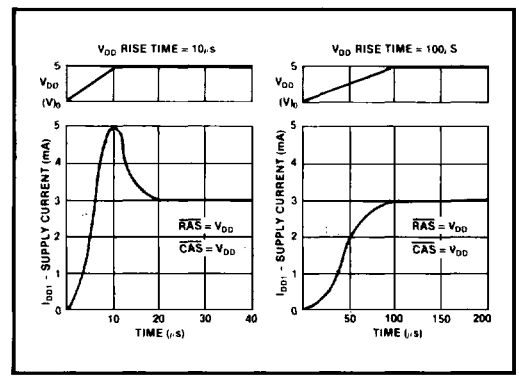


Figure 1. Typical I_{DD} vs. V_{DD} During Power Up

Page Mode Operation

Page Mode operation allows additional columns of the selected device to be accessed at the common row address set. This is done by maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are performed.

Page Mode operation allows a maximum data transfer rate as Row addresses are maintained internally and do not have to be reapplied. During this operation, Read, Write and Read-Modify-Write cycles are possible. Following the entry cycle into Page Mode operation, access is t_{CAC} dependent. The Page Mode cycle is dependent upon $\overline{CAS}$ pulse width (t_{CAS}) and the $\overline{CAS}$ precharge period (t_{CP}).

Extended Page Mode Operation

An optional feature of the 2164A is extended page mode operation which allows an entire page (row) of data to be read or written during a single $\overline{RAS}$ cycle. By providing a fast t_{PC} and long $\overline{RAS}$ pulse width (t_{RPM2}), the 2164A-15 S6493 permits transfers of large blocks of data, such as required by bit-mapped graphic applications.

SYSTEM DESIGN CONSIDERATIONS

Ground and Power Gridding

Ground and power gridding can contribute to excess noise and voltage drops. An example of an unacceptable method is presented in Figure 2. This type of layout results in accumulated transient noise and voltage drops for the device located at the end of each trace (path).

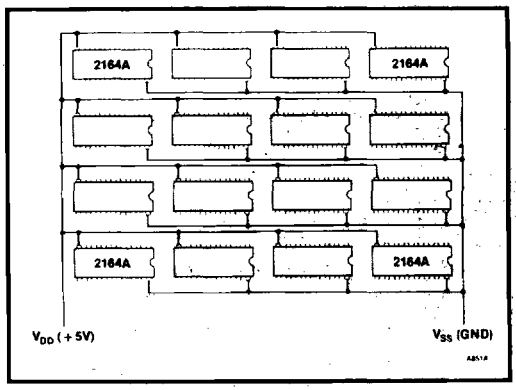


Figure 2. Unacceptable Power Distribution

Transient effects can be minimized by adding extra circuit board traces in parallel to reduce interconnection inductance (Figure 3).

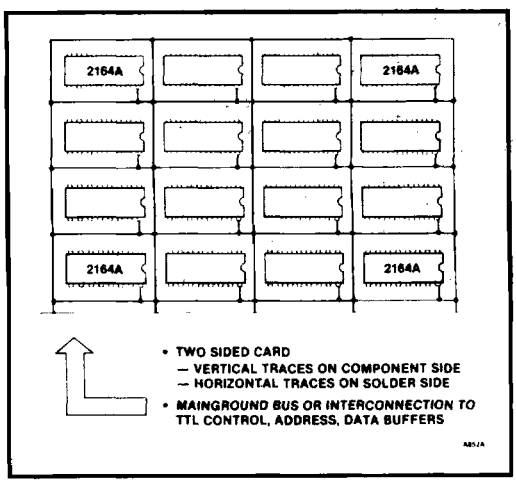


Figure 3. Recommended Power Distribution — Gridding

Power and Ground Plane

A better alternative to power and gridding is power and ground planes. Although this requires two additional inner layers to the PC board, noise and supply voltage fluctuations are greatly reduced. If power and ground planes are used, gridding is optional but typically used for increased reliability of power and ground connections and further reduction of electromagnetic noise.

It is preferable on power/ground planes to use circular voids for device pins rather than slotted voids (Figure 4). This provides maximum decoupling and minimum crosstalk between signal traces.

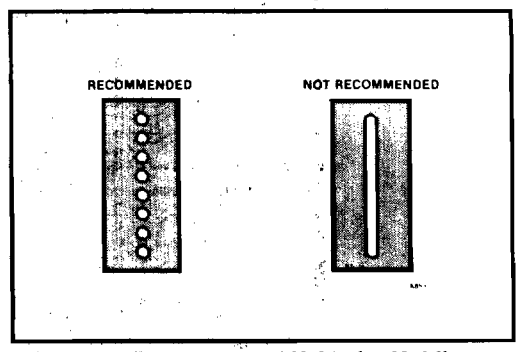


Figure 4. Recommended Voids for Multilayer PC Boards

Power Supply Decoupling

For best results, decoupling capacitors are placed on the memory array board at each memory location (Figure 5). High frequency 0.1 μF ceramic capacitors are the recommended type. Noise is minimized because of the low impedance across the circuit board traces. Typical V_{DD} noise levels for this arrangement are less than 300 mV.

A large tantalum capacitor (typically one 100 μF per 64 devices) is required at the circuit board edge connector power input pins to recharge the 0.1 μF capacitors between memory cycles.

For further details see application note (A.N.) #131, 2164A Dynamic RAM Device Description, or A.N. #133, Designing Memory Systems for Microprocessor Using the Intel 2164A and 2118 Dynamic RAMs.

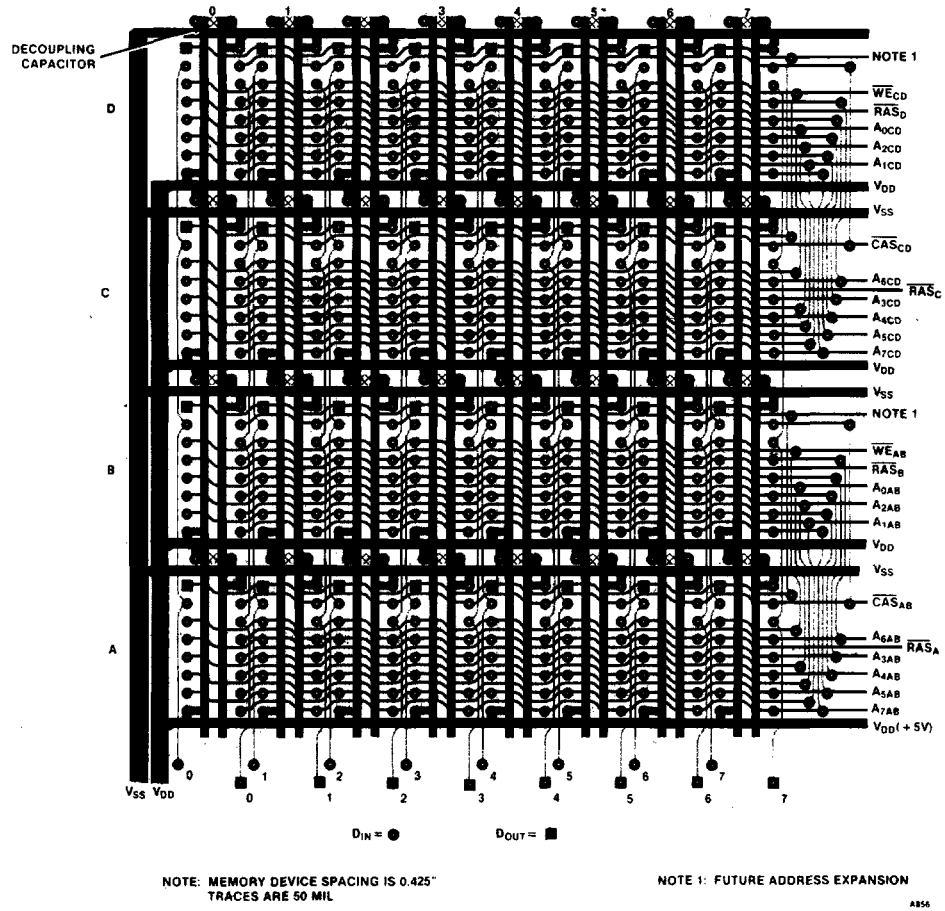


Figure 5. 2164A Memory Array PC Board Layout