LMH6553

LMH6553 900 MHz Fully Differential Amplifier With Output Limiting Clamp

Literature Number: SNOSB07G

National Semiconductor

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LMH6553

900 MHz Fully Differential Amplifier With Output Limiting Clamp

General Description

The LMH6553 is a 900 MHz differential amplifier with an integrated adjustable output limiting clamp. The clamp increases system performance and provides transient over-voltage protection to following stages. The internal clamp feature of the LMH6553 reduces or eliminates the need for external discrete overload protection networks. When used to drive ADCs, the amplifier's output clamp allows low voltage ADC inputs to be protected from being overdriven and damaged by large input signals appearing at the system input. Fast overdrive recovery of 600 ps ensures the amplifier output rapidly recovers from a clamping event and quickly resumes to follow the input signal. The LMH6553 delivers exceptional bandwidth, distortion, and noise performance ideal for driving ADCs up to 14-bits. The LMH6553 could also be used for automotive, communication, medical, test and measurement, video, and LIDAR applications.

With external gain set resistors and integrated common mode feedback, the LMH6553 can be configured as either a differential input to differential output or single ended input to differential output gain block. The LMH6553 can be AC or DC coupled at the input which makes it suitable for a wide range of applications including communication systems and high speed oscilloscope front ends. The LMH6553 is available in 8-pin PSOP and 8-pin LLP packages, and is part of our LMH® high speed amplifier family.

Features

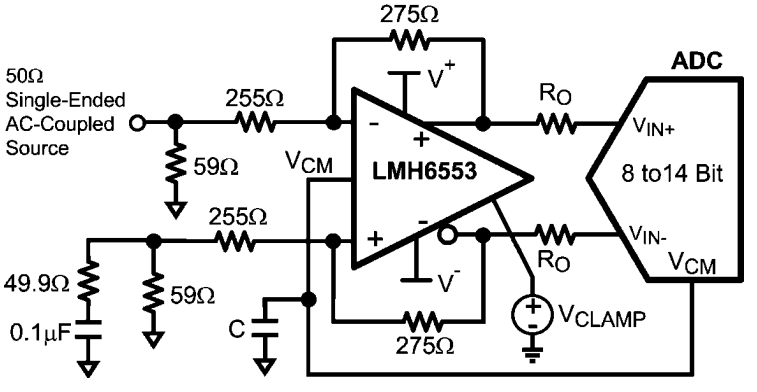
- 900 MHz –3 dB small signal bandwidth @ A_V = 1
- 670 MHz –3 dB large signal bandwidth @ A_V = 1
- –79 dB THD @ 20 MHz
- –92 dB IMD3 @ f_c = 20 MHz
- 10 ns settling time to 0.1%
- 600 ps clamp overdrive recovery time
- 40 mV clamp accuracy with 100% Overdrive
- –0.1 mV/°C clamp temperature drift
- 4.5 to 12 supply voltage operation

Applications

- Differential ADC driver
- Video over twisted pair
- Differential line driver
- Single end to differential converter
- High speed differential signaling
- IF/RF amplifier
- SAW filter buffer/driver
- CCD Output Limiting Amplifier
- Automotive Safety Applications

Typical Application

Single-Ended Input Differential Output ADC Driver



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 5)	
Human Body Model	4000V
Machine Model	350V
Supply Voltage	13.2V
Common Mode Input Voltage	$\pm V_S$
Maximum Input Current (pins 1, 2, 7, 8)	30 mA
Maximum Output Current (pins 4, 5)	(Note 4)
Maximum Junction Temperature	150°C

For soldering specifications
see product folder at www.national.com and
www.national.com/ms/MS/MS-SOLDERING.pdf

Operating Ratings (Note 1)

Operating Temperature Range (Note 3)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Total Supply Voltage	4.5V to 12V
Package Thermal Resistance (θ_{JA})	
8-Pin PSOP	59°C/W
8-Pin LLP	58°C/W

V_S = ±5V Electrical Characteristics (Note 2)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V_S = ±5V, A_V = 1, V_{CM} = 0V, V_{CLAMP} = 3V, R_F = R_G = 275Ω, R_L = 200Ω, for single-ended in, differential out. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
AC Performance (Differential)						
SSBW	Small Signal −3 dB Bandwidth (Note 8)	V_{OUT} = 0.2 V_{PP}, A_V = 1, R_L = 1 kΩ		900		MHz
		V_{OUT} = 0.2 V_{PP}, A_V = 1		720		
		V_{OUT} = 0.2 V_{PP}, A_V = 2		680		
		V_{OUT} = 0.2 V_{PP}, A_V = 4		630		
		V_{OUT} = 0.2 V_{PP}, A_V = 8, (R_F = 400Ω, R_G = 50Ω)		350		
LSBW	Large Signal −3 dB Bandwidth	V_{OUT} = 2 V_{PP}, A_V = 1, R_L = 1 kΩ		670		MHz
		V_{OUT} = 2 V_{PP}, A_V = 1		540		
		V_{OUT} = 2 V_{PP}, A_V = 2		530		
		V_{OUT} = 2 V_{PP}, A_V = 4		490		
		V_{OUT} = 2 V_{PP}, A_V = 8, (R_F = 400Ω, R_G = 50Ω)		350		
	0.1 dB Bandwidth	V_{OUT} = 0.2 V_{PP}, A_V = 1		50		MHz
	0.5 dB Bandwidth	V_{OUT} = 0.2 V_{PP}, A_V = 1		525		MHz
	Slew Rate	4V Step, A_V = 1		2300		V/µs
	Rise/Fall Time, 10%-90%	2V Step		690		ps
	0.1% Settling Time	2V Step		10		ns
	1.0% Settling Time	2V Step		6		ns
Distortion and Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 2 V_{PP}, f = 20 MHz, R_L = 800Ω		−79		dBc
		V_{OUT} = 2 V_{PP}, f = 70 MHz, R_L = 800Ω		−78		
HD3	3rd Harmonic Distortion	V_{OUT} = 2 V_{PP}, f = 20 MHz, R_L = 800Ω		−90		dBc
		V_{OUT} = 2 V_{PP}, f = 70 MHz, R_L = 800Ω		−71		
IMD3	3rd-Order Two-Tone Intermodulation	f_c = 20 MHz, , V_{OUT} = 2 V_{PP} Composite, R_L = 200Ω		−92		dBc
		f_c = 150 MHz, , V_{OUT} = 2 V_{PP} Composite, R_L = 200Ω		−76		
	Input Noise Voltage	f = 100 kHz		1.2		$nV/\sqrt{Hz}$
	Input Noise Current	f = 100 kHz		13.6		$pA/\sqrt{Hz}$
	Noise Figure (See Figure 5)	50Ω System, A_V = 9, 10 MHz		10.3		dB

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
Input Characteristics						
I_{BI}	Input Bias Current (Note 11)		−95	50	95	µA
$I_{Boffset}$	Input Bias Current Differential (Note 7)	V_{CM} = 0V, V_{ID} = 0V, $I_{Boffset}$ = (I_{B-} - I_{B+})/2	−18	2.5	18	µA
CMRR	Common Mode Rejection Ratio (Note 7)	DC, V_{CM} = 0V, V_{ID} = 0V		82		dBc
R_{IN}	Input Resistance	Differential		15		Ω
C_{IN}	Input Capacitance	Differential		0.5		pF
CMVR	Input Common Mode Voltage Range	CMRR > 38 dB	±3.3	±3.6		V
Output Performance						
	Output Voltage Level (Note 7)	Single-Ended Output	−3.7	±3.78	+3.7	V
I_{OUT}	Linear Output Current (Note 7)	V_{OUT} = 0V	±100	±120		mA
I_{SC}	Short Circuit Current	One Output Shorted to Ground V_{IN} = 2V Single-Ended (Note 6)		±150		mA
Clamp Performance						
V_{CLAMP}	V_{CLAMP} Voltage Range	Continuous Operation (Note 11)	V_{CM}		V_{CM} + 2.0	V
	V_{CLAMP} Peak Voltage	(Note 14)			V_{CM} + 3.0	
	Default V_{CLAMP} Voltage	V_{CLAMP} Floating	0.92	1.0	1.08	V
	Upper Clamp Level Accuracy	V_{CLAMP} = 2V, V_{CM} = 1.5V, V_O = 2V, 100% Overdrive	−53	−40	+53	mV
	Lower Clamp Level Accuracy	V_{CLAMP} = 2V, V_{CM} = 1.5V, V_O = 1V, 100% Overdrive	−30	−8	+30	
	Clamp Accuracy Temperature Drift			−0.1		mV/°C
	Clamp Pin Bias Current	V_{IN} = 0V, $V_{CLAMP(MIN)}$ = −3.1 V	−200	−175		µA
		V_{IN} = 0V, $V_{CLAMP(MAX)}$ = +4.5V		150	175	
	Clamp Pin Bias Drift			0.3		µA/°C
	Diff Amp Input Bias Shift	Linear to Clamped Operation		60		µA
	Clamp Pin Input Impedance			30 1		KΩ/pF
	Clamp Pin Feedthrough	f = 10 MHz		−60		dB
	Clamp Bandwidth	0.5V_{DC} + 40 mV_{PP}, SE V_{IN} = 2V		140		MHz
	Clamp Slew Rate	100% Overdrive		64		V/µs
	Clamp Overshoot	V_{IN} = 2V Step, A_V = 2 V/V, V_{CLAMP} = 0.5V, V_{CM} = 0V, 100% Overdrive		125		mV
	Clamp Overshoot	V_{IN} = 2V Step, A_V = 2 V/V, V_{CLAMP} = 2V, V_{CM} = 1.5V, 100% Overdrive		250		mV
	Clamp Overshoot Width	(Note 13)		650		ps
	Clamp Overdrive Recovery Time	V_{IN} = 2V Step, A_V = 2 V/V, V_{CLAMP} = 0.5V, V_{CM} = 0V, 50% Output Crossing		600		ps
	Linearity Guardband (Note 12)	f = 75 MHz, V_{OD} = 2 V_{PP}, R_L = 800, SFDR Down 3 dB		22		mV
Output Common Mode Control Circuit						
	Common Mode Small Signal Bandwidth	V_{IN+} = V_{IN-} = 0		220		MHz
	Slew Rate	V_{IN+} = V_{IN-} = 0		340		V/µs

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
V_{OSCM}	Output Common Mode Error	Common Mode, V_{IN} = Float, V_{CM} = 0	−25	1	25	mV
	Input Bias Current	$V_{CM(TYPICAL)}$ = 0, (Note 9)	−8	−3.5	1	µA
		$V_{CM(MIN)}$ = −3.2 V, (Note 9)	−9	−4.5		
		$V_{CM(MAX)}$ = +3.2V, (Note 9)		−2.5	2	
	Voltage Range		±3.14	±3.18		V
	CMRR	Measure V_{OD}, V_{ID} = 0V		80		dB
	Input Resistance			200		kΩ
	Gain	$\Delta V_{O,CM}/\Delta V_{CM}$	0.995	1.00	1.008	V/V
Miscellaneous Performance						
Z_T	Open Loop Transimpedance	Differential		112		dBΩ
PSRR	Power Supply Rejection Ratio	DC, ΔV_S = ±1V		87		dB
I_S	Supply Current	R_L = ∞	25	29.1	33 **37**	mA

V_S = ±2.5V Electrical Characteristics (Note 2)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V_S = ±2.5V, A_V = 1, V_{CM} = 0V, V_{CLAMP} = 2V, R_F = R_G = 275Ω, R_L = 200Ω, for single-ended in, differential out. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
AC Performance (Differential)						
SSBW	Small Signal −3 dB Bandwidth (Note 8)	V_{OUT} = 0.2 V_{PP}, A_V = 1, R_L = 1 kΩ		875		MHz
		V_{OUT} = 0.2 V_{PP}, A_V = 1		630		
		V_{OUT} = 0.2 V_{PP}, A_V = 2		580		
		V_{OUT} = 0.2 V_{PP}, A_V = 4		540		
		V_{OUT} = 0.2 V_{PP}, A_V = 8 , (R_F = 400Ω, R_G = 50Ω)		315		
LSBW	Large Signal −3 dB Bandwidth	V_{OUT} = 2 V_{PP}, A_V = 1, R_L = 1 kΩ		640		MHz
		V_{OUT} = 2 V_{PP}, A_V = 1		485		
		V_{OUT} = 2 V_{PP}, A_V = 2		435		
		V_{OUT} = 2 V_{PP}, A_V = 4		420		
		V_{OUT} = 2 V_{PP}, A_V = 8, (R_F = 400Ω, R_G = 50Ω)		405		
	0.1 dB Bandwidth	V_{OUT} = 0.2 V_{PP}, A_V = 1		60		MHz
	0.5 dB Bandwidth	V_{OUT} = 0.2 V_{PP}, A_V = 1		236		MHz
	Slew Rate	2V Step, A_V = 1		1350		V/µs
	Rise/Fall Time, 10%-90%	2V Step		860		ps
	0.1% Settling Time	2V Step		10		ns
	1.0% Settling Time	2V Step		6		ns
Distortion and Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 2 V_{PP}, f = 20 MHz, R_L = 800Ω		−80		dBc
		V_{OUT} = 2 V_{PP}, f = 70 MHz, R_L = 800Ω		−72		
HD3	3rd Harmonic Distortion	V_{OUT} = 2 V_{PP}, f = 20 MHz, R_L = 800Ω		−78		dBc
		V_{OUT} = 2 V_{PP}, f = 70 MHz, R_L = 800Ω		−66		
IMD3	3rd-Order Two-Tone Intermodulation	f_c = 20 MHz, V_{OUT} = 2 V_{PP} Composite, R_L = 200Ω		−87		dBc
		f_c = 150 MHz, V_{OUT} = 2 V_{PP} Composite, R_L = 200Ω		−68		
	Input Noise Voltage	f = 100 kHz		1.1		$nV/\sqrt{Hz}$
	Input Noise Current	f = 100 kHz		13.6		$pA/\sqrt{Hz}$

Symbol	Parameter	Conditions	Min (*Note 8*)	Typ (*Note 7*)	Max (*Note 8*)	Units
	Noise Figure (See *Figure 5*)	50Ω System, A_V = 9, 10 MHz		10.3		dB
Input Characteristics						
I_{BI}	Input Bias Current (*Note 11*)		−90	45	90	µA
$I_{Boffset}$	Input Bias Current Differential (*Note 7*)	V_{CM} = 0V, V_{ID} = 0V, $I_{Boffset}$ = (I_{B-} - I_{B+})/2	−24	2	24	µA
CMRR	Common Mode Rejection Ratio (*Note 7*)	DC, V_{CM} = 0V, V_{ID} = 0V		80		dBc
R_{IN}	Input Resistance	Differential		15		Ω
C_{IN}	Input Capacitance	Differential		0.5		pF
CMVR	Input Common Mode Voltage Range	CMRR > 38 dB	±1.0	±1.2		V
Output Performance						
	Output Voltage Swing (*Note 7*)	Differential Output	5.32	5.47		V_{PP}
I_{OUT}	Linear Output Current (*Note 7*)	V_{OUT} = 0V	±75	±95		mA
I_{SC}	Short Circuit Current	One Output Shorted to Ground V_{IN} = 2V Single-Ended (*Note 6*)		±140		mA
Clamp Performance						
V_{CLAMP}	V_{CLAMP} Voltage Range	Continuous Operation (*Note 11*)	V_{CM}		V_{CM} + 2.0	V
	V_{CLAMP} Peak Voltage	(*Note 14*)			V_{CM} + 3.0	
	Default V_{CLAMP} Voltage	V_{CLAMP} Floating	0.42	0.48	0.54	V
	Upper Clamp Level Accuracy	V_{IN} = 0V, V_{CLAMP} = +0.5V, V_{CM} = 0, V_O = +0.5V, 100% Overdrive	−39	−30	+39	mV
	Lower Clamp Level Accuracy	V_{IN} = 0V, V_{CLAMP} = +0.5V, V_{CM} = 0, V_O = −0.5V, 100% Overdrive	−18	6	+18	
	Clamp Accuracy Temperature Drift			−0.1		mV/°C
	Clamp Pin Bias Current	V_{IN} = 0V, V_{CLAMP} = 1V, V_{CM} = 0		23.5		µA
	Clamp Pin Bias Drift			0.3		µA/°C
	Diff Amp Input Bias Shift	Linear to Clamped Operation		50		µA
	Clamp Pin Input Impedance			30 1		kΩ/pF
	Clamp Pin Feedthrough	f = 10 MHz		−60		dB
	Clamp Bandwidth	0.5V_{DC} + 40 mV_{PP}, SE V_{IN} = 2V		125		MHz
	Clamp Slew Rate	100% Overdrive		52		V/µs
	Clamp Overshoot	V_{IN} = 1V Step, A_V = 2 V/V, V_{CLAMP} = 0.5V, V_{CM}= 0V, 100% Overdrive		105		mV
	Clamp Overshoot	V_{IN} = 1V Step, A_V= 2 V/V, V_{CLAMP} = 1V, V_{CM} = 0.5V, 100% Overdrive		105		mV
	Clamp Overshoot Width	(*Note 13*)		650		ps
	Clamp Overdrive Recovery Time	V_{IN} = 2V Step, A_V = 2 V/V, V_{CLAMP} = 0.5V, V_{CM} = 0V, 50% Output Crossing		600		ps
	Linearity Guardband (*Note 12*)	f = 75 MHz, V_{OD} = 2 V_{PP}, R_L = 800, SFDR Down 3 dB		40		mV
Output Common Mode Control Circuit						
	Common Mode Small Signal Bandwidth	V_{IN+} = V_{IN-} = 0		130		MHz
	Slew Rate	V_{IN+} = V_{IN-} = 0		186		V/µs

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
V_{OSCM}	Output Common Mode Error	Common Mode, V_{IN} = float, V_{CM} = 0	−20	2	20	mV
	Input Bias Current	V_{CM} = 0, (Note 9)		−3.5		µA
	Voltage Range		±0.75	±0.81		V
	CMRR	Measure V_{OD}, V_{ID} = 0V		84		dB
	Input Resistance			200		kΩ
	Gain	$\Delta V_{O,CM}/\Delta V_{CM}$	0.995	1.00	1.008	V/V
Miscellaneous Performance						
Z_T	Open Loop Transimpedance	Differential		105		dBΩ
PSRR	Power Supply Rejection Ratio	DC, ΔV_S = ±1V		85		dB
I_S	Supply Current	R_L = ∞	23	26.5	30 **34**	mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. See Applications Section for information on temperature de-rating of this device." Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Note 4: The maximum output current (I_{OUT}) is determined by device power dissipation limitations. See the Power Dissipation section of the Application Section for more details.

Note 5: Human Body Model, applicable std. MIL-STD-883, Method 30157. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 6: Short circuit current should be limited in duration to no more than 10 seconds. See the Power Dissipation section of the Application Information for more details.

Note 7: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 8: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

Note 9: Negative current implies current flowing out of the device.

Note 10: I_{BI} is referred to a differential output offset voltage by the following relationship: $V_{OD(offset)} = I_{BI} * 2R_F$

Note 11: Exceeding limits could result in excessive device current.

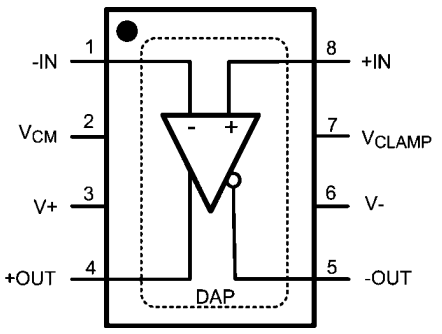
Note 12: Linearity Guardband is defined for an output sinusoid (f = 75 MHz, V_{OD} = 2 V_{PP}). It is the difference between the V_{CLAMP} level and the peak output voltage where the SFDR is decreased by 3 dB.

Note 13: Clamp Overshoot Width is the duration of overshoot in a 100% overdrive condition.

Note 14: This parameter is guaranteed by design and/or characterization and is not tested in production. The condition of V_{CLAMP} = 3V is not intended for continuous operation; continuous operation with V_{CLAMP} = 3V may incur permanent damage to the device.

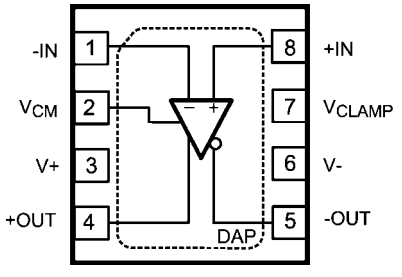
Connection Diagrams

8-Pin PSOP



Top View

8-Pin LLP



Top View

Pin Descriptions

Pin No.	Pin Name	Description
1	-IN	Negative Input
2	V_{CM}	Output Common Mode Control
3	V+	Positive Supply
4	+OUT	Positive Output
5	-OUT	Negative Output
6	V-	Negative Supply
7	V_{CLAMP}	Output Voltage Clamp Control
8	+IN	Positive Input
DAP	DAP	Die Attach Pad (See Thermal Performance section for more information)

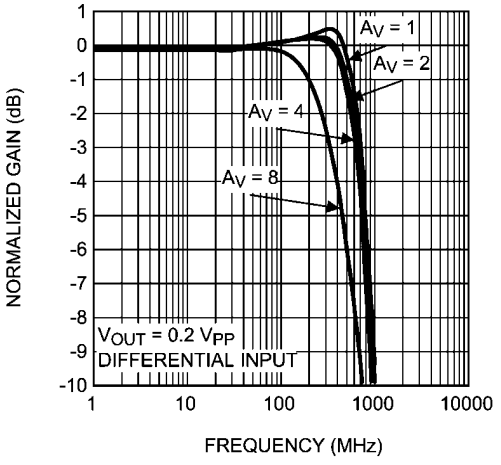
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin PSOP	LMH6553MR	LMH6553MR	95 Units/Rails	MRA08A
	LMH6553MRE		250 Units Tape and Reel	
	LMH6553MRX		2.5k Units Tape and Reel	
8-Pin LLP	LMH6553SD	6553	1k Units Tape and Reel	SDA08C
	LMH6553SDE		250 Units Tape and Reel	
	LMH6553SDX		4.5k Units Tape and Reel	

Typical Performance Characteristics V_S = ±5V

(T_A = 25°C, R_F = R_G = 275Ω, R_L = 200Ω, A_V = 1, for single ended in, differential out, unless specified).

Frequency Response vs. Gain



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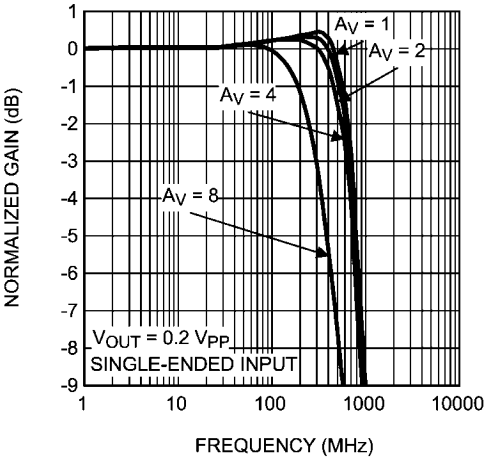
Frequency Response vs. Gain



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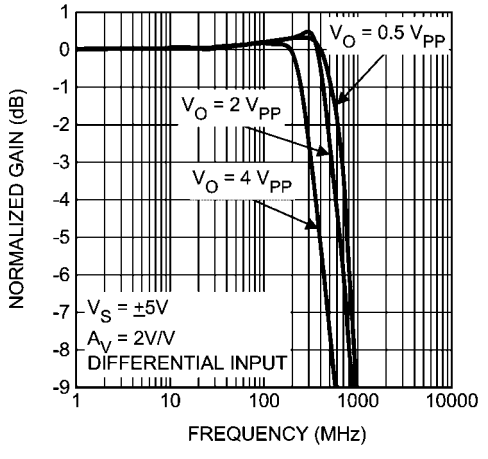
Frequency Response vs. V_{OUT}



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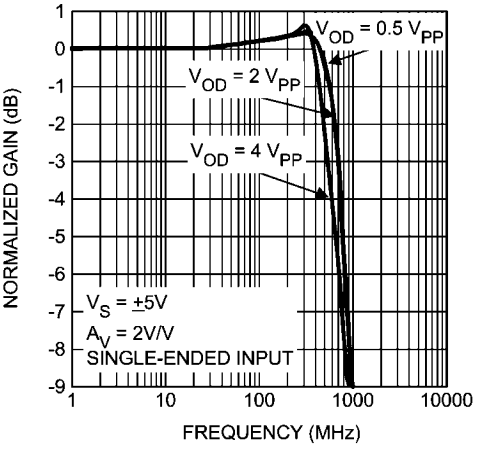
Frequency Response vs. V_{OUT}



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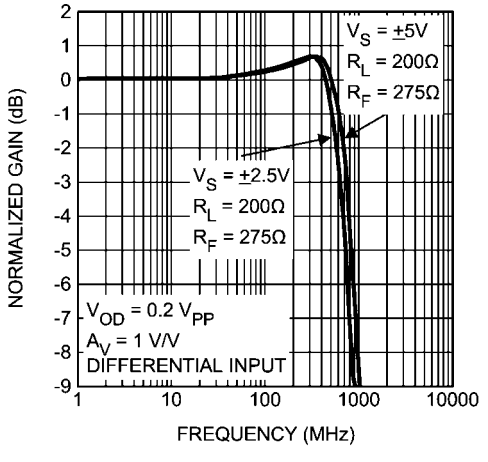
Frequency Response vs. Supply Voltage (R_L = 200Ω)



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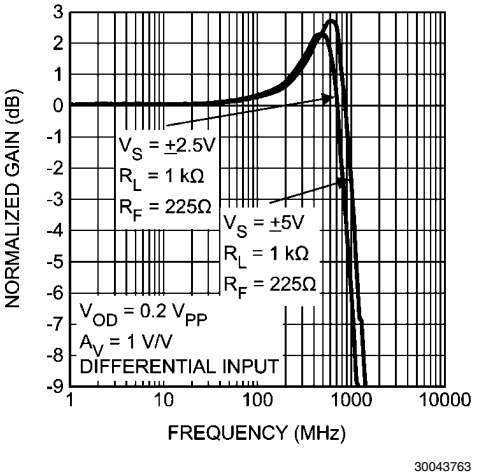
Frequency Response vs. Supply Voltage (R_L = 1 kΩ)



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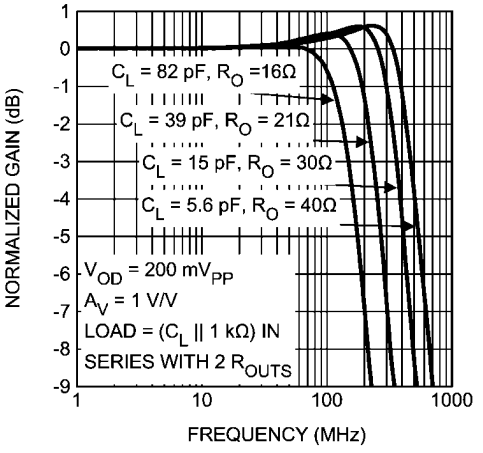
Frequency Response vs. Capacitive Load



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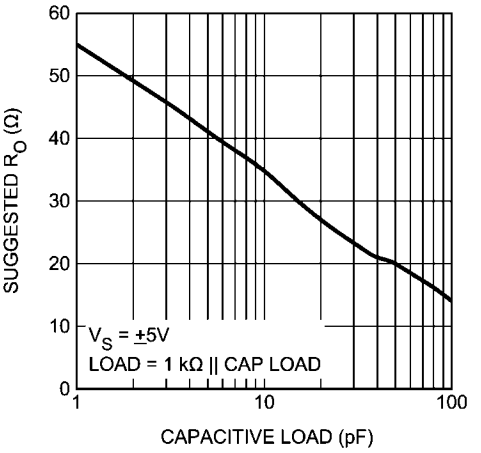
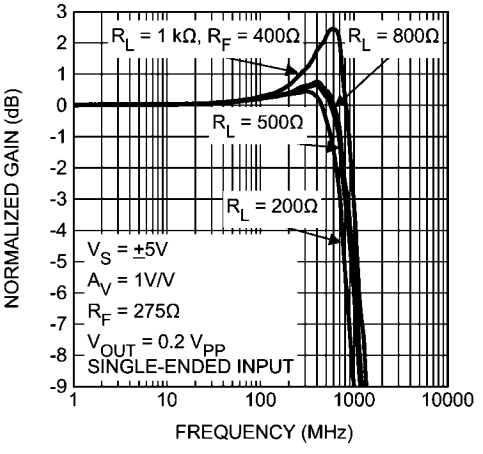
Suggested R_O vs. Capacitive Load



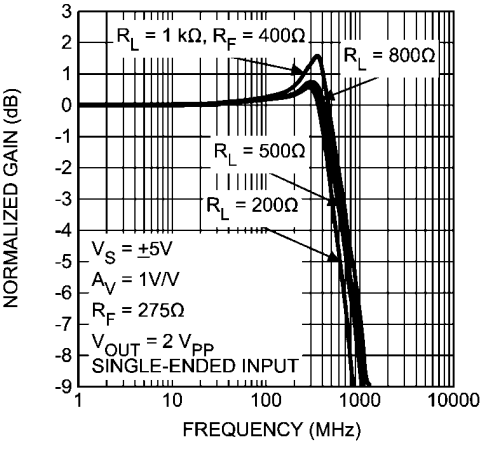
30043722

Frequency Response vs. Resistive Load



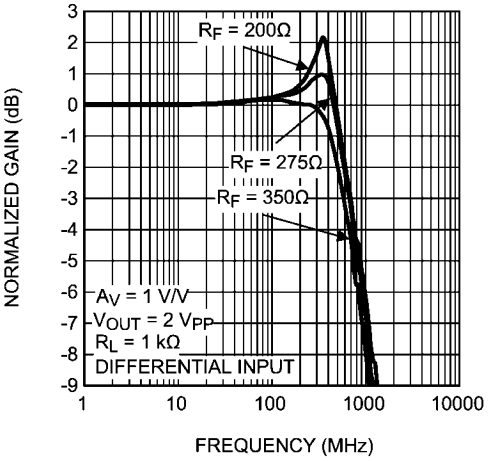
30043759

Frequency Response vs. Resistive Load



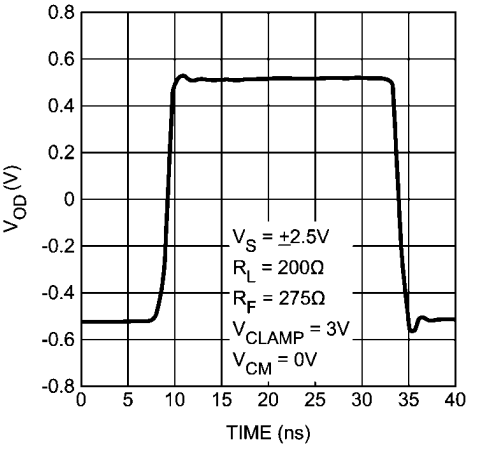
30043760

Frequency Response vs. R_F



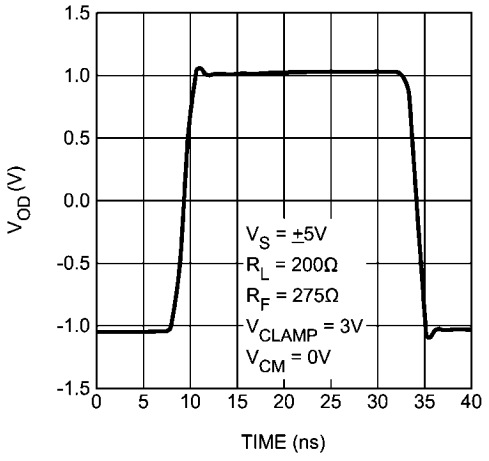
30043761

1 V_{PP} Pulse Response Single-Ended Input



30043726

2 V_{PP} Pulse Response Single-Ended Input



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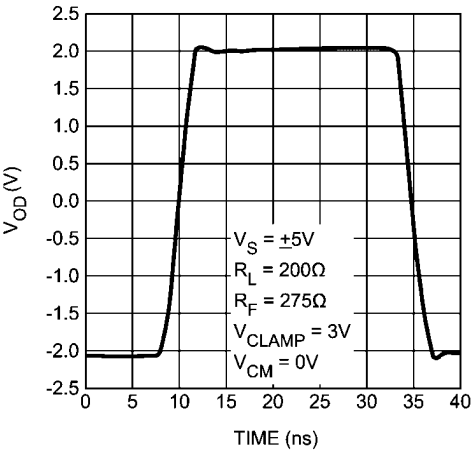
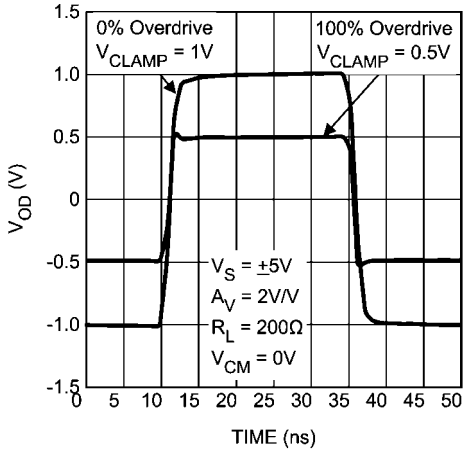
4 V_{PP} Pulse Response Single-Ended Input



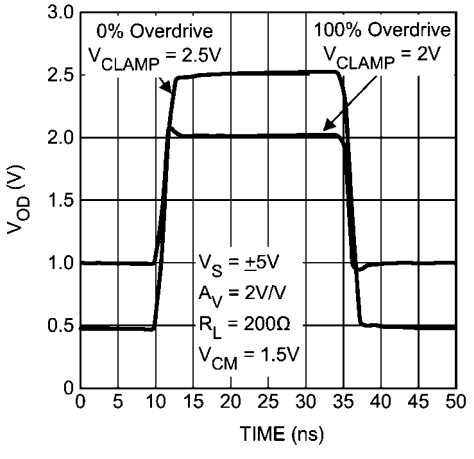
30043725

Pulse Response with 0% and 100% Overdrive



30043774

Pulse Response with 0% and 100% Overdrive



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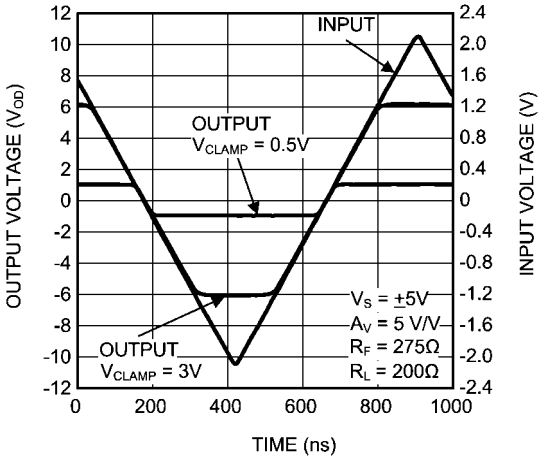
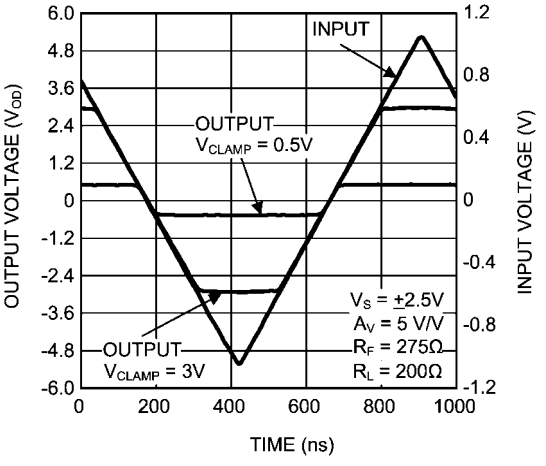
Overdrive Recovery with V_S = ±5V



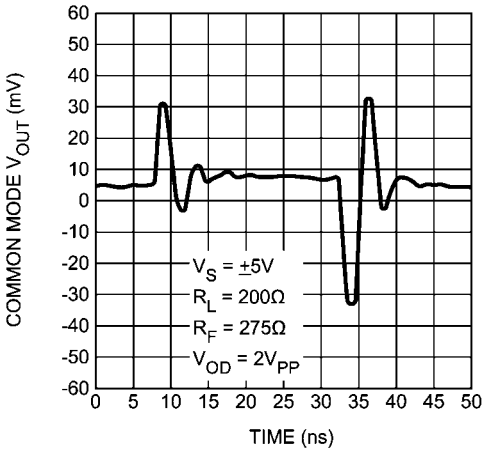
30043757

Overdrive Recovery with V_S = ±2.5V



30043758

Output Common Mode Pulse Response



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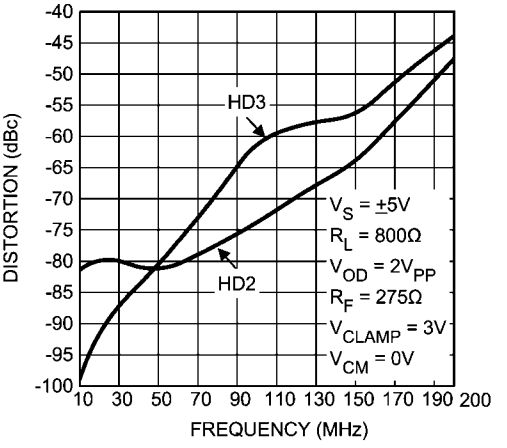
Distortion vs. Frequency Single-Ended Input (R_L=800Ω)



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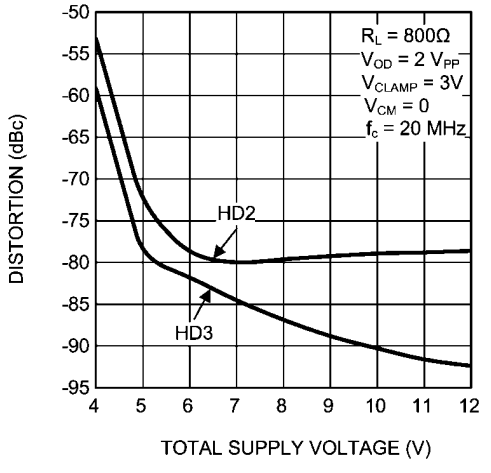
Distortion vs. Supply Voltage (f_c=20Mhz, R_L=800Ω)



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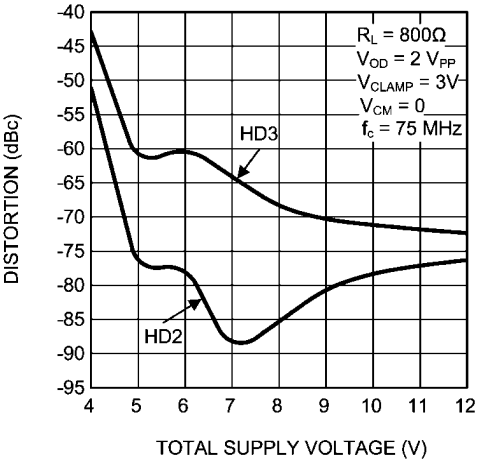
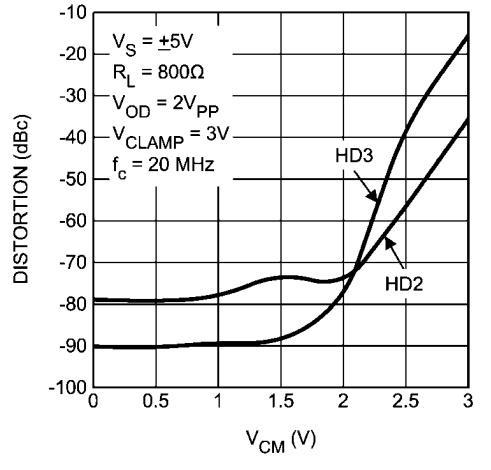
Distortion vs. Supply Voltage (f_c=75Mhz, R_L=800Ω)



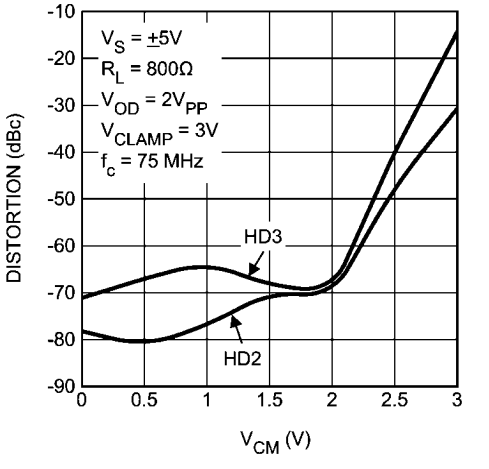
30043737

Distortion vs. V_{CM} (f_c=20Mhz, R_L=800Ω)



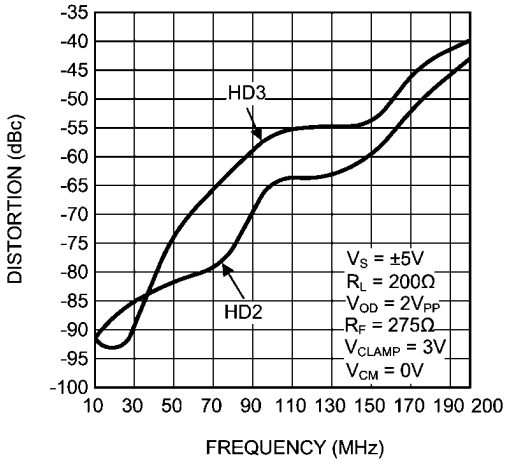
30043738

Distortion vs. V_{CM} (f_c=75Mhz, R_L=800Ω)



30043767

Distortion vs. Frequency Single-Ended Input (R_L=200Ω)



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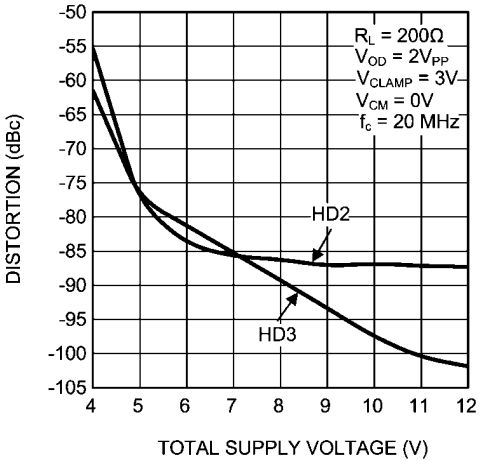
Distortion vs. Supply Voltage (f_c=20Mhz, R_L=200Ω)



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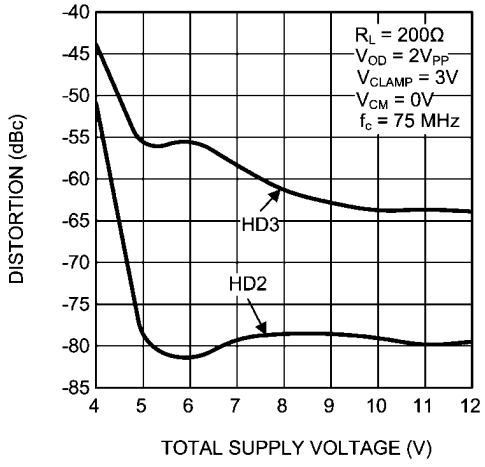
Distortion vs. Supply Voltage (f_c=75Mhz, R_L=200Ω)



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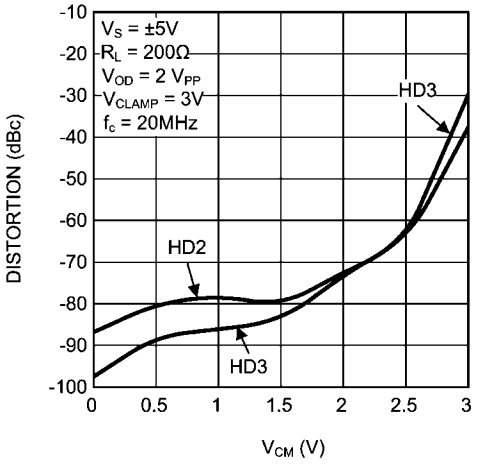
Distortion vs. V_{CM} (f_c=20Mhz, R_L=200Ω)



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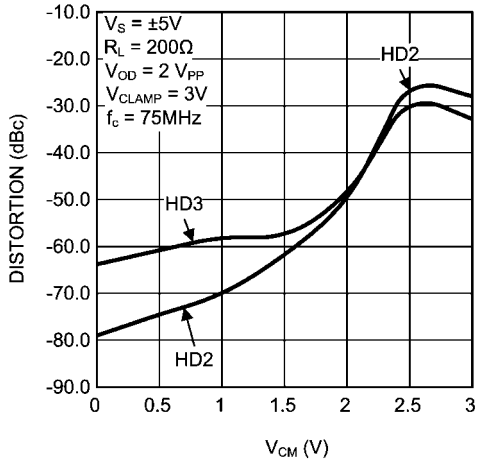
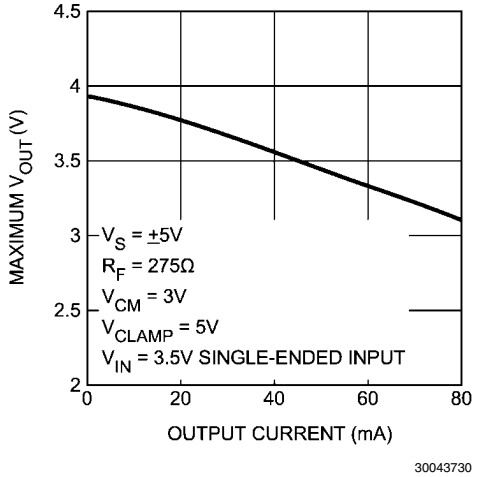
Distortion vs. V_{CM} (f_c=75Mhz, R_L=200Ω)



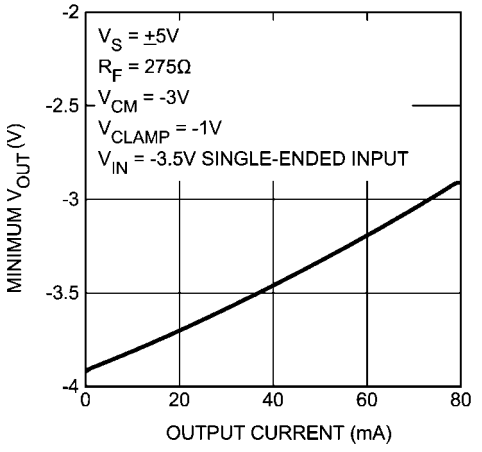
30043785

Maximum V_{OUT} vs. I_{OUT}



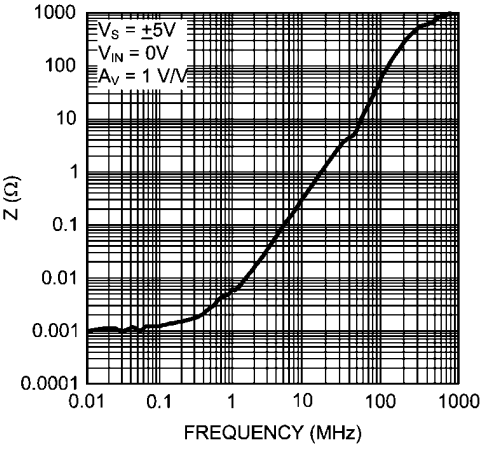
30043730

Minimum V_{OUT} vs. I_{OUT}



30043731

Closed Loop Output Impedance



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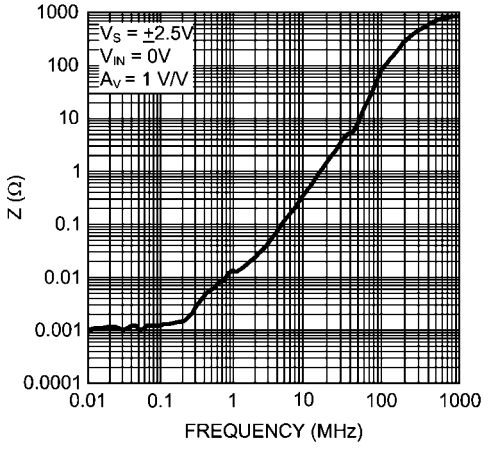
Closed Loop Output Impedance



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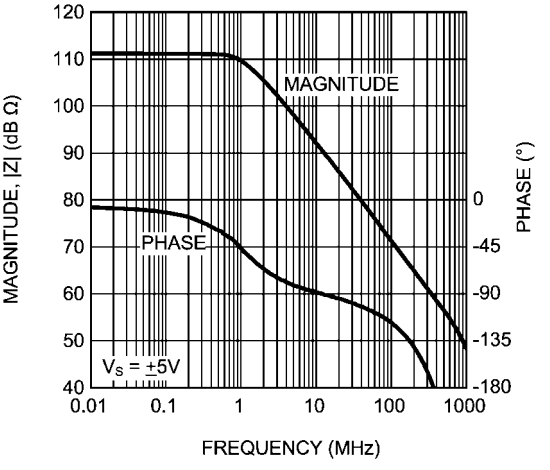
Open Loop Transimpedance



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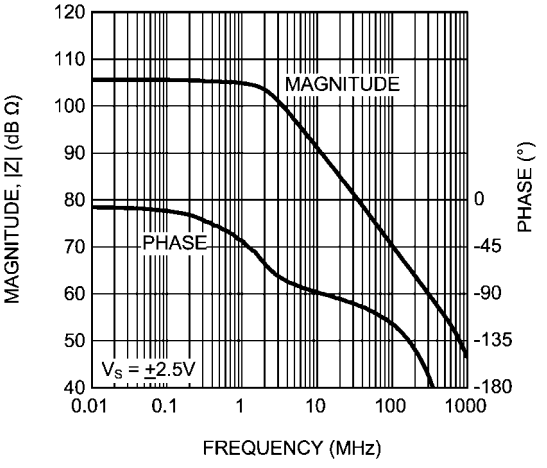
Open Loop Transimpedance



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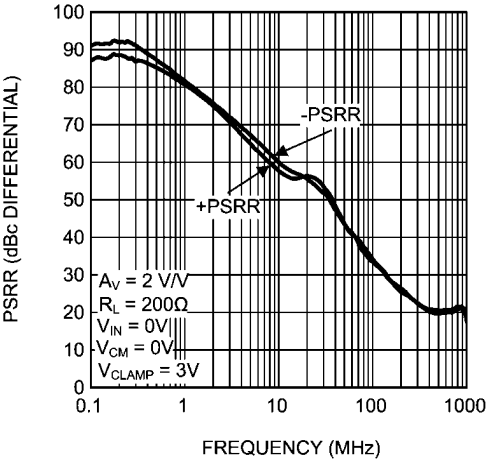
PSRR



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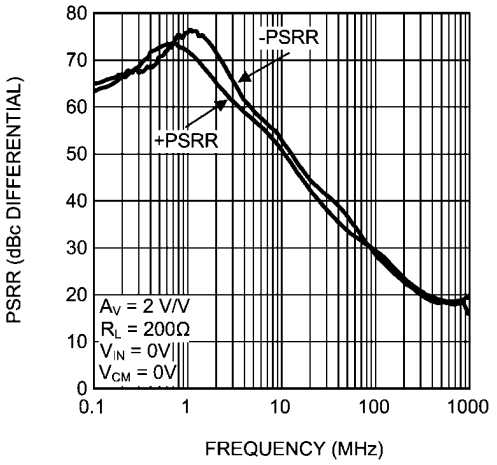
PSRR



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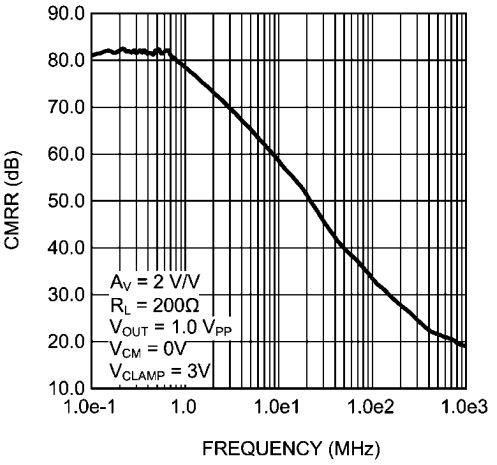
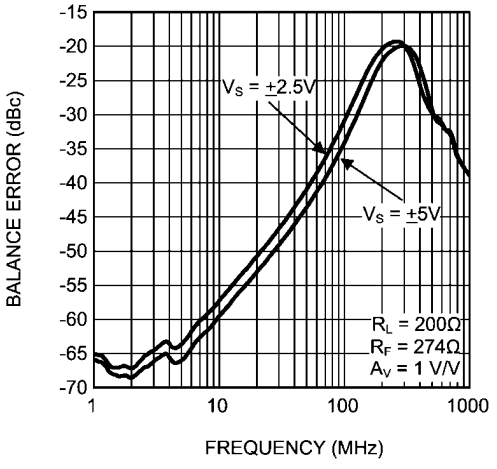
CMRR



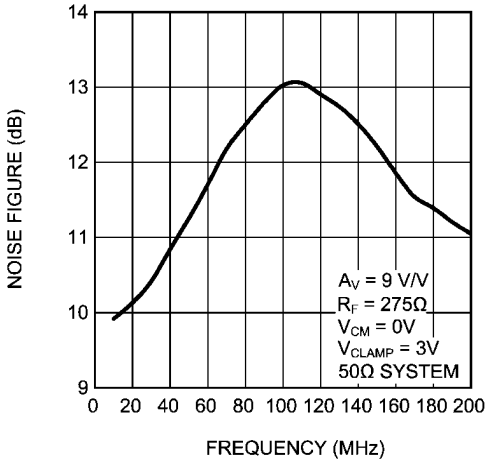
30043733

Balance Error



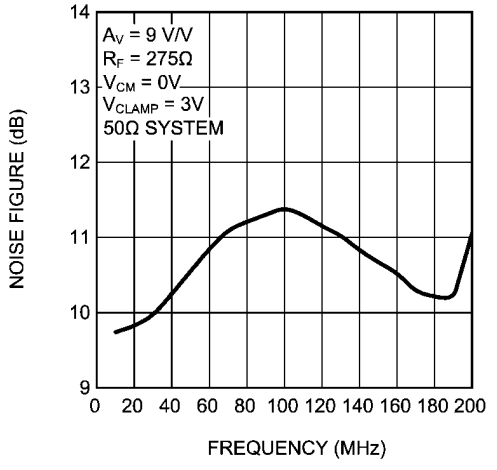
30043713

Noise Figure



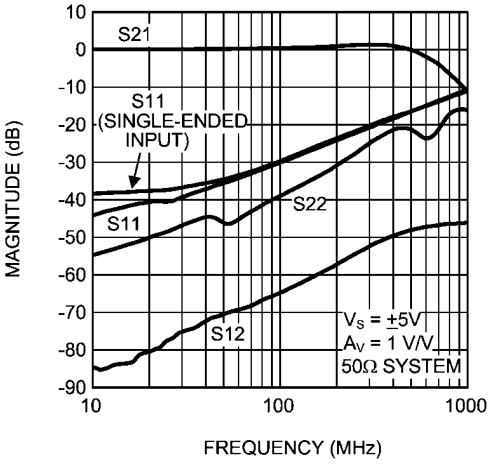
30043745

Noise Figure



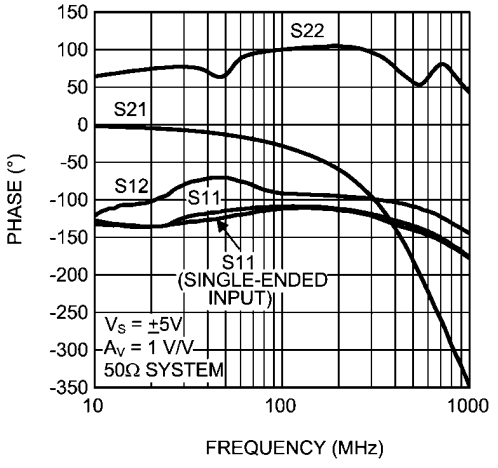
30043746

Differential S-Parameter Magnitude vs. Frequency



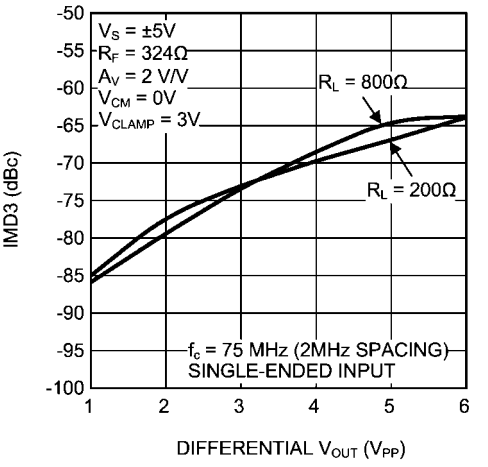
30043755

Differential S-Parameter Phase vs. Frequency



30043756

3rd Order Intermodulation Products vs. V_{OUT}



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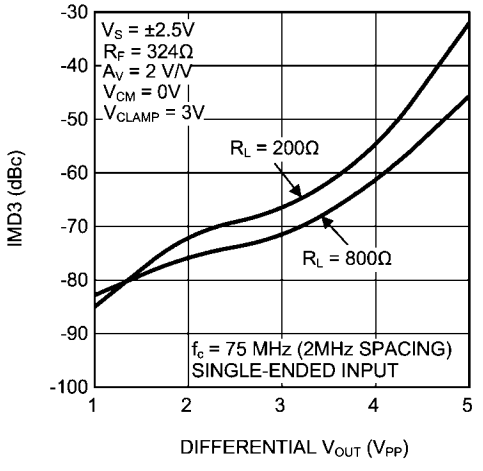
3rd Order Intermodulation Products vs. V_{OUT}



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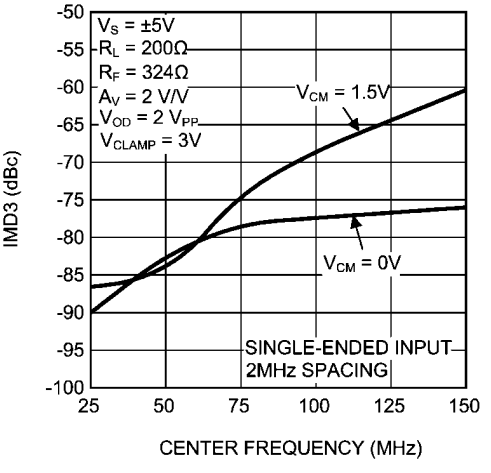
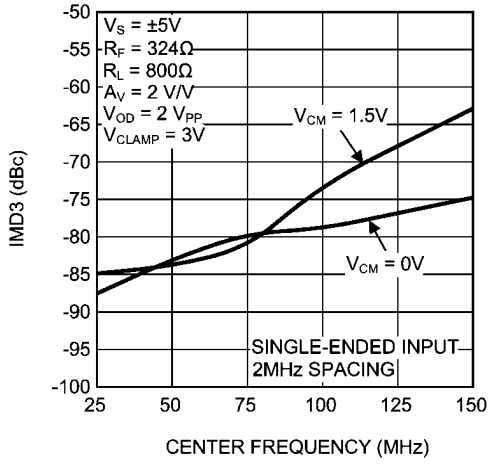
3rd Order Intermodulation Products vs. Center Frequency



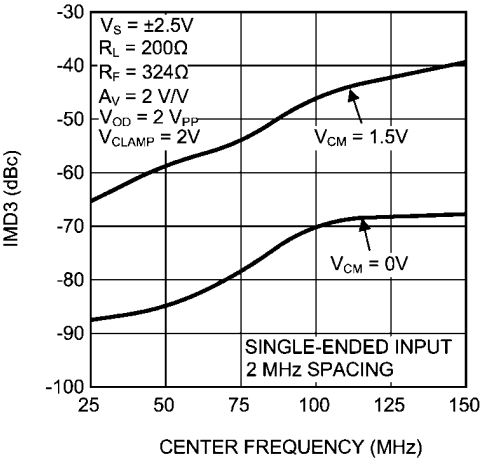
30043777

3rd Order Intermodulation Products vs. Center Frequency



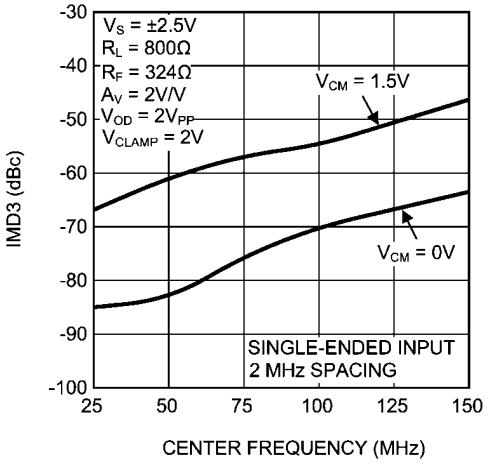
30043765

3rd Order Intermodulation Products vs. Center Frequency



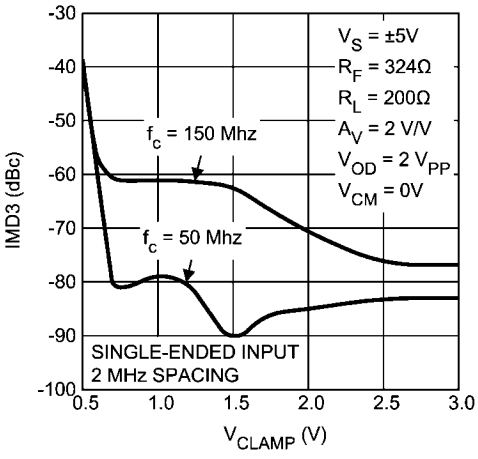
30043778

3rd Order Intermodulation Products vs. Center Frequency



30043779

3rd Order Intermodulation Products vs. V_{CLAMP}



30043780

Application Information

The LMH6553, a fully differential current feedback amplifier with integrated output common mode control and output limiting clamp, is designed to provide protection of following input stages. The common mode feedback circuit sets the output common mode voltage independent of the input common mode, as well as forcing the outputs to be equal in magnitude and opposite in phase, even when only one of the inputs is driven as in single ended to differential conversion.

The proprietary current feedback architecture of the LMH6553 offers gain and bandwidth independence even at high values of gain, simply with the appropriate choice of R_{F1} and R_{F2}. Generally R_{F1} is set equal to R_{F2}, and R_{G1} equal to R_{G2}, so that the gain is set by the ratio R_F/R_G. Matching of these resistors greatly affects CMRR, DC offset error, and output balance. Resistors with 0.1% tolerances are recommended for optimal performance, and the amplifier is internally compensated to operate with optimum gain flatness with values of R_F between 250Ω and 350Ω depending on package selection, PCB layout, and load resistance.

The output common mode voltage is set by the V_{CM} pin with a fixed gain of 1 V/V. This pin should be driven by a low impedance source and should be bypassed to ground with a 0.1 µF ceramic capacitor. Any unwanted signal coupling into the V_{CM} pin will be passed along to the outputs, reducing the performance of the amplifier. This pin must not be left floating.

The LMH6553 can be operated with either a single 5V supply or split +5V and –5V supplies. Operation on a single 5V supply, depending on gain, is limited by the input common mode range; therefore, AC coupling may be required. For example, in a DC coupled input application on a single 5V supply, with a V_{CM} of 1.5V, the input common voltage at a gain of 1 will be 0.75V which is outside the minimum 1.5V to 3.5V input common mode range of the amplifier. The minimum V_{CM} for this application should be greater than 1.5V depending on output signal swing. Alternatively, AC coupling of the inputs in this example results in equal input and output common mode voltages, so a 1.5V input common mode would result. Split supplies allow much less restricted AC and DC coupled operation with optimum distortion performance.

The LMH6553 has a V_{CLAMP} input which allows control of the maximum amplifier output swing to prevent overdriving of following stages such as sensitive ADC inputs and also provides fast recovery from transients that would otherwise saturate the signal path.

RECOMMENDED FEEDBACK RESISTOR

The LMH6553 is available in both an 8-pin LLP and PSOP package. The recommended feedback resistor, R_F, for the LLP package is 275Ω and 325Ω for the PSOP to give a flat frequency response with minimal peaking.

FULLY DIFFERENTIAL OPERATION

The LMH6553 is ideal for a fully differential configuration. The circuit shown in *Figure 1* is a typical fully differential application circuit as might be used to drive an analog to digital converter (ADC). In this circuit the closed loop gain $A_V = V_{OUT}/ V_{IN} = R_F/R_G$, where the feedback is symmetric. The series output resistors, R_O, are optional and help keep the amplifier stable when presented with a capacitive load. Refer to the Driving Capacitive Loads section for details.

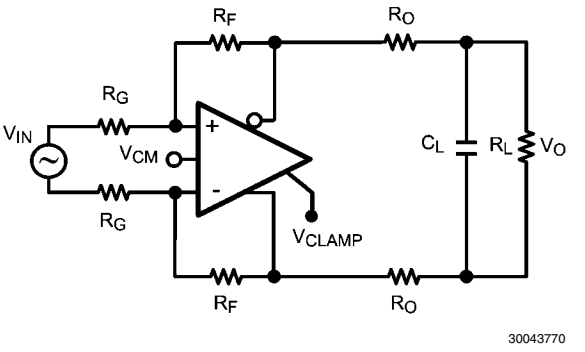


FIGURE 1. Typical Application

When driven from a differential source, the LMH6553 provides low distortion, excellent balance, and common mode rejection. This is true provided the resistors R_F, R_G and R_O are well matched and strict symmetry is observed in board layout.

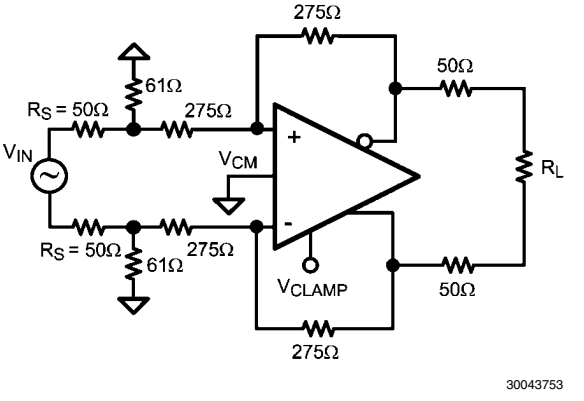


FIGURE 2. Differential S-Parameter Test Circuit

The circuit configuration shown in *Figure 2* was used to measure differential S parameters in a 50Ω environment at a gain of 1 V/V. Refer to the Differential S-Parameter vs. Frequency plots in the Typical Performance Characteristics section for measurement results.

SINGLE-ENDED INPUT TO DIFFERENTIAL OUTPUT OPERATION

In many applications, it is required to drive a differential input ADC from a single-ended source. Traditionally, transformers have been used to provide single to differential conversion, but these are inherently bandpass by nature and cannot be used for DC coupled applications. The LMH6553 provides excellent performance as a single-to-differential converter down to DC. *Figure 3* shows a typical application circuit where an LMH6553 is used to produce a differential signal from a single ended source.

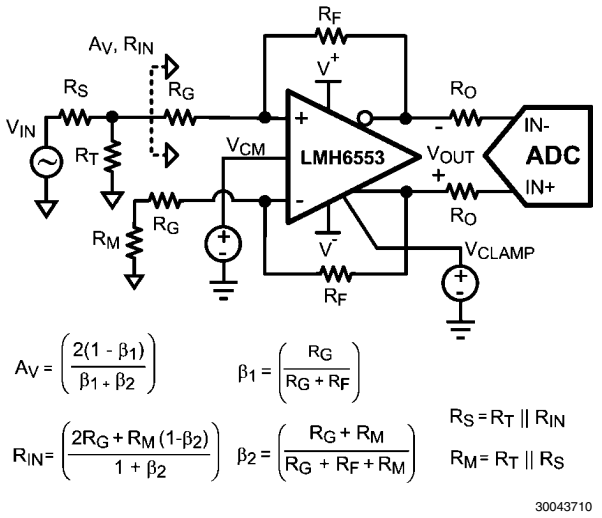


FIGURE 3. Single-Ended Input with Differential Output

When using the LMH6553 in single-to-differential mode, the complementary output is forced to a phase inverted replica of the driven output by the common mode feedback circuit as opposed to being driven by its own complementary input. Consequently, as the driven input changes, the common mode feedback action results in a varying common mode voltage at the amplifier's inputs, proportional to the driving signal. Due to the non-ideal common mode rejection of the amplifier's input stage, a small common mode signal appears at the outputs which is superimposed on the differential output signal. The ratio of the change in output common mode voltage to output differential voltage is commonly referred to as output balance error. The output balance error response of the LMH6553 over frequency is shown in the Typical Performance Characteristics section.

To match the input impedance of the circuit in *Figure 3* to a specified source resistance, R_S, requires that $R_T \parallel R_{IN} = R_S$. The equations governing R_{IN} and A_V for single-to-differential operation are also provided in *Figure 3*. These equations, along with the source matching condition, must be solved iteratively to achieve the desired gain with the proper input termination. Component values for several common gain configurations in a 50Ω environment are given in *Table 1*.

TABLE 1. Gain Component Values for 50Ω System LLP Package

Gain	R_F	R_G	R_T	R_M
0 dB	275Ω	255Ω	59Ω	26.7Ω
6 dB	275Ω	127Ω	68.1Ω	28.7Ω
12 dB	275Ω	54.9Ω	107Ω	34Ω

TABLE 2. Gain Component Values for 50Ω System PSOP Package

Gain	R_F	R_G	R_T	R_M
0 dB	325Ω	316Ω	56.2Ω	26.7Ω
6 dB	325Ω	150Ω	64.9Ω	28Ω
12 dB	325Ω	68.1Ω	88.7Ω	31.6Ω

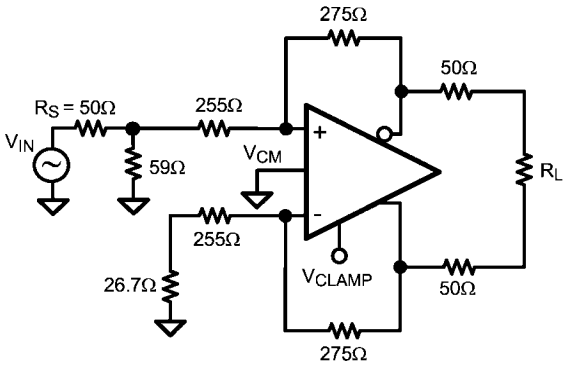


FIGURE 4. Single Ended Input S-Parameter Test Circuit (50Ω System)

The circuit shown in *Figure 4* was used to measure S-parameters for a single-to-differential configuration. The S-parameter plots in the Typical Performance Curves are taken using the recommended component values for 0 dB gain.

SINGLE SUPPLY OPERATION

Single supply operation is possible on supplies from 5V to 10V; however, as discussed earlier, AC input coupling is recommended for low supplies due to input common mode limitations. An example of an AC coupled, single supply, single-to-differential circuit is shown in *Figure 5*. Note that when AC coupling, both inputs need to be AC coupled irrespective of single-to-differential or differential-to-differential configuration. For higher supply voltages, DC coupling of the inputs may be possible provided that the output common mode DC level is set high enough so that the amplifier's inputs and outputs are within their specified operating ranges.

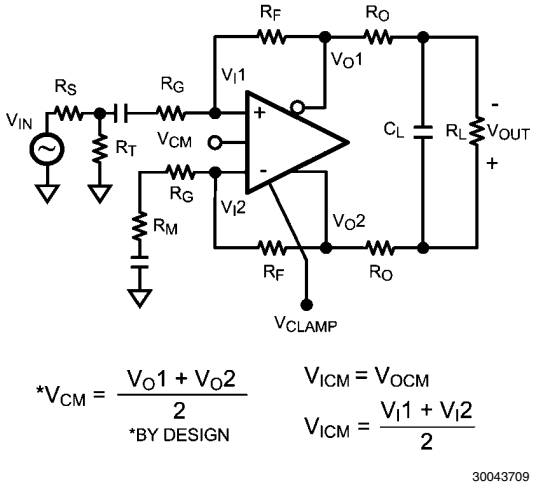


FIGURE 5. AC Coupled for Single Supply Operation

SPLIT SUPPLY OPERATION

For optimum performance, split supply operation is recommended using +5V and –5V supplies; however, operation is possible on split supplies as low as +2.25V and –2.25V and as high as +6V and –6V. Provided the total supply voltage does not exceed the 4.5V to 12V operating specification, asymmetric supply operation is also possible and in some cases advantageous. For example, if 5V DC coupled operation is required for low power dissipation but the amplifier input common mode range prevents this operation, it is still possible with split supplies of (V^+) and (V^-). Where (V^+) - (V^-) = 5V and V^+ and V^- are selected to set the amplifier input common mode voltage to suit the application.

CLAMP OPERATION

The output clamp allows control of the maximum amplifier output swing to prevent overdriving of following stages such as sensitive ADC inputs and provide fast recovery from signal transients that would otherwise saturate the signal path. *Figure 6* shows the relationship between V_{CLAMP} and the +OUT and –OUT outputs. The example circuit shown has a single ended input and is set for a gain of 2 V/V. For proper operation $V_{CM} < V_{CLAMP} < V_{CM} + 2.0V$ and the upper single ended output voltage is limited to the voltage level set at the V_{CLAMP} input. The output common mode control loop forces the lower single ended voltage to be limited to $2*V_{CM} - V_{CLAMP}$. The maximum clamped single ended output swing is therefore equal to $2*(V_{CLAMP} - V_{CM})$ and the maximum differential output swing is therefore equal to $4*(V_{CLAMP} - V_{CM})$. In the example of *Figure 6* with V_{CLAMP} set to 2V and V_{CM} set to 1.5V, the maximum single ended output is therefore 1 V_{PP} centered at 1.5V and the maximum differential output is 2 V_{PP}. This is shown for the case of a 2 V_{PP} input sine wave which for a gain of 2 V/V in unclamped operation would provide single ended outputs at +OUT and -OUT of 2 V_{PP} but is shown being clamp limited to 1 V_{PP}.

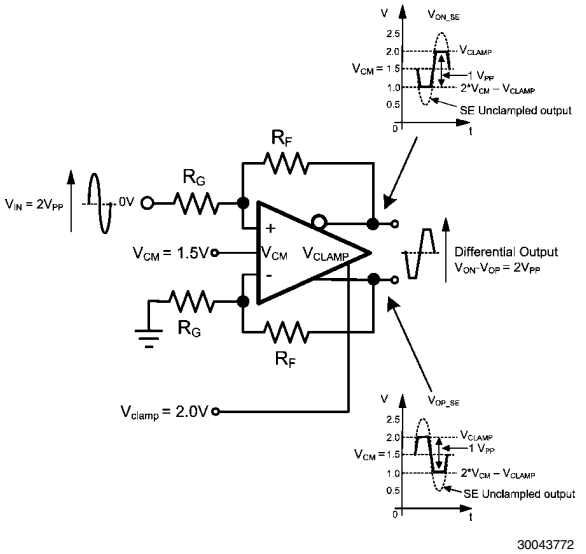


FIGURE 6. Clamp Operation

CLAMP PERFORMANCE

Key clamp performance specifications are listed in the electrical characteristics section. *Figure 7* illustrates the clamp overdrive recovery time which is defined as the difference in input to output propagation delay due to a step change at the input for a clamped output versus a normal linear unclamped, non-saturated output.

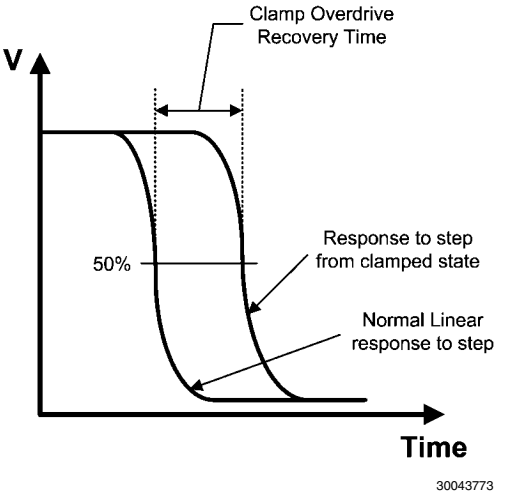


FIGURE 7. Clamp Overdrive Recovery Time

MAXIMUM OUTPUT LEVEL

The maximum unclamped output swing in normal operation is $4V_{PP}$ single ended or 8 V_{PP} differential due to the requirement that $V_{CLAMP} < V_{CM} + 2.0V$. For split supply operation of +5V and –5V, the maximum output voltage is limited by the output stage's ability to swing close to either supply ($V_{OUT} < \pm 3.7V$). As shown in *Figure 8*, if V_{CLAMP} is set > 3.7V, the amplifier output will saturate at the positive supply before the clamp can operate and similarly if $2*V_{CM} - V_{CLAMP} < -3.7V$, the amplifier output will saturate at the negative supply.

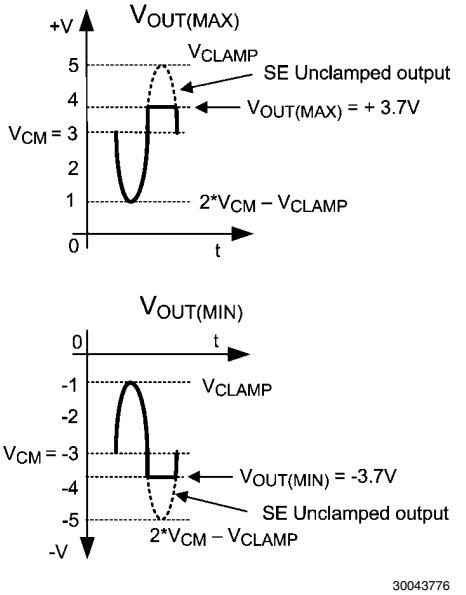


FIGURE 8. Split Supply $V_{OUT(MAX)}$ and $V_{OUT(MIN)}$ Output Levels

OUTPUT NOISE PERFORMANCE AND MEASUREMENT

Unlike differential amplifiers based on voltage feedback architectures, noise sources internal to the LMH6553 refer to the inputs largely as current sources, hence the low input referred voltage noise and relatively higher input referred current noise. The output noise is therefore more strongly coupled to the value of the feedback resistor and not to the closed loop gain, as would be the case with a voltage feedback differential amplifier. This allows operation of the LMH6553 at much higher gain without incurring a substantial noise performance penalty, simply by choosing a suitable feedback resistor.

Figure 9 shows a circuit configuration used to measure noise figure for the LMH6553 in a 50Ω system. An R_F value of 275Ω is chosen for the PSOP package to minimize output noise while simultaneously allowing both high gain (9 V/V) and proper 50Ω input termination. Refer to the section titled Single-Ended Input Operation for calculation of resistor and gain values. Noise figure values at various frequencies are shown in the plot titled Noise Figure in the Typical Performance Characteristics section.

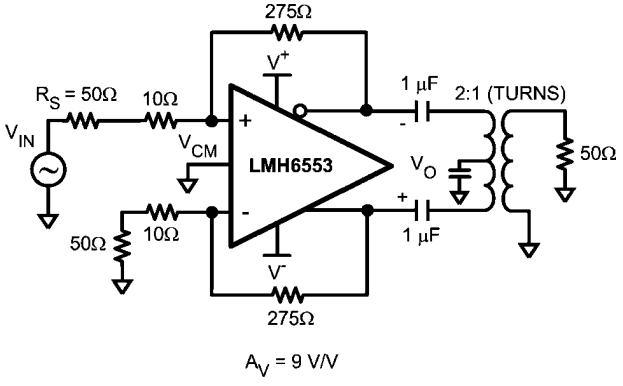


FIGURE 9. Noise Figure Circuit Configuration

DRIVING ANALOG TO DIGITAL CONVERTERS

Analog-to-digital converters present challenging load conditions. They typically have high impedance inputs with large and often variable capacitive components. As well, there are usually current spikes associated with switched capacitor or sample and hold circuits. *Figure 10* shows the LMH6553 driving the ADC14C105. The amplifier is configured to provide a gain of 2 V/V in a single-to-differential mode. The LMH6553 common mode voltage is set by the ADC14C105. The 0.1 µF capacitor, in series with the 49.9Ω resistor, is inserted to ground across the 68.1Ω resistor to balance the amplifier inputs. The circuit in *Figure 10* has a 2nd order lowpass LC filter formed by the 620 nH inductors along with the 22 pF capacitor across the differential inputs of the ADC14C105. The filter has a pole frequency of about 50 MHz. The two 100Ω resistors serve to isolate the capacitive loading of the ADC from the amplifier and ensure stability. For switched capacitor input ADCs, the input capacitance will vary based on the clock cycle, as the ADC switches between the sample and hold mode. See your particular ADC's datasheet for details.

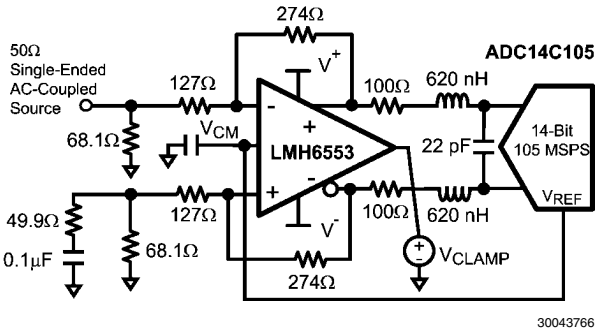


FIGURE 10. Driving a 14-bit ADC

Figure 11 shows the SFDR and SNR performance vs. frequency for the LMH6553 and ADC14C105 combination circuit with the ADC input signal level at −1 dBFS. The ADC14C105 is a single channel 14-bit ADC with maximum sampling rate of 105 MSPS. The amplifier is configured to provide a gain of 2 V/V in single to differential mode. An external bandpass filter is inserted in series between the input signal source and the amplifier to reduce harmonics and noise from the signal generator. In order to properly match the input impedance seen at the LMH6553 amplifier inputs, R_M is chosen to match Z_S || R_T for proper input balance.

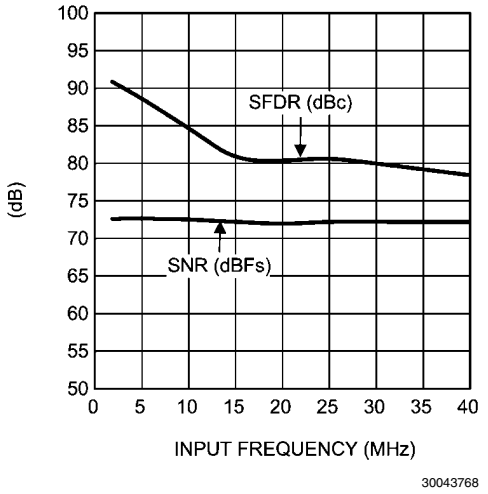


FIGURE 11. LMH6553/ADC14C105 SFDR and SNR Performance vs. Frequency

The amplifier and ADC should be located as close together as possible. Both devices require that the filter components be in close proximity to them. The amplifier needs to have minimal parasitic loading on it's outputs and the ADC is sensitive to high frequency noise that may couple in on its inputs. Some high performance ADCs have an input stage that has a bandwidth of several times its sample rate. The sampling process results in all input signals presented to the input stage mixing down into the first Nyquist zone (DC to Fs/2).

The LMH6553 is capable of driving a variety of National Semiconductor Analog-to-Digital Converters. This is shown in Table 3, which offers a list of possible signal path ADC and amplifier combinations. The use of the LMH6553 to drive an ADC is determined by the application and the desired sampling process (Nyquist operation, sub-sampling or over-sampling). See application note AN-236 for more details on the sampling processes and application note AN-1393 'Using

High Speed Differential Amplifiers to Drive ADCs. For more information regarding a particular ADC, refer to the particular ADC datasheet for details.

TABLE 3. DIFFERENTIAL INPUT ADCs COMPATIBLE WITH LMH6553 DRIVER

Product Number	Max Sampling Rate (MSPS)	Resolution	Channels
ADC1173	15	8	SINGLE
ADC1175	20	8	SINGLE
ADC08351	42	8	SINGLE
ADC1175-50	50	8	SINGLE
ADC08060	60	8	SINGLE
ADC08L060	60	8	SINGLE
ADC08100	100	8	SINGLE
ADC08200	200	8	SINGLE
ADC08500	500	8	SINGLE
ADC081000	1000	8	SINGLE
ADC08D1000	1000	8	DUAL
ADC10321	20	10	SINGLE
ADC10D020	20	10	DUAL
ADC10030	27	10	SINGLE
ADC10040	40	10	DUAL
ADC10065	65	10	SINGLE
ADC10DL065	65	10	DUAL
ADC10080	80	10	SINGLE
ADC11DL066	66	11	DUAL
ADC11L066	66	11	SINGLE
ADC11C125	125	11	SINGLE
ADC11C170	170	11	SINGLE
ADC12010	10	12	SINGLE
ADC12020	20	12	SINGLE
ADC12040	40	12	SINGLE
ADC12D040	40	12	DUAL
ADC12DL040	40	12	DUAL
ADC12DL065	65	12	DUAL
ADC12DL066	66	12	DUAL
ADC12L063	63	12	SINGLE
ADC12C080	80	12	SINGLE
ADC12DS080	80	12	DUAL
ADC12L080	80	12	SINGLE
ADC12C105	105	12	SINGLE
ADC12DS105	105	12	DUAL
ADC12C170	170	12	SINGLE
ADC14L020	20	14	SINGLE
ADC14L040	40	14	SINGLE
ADC14C080	80	14	SINGLE
ADC14DS080	80	14	DUAL
ADC14C105	105	14	SINGLE
ADC14DS105	105	14	DUAL
ADC14155	155	14	SINGLE

DRIVING CAPACITIVE LOADS

As noted previously, capacitive loads should be isolated from the amplifier outputs with small valued resistors. This is particularly the case when the load has a resistive component that is 500Ω or higher. A typical ADC has capacitive components of around 10 pF and the resistive component could be 1000Ω or higher. If driving a transmission line, such as 50Ω coaxial or 100Ω twisted pair, using matching resistors will be sufficient to isolate any subsequent capacitance. For other applications see the Suggested R_{OUT} vs. Capacitive Load charts in the Typical Performance Characteristics section.

BALANCED CABLE DRIVER

With up to 8 V_{PP} differential output voltage swing and 100 mA of linear drive current the LMH6553 makes an excellent cable driver as shown in *Figure 12*. The LMH6553 is also suitable for driving differential cables from a single ended source.

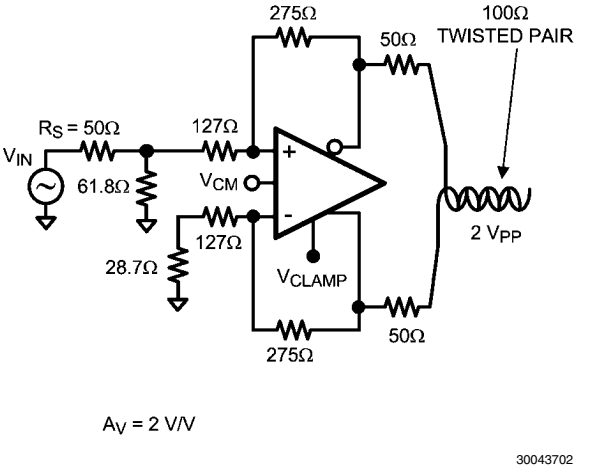


FIGURE 12. Fully Differential Cable Driver

POWER SUPPLY BYPASSING

The LMH6553 requires supply bypassing capacitors as shown in *Figure 13* and *Figure 14*. The 0.01 µF and 0.1 µF capacitors should be leadless SMT ceramic capacitors and should be no more than 3 mm from the supply pins. These capacitors should be star routed with a dedicated ground return plane or trace for best harmonic distortion performance. A small capacitor, ~0.01 µF, placed across the supply rails, and as close to the chip's supply pins as possible, can further improve HD2 performance. Narrow traces or small vias will reduce the effectiveness of bypass capacitors. Also shown in both figures is a capacitor from the V_{CM} and V_{CLAMP} pins to ground. These inputs are high impedance and can provide a coupling path into the amplifier for external noise sources, possibly resulting in loss of dynamic range, degraded CMRR, degraded balance and higher distortion.

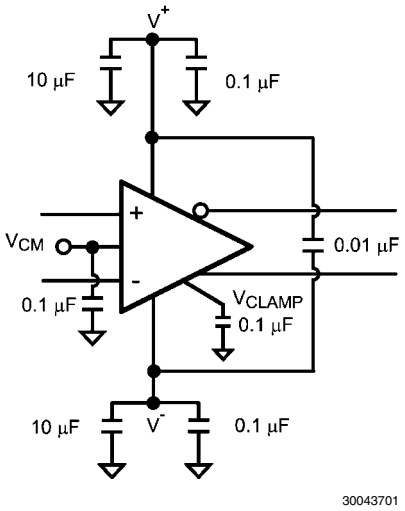


FIGURE 13. Split Supply Bypassing Capacitors

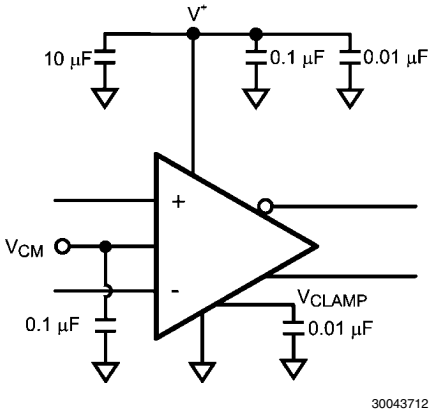


FIGURE 14. Single Supply Bypassing Capacitors

POWER DISSIPATION

The LMH6553 is optimized for maximum speed and performance in the small form factor of the standard LLP package. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} of 150°C is never exceeded.

Follow these steps to determine the maximum power dissipation for the LMH6553:

1. Calculate the quiescent (no-load) power: $P_{AMP} = I_{CC}^* V_S$, where $V_S = V^+ - V^-$. (Be sure to include any current through the feedback network if V_{CM} is not mid-rail.)
2. Calculate the RMS power dissipated in each of the output stages: P_D (rms) = rms $((V_S - V^+_{OUT}) * I^+_{OUT})$ + rms $((V_S - V^-_{OUT}) * I^-_{OUT})$, where V_{OUT} and I_{OUT} are the voltage and the current measured at the output pins of the differential amplifier as if they were single ended amplifiers and V_S is the total supply voltage.
3. Calculate the total RMS power: $P_T = P_{AMP} + P_D$.

The maximum power that the LMH6553 package can dissipate at a given temperature can be derived with the following equation:

$P_{MAX} = (150° - T_{AMB})/\theta_{JA}$, where T_{AMB} = Ambient temperature (°C) and θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W). For the PSOP package θ_{JA} is 59°C/W; LLP package θ_{JA} is 58°C/W.

NOTE: If V_{CM} is not mid-rail, then there will be quiescent current flowing in the feedback network. This current should be included in the thermal calculations and added into the quiescent power dissipation of the amplifier.

THERMAL PERFORMANCE

The LMH6553 is available in both the PSOP and LLP packages. Both packages are designed for enhanced thermal performance and features an exposed die attach pad (DAP) at the bottom center of the package that creates a direct path to the PCB for maximum power dissipation. The DAP is floating and is not electrically connected to internal circuitry.

The thermal advantage of the two packages is fully realized only when the exposed die attach pad is soldered down to a thermal land on the PCB board with thermal vias planted underneath the thermal land. The thermal land can be connected to any power or ground plane within the allowable supply voltage range of the device. The junction-to-ambient thermal resistance (θ_{JA}) of the LMH6553 can be significantly lowered, as opposed to an alternative with no direct soldering to a thermal land. Based on thermal analysis of the LLP package, the junction-to-ambient thermal resistance (θ_{JA}) can be improved by a factor of two when the die attach pad of the LLP package is soldered directly onto the PCB with thermal land and thermal vias are 1.27 mm and 0.33 mm respectively. Typical copper via barrel plating is 1 oz, although thicker copper may be used to further improve thermal performance.

For more information on board layout techniques for the LLP package, refer to Application Note 1187 “Leadless Lead Frame Package (LLP).” This application note also discusses package handling, solder stencil and the assembly process.

ESD PROTECTION

The LMH6553 is protected against electrostatic discharge (ESD) on all pins. The LMH6553 will survive 4000V Human Body model and 350V Machine model events. Under normal operation the ESD diodes have no effect on circuit performance. The current that flows through the ESD diodes will either exit the chip through the supply pins or through the device, hence it is possible to power up a chip with a large signal applied to the input pins.

BOARD LAYOUT

The LMH6553 is a very high performance amplifier. In order to get maximum benefit from the differential circuit architecture, board layout and component selection are very critical. The circuit board should have a low inductance ground plane and well bypassed wide supply lines. External components should be leadless surface mount types. The feedback network and output matching resistors should be composed of short traces and precision resistors (0.1%). The output matching resistors should be placed within 3 or 4 mm of the amplifier as should the supply bypass capacitors. Refer to the section titled Power Supply Bypassing for recommendations on bypass circuit layout. Evaluation boards are available free of charge through the product folder on National’s web site.

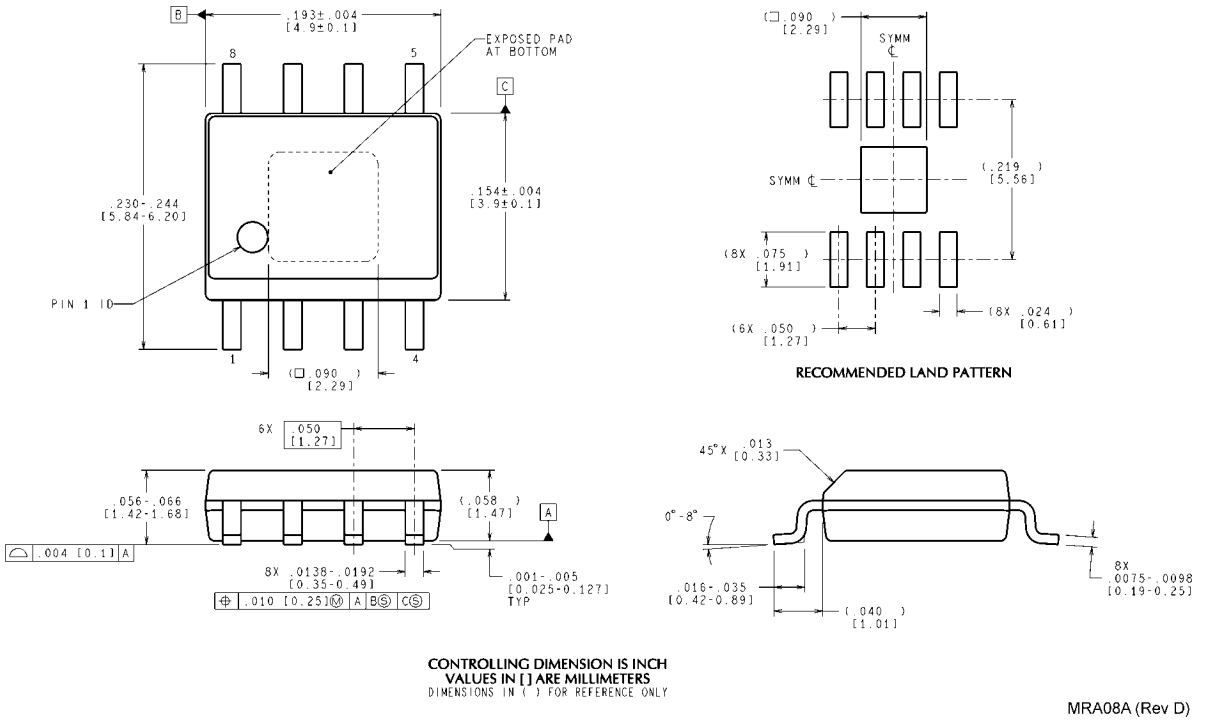
By design, the LMH6553 is relatively insensitive to parasitic capacitance at its inputs. Nonetheless, ground and power plane metal should be removed from beneath the amplifier and from beneath R_F and R_G for best performance at high frequency.

With any differential signal path, symmetry is very important. Even small amounts of asymmetry can contribute to distortion and balance errors.

EVALUATION BOARD

See the LMH6553 Product Folder on www.national.com for evaluation board availability and ordering information.

Physical Dimensions inches (millimeters) unless otherwise noted



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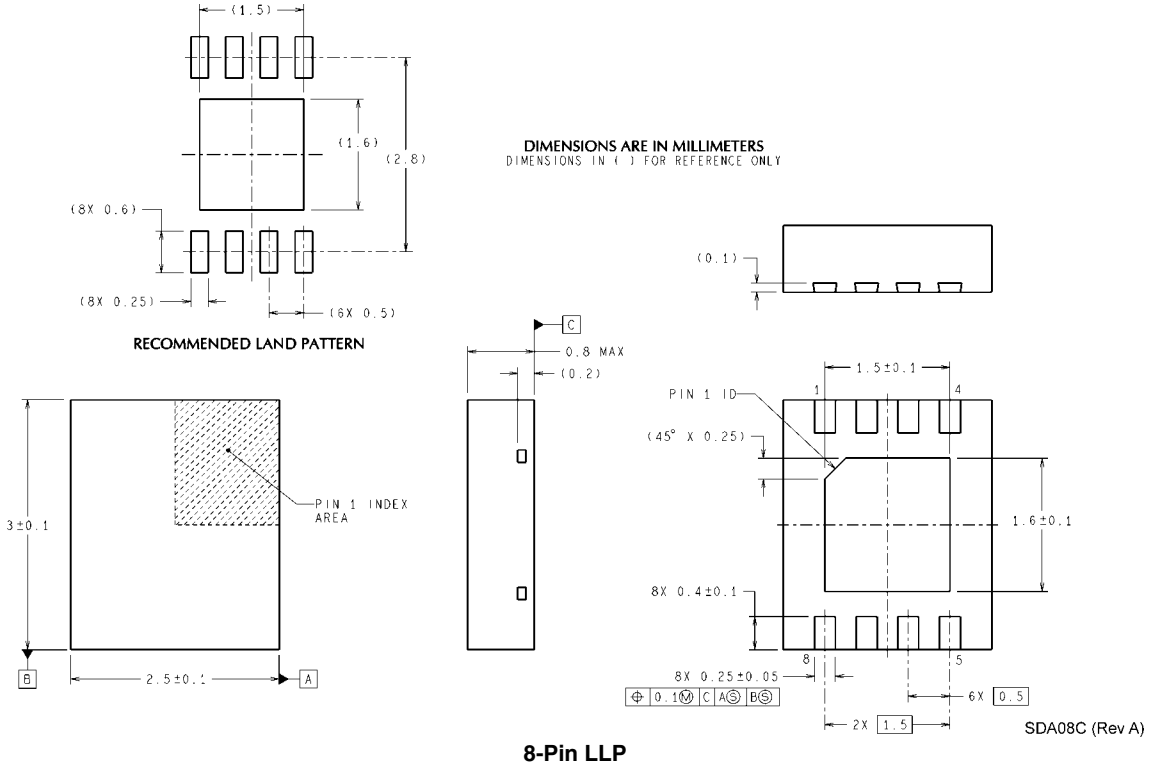
MRA08A (Rev D)

8-Pin PSOP
NS Package Number MRA08A



SDA08C (Rev A)

8-Pin LLP
NS Package Number SDA08C

Notes

Notes

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LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
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