

**128K x 8
64K x 8
CMOS DUAL-PORT
STATIC RAM MODULE**

**PRELIMINARY
IDT7M1001
IDT7M1003**

T-46-23-14

FEATURES

- High density 1M/512K CMOS dual-port static RAM module
- Fast access times:
 - commercial - 25, 30, 35, 40, 50, 65ns
 - military - 35, 40, 50, 65, 80ns
- Fully asynchronous read/write operation from either port
- Full on-chip hardware support of semaphore signaling between ports
- Surface mounted LCC (leadless chip carriers) components on a 64-pin sidebraze DIP (Dual In-line Package)
- Multiple Vcc and GND pins for maximum noise immunity
- Single 5V (±10%) power supply
- Input/outputs directly TTL compatible

DESCRIPTION:

The IDT7M1001/IDT7M1003 is a 128K x 8 /64K x 8 high-speed CMOS dual-port static RAM module constructed on a multilayer ceramic substrate using eight IDT7006 (16K x 8) dual-port RAMs and two IDT FCT138 decoders or depopulated using only four IDT7006s and two decoders.

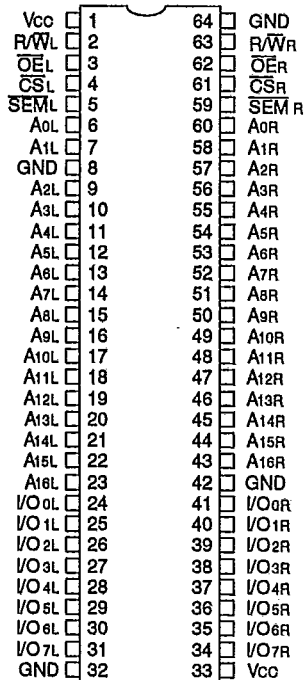
This module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. System performance is enhanced by facilitating port-to-port communication via semaphore (SEM) "handshake" signaling. The IDT7M1001/1003 module is designed to be used as stand-alone dual-port RAM where on-chip hardware port arbitration is not needed. It is the users responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports.

The IDT7M1001/1003 module is packaged on a multilayer co-fired ceramic 64-pin DIP (Dual In-line Package) with dimensions of only 3.2" x 0.62" x 0.38". Maximum access times as fast as 25ns over the commercial temperature range and 35ns over the military temperature range are available.

All inputs and outputs of the IDT7M1001/1003 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation of the module.

All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION(1)



DIP
TOP VIEW

2804 drw 01

NOTE:

1. For the IDT7M1003 (64K x 8) version, Pins 23 & 43 must be connected to GND for proper operation of the module.

PIN NAMES

Left Port	Right Port	Description
A (0-16)L	A (0-16)R	Address Inputs
I/O (0-7)L	I/O (0-7)R	Data Inputs/Outputs
R/WL	R/WR	Read/Write Enables
CSL	CSR	Chip Select
OEL	OER	Output Enable
SEML	SEMR	Semaphore Control
Vcc		Power
GND		Ground

2804 tbl 01

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

APRIL 1992

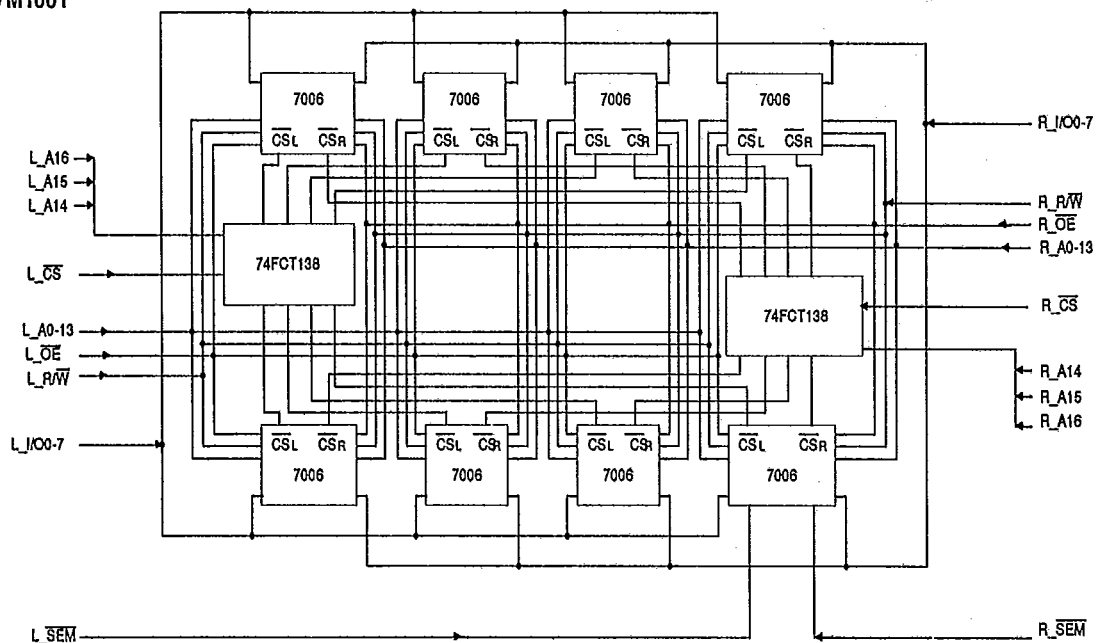
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DSC-70053

FUNCTIONAL BLOCK DIAGRAM

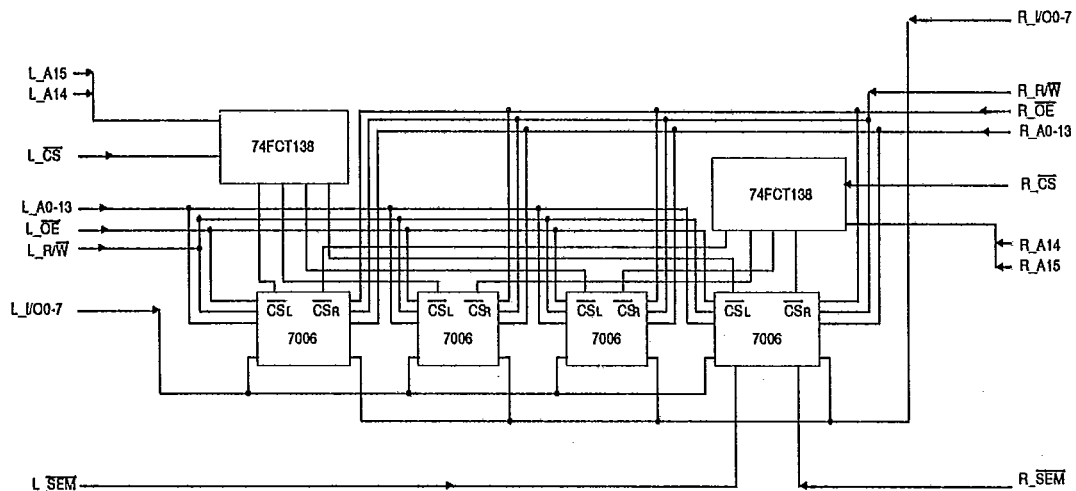
T-46-23-14

7M1001



2804 drw 02

7M1003



2804 drw 03



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2804 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE⁽¹⁾ (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Test Conditions	Max.	Unit
CIN1	Input Capacitance (CS or SEM)	VIN = 0V	15	pF
CIN2	Input Capacitance (Data, Address, All Other Controls)	VIN = 0V	100	pF
COU	Output Capacitance (Data)	VOUT = 0V	100	pF

2804 tbl 03

NOTE:
1. This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2804 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	-	6.0	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	-	0.8	V

2804 tbl 05

NOTE:
1. VIL (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

(Vcc = 5V ± 10%, TA = -55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Commercial			Military			Unit
			Min.	Max. ⁽¹⁾	Max. ⁽²⁾	Min.	Max. ⁽¹⁾	Max. ⁽²⁾	
Icc2	Dynamic Operating Current (Both Ports Active)	Vcc = Max., CS ≤ VIL, SEM ≥ VIH Outputs Open, f = fMAX	—	940	660	—	1130	790	mA
Icc1	Standby Supply Current (One Port Active)	Vcc = Max., L_CS or R_CS ≥ VIH Outputs Open, f = fMAX	—	750	470	—	905	565	mA
ISB1	Standby Supply Current (TTL Levels)	Vcc = Max., L_CS and R_CS ≥ VIH Outputs Open, f = fMAX L_SEM and R_SEM ≥ Vcc - 0.2V	—	565	285	—	685	345	mA
ISB2	Full Standby Supply Current (CMOS Levels)	L_CS and R_CS ≥ Vcc - 0.2V VIN > Vcc 0.2V or < 0.2V L_SEM and R_SEM ≥ Vcc - 0.2V	—	125	65	—	245	125	mA

2804 tbl 06

NOTES:
1. IDT7M1001 (128K x 8) version only.
2. IDT7M1003 (64K x 8) version only.

DC ELECTRICAL CHARACTERISTICS

T-46-23-14

(Vcc=5.0V ± 10%, TA = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7M1001		IDT7M1003		Unit
			Min.	Max.	Min.	Max.	
ILI	Input Leakage (Address, Data & Other Controls)	Vcc = Max. VIN = GND to Vcc	—	80	—	40	μA
LI	Input Leakage (CS and SEM)	Vcc = Max. VIN = GND to Vcc	—	10	—	10	μA
ILO	Output Leakage (Data)	Vcc = Max. CS ≥ VIH, VOUT = GND to Vcc	—	80	—	40	μA
VOL	Output Low Voltage	Vcc = Min. IOL = 4mA	—	0.4	—	0.4	V
VOH	Output High Voltage	Vcc = Min. IOH = -4mA	2.4	—	2.4	—	V

2804 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2804 tbl 08

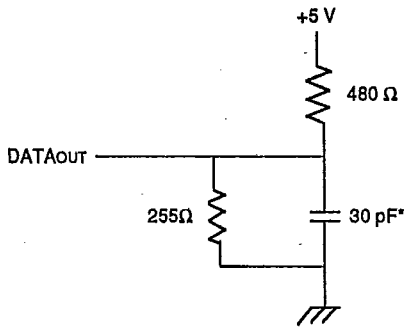


Figure 1. Output Load

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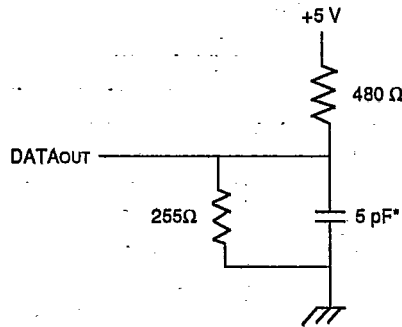


Figure 2. Output Load
(for tCLZ, tCHZ, tOLZ, tOHZ, tWHZ, tOW)

2804 drw 05

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

T-46-23-14

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	-25 ⁽⁶⁾		-30 ⁽⁶⁾		-35 ⁽⁶⁾		-40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t _{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	ns
t _{AA}	Address Access Time	—	25	—	30	—	35	—	40	ns
t _{ACS} ⁽²⁾	Chip Select Access Time	—	25	—	30	—	35	—	40	ns
t _{OE}	Output Enable Access Time	—	13	—	15	—	20	—	25	ns
t _{OH}	Output Hold From Address Change	3	—	3	—	3	—	3	—	ns
t _{CLZ} ⁽¹⁾	Chip Select to Output In Low Z	3	—	3	—	3	—	3	—	ns
t _{CHZ} ⁽¹⁾	Chip Deselect to Output In High Z	—	18	—	20	—	20	—	20	ns
t _{OLZ} ⁽¹⁾	Output Enable to Output In Low Z	3	—	3	—	3	—	3	—	ns
t _{OHZ} ⁽¹⁾	Output Disable to Output In High Z	—	18	—	20	—	20	—	20	ns
t _{PU} ⁽¹⁾	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t _{PD} ⁽¹⁾	Chip Disable to Power Down Time	—	50	—	50	—	50	—	50	ns
t _{SCP}	SEM Flag Update Pulse (OE or SEM)	12	—	12	—	15	—	15	—	ns
Write Cycle										
t _{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	ns
t _{EW} ⁽²⁾	Chip Select to End of Write	20	—	25	—	30	—	35	—	ns
t _{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	ns
t _{AS1} ⁽³⁾	Address Set-up to Write Pulse Time	5	—	5	—	5	—	5	—	ns
t _{AS2}	Address Set-up to CS Time	0	—	0	—	0	—	0	—	ns
t _{WP}	Write Pulse Width	20	—	25	—	30	—	35	—	ns
t _{WR} ⁽⁴⁾	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t _{DW}	Data Valid to End of Write	15	—	20	—	25	—	30	—	ns
t _{DH} ⁽⁴⁾	Data Hold Time	0	—	0	—	0	—	0	—	ns
t _{OHZ} ⁽¹⁾	Output Disable to Output In High Z	—	18	—	20	—	20	—	20	ns
t _{WHZ} ⁽¹⁾	Write Enable to Output In High Z	—	18	—	20	—	20	—	20	ns
t _{OW} ^(1, 4)	Output Active from End of Write	0	—	0	—	0	—	0	—	ns
t _{SWRD}	SEM Flag Write to Read Time	10	—	13	—	15	—	15	—	ns
t _{SPS}	SEM Flag Contention Window	10	—	13	—	15	—	15	—	ns
Port-to-Port Delay Timing										
t _{WDD} ⁽⁶⁾	Write Pulse to Data Delay	—	50	—	55	—	60	—	65	ns
t _{DD} ⁽⁶⁾	Write Data Valid to Read Data Valid	—	35	—	40	—	45	—	50	ns

NOTES:

2804 tbl 09

1. This parameter is guaranteed by design but not tested.
2. To access RAM $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. t_{AS1} = 0 if R/W is asserted low simultaneously with or after the \overline{CS} low transition.
4. For CS controlled write cycles, t_{WA} = 5ns, t_{DH} = 5ns, t_{OW} = 5ns.
5. Preliminary specifications only.
6. Port-to-Port delay through the RAM cells from the writing port to the reading port.

AC ELECTRICAL CHARACTERISTICS

T-46-23-14

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	-50		-65		-80		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t _{RC}	Read Cycle Time	50	—	65	—	80	—	ns
t _{AA}	Address Access Time	—	50	—	65	—	80	ns
t _{ACS} ⁽²⁾	Chip Select Access Time	—	50	—	65	—	80	ns
t _{OE}	Output Enable Access Time	—	30	—	35	—	40	ns
t _{OH}	Output Hold From Address Change	3	—	3	—	3	—	ns
t _{OLZ} ⁽¹⁾	Chip Select to Output in Low Z	3	—	3	—	3	—	ns
t _{OHZ} ⁽¹⁾	Chip Deselect to Output in High Z	—	25	—	30	—	35	ns
t _{OLZ} ⁽¹⁾	Output Enable to Output in Low Z	3	—	3	—	3	—	ns
t _{OHZ} ⁽¹⁾	Output Disable to Output in High Z	—	25	—	30	—	35	ns
t _{PU} ⁽¹⁾	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t _{PD} ⁽¹⁾	Chip Disable to Power Down Time	—	50	—	50	—	50	ns
t _{SOP}	SEM Flag Update Pulse (OE or SEM)	15	—	20	—	20	—	ns
Write Cycle								
t _{WC}	Write Cycle Time	50	—	65	—	80	—	ns
t _{EW} ⁽²⁾	Chip Select to End of Write	40	—	50	—	55	—	ns
t _{AW}	Address Valid to End of Write	40	—	50	—	55	—	ns
t _{AS1} ⁽³⁾	Address Set-up to Write Pulse Time	5	—	5	—	5	—	ns
t _{AS2}	Address Set-up to CS Time	0	—	0	—	0	—	ns
t _{WP}	Write Pulse Width	40	—	45	—	50	—	ns
t _{WR} ⁽⁴⁾	Write Recovery Time	0	—	0	—	0	—	ns
t _{DW}	Data Valid to End of Write	35	—	40	—	45	—	ns
t _{DH} ⁽⁴⁾	Data Hold Time	0	—	0	—	0	—	ns
t _{OZH} ⁽¹⁾	Output Disable to Output in High Z	—	25	—	30	—	35	ns
t _{WHZ} ⁽¹⁾	Write Enable to Output in High Z	—	25	—	30	—	35	ns
t _{OW} ^(1,4)	Output Active from End of Write	0	—	0	—	0	—	ns
t _{SWRD}	SEM Flag Write to Read Time	15	—	15	—	15	—	ns
t _{SPS}	SEM Flag Contention Window	15	—	15	—	15	—	ns
Port-to-Port Delay Timing								
t _{WDD} ⁽⁵⁾	Write Pulse to Data Delay	—	70	—	85	—	95	ns
t _{DDD} ⁽⁵⁾	Write Data Valid to Read Data Valid	—	55	—	70	—	80	ns

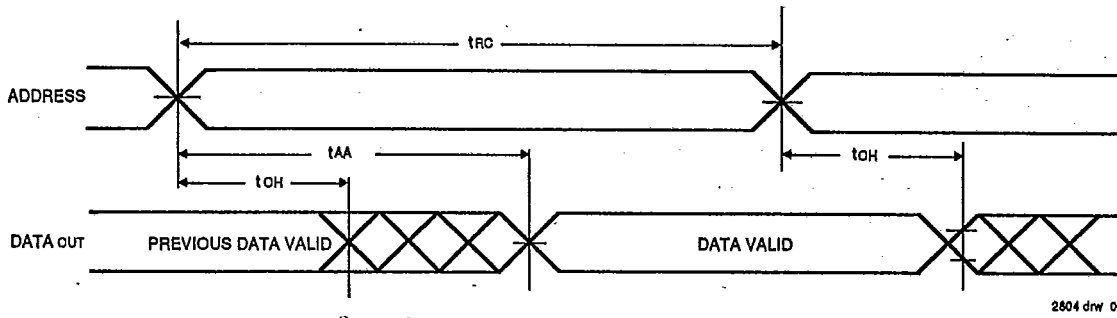


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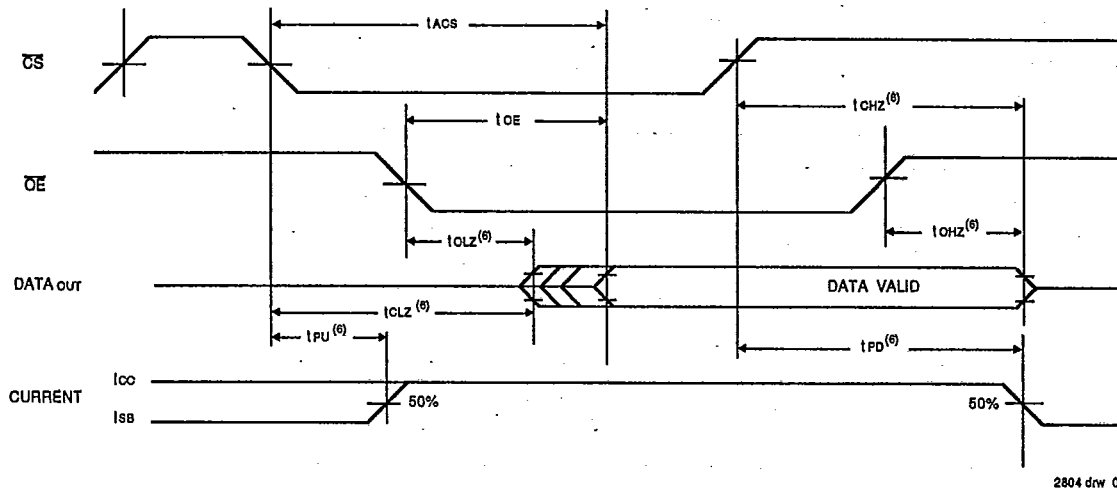
1. This parameter is guaranteed by design but not tested.
2. To access RAM CS ≤ V_{IL} and SEM ≥ V_{IH}. To access semaphore, CS ≥ V_{IH} and SEM ≤ V_{IL}.
3. t_{AS1} = 0 if R/W is asserted low simultaneously with or after the CS low transition.
4. For CS controlled write cycles, t_{WR} = 5ns, t_{DH} = 5ns, t_{OW} = 5ns.
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.

TIMING WAVEFORM OF READ CYCLE NO. 1 (EITHER SIDE)^(1,2,4)

T-46-23-14



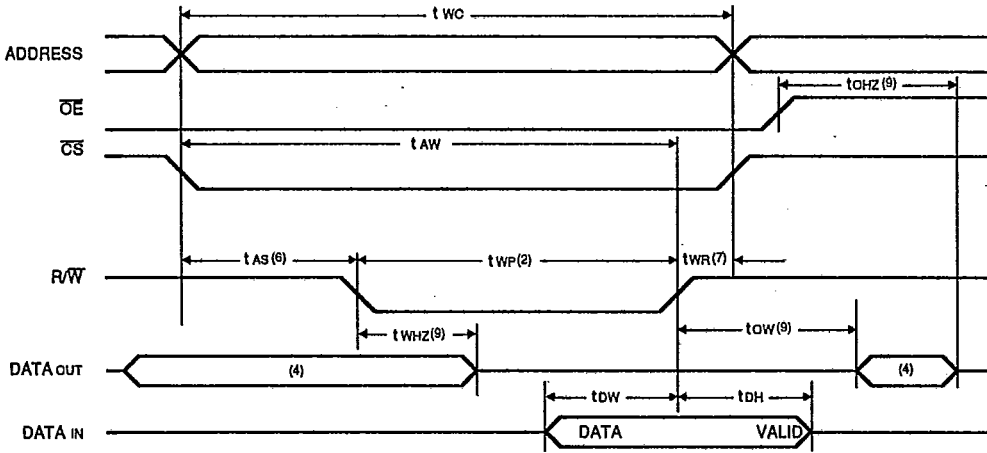
TIMING WAVEFORM OF READ CYCLE NO. 2 (EITHER SIDE)^(1,3,5)



NOTES:

1. $\overline{R/\overline{W}}$ is High for Read Cycles
2. Device is continuously enabled. $\overline{CS} = \text{Low}$. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with \overline{CS} transition low.
4. $\overline{OE} = \text{Low}$.
5. To access RAM, $\overline{CS} = \text{Low}$, $\overline{SEM} = \text{H}$. To access semaphore, $\overline{CS} = \text{H}$ and $\overline{SEM} = \text{Low}$.
6. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/W CONTROLLED TIMING)^(1,3,5,8)

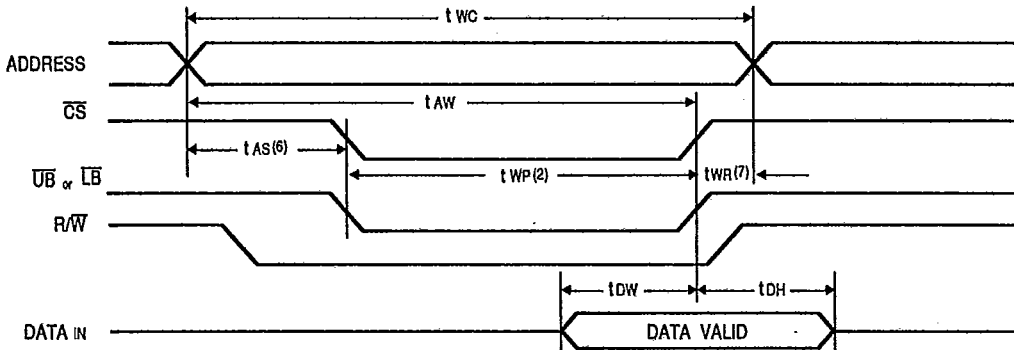


NOTES:

1. R/W is High for Read Cycles
2. Device is continuously enabled. CS = Low, UB or LB = Low. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with CS transition low.
4. OE = Low.
5. To access RAM, CS = Low, UB or LB = Low, SEM = H. To access semaphore, CS = H and SEM = Low.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If OE is Low during a R/W controlled write cycle, the write pulse width must be larger of tWP or (tWZ + tOW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If OE is High during a R/W controlled write cycle, this requirement does not apply and the write pulse width be as short as the specified tWP.
9. This parameter is guaranteed by design but not tested.

2804 drw 08

TIMING WAVEFORM OF WRITE CYCLE NO. 2 (CS CONTROLLED TIMING)^(1,3,5,8)



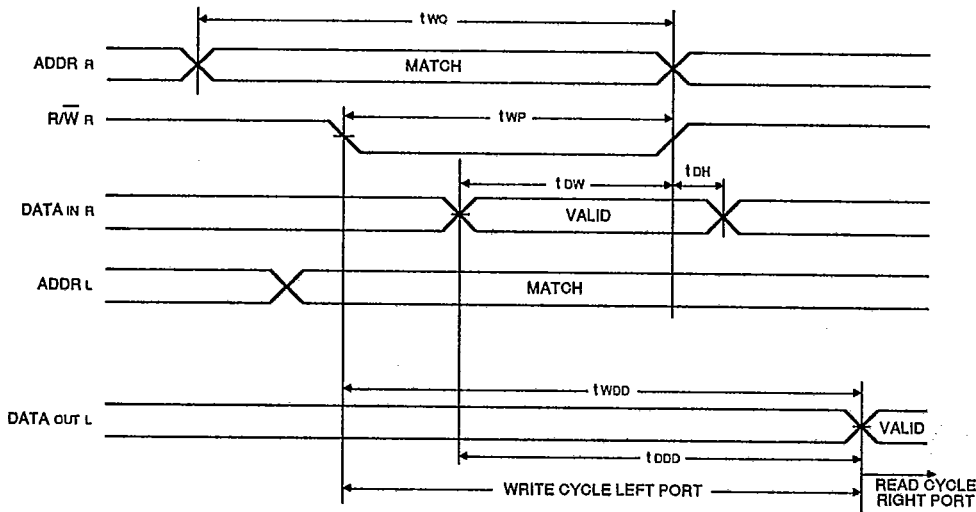
NOTES:

1. R/W must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a Low UB or LB and a Low CS and a Low R/W for memory array writing cycle.
3. tWR is measured from the earlier of CS or R/W (or SEM or R/W) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the CS or SEM low transition occurs simultaneously with or after the R/W low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If OE is low during a R/W controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tOW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If OE is high during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. This parameter is guaranteed by design but not tested.

2804 drw 09

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY⁽¹⁾

T-46-23-14



NOTE:
1. $L_{CS} = R_{CS} = \text{Low}$

2804 drw 12

TRUTH TABLES

TABLE I: NON-CONTENTION READ/WRITE CONTROL⁽¹⁾

Inputs ⁽¹⁾				Outputs	Mode
\overline{CS}	R/W	\overline{OE}	SEM	I/O ₀ - I/O ₇	
H	X	X	H	Hi-Z	Deselected: Power Down
L	L	X	H	DATAIN	Write to Both Bytes
L	H	L	H	DATAOUT	Read Both Bytes
X	X	H	X	Hi-Z	Outputs Disabled

NOTE:
1. A_{0L} — A₁₂ ≠ A_{0R} — A_{12R}

2804 tbl 11

TABLE II: SEMAPHORE READ/WRITE CONTROL⁽¹⁾

Inputs				Outputs	Mode
\overline{CS}	R/W	\overline{OE}	SEM	I/O ₀ - I/O ₇	
H	H	L	L	DATAOUT	Read Data in Semaphore Flag
X		X	L	DATAIN	Write Data into Semaphore Flag
L	X	X	L	—	Not Allowed

NOTE:
1. A_{0L} — A₁₂ ≠ A_{0R} — A_{12R}

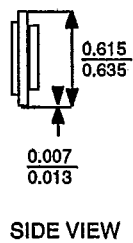
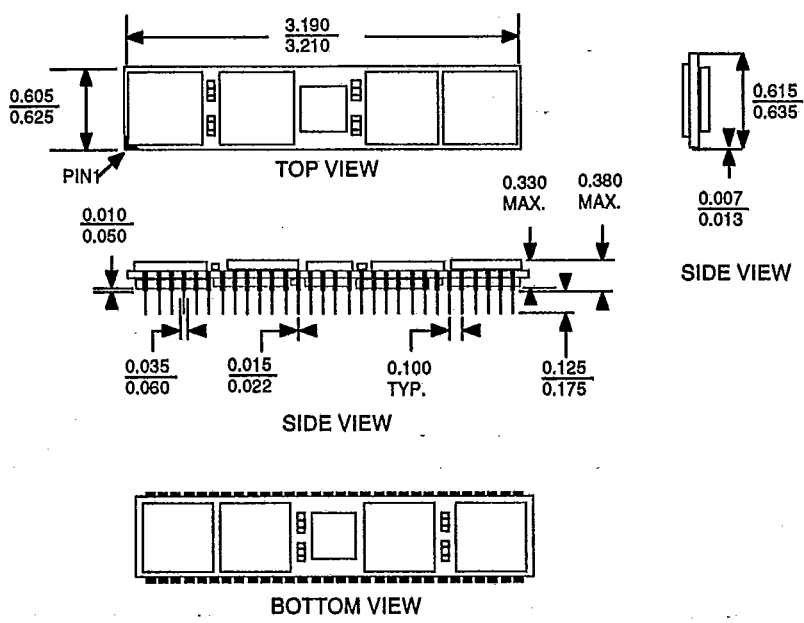
2804 tbl 12

SEMAPHORE OPERATION

For more details regarding semaphores & semaphore operations, please consult the IDT7006 datasheet.

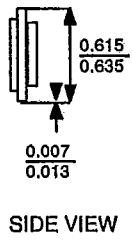
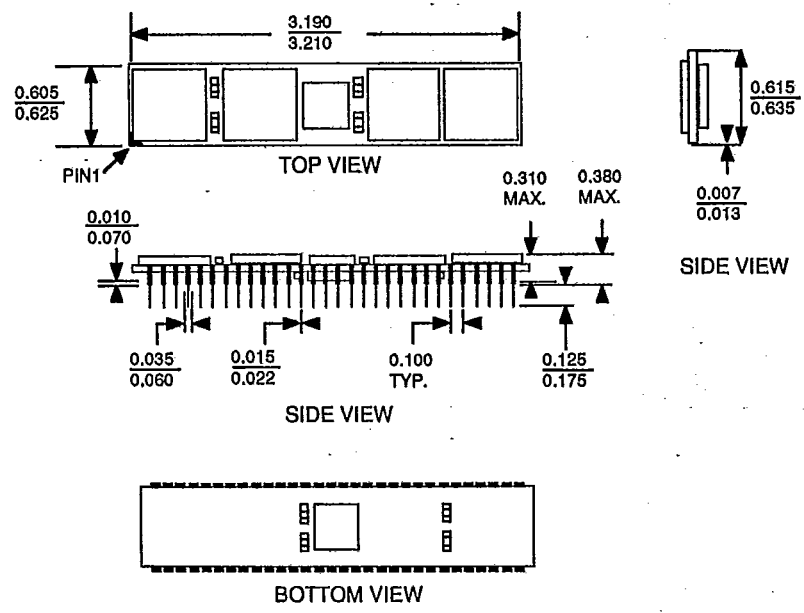
PACKAGE DIMENSIONS
7M1001

T-46-23-14



2804 drw 13

7M1003



2804 drw 14