MICRO NETWORKS

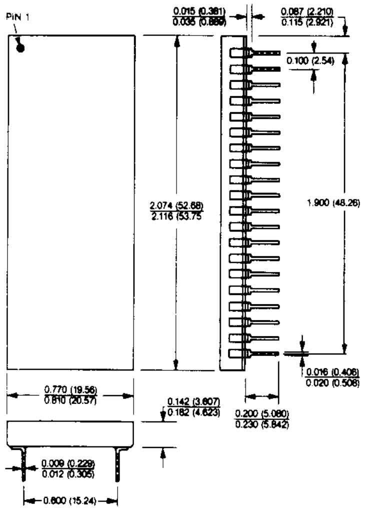
MN5249

400nsec, 12-Bit
A/D CONVERTER

FEATURES

- 400nsec Maximum Conversion Time
- Guaranteed 2.5MHz Conversion Rate
- 2MHz Sampling Rate When Used with MN376 T/H Amplifier
- No Missing Codes Guaranteed Ov Temperature
- Small 40-Pin DIP
- ±2.5 Watt Power Consumption
- TTL Compatible
- 3-State Output Buffer
- MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility

40 PIN DIP



Dimensions in Inches
(millimeters)

DESCRIPTION

MN5249 is a 400nsec, 12-bit A/D converter that guarantees 2.5MHz conversion rates. When used with MN376 high-speed T/H amplifiers, these A/D's can be configured to form bonafide, 2MHz, sample-and-convert systems that can digitize full-scale (5V) input signals with bandwidths up to 1MHz. These systems typically achieve signal-to-noise ratios of 70dB with harmonics down more than −80dB while digitizing 1MHz signals at the Nyquist rate.

Packaged in a standard, 40-pin, double-wide, hermetically sealed, ceramic dual-in-line, MN5249 offers an outstanding combination of resolution, speed, size and cost. This TTL compatible device achieves its sub-500nsec conversion speed using the digitally corrected subranging (serial-parallel) A/D conversion technique. Recent advances in monolithic flash A/D converters and monolithic DAC's and improvements in digital error correcting techniques have enabled us to reduce chip count over previous designs while improving performance.

MN5249 has a ±2.5V input range and a user-optional, 3-state output buffer to facilitate μP interfacing. A "T/H Control" output line is provided with all the necessary delays for direct T/H control. All models guarantee ±0.024% FSR integral linearity and "no missing codes" for 12 bits over their entire specified temperature range.

MN5249 is an ideal design solution for high-speed digitizing applications in which speed, accuracy, size and reliability are paramount considerations. Typical applications include spectrum, vibration, waveform and transient analyzers; radar, sonar and video digitizers; medical imaging equipment; digital filters; and multiplexed or simultaneous-sampling data acquisition systems.

The MN5249H/B is available with Environmental Stress Screening while the MN5249H/B CH is screened in accordance with MIL-H-38534. Contact the factory for availability of CH device types.

April 1989

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN5249 400nsec 12-Bit A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C (case)
Specified Temperature Range:	
MN5249	0°C to +70°C (case)
MN5249E, MN5249E/B	−25°C to +85°C (case)
MN5249H, MN5249H/B	−55°C to +125°C (case)
Storage Temperature Range	−65°C to +150°C
+15V Supply (+Vcc, Pin 17)	−0.5 to +18 Volts
−15V Supply (−Vcc, Pin 25)	+0.5 to −18 Volts
+5V Supply (+Vdd, Pins 5,29,40)	−0.5 to +7 Volts
−5.2V Supply (−Vdd, Pin 14)	0 to −7 Volts
Digital Inputs (Pins 7, 12)	−0.5 to +5.5 Volts
Analog Input (Pin 22)	−3.5 to +3.5 Volts

ORDERING INFORMATION

PART NUMBER ———— MN5249 H/B CH

Standard Part is specified for 0°C to +70°C operation.

Add "E" suffix for specified −25°C to +85°C (case) operation.

Add "H" suffix for specified −55°C to +125°C (case) operation.

Add "/B" to "H" devices for Environmental Stress Screening.

Add "CH" to "H/B" devices for 100% screening according to MIL-H-38534.

Contact factory for availability of "CH" device types.

SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V, −Vdd = −5.2V unless otherwise indicated)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range		±2.5		Volts
Input Impedance (Note 1)		500//10		Ω//pF
DIGITAL INPUTS (Start Convert, OE)				
Logic Levels: Logic "1" Logic "0"	+2.0		 +0.8	Volts Volts
Logic Currents: Logic "1" (V_{IH} = +2.7) Logic "0" (V_{IL} = +0.4V)			+20 −0.4	μA mA
TRANSFER CHARACTERISTICS (Note 2)				
Integral Linearity Error: Initial (+25°C) Over Temperature (Note 3)		±½ ±½	±1 ±1	LSB LSB
12-Bit No Missing Codes	Guaranteed Over Temperature			
Full Scale Absolute Accuracy Error (Note 4): Initial (+25°C) Over Temperature (Note 3)		±0.05 ±0.1	±0.15 ±0.3	%FSR %FSR
Bipolar Zero Error (Note 5): Initial (+25°C) Over Temperature (Note 3) Drift (Note 3)		±0.05 ±0.1 ±10	±0.1 ±0.2 ±25	%FSR %FSR ppm of FSR/°C
Gain Error (Note 6): Initial (+25°C) Over Temperature (Note 3) Drift (Note 3)		±0.05 ±0.1 ±20	±0.1 ±0.3 ±40	% % ppm/°C
DIGITAL OUTPUTS (Parallel, OR/UR, T/H Control, Status, $\overline{\text{MSB}}$)				
Output Coding (Note 7)	Offset Binary			
Output Logic Levels: Logic "1" ($I_{SOURCE} \leq 100\mu A$) Logic "0" ($I_{SINK} \leq 2mA$)	+2.7		 +0.5	Volts Volts
Leakage (Bit 1 – Bit 12) in High-Z State: Logic "1" (V_{OH} = +2.7V) Logic "0" (V_{OL} = +0.4V)			+10 −10	μA μA
DYNAMIC CHARACTERISTICS				
Conversion Time (Note 8) Conversion Rate (Note 8)	 2.5	375 2.7	400	nsec MHz
Start Convert Pulse Width (Notes 1, 9)	50			nsec
Delay Falling Edge of Start to Status="1" (Note 1) Delay Falling Edge of Start to Previous Output Data Invalid (Note 1) Delay Falling Edge of Start to Falling Edge of T/H Control		45 280 280	 300	nsec nsec nsec
Delay Falling Edge of Status to Output Data Valid (Note 1) Delay Falling Edge of Enable to Output Data Valid (Note 1)			0 50	nsec nsec
REFERENCE OUTPUT				
Internal Reference (Note 1): Voltage Accuracy Drift External Current		+5 ±2 ±10 5		Volts % ppm/°C μA

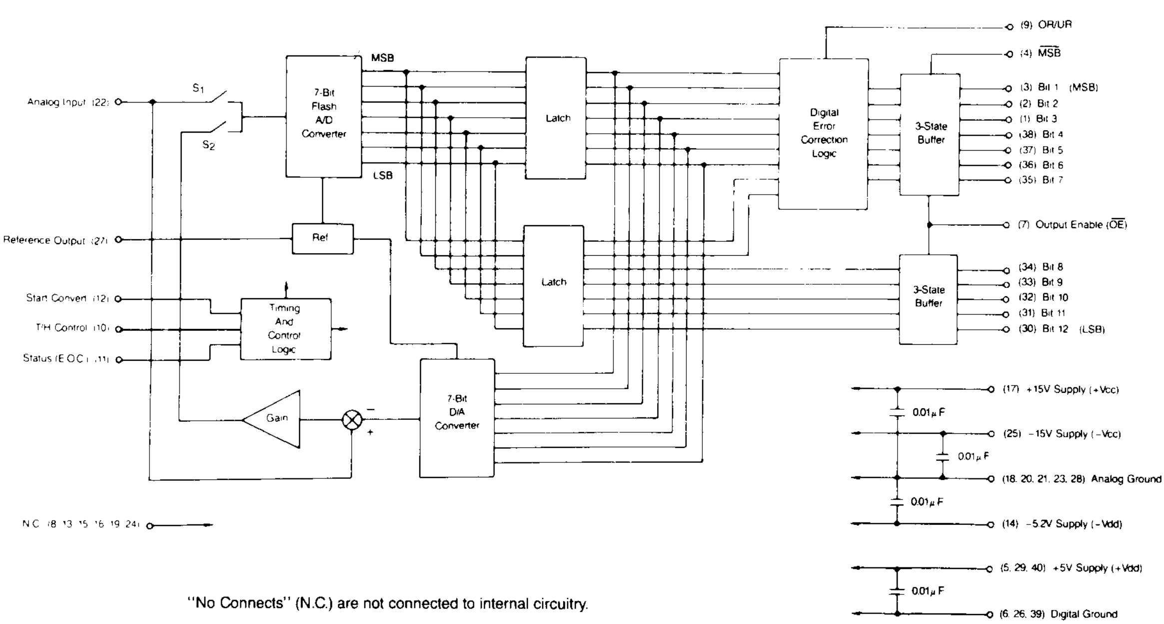
POWER SUPPLIES	MIN.	TYP.	MAX.	UNITS
Power Supply Range: +15V Supply	+14.55	+15	+15.45	Volts
−15V Supply	−14.55	−15	−15.45	Volts
+5V Supply	+4.75	+5	+5.25	Volts
−5.2V Supply	−5	−5.2	−5.4	Volts
Power Supply Rejection (Note 10): +15V Supply	−50	−72		dB
−15V Supply	−50	−66		dB
+5V Supply	−50	−68		dB
−5.2V Supply	−50	−57		dB
Current Drain: +15V Supply		+40	+50	mA
−15V Supply		−64	−75	mA
+5V Supply		+200	+250	mA
−5.2V Supply		−50	+60	mA
Power Consumption		2.82	3.44	Watts

SPECIFICATION NOTES:

1. These parameters are listed for reference only and are not tested.
2. FSR=full scale range, and for the MN5249, FSR=5 Volts. For a 12-bit converter, 1LSB=0.024% FSR.
3. Listed specifications apply over the 0°C to +70°C (case) temperature range for standard product; over the −25°C to +85°C (case) temperature range for MN5249E and MN5249E/B; and over the −55°C to +125°C (case) temperature range for MN5249H and MN5249H/B.
4. Full scale accuracy specifications apply at both positive and negative full scale for bipolar input ranges. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1110 to 1111 1111 1111 and from 0000 0000 0000 to 0000 0000 0001. The former transition ideally occurs at an input voltage 1½LSB's below the nominal positive full scale voltage. The latter ideally occurs ½LSB above the nominal negative full scale voltage. See Digital Output Coding.
5. Bipolar zero error is defined as the difference between the actual and the ideal input voltage at which the 0111 1111 1111 to 1000 0000 0000 transition occurs. The ideal value at which this transition should occur is −½LSB. See Digital Output Coding.
6. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 1111 1111 1111 to 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0001 to 0000 0000 0000. Initial gain error is adjustable to zero with an external potentiometer.
7. See Output Coding table for details.
8. Conversion time is measured from the falling edge of Start Convert to the falling edge of Status (E.O.C.). See Timing Diagram.
9. The rising edge of Start Convert resets internal timing circuits ensuring that the first conversion after "powerup" produces valid output data. The falling edge of Start Convert actually initiates the conversion process.
10. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 or 0000 0000 0000 to 0000 0000 0001 output transitions occur versus a change in power-supply voltage.

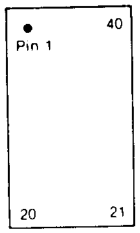
Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

BLOCK DIAGRAM



"No Connects" (N.C.) are not connected to internal circuitry.

PIN DESIGNATIONS



1	Bit 3	40	+5V Supply (+Vdd)
2	Bit 2	39	Digital Ground
3	Bit 1 (MSB)	38	Bit 4
4	$\overline{MSB}$	37	Bit 5
5	+5V Supply (+Vdd)	36	Bit 6
6	Digital Ground	35	Bit 7
7	Output Enable ($\overline{OE}$)	34	Bit 8
8	N.C.	33	Bit 9
9	Over/Underrange (OR/UR)	32	Bit 10
10	T/H Control	31	Bit 11
11	Status (E.O.C.)	30	Bit 12 (LSB)
12	Start Convert	29	+5V Supply (+Vdd)
13	N.C.	28	Analog Ground
14	−5.2V Supply (−Vdd)	27	Reference Output (+5V)
15	N.C.	26	Digital Ground
16	N.C.	25	−15V Supply (−Vcc)
17	+15V Supply (+Vcc)	24	N.C.
18	Analog Ground	23	Analog Ground
19	N.C.	22	Analog Input
20	Analog Ground	21	Analog Ground

NOTES:

1. "No Connects" (N.C.) are not connected to internal circuitry.

APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION—MN5249 is a multistage (two-step) A/D converter. It employs the Micro Networks Serial-Parallel conversion technique (sometimes referred to as the subranging technique) with digital error correction. The technique uses two 7-bit flash A/D converters (actually a single 7-bit flash converter is used twice) in a configuration that yields a resolution (12 bits) that is beyond the practical limits of what can be achieved in a single high-resolution flash converter. The technique trades off speed against resolution, and in the case of MN5249 against size, as putting the device in a single DIP package necessitates additional considerations. For a detailed discussion of the Serial-Parallel conversion technique and digital error correction, please refer to the MN5245/5246 data sheet.

Start Convert must be a positive pulse with a minimum pulse width of 50nsec (100nsec maximum if continuously converting at maximum conversion rate) and must remain low during the conversion. The rising edge of Start Convert resets the timing logic ensuring that all timing pulses are set to the proper state and that the first conversion following "power on" produces valid digital output data. The falling edge of Start Convert initiates the conversion setting T/H Control and Status (E.O.C.) to logic "1's". The T/H Control remains a logic "1" for 300nsec maximum after the falling edge of Start Convert and returns to a logic "0" signaling that the "analog-processing" portion of the conversion is complete and that a constant-value analog input signal is no longer required. Status remains a logic "1" for 400nsec maximum after the falling edge of Start Convert. Status returning low, signifies that the conversion process is complete and that parallel output data is valid.

The T/H Control signal enables designers to achieve maximum sampling rates from T/H-A/D pairs (MN376-MN5249 for example) by allowing the T/H to acquire the next analog voltage to be converted during the digital error correction process rather than waiting until the fall of Status.

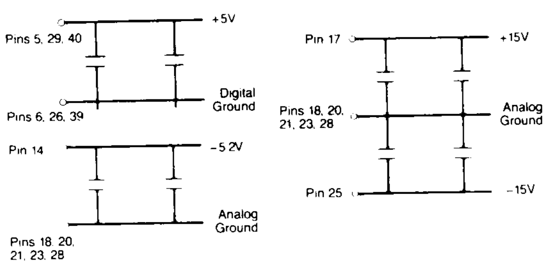
Valid parallel output data is available on the falling edge of Status and remains valid during the next conversion for 280nsec (typ) after the next falling edge of Start Convert. See Timing Diagram. This allows the use of rising and falling edges of either Start Convert or Status for latching output data.

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracy and performance from the MN5249. Analog Ground (pins 18, 20, 21, 23, 28) is not connected internally to Digital Ground (pins 6, 26, 39). All ground pins should be tied together as close to the unit as possible and connected to system analog ground, preferably through a large analog ground plane underneath the package. If p.c. card ground lines must be run separately, wide conductor runs should be used with 0.01μF ceramic capacitors interconnecting them as close to the package as possible.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Care should be taken to avoid long runs or analog runs close to digital lines.

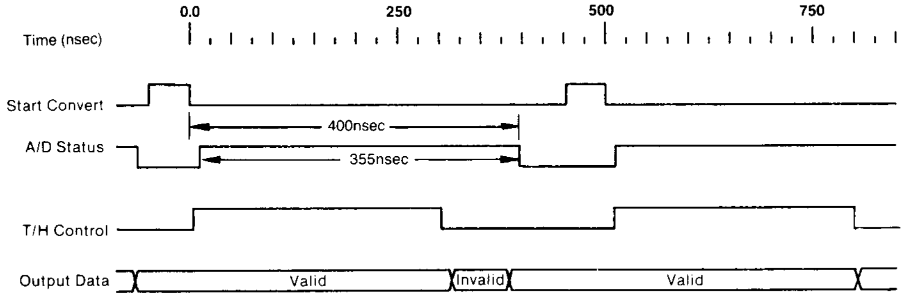
Power supply connections should be short and direct, and all power supplies should be decoupled with high-frequency bypass capacitors to ground. 1μF tantalum capacitors in parallel with 0.01μF ceramic capacitors are the most effective combination. Single 1μF ceramic capacitors can be used if necessary to save board space.

A 0.1μF capacitor should be connected from Reference Output (pin 27) to system analog ground.



POWER SUPPLY DECOUPLING

TIMING DIAGRAM

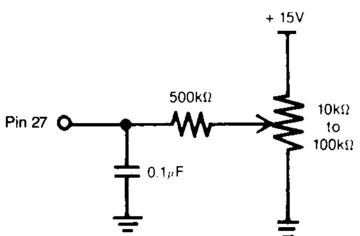


TIMING DIAGRAM NOTES:

1. Minimum start convert pulse width is 50nsec. The rising edge of start convert resets internal timing circuits ensuring that T/H Control (pin 10) is set to a logic "0" and that the first conversion made upon "powerup" is valid. The falling edge of Start Convert initiates the conversion, and Start Convert must remain low for 350nsec minimum. See section labeled Start Convert.
2. Status rises to a "1" typically 45nsec after the falling edge of Start Convert.
3. Conversion time is defined as the time from the falling edge of Start Convert to the falling edge of Status and is specified as 400nsec maximum.
4. Digital output data from the previous conversion remains valid typically 280nsec after the falling edge of Start and 235nsec after the rising edge of Status.
5. Digital output data is valid on the falling edge of Status.
6. Output data is enabled and becomes valid a maximum of 50nsec after Output Enable ($\overline{OE}$, pin 7) is brought low. See section labeled Output Enable.
7. The falling edge of T/H Control occurs 300nsec maximum after the falling edge of Start Convert. See section labeled Start Convert.

REFERENCE IN/OUT, GAIN ADJUST—Pin 27 on MN5249 serves a unique function. The device's internal +5V ±2% reference is brought out at this point and can be used to drive external loads. If used for this purpose, pin 27 should be buffered with a FET-input device as drawing more than 5μA from the internal reference will affect MN5249 accuracy and linearity. Pin 27 can also be used as a Reference In point if it is necessary to operate MN5249 from an external reference. An application requiring an external reference might be one in which it is necessary to have a number of devices operate from the same reference in order to track each other in changing temperatures. The applied reference should be +5V ±250mV.

Pin 27 also functions as the gain-adjust point for MN5249. Gain adjustment is accomplished using a 10kΩ to 100kΩ trimming potentiometer and a 500kΩ series resistor as shown below. The series resistor can be ±20% carbon composition or better. The multiturn potentiometer should have a TCR of 100ppm/°C or less to minimize drift with temperature. Gain adjusting is normally accomplished by applying the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 digital-output transition is ideally supposed to take place and adjusting the pot until the transition is observed.



Gain Adjust Range = ±0.2% FSR

OVERRANGE/UNDERRANGE—An overrange/underrange output (OR/UR, pin 9) is provided and will be set to a logic "1" if an over or underrange condition exists. An input voltage 1 LSB more positive than the voltage at which the 1111 1111 1110 to 1111 1111 1111 transition occurs will set the OR/UR output to a logic "1" and parallel output bits will remain at all "1's". Similarly, an input voltage 1 LSB more negative than the voltage at which the 0000 0000 0001 to 0000 0000 0000 transition occurs will set the OR/UR output to a logic "1" and parallel output bits will remain at all "0's."

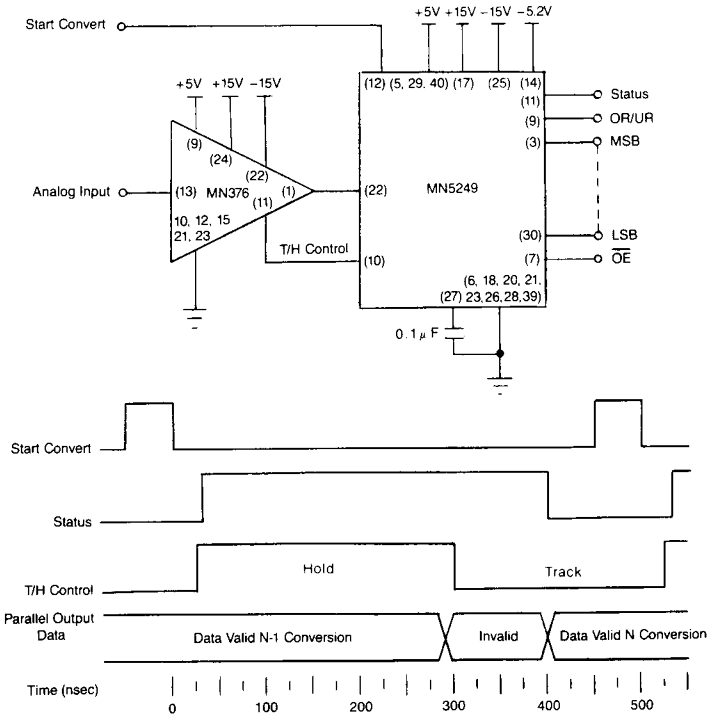
STATUS OUTPUT/DATA VALID—The Status or End of Conversion (E.O.C., pin 11) is set to a logic "1" by the falling edge of Start Convert; remains high during the conversion; and is set to a logic "0" when the conversion is complete. Digital output data is valid on the falling edge of Status and remains valid 280nsec after Start Convert goes low initiating the next conversion. When making successive conversions, any of the edges occurring during the beginning of the data-valid period (fall of Status, falling edge of the next Start Convert, rising edge of Status, etc.) are best suited for this purpose. Also, output data can be enabled during this data-valid period by bringing Output Enable ($\overline{OE}$, pin 7) low. The delay from the falling edge of $\overline{OE}$ to output data enabled is 50nsec maximum.

MN5249

TRACK/HOLD CONTROL—The Track/Hold Control (T/H Control, pin 10) output is provided so that designers can achieve maximum throughput without additional glue chips when using a track-hold amplifier with MN5249. This output signal is set to a logic "1" by the falling edge of Start Convert and remains high during the "analog-processing" portion of the A/D's conversion cycle. It drops back low when the "digital-processing" portion of the conversion cycle commences, signaling that it is no longer necessary to maintain a stable analog input. Use of this signal allows a companion T/H amplifier to acquire and track the next analog input signal to be converted during the "digital-processing" portion of the present conversion. T/H Control remains low until the falling edge of the next Start Convert signal.

The diagram below shows the MN376, high-speed T/H amplifier and the MN5249 configured as a 2MHz, 12-bit sampling system. Maximum throughput is achieved because the MN376's T/H Command input is driven directly by the MN5249's T/H Control output.

MN376-MN5249 2MHz Sampling System



DIGITAL OUTPUT CODING

Analog Input	Digital Output
MN5249	**MSB LSB**
+2.5000	1111 1111 1111
+2.4982	1111 1111 111Ø*
+0.0006	1000 0000 000Ø*
−0.0006	ØØØØ ØØØØ ØØØØ*
−0.0018	0111 1111 111Ø*
−2.4994	0000 0000 000Ø*
−2.5000	0000 0000 0000

NOTES:

1. For a 12-bit converter with a 5 Volt FSR, 1LSB=1.22mV.
2. Coding is offset binary.

*Analog voltages listed are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400