Standard Products

UT14AD20P 14-bit, 20MSps Pipeline Analog-to-Digital Converter

Advanced Data Sheet
February, 2012
www.aeroflex.com/AtoD

FEATURES

- 14-bit, 20MSps pipeline ADC
- Differential analog input
- Differential or single-ended clock input
- 74.4dBFS SNR, 92dBc SFDR
- Parallel LVDS or CMOS, single or double data rate (SDR/DDR) outputs with output enable
- LVDS 100-Ohm internal termination option
- Built-in digital output test patterns
- Offset binary or 2's complement output format
- Internal dither capability
- Internal Sample and Hold Amplifier (SHA)
- Internal or external voltage reference
- SPI Port for device programming
- Powerdown and Sleep modes
- Asynchronous reset input for system failure diagnostics and recovery
- Internal auxiliary keep-alive clock for recovery from slow- or stop-clock events
- Selectable 3.3/1.8V dual or 3.3V single analog supply; 2.0 to 3.3V output driver supply
- 1.49W (LVDS) or 1.28W (CMOS) power consumption
- -55°C to +125°C Temperature range (TBD)
- Operational environment:
  - Total dose: >300 krad(Si)
  - SEL Immune: Up to 120 MeV-cm^2/mg
- Packaging options:
  - 100 CQFP
- Standard Microcircuit Drawing TBD
  - QML Q and V pending

APPLICATIONS

- Military/Aerospace telecommunications and imaging
- Medical electronics (X-Ray, MRI)
- Remote telemetry

INTRODUCTION

The UT14AD20P is a 14-bit, 20-MSps CMOS pipeline analog-to-digital converter (ADC), designed in a monolithic CMOS process using Aeroflex's technology for harsh operational environments.

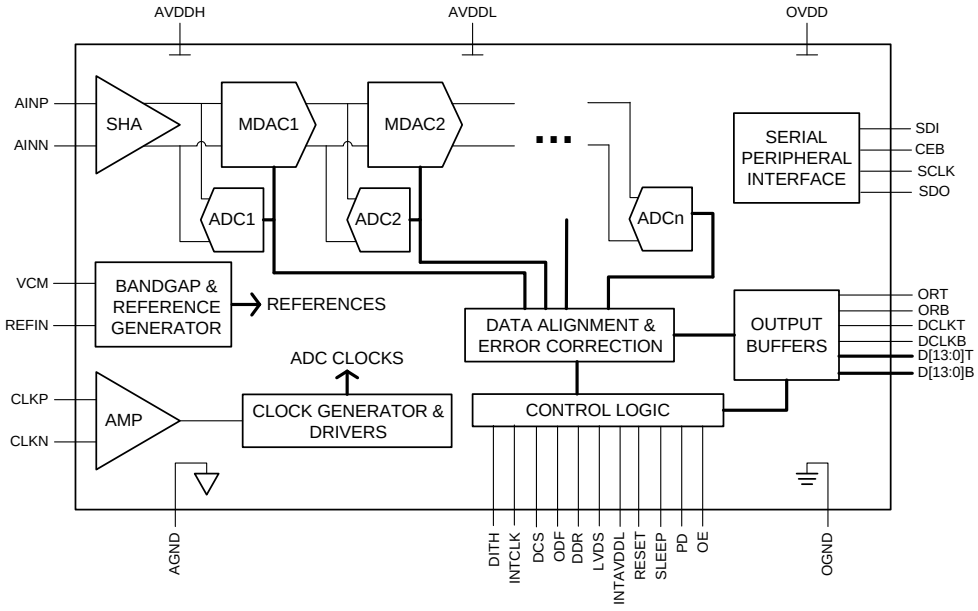


Figure 1: UT14AD20P Block Diagram

FUNCTIONAL DESCRIPTION

The UT14AD20P is a 14-bit, 20-MSps CMOS pipeline analog-to-digital converter (ADC), designed in a monolithic CMOS process using Aeroflex's technology for harsh operational environments. Its low noise (74.4dBFS SNR) and distortion performance (92dBc SFDR) make this ADC ideal for those telecommunication and imaging data processing applications posing the most severe electrical and environmental requirements. The full-scale range of the differential analog input is set to 2.5Vp-p by the internal voltage reference circuit. The user may provide an external reference by driving the REFIN pin (nominal voltage 1.25V). The input Sample-and-Hold Amplifier (SHA) samples the analog input at up to 20MSps with a full-power bandwidth of TBD MHz. The clock input determines the sampling edge of the SHA: the UT14AD20P achieves an RMS sampling jitter of TBDfs when a 2-V amplitude differential clock input is used. The optional duty-cycle stabilization internally produces 50% clock phases even when the externally provided clock features up to 25% - 75% duty cycle skew. An internal dither function for improved linearity of the conversion of small-signal analog inputs can also be optionally selected. Typical linearity specifications of the ADC are ±0.75LSB INL and ±0.1LSB DNL.

The digital outputs can be either in LVDS or CMOS format, in Single or Double Data Rate (SDR/DDR). The output drivers for either output mode have their own supply (OVDD), which can be set from 3.3V down to as low as 2.0V to alleviate the digital output coupling into the sensitive analog input or clock. In LVDS mode, an optional internal 100Ohm termination can also be selected. Internal digital output patterns can be activated to troubleshoot different "stuck-at" fixture failures. The UT14AD20P provides two output data formats: straight binary and 2's complement. The Output Enable control can be used to put all digital outputs in high impedance state, while leaving the internal analog circuitry fully active. The over-range flag OR is set high whenever the analog input exceeds the full-scale range. If the analog input is below its minimum, i.e. AINP-AINN < -1.25V, OR goes to logic 1 and data D[13:0] is set to its minimum value (0000x for the offset binary output format and 8000x for 2's complement). An analog input larger than the maximum AINP-AINN > +1.25V will set the OR flag to 1 and D[13:0]=3FFFx (offset binary) or D[13:0]=1FFFx (2's complement).

The SPI ports (Serial Peripheral Interface) provide a serial alternative to all parallel control inputs and allow the user to activate additional internal functions. Power Down turns off all internal analog circuits and places all digital outputs in a high-impedance state. The power consumption is reduced to 5mW. Coming out of Power Down mode, it will take approximately 2ms for the UT14AD20P to regain full performance to specification. The longest recovery delay is due to the internal voltage reference circuit. In the applications where this recovery time is not acceptable, the user may put the UT14AD20P in Sleep mode. All the analog circuits except the reference generator will be powered down, and all digital outputs will be in the high-impedance state. The power consumption in the sleep mode is approximately 90mW, and the recovery time is approximately 20µs. The RESET input allows the instantaneous refresh of the digital logic status without interrupting the ADC operation.

The datasheet specified performance of the ADC is guaranteed down to 1MSps. However, when the clock input is stopped or slows down below 650kHz, an internal clock signal can be optionally generated to refresh dynamic critical circuits and eliminate any recovery time.

The UT14AD20P can run on dual 3.3/1.8V analog supplies, or on a single 3.3V supply with internal sub-regulation.

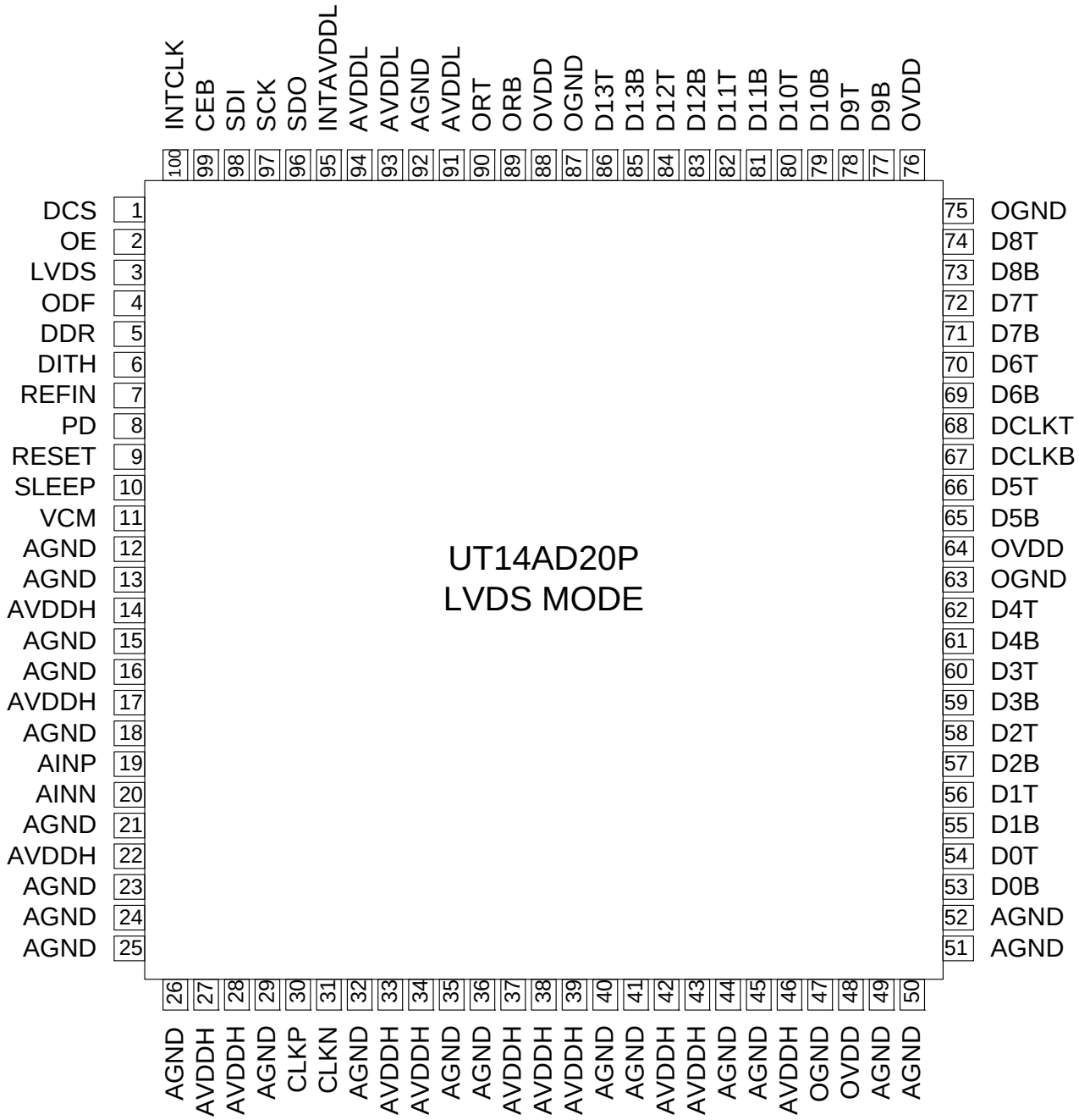


Figure 2: 100-Lead CQFP Pinout for LVDS Output Mode (Single Data Rate)

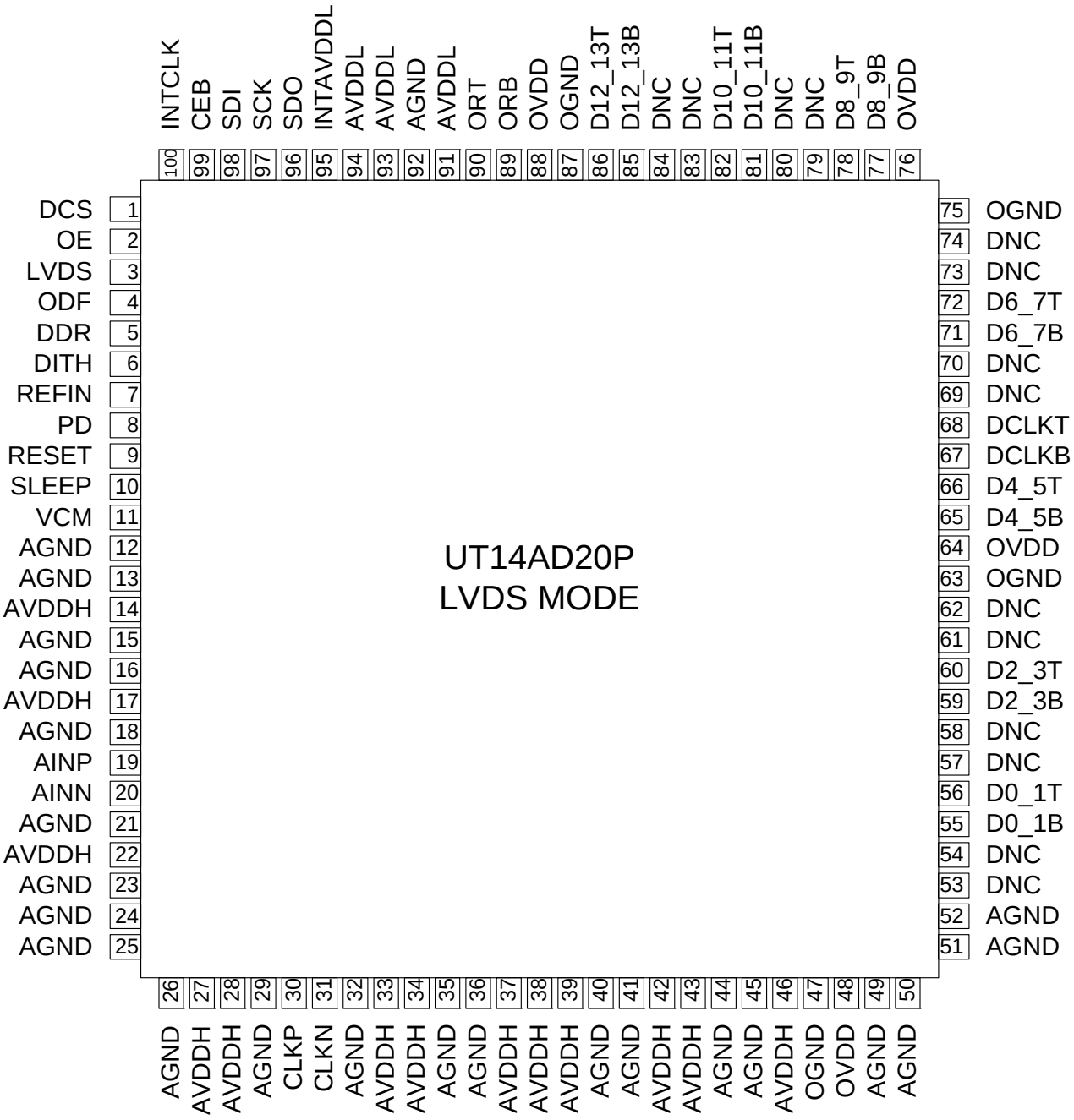


Figure 3: 100-Lead CQFP Pinout for LVDS Output Mode (Double Data Rate)

Table 1: Pin Descriptions (LVDS Mode, SDR and DDR)

Pin Name	Pin Number	Function
AINP	19	Positive side of differential analog input.
AINN	20	Negative side of differential analog input.
VCM	11	Analog voltage output to be used for analog input common mode conditioning.
REFIN	7	External voltage reference input. For 2.5Vp-p ADC full scale, drive this pin to 1.25V. Tie to 3.3Vwhen the internal reference is used.
CLKP	30	Positive side of differential clock input or single ended clock input.
CLKN	31	Negative side of differential clock input. Add an external bypass capacitor of 0.1 μF to ground when single ended clock is used.
AGND	12,13,15, 16,18, 21,23,24, 25, 26,29, 32,35,36, 40,41,44, 45 49,50, 51,52,92	Analog ground.
SDI	98	Serial Port Interface (SPI) serial data input.
CEB	99	SPI chip enable input (active low).
SCLK	97	SPI clock input.
SDO	96	SPI serial data output.
PD	8	Power down input. Logic 1 powers down all analog circuitry and places all digital outputs in a high impedance state.
LVDS	3	Output LVDS CMOS selection pin. Logic 1 is for LVDS, and logic 0 CMOS.
SLEEP	10	Sleep mode input. Logic 1 is same as PD=1, except the internal reference remains active.
OE	2	Output enable input. Logic 1 enables the output buffers. Logic 0 will force all data outputs in a high impedance state.
OGND	47,63,75, 87	Digital output buffer ground.
D[13:0]T (LVDS SDR)	54,56,58, 60,62,66, 70,72,74, 78,80,82, 84,86	Digital positive LVDS outputs. D[13]T is the MSB.
D[12_13:0_1]T (LVDS DDR)	56,60,66, 72,78,82, 86	Digital positive LVDS outputs. D[13]T is the MSB.

D[13:0]B (LVDS SDR)	53,55,57, 59,61,63, 67,71,73, 75,79,81, 83,85	Digital negative LVDS outputs. D[15]B is the MSB.
D[12_13:0_1]B (LVDS DDR)	55,59,65, 71,77,81, 85	Digital negative LVDS outputs. D[15]B is the MSB.
DCLKT	68	Digital positive LVDS clock output.
DCLKB	67	Digital negative LVDS clock output.
ORT	90	LVDS out of range output. Logic 1 indicates the analog input is out of range.
ORB	89	LVDS out of range negative output.
OVDD	48,64,76, 88	Digital output driver supply: can independently range from AVDDH down to a minimum of 2.0V.
AVDDL	91,93,94	Analog 1.8V supply.
AVDDH	14,17,22, 27,28,33, 34,37,38, 39,42,43, 46	Analog 3.3V supply.
DNC (LVDS DDR)	53,54,57, 58,61,62, 69,70,73, 74,79,80, 83,84	Do Not Connect.
DCS	1	Duty Cycle Stabilizer digital control input. Logic 1 enables the duty cycle 50% equalization circuit. Logic 0 adopts the external clock duty cycle as is.
INTAVDDL	95	Internal Analog 1.8V supply digital control input. Logic 1 enables single 3.3V supply operation by activating an internal voltage subregulator; the AVDDL pins must be decoupled to ground in this mode. Logic 0 selects dual 3.3V and 1.8V supply mode, with the analog 1.8V provided through the AVDDL pins.
DDR	5	Double Data Rate digital control input. Logic 1 enables time multiplexing of 2 bits on each output (LSB first, then MSB) synchronized with both edges of the clock output. Logic 0 provides 1 bit for each output driver and is synchronized with the rising edge of the clock output.
DITH	6	Dither digital control input. Logic 1 activates a user-transparent, internal dither function to enhance the ADC linearity and improve distortion of small signal inputs.
RESET	9	Soft reset digital input pin. Logic 1 forces a re-initialization of all the internal soft-programmed registers, as well as a refresh of the digital logic status.
ODF	4	Output Data Format digital control input. Logic 1 selects 2's complement, Logic 0 selects offset binary format.
INTCLK	100	Internal clock override digital control input. When the externally provided clock frequency falls below 650kHz, Logic 1 forces an internal fixed-frequency 500kHz clock to refresh the dynamic circuits; Logic 0 allows the internal clock to track the external signal even below 650kHz.

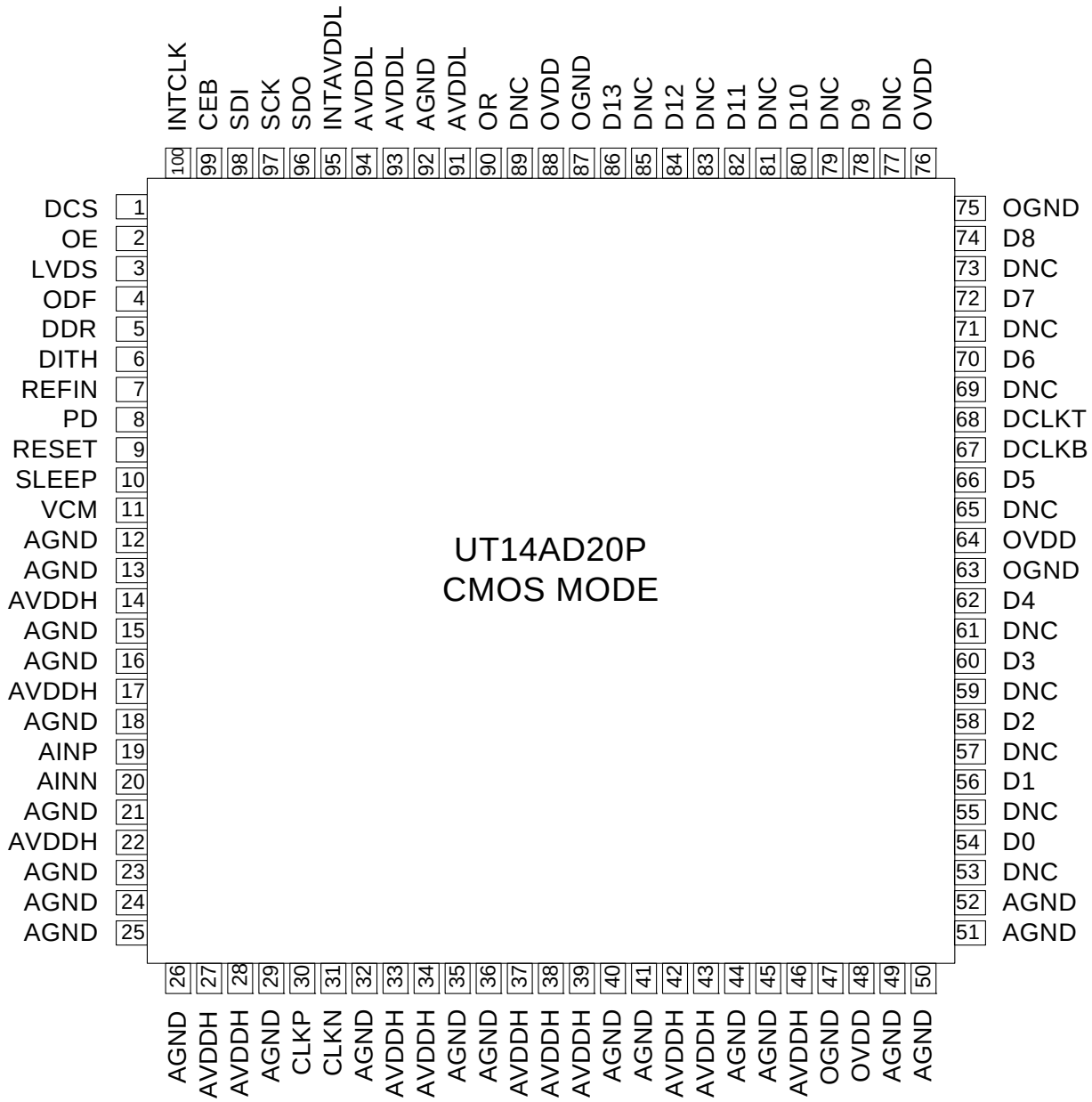


Figure 4: 100-Lead CQFP Pinout for CMOS Output Mode (Single Data Rate)

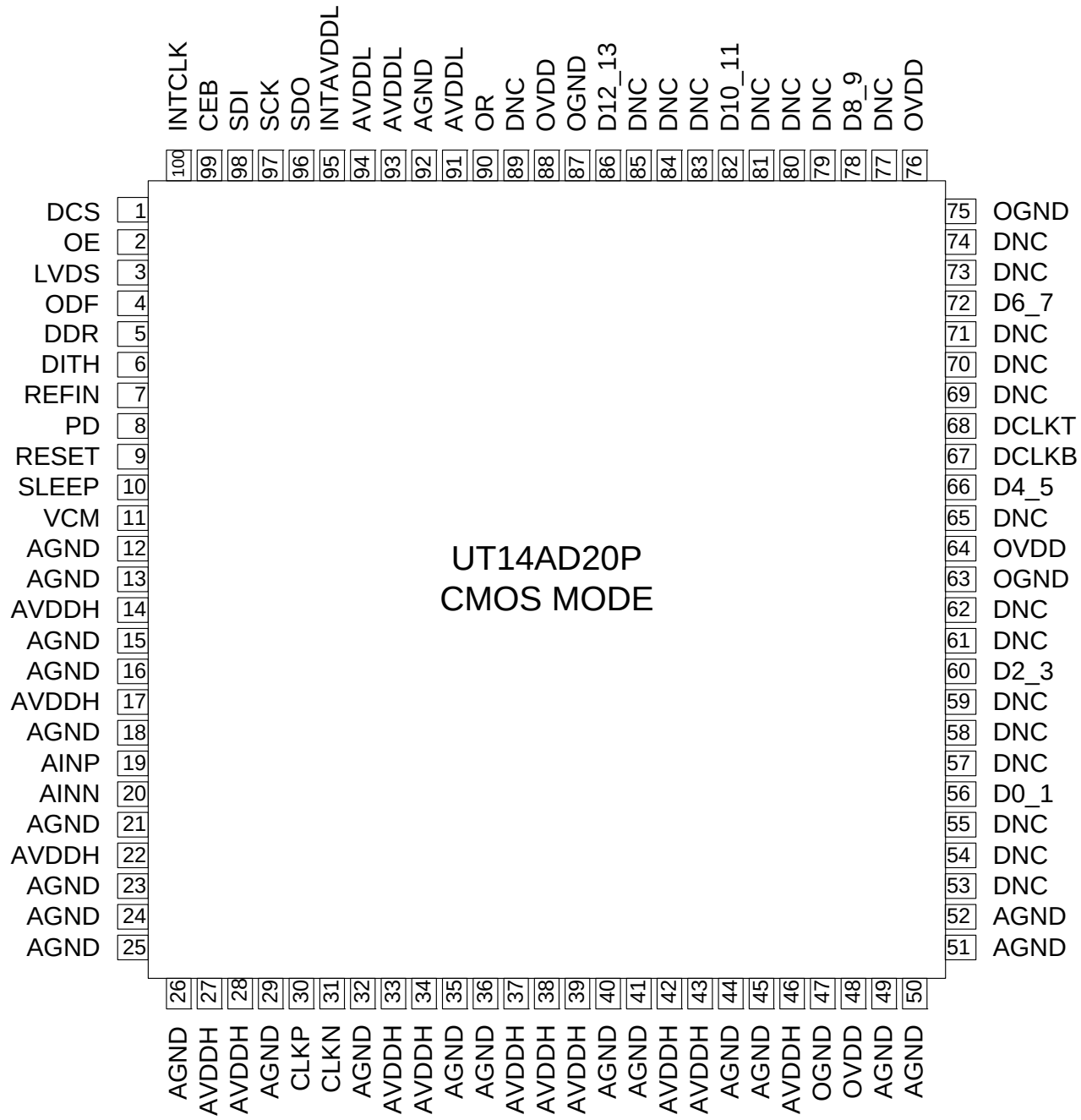


Figure 5: 100-Lead CQFP Pinout for CMOS Output Mode (Double Data Rate)

Table 2: Pin Descriptions (CMOS Mode, SDR and DDR)

Pin Name	Pin Number	Function
AINP	19	Positive side of differential analog input.
AINN	20	Negative side of differential analog input.
VCM	11	Analog voltage output to be used for analog input common mode conditioning.
REFIN	7	External voltage reference input. For 2.5Vp-p ADC fullscale, drive this pin to 1.25V. Tie to 3.3V when the internal reference is used.
CLKP	30	Positive side of differential clock input or single ended clock input.
CLKN	31	Negative side of differential clock input. Add an external bypass capacitor of 0.1µF to ground when single ended clock is used.
AGND	12,13,15, 16,18, 21,23,24, 25, 26,29, 32,35,36, 40,41,44, 45,49,50, 51,52,92	Analog ground.
SDI	98	Serial Port Interface (SPI) serial data input.
CEB	99	SPI chip enable input (active low).
SCLK	97	SPI clock input.
SDO	96	SPI serial data output.
PD	8	Power down input. Logic 1 powers down all analog circuitry and places all digital outputs in a high impedance state.
LVDS	3	Output LVDS CMOS selection pin. Logic 1 is for LVDS, and logic 0 CMOS.
SLEEP	10	Sleep mode input. Logic 1 is same as PD=1, except the internal reference remains active.
OE	2	Output enable input. Logic 1 enables the output buffers. Logic 0 will force all data outputs in a high impedance state.
OGND	47,63,75, 87	Digital output buffer ground.
D[13:0] (CMOS SDR)	54,56,58, 60,62,66, 70,72,74, 78,80,82, 84,86	Digital positive CMOS outputs. D[13] is the MSB.
D[12_13:0_1] (CMOS DR)	56,60,66, 72,78,82, 86	Digital positive CMOS outputs. D[13] is the MSB.
DCLKT	68	Digital CMOS clock output.
DCLKB	67	Digital CMOS complementary clock output.
OR	90	CMOS out of range output. Logic 1 indicates the analog input is out of range.
OVDD	89	Digital output driver supply: can independently range from AVDDH down to a minimum of 2.0V.

AVDDL	91,93,94	Analog 1.8V supply.
AVDDH	14,17,22, 27,28,33, 34,37,38, 39,42,43, 46	Analog 3.3V supply.
DNC (CMOS SDR)	53,55,57, 59,61,65, 69,71,73, 77,79,81, 83,85	Do Not Connect.
DNC (CMOS DDR)	53,54,55, 57,58,59, 61,62,65, 69,70,71, 73,74,77, 79,80,81, 83,84,85	Do Not Connect.
DCS	1	Duty Cycle Stabilizer digital control input. Logic 1 enables the duty cycle 50% equalization circuit. Logic 0 adopts the external clock duty cycle as is.
INTAVDDL	95	Internal Analog 1.8V supply digital control input. Logic 1 enables single 3.3V supply operation by activating an internal voltage subregulator; the AVDDL pins can optionally be decoupled to ground in this mode. Logic 0 selects dual 3.3V and 1.8V supply mode with the analog 1.8V provided through the AVDDL pins.
DDR	5	Double Data Rate digital control input. Logic 1 enables time multiplexing of 2 bits on each output (LSB first, then MSB) synchronized with both edges of the clock output. Logic 0 provides 1 bit for each output driver and is synchronized with the rising edge of the clock output.
DITH	6	Dither digital control input. Logic 1 activates a user-transparent, internal dither function to enhance the ADC linearity and improve distortion of small signal analog inputs.
RESET	9	Soft Reset digital input pin. Logic 1 forces a re-initialization of all the internal soft-programmed registers and the reset of all internal reference and common-mode circuitry, as well as a refresh of the digital logic status...
ODF	4	Output Data Format digital control input. Logic 1 selects 2's complement, Logic 0 selects offset binary format.
INTCLK	100	Internal clock override digital control input. When the externally provided clock frequency falls below 650kHz, Logic 1 forces an internal fixed-frequency 500kHz clock to refresh the dynamic circuits; Logic 0 allows the internal clock to track the external signal even below 650kHz.

OPERATIONAL ENVIRONMENT

PARAMETER	LIMIT	UNITS
Total Ionizing Dose (TID)	300	krad(Si)
Single Event Latchup (SEL)	>120	MeV-cm^2/mg
Single Event Upset Threshold (SEU)	TBD	MeV-cm^2/mg

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	LIMITS
AVDDH	Analog 3.3V Supply Voltage	-0.3V to 4V
AVDDL	Analog 1.8V Supply Voltage	-0.3V to 2.2V
OVDD	Output Supply	-0.3V to 4V
AGND	Ground	-0.3V to 1V
OGND	Output Ground	-0.3V to 1V
	Analog Input/Analog Clock	-0.3V to AVDDH+0.3V
	Digital Input/SPI Input	-0.3V to AVDDH+0.3V
	SPI Output	-0.3V to AVDDH+0.3V
T_{STG}	Storage Temperature	-65^{o}C to +150^{o}C
	Digital Output	-0.3V to AVDDH+0.3V
P_D	Power Dissipation (T_J < 150^{o}C) [2]	4400mW
TEMP	Operating Temperature Range	-55^{o}C to +125^{o}C

Notes:

1. Applying levels of stress in excess of the absolute maximum ratings may cause instantaneous and/or permanent damage to the device. Levels of stress between the maximum recommended operating conditions and the absolute maximum ratings will significantly degrade the performance, as well as shorten the life time, of the device.
2. The absolute maximum P_D rating was determined per MIL-STD-883, Method 1012, Section 3.4.1: $P_D = (T_J(MAX)-T_C(MAX)/\Theta_{JC})$. Usage of epoxy adhesive with thermal conductivity better than 10W/m-^{o}C between the ceramic case and the circuit board is suggested.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE
AVDDH	Analog High Positive Supply Voltage [1]	3.3V
AVDDL	Analog Low Positive Supply Voltage	1.8V
AGND	Analog Negative Supply Voltage	0V
OVDD	Output Positive Supply Voltage	2.0V to 3.3V
OGND	Output Negative Supply Voltage	0V
T_C	Case Operating Temperature Range	-55°C to +125°C
T_J	Junction Operating Temperature [2]	-55°C to +150°C

Notes:
1. Simulated to 3.6V.
2. Thermal resistance Θ_{JC} of junction-to-case is 5.6 °C/W.

DC ELECTRICAL CHARACTERISTICS [1]

(AVDDH =3.3V ± 5%, AVDDL=1.8V ± 5%, OVDD=3.3V thru 2.0V; -55°C ≤ T_C ≤ +125°C), A_{IN}=-1dBFS

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
INL	Integral non-linearity	Ramp test. zero-end corrected [2]		±0.75	TBD	LSB
DNL	Differential non-linearity	Ramp test [2]		±0.1	TBD	LSB
V_{OS}	ADC offset	Saturated ramp test [2]		±0.3	TBD	mV
	ADC offset drift	Saturated ramp test [3]		TBD		µV/°C
G_ε	ADC gain error	External REFIN level [2]		TBD	TBD	% of FS
	ADC gain error drift	External REFIN [3] Internal REFIN [3]		±TBD ±TBD		% of FS/°C
	ADC noise floor	Shorted ADC inputs [3]		1.1		LSB_{RMS}

Notes:

1. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
2. Parameters guaranteed by test.
3. Parameters guaranteed by characterization.

AC ELECTRICAL CHARACTERISTICS [1]

(AVDDH=3.3V ±5%, AVDDL=1.8V ±5%, OVDD=3.3V thru 2.0V; -55°C ≤ T_C ≤ +125°C), A_{IN}=-1dBFS

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
	Resolution			14		bits
SNR	Signal-to-Noise Ratio	Fin=5MHz, Tamb=25°C [3] Fin=5MHz [2] Fin=30MHz, Tamb=25°C [3] Fin=70MHz, Tamb=25°C [3] Fin=70MHz [2] Fin=100MHz, Tamb=25°C [3]	 TBD TBD 	74.4 TBD 72.6 70.5 TBD 68.0		dBFS
SFDR HD2, HD3	Spurious-Free Dynamic Range 2nd, 3rd harmonic	Fin=5MHz, Tamb=25°C [3] Fin=5MHz [2] Fin=30MHz, Tamb=25°C [3] Fin=70MHz, Tamb=25°C [3] Fin=70MHz [2] Fin=100MHz, Tamb=25°C [3]	 TBD TBD 	92 TBD 88 87 TBD 80		dBc
SFDR >HD4	Spurious-Free Dynamic Range 4th harmonic and beyond	Fin=5MHz, Tamb=25°C [3] Fin=5MHz [2] Fin=30MHz, Tamb=25°C [3] Fin=70MHz, Tamb=25°C [3] Fin=70MHz [2] Fin=100MHz, Tamb=25°C [3]	 TBD TBD 	95 TBD 95 92 TBD 90		dBc
SINAD	Signal-to-Noise+Distortion Ratio	Fin=5MHz, Tamb=25°C [3] Fin=5MHz [2] Fin=30MHz, Tamb=25°C [3] Fin=70MHz, Tamb=25°C [3] Fin=70MHz [2] Fin=100MHz, Tamb=25°C [3]	 TBD TBD 	74.2 TBD 72.4 70.3 TBD 67.7		dBFS
SFDR @ -25dBFS	Spurious-Free Dynamic Range: small amplitude vs dither	Fin=5MHz, Dither OFF [3] Fin=5MHz, Dither ON [2] Fin=30MHz, Dither OFF [3] Fin=30MHz, Dither ON [3] Fin=70MHz, Dither OFF [3] Fin=70MHz, Dither ON [3] Fin=100MHz, Dither OFF [3] Fin=100MHz, Dither ON [3]	 TBD 	105 115 105 115 103 110 100 105		dBFS
IMD3	Inter-modulation distortion	Fin1=4MHz+Fin2=6MHz @ -7dBFS [3] Fin1=69MHz+Fin2=71MHz @ -7dBFS [3]		TBD TBD		dBc

Notes:

1. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25^{o}C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
2. Parameters guaranteed by test.
3. Parameters guaranteed by characterization.

ANALOG INPUT CHARACTERISTICS [1]

(AVDDH=3.3V ± 5%, -55°C ≤ T_C ≤ +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{RANGE}	Differential analog input swing			2.5		V_{P-P}
FPBW	Full-power analog input BW	BW @ -3dBFS with series R_{IN} <25Ω [3]		TBD		MHz
V_{CM-IN}	Analog input common-mode	[2]	TBD	1.5	TBD	V
	Analog input leakage	0 ≤ (AINP, AINN) ≤ AVDDH [2]	-1		1	µA
	REFIN input leakage	0 ≤ REFIN ≤ AVDDH [2]	-1		1	µA
C_{IN}	Analog input capacitance single-ended	Sampling (CLKP > CLKN) Holding (CLKP < CLKN)		15 3		pF pF
t_{ACQ}	Sample/Hold acquisition delay	[3]		800		ps
σ_T	Sample/Hold aperture period jitter	Coherent sampling method [3]		TBD		fs_{RMS}
$CMRR_{IN}$	Analog input common-mode rejection ratio	0.875V≤ (AINP=AINN) ≤2.125V [3]		TBD		dB

Notes:

1. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
2. Parameters guaranteed by test.
3. Parameters guaranteed by characterization.

COMMON-MODE OUTPUT CHARACTERISTICS [1]

(AVDDH=3.3V ± 5%, -55°C ≤ T_C ≤ +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{CM}	Common-mode bias output	No current load applied [2]	1.425	1.5	1.575	V
	Common-mode bias temperature drift	No current load applied [3]		TBD		ppm/°C
$PSRR_{CM}$	Common-mode stability vs supply	Analog 3.3V supply within spec [3]		TBD		mV/V
R_{CM}	Common-mode output resistance	Current loads <1mA (source and sink) [3]		TBD		Ω

Notes:

1. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
2. Parameters guaranteed by test.
3. Parameters guaranteed by characterization.

DIGITAL INPUT CHARACTERISTICS [1]

(AVDDH=3.3V ± 5%, AVDDL=1.8V ± 5%, -55°C ≤ T_C ≤ +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
	Differential clock input swing	[2]	0.2			V_{P-P}
$V_{CM\ CLK}$	Clock input common-mode	When internally provided When externally forced	1.0	1.6	3.0	V
R_{CLK}	Clock input resistance single-ended			6.1		kΩ
C_{CLK}	Clock input capacitance single-ended			4		pF
V_{IH}	Digital input HIGH	[2]	2			V
V_{IL}	Digital input LOW	[2]			0.8	V
	Digital input leakage	0 ≤ Digital input ≤ AVDD [2]			±10	µA
C_{DIG}	Digital input capacitance			3		pF

Notes:

1. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
2. Parameters guaranteed by test.

DIGITAL OUTPUT CHARACTERISTICS [1]

(AVDDH=3.3V ± 5%, AVDDL=1.8V ± 5%, -55°C ≤ T_C ≤ +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
CMOS Data Outputs - OVDD = 3.3V						
V_{OH}	Digital output HIGH	200µA current sourced [2]	3.1	3.29		V
V_{OL}	Digital output LOW	2mA current sunk [2]		0.1	0.4	V
I_{SOURCE}	Digital output source current	Digital output = 0V		-50		mA
I_{SINK}	Digital output sink current	Digital output = 3.3V		50		mA
CMOS Data Outputs - OVDD = 2.5V						
V_{OH}	Digital output HIGH	200µA current sourced		2.49		V
V_{OL}	Digital output LOW	2mA current sunk		0.1		V
CMOS Data Outputs - OVDD = 2.0V						
V_{OH}	Digital output HIGH	200µA current sourced		1.99		V
V_{OL}	Digital output LOW	2mA current sunk		0.1		V
LVDS Data Outputs - OVDD = 3.3V						
ΔV_{LVDS}	Differential digital output	100Ω differential load [2]	250 -450	350 -350	450 250	mV mV
CM_{LVDS}	Common-mode digital output	100Ω differential load [2]	1.1	1.25	1.4	V
	Digital output source circuit	Digital output = 0V		-50		mA
	Digital output sink circuit	Digital output = 3.3V		50		mA

Notes:

1. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
2. Parameters guaranteed by test.

SYNCHRONIZATION CHARACTERISTICS [1]

(AVDDH=3.3V ± 5%, AVDDL=1.8V ± 5%, -55°C ≤ T_C ≤ +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
f_S	Sampling clock frequency	Normal operation [3]	1		20	MHz
$T_S/2$	Clock LOW and clock HIGH half-cycles	Duty-cycle stabilizer OFF [3] Duty-cycle stabilizer ON [3]	TBD 12.5	25 25	500 500	ns ns
f_{MIN}	External clock frequency threshold for keep-alive activation			650		kHz
f_{KA}	Internal keep-alive clock frequency	In-sleep mode or external clock slower than frequency threshold		500		kHz
	ADC latency	Single data rate - SDR Double data rate - DDR		5.5 5.5-6		Cycles
CMOS Data Outputs - OVDD = 3.3V						
$t_{DATAOUT}$	Input clock to data delay	[3]				ns
t_{CLKOUT}	Input clock to output clock delay	[3]				ns
$\Delta t_{CLK-DATA}$	Output clock to data skew	[3]				ns
t_{RISE}	Digital output rise time	with 1pF load				ns
t_{FALL}	Digital output fall time	with 1pF load				
LVDS Data Outputs - OVDD = 3.3V						
$t_{DATAOUT}$	Input clock to data delay	[3]				ns
t_{CLKOUT}	Input clock to output clock delay	[3]				ns
$\Delta t_{CLK-DATA}$	Output clock to data skew	[3]				ns
t_{RISE}	Digital output rise time	with 100Ω with 1pF differential load				ns
t_{FALL}	Digital output fall time	with 100Ω with 1pF differential load				ns
CMOS Data Outputs - OVDD = 2.0V						
$t_{DATAOUT}$	Input clock to data delay	[3]				ns
t_{CLKOUT}	Input clock to output clock delay	[3]				ns
$\Delta t_{CLK-DATA}$	Output clock to data skew	[3]				ns
t_{RISE}	Digital output rise time	with 1pF load				ns
t_{FALL}	Digital output fall time	with 1pF load				ns

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
LVDS Data Outputs - OVDD = 2.0V						
$t_{DATAOUT}$	Input clock to data delay	3				ns
t_{CLKOUT}	Input clock to output clock delay	3				ns
$\Delta t_{CLK-DATA}$	Output clock to data skew	3				ns
t_{RISE}	Digital output rise time	with 100Ω with 1pF differential load				ns
t_{FALL}	Digital output fall time	with 100Ω with 1pF differential load				ns

Notes:

1. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25^{o}C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
2. No note.
3. Parameters guaranteed by characterization.

POWER CONSUMPTION[1]

(AVDDH=3.3V ± 5%, AVDDL=1.8V ± 5%, -55°C ≤ T_C ≤ +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
AVDDH	Analog 3.3V supply		3.135	3.3	3.465	V
AVDDL	Analog 1.8V supply		1.7	1.8	1.9	V
P_{PD}	Consumption in power-down	External 1.8V supply [3] Internal regulated 1.8V supply [3]		4 5		mW mW
P_{SL}	Consumption in sleep mode	External 1.8V supply [3] Internal regulated 1.8V supply[3]		91 92		mW
CMOS Data Outputs						
OV_{DD}	Output supply		2.0	3.3	3.6	V
I_{AVDDH}	Analog 3.3V supply current	External 1.8V supply [2] Internal regulated 1.8V supply [2]		383 388	TBD	mA
I_{AVDDL}	Analog 1.8V supply current	External 1.8V supply [2]		7	TBD	mA
P_D	Total power consumption	External 1.8V supply [2] Internal regulated 1.8V supply [2]		1277 1280	TBD	mW
LVDS Data Outputs						
OV_{DD}	Output supply		2.0	3.3	3.6	V
I_{AVDDH}	Analog 3.3V supply current	External 1.8V supply [2] Internal regulated 1.8V supply [2]		383 388	TBD	mA
I_{AVDDL}	Analog 1.8V supply current	External 1.8V supply [2]		7	TBD	mA
I_{OVDD}	Output supply current	Single termination mode [2] Double termination mode [2]		63 125	TBD	mA
P_D	Total power consumption	External 1.8V supply [2] (single termination mode) Internal regulated 1.8V supply [2] (single termination mode)		1484 1489	TBD	mW

Notes:

1. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
2. Parameters guaranteed by test.
3. Parameters guaranteed by characterization.

PACKAGING

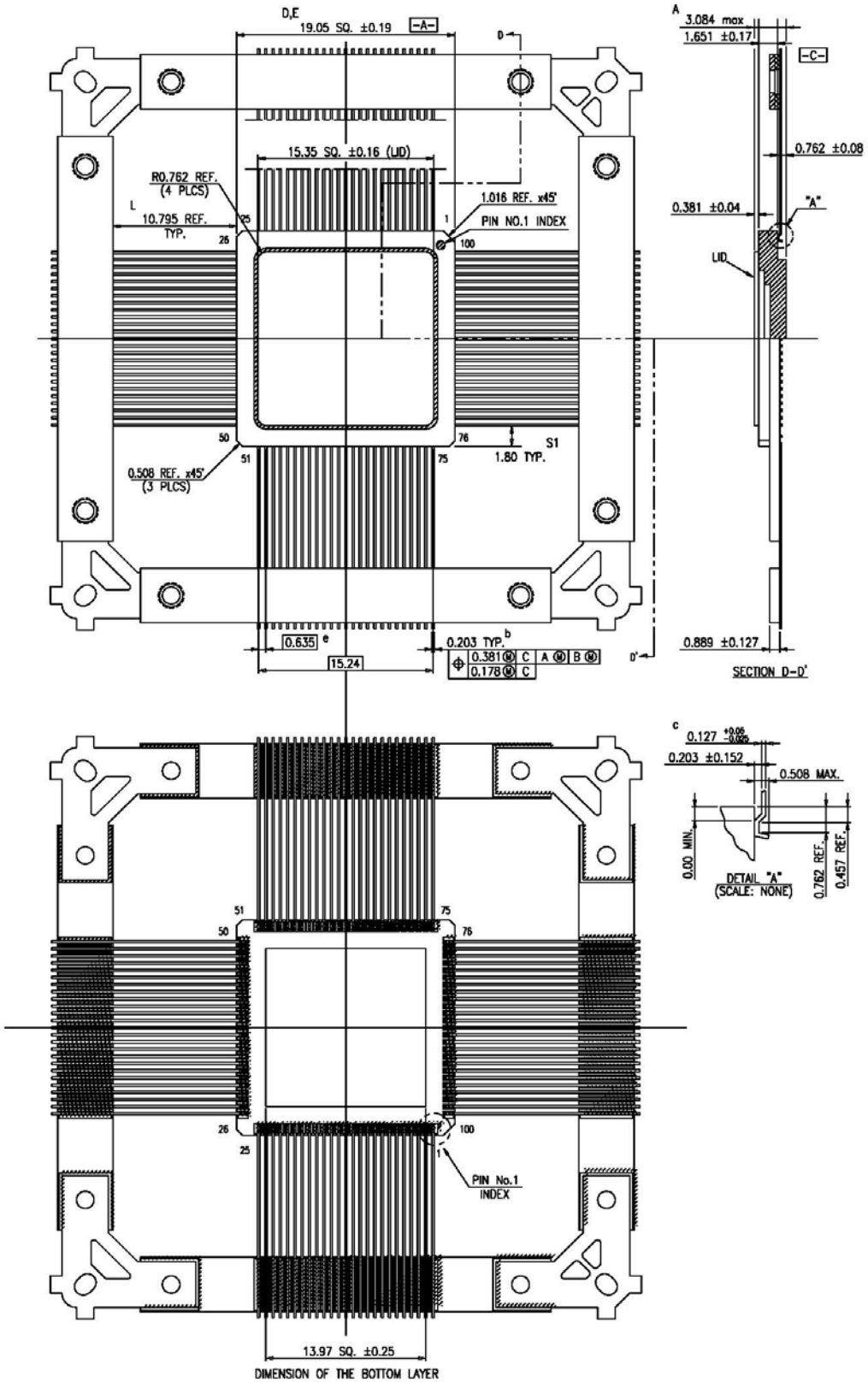
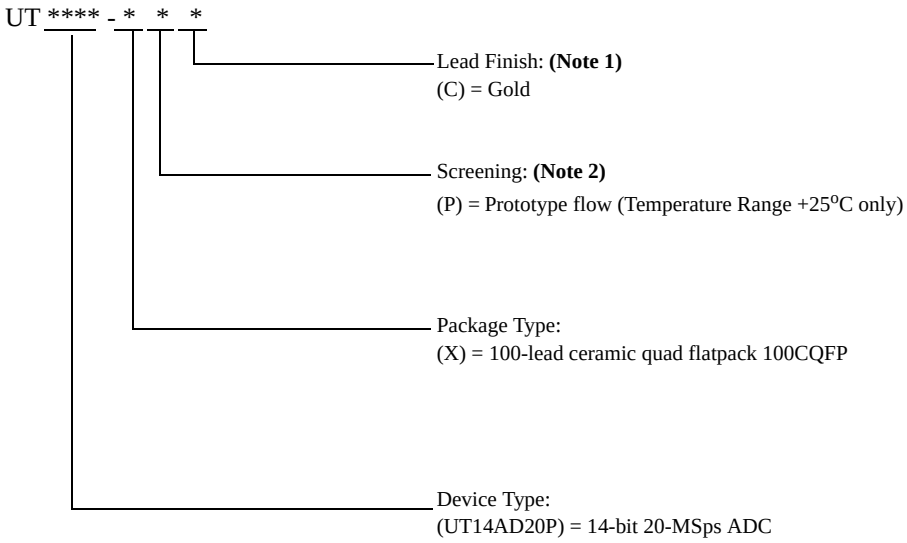


Figure 6: 100-Lead CQFP Pinout for CMOS Output Mode (Double Data Rate)

ORDERING INFORMATION

UT14AD20P 14-bit 20-MSps Pipeline A-to-D Converter



Notes:
1. Lead finish is "C" (Gold) only.
2. Prototype flow per Aeroflex Colorado Springs Manufacturing Flows Document. Radiation neither tested nor guaranteed.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced HiRel

COLORADO
Toll Free: 800-645-8862
Fax: 719-594-8468

INTERNATIONAL
Tel: 805-778-9229
Fax: 805-778-1980

NORTHEAST
Tel: 603-888-3975
Fax: 603-888-4585

SE AND MID-ATLANTIC
Tel: 321-951-4164
Fax: 321-951-4254

WEST COAST
Tel: 949-362-2260
Fax: 949-362-2266

CENTRAL
Tel: 719-594-8017
Fax: 719-594-8468

www.aeroflex.com *info-ams@aeroflex.com*

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