

SN54AHCT125, SN74AHCT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCLS264A – DECEMBER 1995 – REVISED MARCH 1996

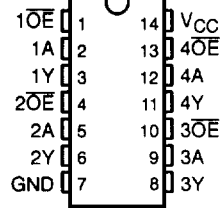
- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

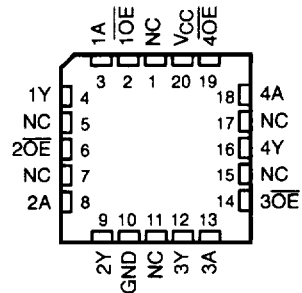
The 'AHCT125 are quadruple bus buffer gates featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high. When \overline{OE} is low, the respective gate passes the data from the A input to its Y output.

The SN54AHCT125 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHCT125 is characterized for operation from -40°C to 85°C .

SN54AHCT125 . . . J OR W PACKAGE
SN74AHCT125 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT125 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

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UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

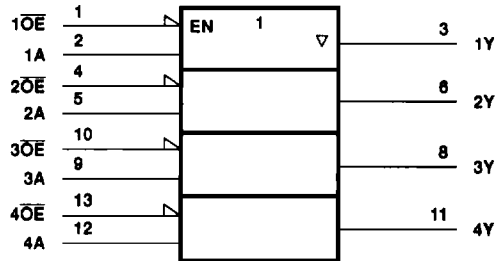
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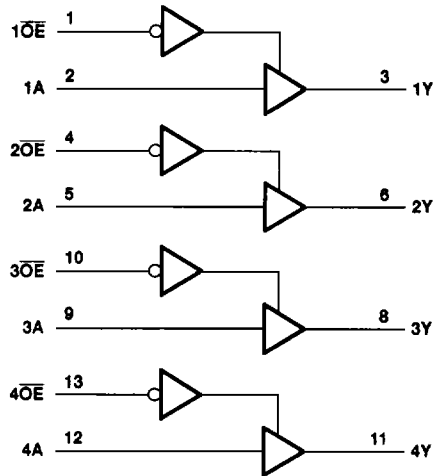
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

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SCLS264A – DECEMBER 1995 – REVISED MARCH 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Note 1)	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	-20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT125		SN74AHCT125		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage			0.8	0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		-8		-8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54AHCT125		SN74AHCT125		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50 \mu\text{A}$	4.5 V	3.15	3.65		3.15	MAX	3.15	V	
	$I_{OH} = -8 \text{ mA}$					2.4	MAX	2.4		
V_{OL}	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1		MAX	0.1	V	
	$I_{OL} = 8 \text{ mA}$				0.36		MAX	0.44		
I_I	A or \overline{OE} inputs	$V_I = V_{CC}$ or GND	5.5 V		±0.1		±1		±1	μA
I_{OZ}		$V_O = V_{CC}$ or GND	5.5 V		±0.25		±2.5		±2.5	μA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		2		20		20	μA
ΔI_{CC}^\ddagger		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V		1.35		1.5		1.5	mA
C_i		$V_I = V_{CC}$ or GND	5 V		4	10			10	pF
C_o		$V_O = V_{CC}$ or GND	5 V		15					pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT125				UNIT	
				$T_A = 25^\circ\text{C}$			MIN		MAX
				MIN	TYP	MAX			
t_{PLH}^*	A	Y	$C_L = 15\text{ pF}$	3.8	5.5	1	6.5	ns	
t_{PHL}^*				3.8	5.5	1	6.5		
t_{PZH}^*	\overline{OE}	Y	$C_L = 15\text{ pF}$	3.6	5.1	1	6	ns	
t_{PZL}^*				3.6	5.1	1	6		
t_{PHZ}^*	\overline{OE}	Y	$C_L = 15\text{ pF}$	4.6	6.8	1	8	ns	
t_{PLZ}^*				4.6	6.8	1	8		
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	5.3	7.5	1	8.5	ns	
t_{PHL}				5.3	7.5	1	8.5		
t_{PZH}	\overline{OE}	Y	$C_L = 50\text{ pF}$	5.1	7.1	1	8	ns	
t_{PZL}				5.1	7.1	1	8		
t_{PHZ}	\overline{OE}	Y	$C_L = 50\text{ pF}$	6.1	8.8	1	10	ns	
t_{PLZ}				6.1	8.8	1	10		

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT125				UNIT	
				$T_A = 25^\circ\text{C}$			MIN		MAX
				MIN	TYP	MAX			
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	3.8	5.5	1	6.5	ns	
t_{PHL}				3.8	5.5	1	6.5		
t_{PZH}	\overline{OE}	Y	$C_L = 15\text{ pF}$	3.6	5.1	1	6	ns	
t_{PZL}				3.6	5.1	1	6		
t_{PHZ}	\overline{OE}	Y	$C_L = 15\text{ pF}$	4.6	6.8	1	8	ns	
t_{PLZ}				4.6	6.8	1	8		
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	5.3	7.5	1	8.5	ns	
t_{PHL}				5.3	7.5	1	8.5		
t_{PZH}	\overline{OE}	Y	$C_L = 50\text{ pF}$	5.1	7.1	1	8	ns	
t_{PZL}				5.1	7.1	1	8		
t_{PHZ}	\overline{OE}	Y	$C_L = 50\text{ pF}$	6.1	8.8	1	10	ns	
t_{PLZ}				6.1	8.8	1	10		

output-skew characteristics, $C_L = 50\text{ pF}$ (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74AHCT125				UNIT	
				$T_A = 25^\circ\text{C}$			MIN		MAX
				MIN	TYP	MAX			
$t_{sk(o)}$	A	Y	$5\text{ V} \pm 0.5\text{ V}$			1	1	ns	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

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SCLS264A - DECEMBER 1995 - REVISED MARCH 1996

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

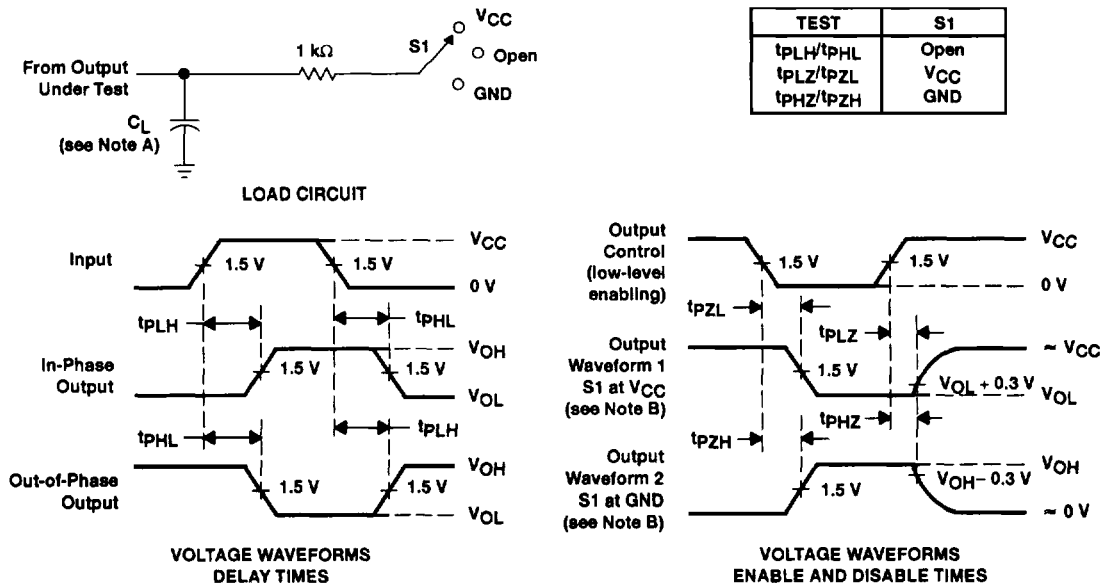
PARAMETER	SN74AHCT125		UNIT
	MIN	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}	0.8		V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}	-0.8		V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}	4.4		V
$V_{IH(D)}$ High-level dynamic input voltage	2		V
$V_{IL(D)}$ Low-level dynamic input voltage	0.8		V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	14	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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