

# R144EFXL and R144EFXL-CID Low Power 14400 bps MONOFAX<sup>®</sup> Modem

## Introduction

The Rockwell R144EFXL MONOFAX<sup>®</sup> modem is a synchronous 14400 bits per second (bps) half-duplex modem with error detection and DTMF reception. It has low power consumption and requires only a single +5VDC power supply. The modem is packaged in a 100-pin plastic quad flat pack (PQFP). The R144EFXL-CID is identical to the R144EFXL with the addition of Caller ID reception. Unless otherwise noted, all references to R144EFXL also include the R144EFXL-CID.

The modem can operate over the public switched telephone network (PSTN) through line terminations provided by a data access arrangement (DAA).

The modem satisfies the requirements specified in CCITT recommendations V.33, V.17, V.29, V.27 ter, V.21 Channel 2 (FSK), T.4, and T.3, and meets the binary signaling requirements of T.30.

The modem can operate at 14400, 12000, 9600, 7200, 4800, 2400, or 300 bps. The modem supports the V.17 signaling rates of 14400, 12000, 9600, and 7200 bps using trellis-coded modulation (TCM). In addition, the modem supports V.27 ter and V.17 short trains.

The modem can also perform HDLC framing according to T.30 at 14400, 12000, 9600, 7200, 4800, 2400, or 300 bps.

An FSK flag pattern (7E) detector facilitates FSK detection in the high speed receiver.

The modem includes a programmable DTMF receiver and three programmable tone detectors which operate concurrently with the V.21 channel 2 (FSK) receiver. The three programmable tone detectors also operate concurrently with the voice mode receiver.

The voice mode allows the host computer (DTE) to efficiently transmit and receive audio signals and messages.

General purpose input/output (GPIO) and general purpose input (GPI) pins are available for host assignment.

The modem's small size, single voltage supply, and low power consumption allow the design of compact system enclosures for use in both office and home environments.

Additional modem information is described in the R144EFXL MONOFAX Modem Designer's Guide (Order No. 895).

## Features

- Group 3 facsimile transmission/reception
  - CCITT V.33, V.17, V.29, V.27 ter, V.21 Channel 2 (FSK), T.4, and T.30
  - HDLC framing at all speeds
- Group 2 facsimile transmission/reception
  - CCITT T.3
  - External clock tracking
- V.27 ter short train
- V.29 short train
- Concurrent DTMF reception, FSK flag pattern (7E) detection, and tone detection
- Caller ID reception (R144EFXL-CID only)
- FSK flag pattern detect during high speed reception
- Voice mode transmission/reception
- 2-wire half-duplex
- Programmable transmit level: 0 to -15 dBm
- Programmable transmit analog attenuation: 0 dB to 14 dB in 2 dB steps
- Receive dynamic range: 0 to -43 dBm
- Programmable dual tone generation
- Programmable tone detection
- Programmable turn-on and turn-off thresholds
- Programmable interface memory interrupt
- Diagnostic capability
  - Allows telephone line quality monitoring
- Equalization
  - Automatic adaptive equalizer
  - Fixed digital compromise equalizer
- DTE interface: two alternate ports
  - Selectable microprocessor bus (6500 or 8085)
  - CCITT V.24 (EIA-232-D compatible) interface
- TTL and CMOS compatible
- Low power consumption:
  - Operating mode: 270 mW (typical)
  - Sleep mode: 17 mW (typical)
- Single +5VDC power supply
- Single package: 100-pin PQFP
- Hardware compatible with the R96DFXL MONOFAX modem
- Software compatible with all MONOFAX modems

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## TECHNICAL SPECIFICATIONS

### Configurations, Signaling Rates and Data Rates

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed in Table 1.

### Tone Generation

The modem can generate voice-band single or dual tones from 0 Hz to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated. Dual tone generation allows the modem to operate as a programmable DTMF dialer.

### Caller ID Reception (R144EFXL-CID Only)

Caller ID reception (CID) allows the called Customer Premises Equipment (CPE) to receive a calling party's directory number and the date and time of the call during the first 4-second silent interval in the ringing cycle.

### Data Encoding

The data encoding conforms to CCITT recommendations V.33, V.17, V.29, V.27 ter, V.21 Channel 2, and T.3.

### Automatic Adaptive Equalizer

An adaptive equalizer in V.33, V.17, V.29 and V.27 ter modes compensates for transmission line amplitude and group delay distortion.

### Fixed Digital Cable Compromise Equalizer

Compromise equalization can improve performance when operating over low quality lines. The modem has a selectable fixed digital compromise cable equalizer in the high speed receive and transmit data path.

### Transmitted Data Spectrum

The transmitted data spectrum is shaped in the baseband by an excess bandwidth finite impulse response (FIR) filter with the following characteristics:

When operating at 2400 baud, the transmitted spectrum is shaped by a square root of 20% raised cosine filter.

When operating at 1600 baud, the transmitted spectrum is shaped by a square root of 50% raised cosine filter.

When operating at 1200 baud, the transmitted spectrum is shaped by a square root of 90% raised cosine filter.

The out-of-band transmitter energy levels in the 4 - 50 kHz frequency range are below -55.0 dBm.

**Table 1. Configurations, Signaling Rates, and Data Rates**

Configuration	Modulation	Carrier Frequency (Hz) ±0.01%	Data Rate (bps) ±0.01%	Baud (Symbols/Sec.)	Bits /Symbol	Constellation Points
V.17/V.33 14400	TCM	1700 or 1800	14400	2400	6	128
V.17/V.33 12000	TCM	1700 or 1800	12000	2400	5	64
V.17 9600	TCM	1700 or 1800	9600	2400	4	32
V.17 7200	TCM	1700 or 1800	7200	2400	3	16
V.29 9600	QAM	1700	9600	2400	4	16
V.29 7200	QAM	1700	7200	2400	3	8
V.29 4800	QAM	1700	4800	2400	2	4
V.27 ter 4800	DPSK	1800	4800	1600	3	8
V.27 ter 2400	DPSK	1800	2400	1200	2	4
V.21 Channel 2 300	FSK	1650, 1850	300	300	1	–
T.3 (Group 2)	VSAMPM	2100	–	–	–	–

#### Notes:

- Modulation legend:
 

QAM:	Quadrature Amplitude Modulation
DPSK:	Differential Phase Shift Keying
FSK:	Frequency Shift Keying
TCM:	Trellis-Coded Modulation
VSAMPM	Vestigial Sideband Amplitude Modulation - Phase Modulation

**Turn-on and Turn-off Sequences**

Transmitter turn-on sequence times are shown in Table 2.

Transmitter turn-off sequence times are shown in Table 3.

**Table 2. Turn-On Sequence Times**

Configuration	~RTS On to ~CTS On	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled
V.17/V.33	1393 ms	1600 ms
V.17 Short Train	142 ms	349 ms
V.29 Long Train	253 ms	441 ms
V.29 Short Train	75 ms	282 ms
V.27 ter 4800 bps Long Train	708 ms	915 ms
V.27 ter 4800 bps Short Train	50 ms	257 ms
V.27 ter 2400 bps Long Train	943 ms	1150 ms
V.27 ter 2400 bps Short Train	67 ms	274ms
V.21 Channel 2 300 bps	≤14 ms	≤14 ms
Group 2	≤400 ms	≤400 ms

**Table 3. Turn-Off Sequence Times**

Configuration	Data and Scrambled Ones	No Transmitted Energy	Total
V.33/V.17	13.3 ms	20 ms	33.3 ms
V.17 Short Train	13.3 ms	20 ms	33.3 ms
V.29 (all speeds)	5 ms	20 ms	25 ms
V.27 ter 4800 bps Long Train	7 ms	20 ms	27 ms
V.27 ter 4800 bps Short Train	7 ms	20 ms	27 ms
V.27 ter 2400 bps Long Train	10 ms	20 ms	30 ms
V.27 ter 2400 bps Short Train	10 ms	20 ms	30 ms
V.21 Channel 2 300 bps	7 ms	0 ms	7 ms

**Notes:**

- In parallel data mode, the turn-off sequence may be extended by 8 bit times.
- In HDLC mode, the turn-off sequence may be extended by more than 8 bit times.

**Transmit Level**

The transmitter output level is programmable in the DSP RAM from 0 dBm to -15.0 dBm and is accurate to ±1.0 dBm. The modem adjusts the output level by digitally scaling the output to the transmitter's digital-to-analog converter.

Additionally, the modem can be programmed to attenuate the transmit output level from 0 dB to -14 dB in the analog section in steps of 2 dB using the TXLOSS1 - TXLOSS3 input pins.

**Scrambler/Descrambler**

The modem incorporates a self-synchronizing scrambler/descrambler in accordance with V.33, V.17, V.29, or V.27 ter recommendations, depending on the selected configuration.

**Receive Dynamic Range**

The receiver satisfies PSTN performance requirements for received line signal levels from 0 dBm to -43 dBm measured at the Receiver Analog Input (RXA) input. An external input buffer and filter must be supplied between RXA and RXIN.

The default values of the programmable Received Line Signal Detector (~RLSD) turn-on and turn-off threshold levels are -43 dBm and -48 dBm, respectively. The ~RLSD threshold levels can be programmed over the following range:

Turn on: -10 dBm to -47 dBm

Turn off: -10 dBm to -52 dBm

**Receiver Timing**

The timing recovery circuit can track a ±0.01% frequency error in the associated transmit timing source.

**Carrier Recovery**

The carrier recovery circuit can track a ±7 Hz frequency offset in the received carrier.

**Clamping**

Received Data (RXD) is clamped to a constant mark whenever ~RLSD is off.

**Tone Detectors**

Tone detectors 1 and 2 operate in all non-high speed receive modes. Tone detector 3 operates in all receive modes. The tone detectors can also operate as one 12th order filter in non-high speed receive modes. The filter coefficients of each filter are host programmable in RAM.

**Voice Mode**

The voice mode enables the host to efficiently transmit and receive audio signals and messages. In this mode, the host can directly access modem analog-to-digital (A/D) and digital-to-analog (D/A) converters. Incoming analog voice signals can then be converted to digital format and digital signals can be converted to analog voice output.

**Sleep Mode**

The modem can be put into low power Sleep mode by writing 0 into the Sleep Mode Enable DSP RAM parameter. When this occurs, the modem XTLI pin is pulled down internally with 10K - 30K ohms impedance to disable the internal oscillator. All of the oscillator outputs (e.g., XCLK, YCLK, DCLK, etc.) are disabled and the GPIO lines pulled up to +5VD with about 50K ohms impedance. The power consumption will drop to about 17 mW if a crystal is used or to about 33 mW if an external oscillator is used (since XTLI and XTLO are still active). In either case, the XCLK and YCLK outputs are disabled, therefore, the host cannot use either clock in the Sleep mode. Return to normal operation is initiated when the Power-On-Reset Input (~PORI) signal is asserted or the host writes to any modem interface memory location. The modem will perform self-test, configure itself to power-on-reset default conditions, and be ready for normal use within 30 ms.

**General Specifications**

The modem power and environmental requirements are listed in Table 4 and Table 5, respectively.

**Table 4. Current Requirements**

Mode	Current (Typ.) @25°C	Current (Max.) @0°C
Normal	54 mA	60 mA
Sleep	54 mA	60 mA

**Note**

- Operating voltage = 5.0V ± 5%.
- Typical current listed for 5.0V; maximum current listed for 5.25V.
- Input Ripple ≤ 0.1 V<sub>peak-peak</sub>. The amplitude of any frequency between 20 kHz and 150 kHz must be less than 500 μV<sub>peak</sub>.

**Table 5. Environmental Requirements**

Parameter	Specification
Temperature	
Operating	0°C to +70°C (32°F to 158°F)
Storage	-55°C to +125°C (-67°F to 257°F)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

**HARDWARE INTERFACE**

The hardware interface signals are shown in Figure 1. In Figure 1, any point that is active when exhibiting the relatively more negative voltage of a two-voltage system (e.g., 0 VDC for TTL or -12 VDC for EIA/TIA-232-E) is called active low and is represented by a small circle at the signal point. Active low signals are indicated by a tilde (~), e.g., ~RESET.

Edge-triggered clocks are indicated by a small triangle (e.g., DCLK).

Open-collector (open-source or open-drain) outputs are denoted by a small half circle (e.g., signal ~IRQ).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low, while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

Pin signal assignments are shown in Figure 2 (100-pin PQFP).

**SOFTWARE INTERFACE**

Modem functions are implemented in firmware executing in the MDP DSP.

**INTERFACE MEMORY**

The DSP communicates with the host processor by means of a dual-port, interface memory. This interface memory contains thirty-two 8-bit registers, labeled register 00 through 1F. Each register can be read from, or written into, by both the host and the DSP.

The host controls modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through interface memory. The host monitors modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

**DSP RAM ACCESS**

The DSP contains 16-bit words RAM. Because the DSP is optimized for performing complex arithmetic, the RAM is organized into real (X RAM) and imaginary (Y RAM) parts. The host processor can read or write both the X RAM and the Y RAM.

DSP interface memory is an intermediary during data exchanges between the host and DSP RAM. The address stored in interface memory RAM address registers by the host determines the DSP RAM address for data access.

The DSP RAM interface memory bits, access functions, codes, and registers are defined in the designer's guide.

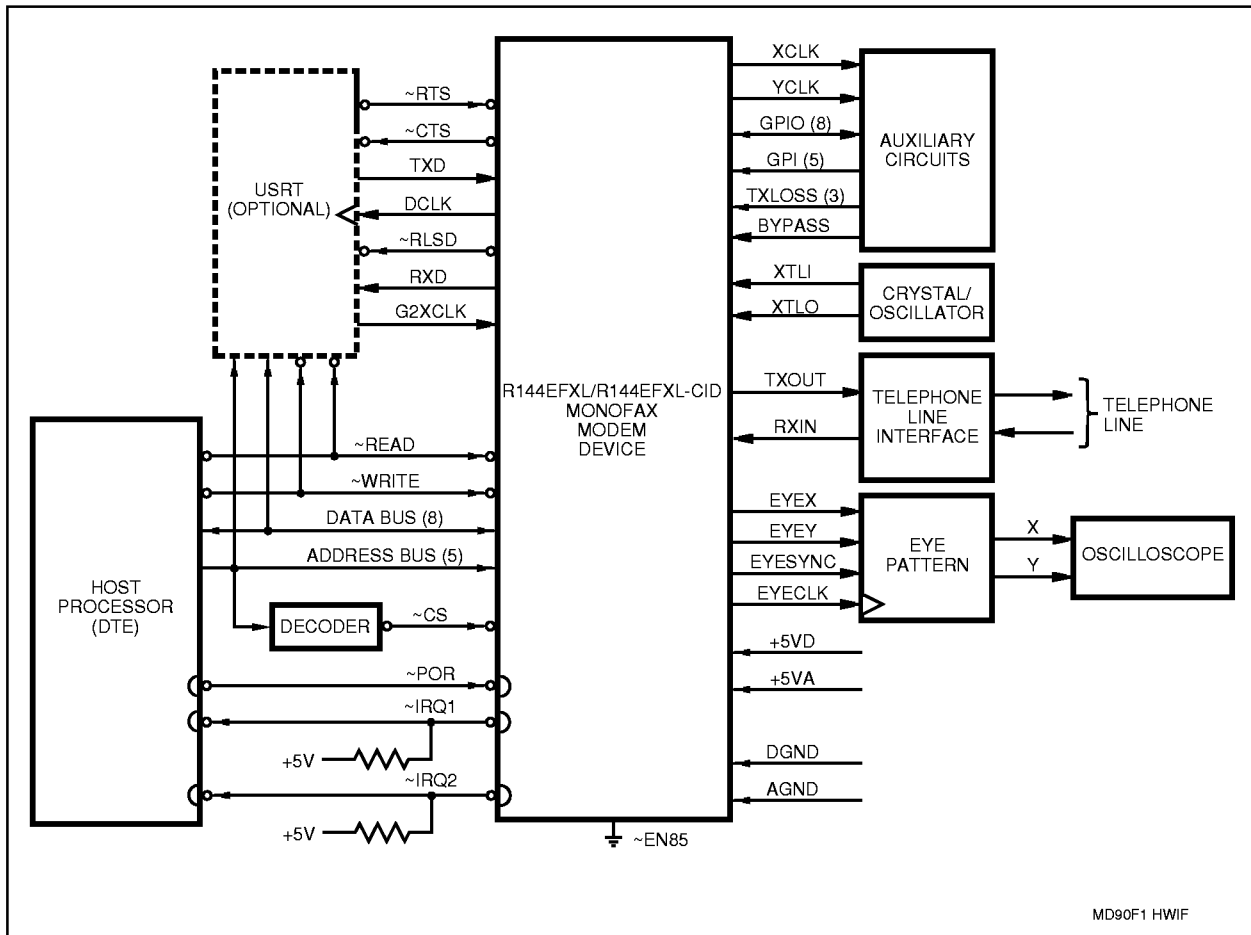


Figure 1. Modem Functional Interconnect Diagram

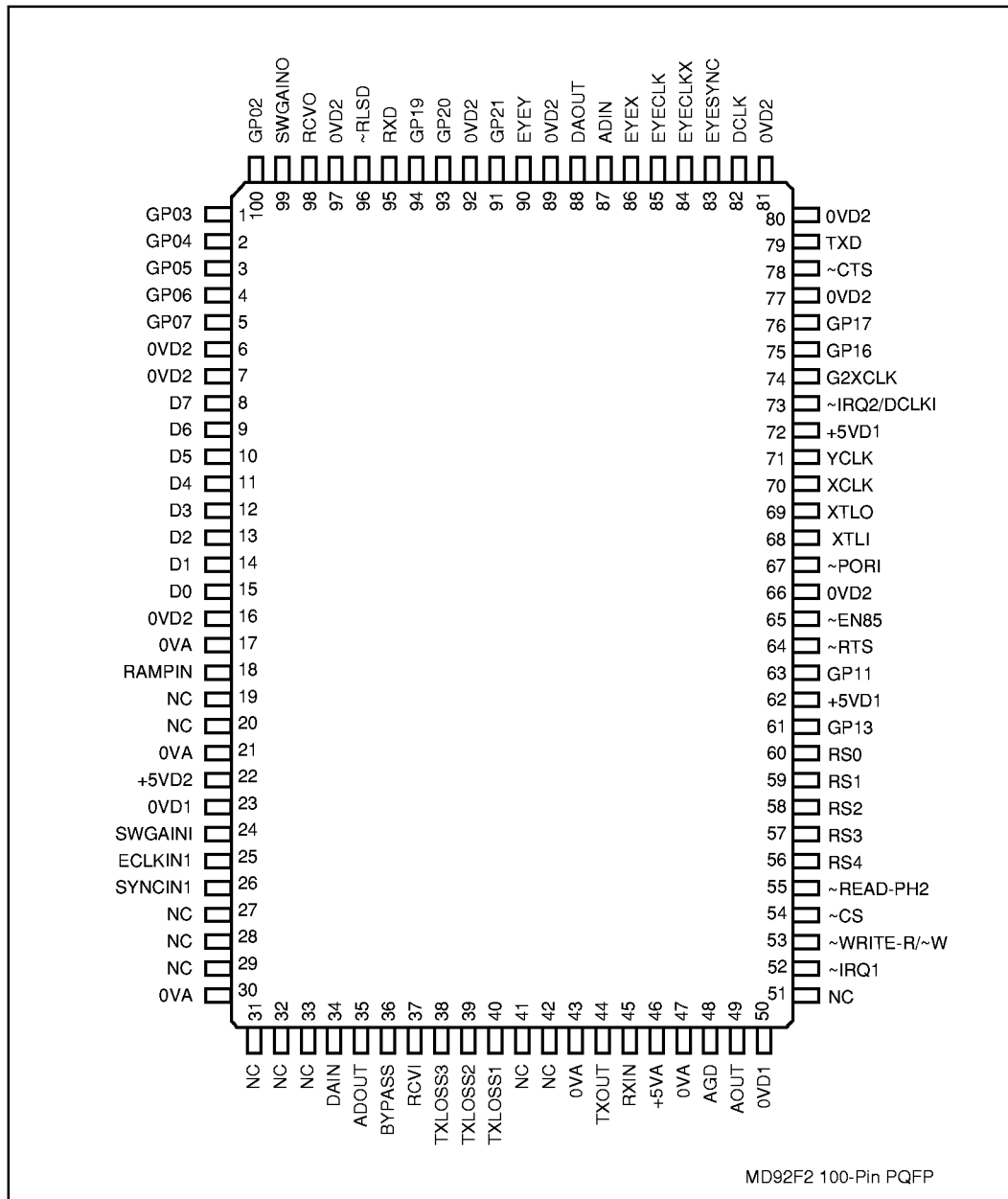


Figure 2. Pin Signals - 100-Pin PQFP

## NOTES

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