OKI Semiconductor

MSM7545

Voice Scrambler for Cordless Telephone

GENERAL DESCRIPTION

MSM7545 is a voice scrambler LSI for cordless telephone.

This LSI converts voice signal into scrambled voice signal and also restores scrambled voice signal to voice signal.

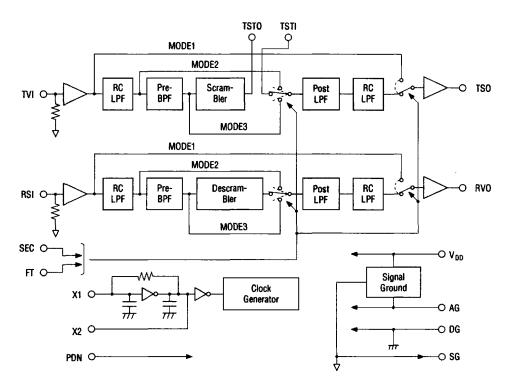
FEATURES

- This chip is available to transmit modern signal and also transmit scrambled voice signal through wireless transmit path (0.3 kHz to 3.0 kHz).
- Transmit function and receive function operate separately.
- Built-in band path filter (before voice scrambler).
- Built-in low path filter (after voice scrambler).
- Built-in crystal oscillation circuit.
- Wide range power supply voltage (2.8 V to 5.5 V).
- Package:

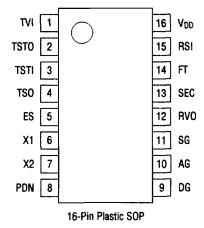
16-pin plastic SOP

(SOP16-P-300-K) (Product name: MSM7545MS-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



PIN DESCRIPTION

Pin No.	Name	Description						
1	TVI	Transmit voice signal input.						
2	TST0	Device to	Device test.					
3	TSTI	TSTO an	TSTO and TSTI should be connected directry.					
4	TSO	Scramble	ed voice si	gnał output.				
		Device to	Device test.					
5	ES	Please left open.						
	<u> </u>	Input an	d output co	onnected to the crystal oscillator.				
•	V4	3.6864 N	MHz crysta	shall be connected. When an external clock is applied for				
6	X1	MSM754	45's oscilat	tion source, it has to be input to X2. In this case, X2 has to be Al				
7	X2	coupled	with exteri	nal clock by the capacitor of 200 pF and X1 shall be left open.				
		Refer to	application	n circuit.				
		Power d	own contro	ol .				
_		"1" : Power down						
8	PDN	"0" : Power on						
		When di	gital "1" is	applied to PDN pin, all the path is powered down.				
9	DG		round, 0 V	<u> </u>				
10	AG	Analog ground, 0 V.						
	SG	Built-in analog signal ground.						
		The DC voltage is approximately half of V _{DD} .						
11		It is necessary to put a bypass capacitor from SG to GND and SG to V _{DD} in close						
		approximately to the device.						
12	RV0	Received	Received voice signal output.					
	250	Scramb	e mode an	d trough mode selection.				
13	SEC	Refer to FT pin description.						
		Voice signal path selection.						
		FT	SEC	Signal path				
		FI	SEC					
		0	0	Through mode 1: Input AMP output is connected to output				
				buffer.				
14	FT	0	1	Voice scrambler and descrambler work.				
		l .	1	Through mode 2: Only POST LPF is connected to the path.				
		1	0	This mode is available to use as a splatter				
			<u> </u>	filter.				
		1	1	Through mode 3: All filter is connected, scrambler and				
		l ——		descrambler doesn't work.				
		Transmi	it path and	Receive path also work.				
15	RSI		led voice is					
		Powers						
16	V _{DD}	A bypass capacitor between V _{DD} and AG, DG is indispensable to						
- •	.00	ensure the performance.						

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit		
Power Supply Voltage	V _{DD}	T- 0500	-0.3 to 7.0			
Analog Input Voltage *1	VIA	Ta = 25°C	-0.3 to V _{DD} + 0.3	 		
Digital Input Voltage *2	V _{ID}	With respect to AG and DG	-0.3 to V _{DD} + 0.3			
Operating Temperature	Top		-30 to 70	1		
Storage Temperature	TSTG	_	-55 to 150	oc		

^{*1} TVI, RSI, TSTI

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit	
	VDD	_	2.8	3.6	5.5	V	
Power Supply Voltage	AG, DG			0	_		
Operating Temperature	Тор		-30	25	70	°C	
Cristal Frequency	fx'TAL	_	3.6790	3.6864	3.6938	MHz	

^{*2} PDN, FT, SEC

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

 $(V_{DD} = 2.8 \text{ V to } 5.5 \text{ V}, \text{ Ta} = -30^{\circ}\text{C to } 70^{\circ}\text{C})$

Parameter	Symbol	Conditio	Min.	Тур.	Max.	Unit	
	loo	Operating	3.6 V	_	3.0	_	
2		mode	5.5 V		8.5	14.0	mA
Power Supply Current	IDDS	Power down	3.6 V		1.0	20	
		mode	5.5 V		1.0	20	
	ΙĻ	VIN = 0 V		-10	_	10	μA
Input Leakage Current *1	lін	VIN = VDD		-10	_	10	
Innua Malhana #d	VIL			0		0.6	ν
Input Voltage *1	ViH			0.8VDD	_	VDD	

^{*1} PDN, FT, SEC

Internal Signal Ground (SG)

 $(V_{DD} = 2.8 \text{ V to } 5.5 \text{ V}, Ta = -30^{\circ}\text{C to } 70^{\circ}\text{C})$

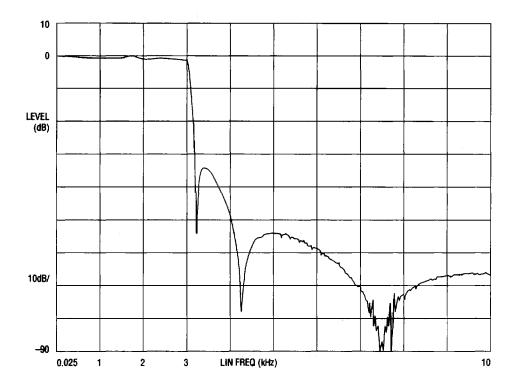
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
DC Voltage	Vsg	Without DC Load	$\frac{V_{DD}}{2} - 0.1$	V _{DD} 2	$\frac{V_{DD}}{2} + 0.1$	v

Analog Interface Characteristics

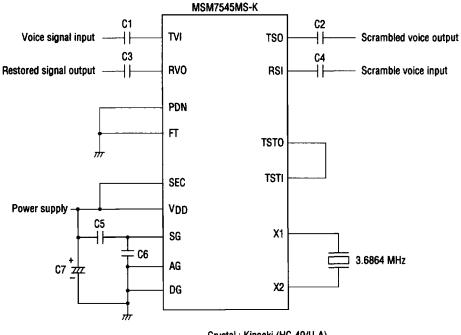
 $(V_{DD} = 2.8 \text{ V to } 5.5 \text{ V}, Ta = -30^{\circ}\text{C to } 70^{\circ}\text{C})$

Parameter	Symbol	Pin	Condition		Min.	Тур.	Max.	Unit
Input Resistance	Rin	TVI, RSI	fin≤4 kHz		40	100	300	kΩ
Maximum Input		TVI, RSI	Ann dilate	VDD = 2.8 V	_		1.2	Vpp
Signal Level	Vin	TSTI	fin = 1 kHz	VDD = 5.0 V	_		2.4	
Gain	Gin		fin =	1 kHz	-1	0	+1	dB
Output Resistance	Rout		fin ≤ 4 kHz		_		1	
Output Load Resistance	RLOAD	700			40	_	_	kΩ
Output Distortion	Host	TSO RVO			_	_	1	%
Out put Load Cpacitance	CLOAD	NVU	_			_	40	pF
Output DC Voltage	Voc		_		$\frac{VDD}{2} - 0.1$	VDD 2	VDD + 0.1	٧

POST-LPF FREQUENCY RESPONSE



APPLICATION CIRCUIT



C1, C2, C3, C4 = 0.1 μ F $C5, C6, C7 = 1.0 \mu F$

Crystal: Kinseki (HC-49/U-A)

External Clock Application

