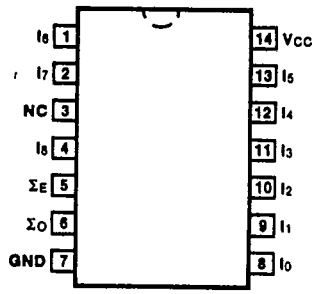
54S/74S280

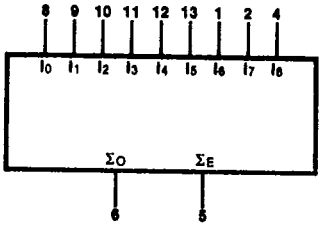
9-BIT PARITY GENERATOR/CHECKER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '280 is a high speed parity generator/checker that accepts nine bits of input data and detects whether an even or an odd number or these inputs are HIGH. If an even number of inputs are HIGH, the Sum Even output is HIGH. If an odd number are HIGH, the Sum Even output is LOW. The Sum Odd output is the complement of the Sum Even output.

LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +70°C	PKG TYPE
Plastic DIP (P)	A	74S280PC		9A
Ceramic DIP (D)	A	74S280DC	54S280DM	6A
Flatpak (F)	A	74S280FC	54S280FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

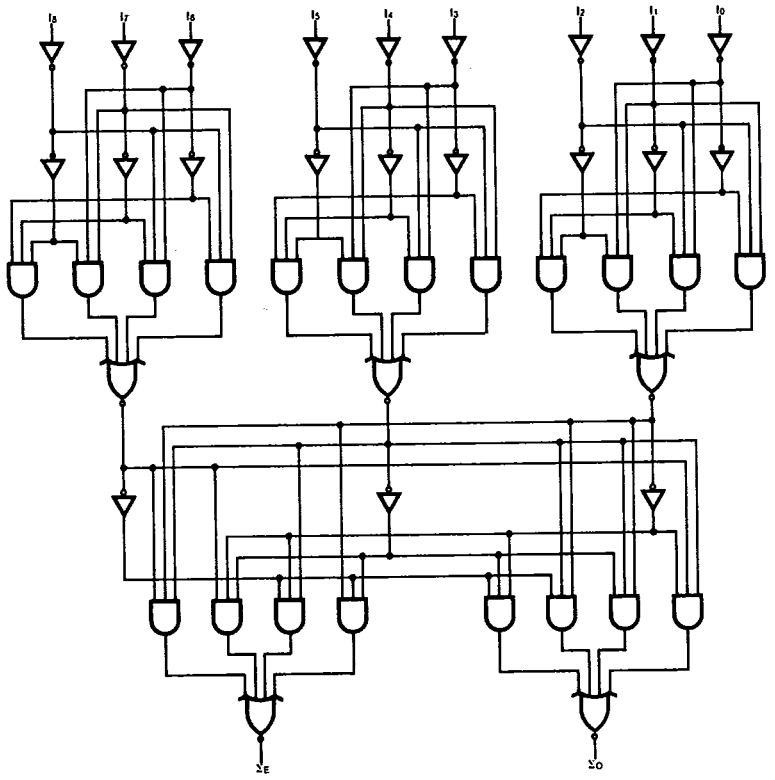
PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW
I0 — I8	Data Inputs	1.25.1.25
ΣO	Odd Parity Output	25/12.5
ΣE	Even Parity Output	25/12.5

TRUTH TABLE

NUMBER OF INPUTS I0 — I8 THAT ARE HIGH	OUTPUTS Σ EVEN	OUTPUTS Σ ODD
0, 2, 4, 6, 8,	H	L
1, 3, 5, 7, 9	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74S Min	54/74S Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		99	mA	V_{CC} = Max, T_A = 25°C All Inputs = Gnd
		XC		105		
		XM		94	mA	V_{CC} = Max, T_A = 125°C All Inputs = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/47S C_L = 15 pF R_L = 280 Ω Min	54/47S Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay I_n to Σ_E		21 18	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay I_n to Σ_O		21 18	ns	Figs. 3-1, 3-20