June 1991
Edition 3.0

FUJITSU

DATA SHEET

MB81C1001A-70L/-80L/-10L

CMOS 1M x 1 BIT NIBBLE MODE LOW POWER DRAM

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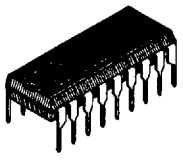
CMOS 1,048,576 X 1 Bit Nibble Mode Low Power DRAM

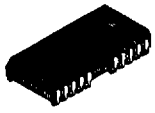
The Fujitsu MB81C1001A is a CMOS, fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1001A has been designed for mainframe memories, buffer memories, and video image memories requiring high speed, high–band width output with low power dissipation, as well as for memory systems of handheld computers which need very low power dissipation.

Fujitsu's advanced three–dimensional stacked capacitor cell technology gives the MB81C1001A high α–ray soft error immunity and extended refresh time.

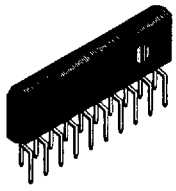
CMOS technology is used in the peripheral circuits to provide low power dissipation and high speed operation.



DIP–18P–M04



LCC–26P–M04



ZIP–20P–M02

FPT–24P–M04

FPT–24P–M05

PRODUCT LINE & FEATURES

Parameter	MB81C1001A –70L	MB81C1001A –80L	MB81C1001A –10L
$\overline{RAS}$ Access Time	70ns max.	80ns max.	100ns max.
Random Cycle Time	125ns min.	140ns min.	170ns min.
Address Access Time	35ns max.	40ns max.	50ns max.
$\overline{CAS}$ Access Time	20ns max.	20ns max.	25ns max.
Nibble Mode Cycle Time	40ns min.	40ns min.	45ns min.
Low Power Dissipation • Operating current	374mW max.	341mW max.	297mW max.
• Standby current	5.5mW max. (TTL level) / 1.4mW max. (CMOS level)		

- 1,048,576 words x 1 bit organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 64ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$–before–$\overline{RAS}$, or Hidden Refresh
- Nibble Mode, Read–Modify–Write capavility
- On chip substrate bias generator for high performance

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to VSS	V_{IN}, V_{OUT}	–1 to +7	V
Voltage of V_{CC} supply relative to VSS	V_{CC}	–1 to +7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	—	50	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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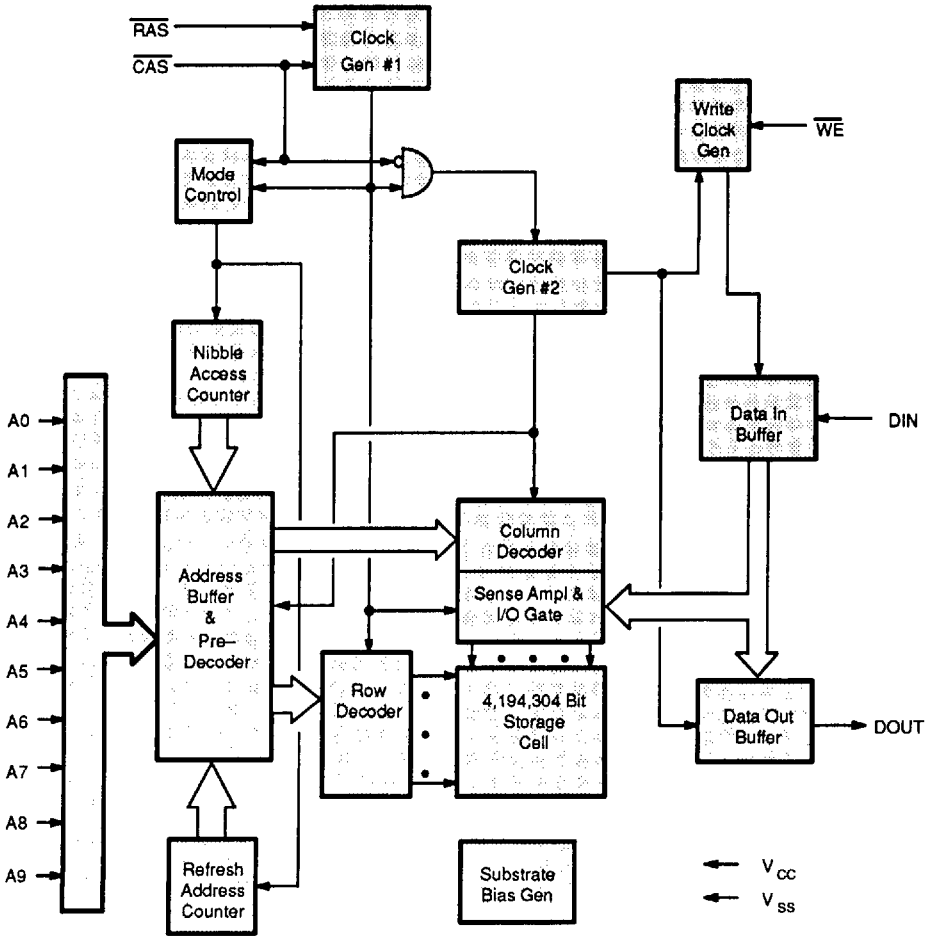
Fig. 1 – MB81C1001A DYNAMIC RAM – BLOCK DIAGRAM

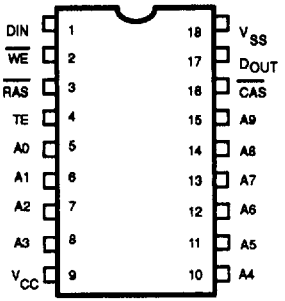


CAPACITANCE (T_A = 25°C, f = 1MHz)

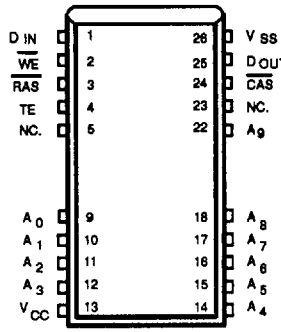
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9, D_{IN}	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	5	pF
Output Capacitance, D_{OUT}	C_{OUT}	—	6	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

18-Pin DIP:
(TOP VIEW)



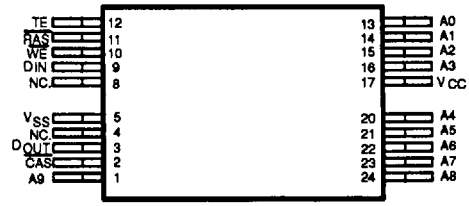
26-Pin SOJ:
(TOP VIEW)



24-Pin FPT :
(TOP VIEW)

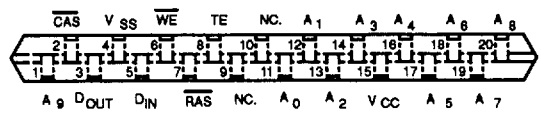
<Normal Bend : FPT-24P-M04>

<Reverse Bend : FPT-24P-M05>



Designator	Function
D_{IN}	Data Input.
D_{OUT}	Data Output.
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A9	Address inputs.
VCC	+5 volt power supply.
TE	Test Enable (will be available).
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

20-Pin ZIP:
(TOP VIEW)



RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	−2.0	—	0.8	V	

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty input bits are required to decode any one of 1,048,576 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0–through–A9 and latched with the row address strobe ($\overline{RAS}$) then, ten column address bits are input and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Data is written into the MB81C1001A during write or read–modify–write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. In an early write cycle, data input is strobed by $\overline{CAS}$, and set up and hold times are referenced to $\overline{CAS}$. In a delayed write or read–modify–write cycle, $\overline{WE}$ is set low after $\overline{CAS}$. Thus, data input is strobed by $\overline{WE}$, and set up and hold times are referenced to $\overline{WE}$.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD}, t_{RAD} (max).

tAA : from column address input when t_{RAD} is greater then t_{RAD} (max).

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) **Notes 3**

Parameter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	IOH = –5 mA	2.4	—	—	V
Output low voltage		V_{OL}	IOL = 4.2 mA	—	—	0.4	V
Input leakage current (any input)		$I_{I(L)}$	0V ≤ VIN ≤ 5.5V; 4.5V ≤ VCC ≤ 5.5V; VSS=0V;All other pins not under test =0V	–10	—	10	µA
Output leakage current		$I_{O(L)}$	0V ≤ VOUT ≤ 5.5V; Data out disabled	–10	—	10	µA
Operating current (Average power supply current) [2]	MB81C1001A–70L	ICC_1	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	68	mA
	MB81C1001A–80L					62	
	MB81C1001A–10L					54	
Standby current (Power supply current)	TTL level	ICC_2	$\overline{RAS}$=$\overline{CAS}$=VIH	—	—	1.0	mA
	CMOS level		$\overline{RAS}$=$\overline{CAS}$ ≥ VCC–0.2V			0.25	
Refresh current #1 (Average power supply current) [2]	MB81C1001A–70L	ICC_3	$\overline{CAS}$=VIH, $\overline{RAS}$ cycling; t_{RC}= min	—	—	68	mA
	MB81C1001A–80L					62	
	MB81C1001A–10L					54	
Nibble Mode current [2]	MB81C1001A–70L	ICC_4	$\overline{RAS}$ = VIL, $\overline{CAS}$ cycling; t_{NC} = min	—	—	22	mA
	MB81C1001A–80L					22	
	MB81C1001A–10L					20	
Refresh current #2 (Average power supply current) [2]	MB81C1001A–70L	ICC_5	$\overline{RAS}$ cycling ; $\overline{CAS}$–before–$\overline{RAS}$; t_{RC} = min	—	—	68	mA
	MB81C1001A–80L					62	
	MB81C1001A–10L					54	
Battery Back up current (Average power supply current)	MB81C1001A–70L	ICC_6	$\overline{RAS}$ cycling ; $\overline{CAS}$–before–$\overline{RAS}$; t_{RC} =125 µs, t_{RAS} =min. to 1 µs, D_{OUT}=open. Other pin ≥ Vcc–0.2V or ≤ 0.2V	—	—	250	µA
	MB81C1001A–80L						
	MB81C1001A–10L						

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1001A -70L		MB81C1001A -80L		MB81C1001A -10L		Unit
				Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	64	—	64	—	64	ms
2	Random Read/Write Cycle Time		t_{RC}	125	—	140	—	170	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	145	—	165	—	200	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	70	—	80	—	100	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	20	—	20	—	20	ns
6	Column Address Access Time	8,9	t_{AA}	—	35	—	40	—	50	ns
7	Output Hold Time		t_{OH}	0	—	0	—	0	—	ns
8	Output Buffer Turn on Delay Time		t_{ON}	0	—	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	15	—	20	—	20	ns
10	Transition Time		t_T	2	50	2	50	2	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	45	—	50	—	60	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	70	100000	80	100000	100	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	20	—	20	—	25	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	50	20	60	25	75	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	20	—	20	—	25	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	70	—	80	—	100	—	ns
18	$\overline{CAS}$ Precharge Time (C–B–R cycle)	17	t_{CPN}	10	—	10	—	10	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	10	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	12	—	15	—	15	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	35	15	40	20	50	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	35	—	40	—	50	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0		0		0		ns
29	Write Command Hold Time		t_{WCH}	10	—	12	—	15	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	10	—	12	—	15	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	20	—	25	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	12	—	15	—	20	—	ns
33	DIN Set Up Time		t_{DS}	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	10	—	12	—	15	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1001A -70L		MB81C1001A -80L		MB81C1001A -10L		Unit
				Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ to $\overline{WE}$ Delay Time	15	t_{RWD}	70	—	80	—	100	—	ns
36	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	20	—	20	—	25	—	ns
37	Column Address to $\overline{WE}$ Delay Time	15	t_{AWD}	35	—	40	—	50	—	ns
38	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	0	—	0	—	0	—	ns
39	$\overline{CAS}$ Set Up Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	ns
40	$\overline{CAS}$ Hold Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CHR}	10	—	12	—	15	—	ns
50	Nibble Mode Read/Write Cycle Time		t_{NC}	40	—	40	—	45	—	ns
51	Nibble Mode Read–Modify–Write Cycle Time		t_{NRWC}	60	—	60	—	70	—	ns
52	Access Time from $\overline{CAS}$ Precharge	9,16	t_{NPA}	—	35	—	35	—	40	ns
53	Nibble Mode $\overline{CAS}$ Precharge Time		t_{NCP}	10	—	10	—	10	—	ns

Notes:

1. Referenced to VSS
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   Icc depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC1}, I_{CC3} and I_{CC5} are specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC4} is specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. An Initial pause ($\overline{RAS}$ =$\overline{CAS}$ =VIH) of 200µs is required after power–up followed by any eight $\overline{RAS}$ –only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ –before–$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min)+ 2t_T + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and Dout pin will maintain high impedance state thoughout the entire cycle. If $t_{CWD} > t_{CWD}$ (min), $t_{RWD} > t_{RWD}$ (min), and $t_{AWD} > t_{AWD}$ (min), the cycle is a read modify–write cycle and data from the selected cell will apper at the Dout pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the Dout pin, and write operation can be exected by satisfying t_{RWL}, t_{CWL}, and t_{RAL} specifications.
16. t_{NPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{NCP} is long, t_{NPA} is longer than t_{NPA} (max).
17. Assumes that $\overline{CAS}$ –before– $\overline{RAS}$ refresh only.

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Fig. 2 – t_{RAC} vs. t_{RCD}

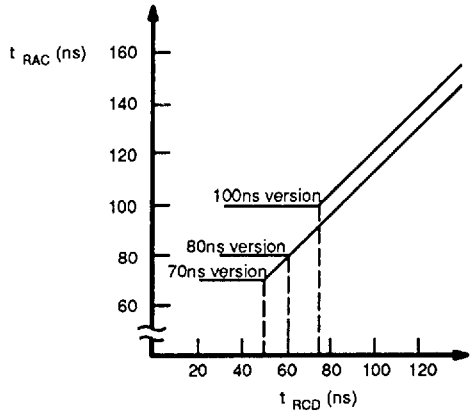
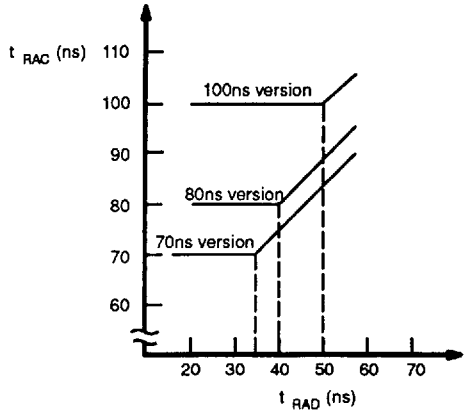


Fig. 3 – t_{RAC} vs. t_{RAD}



FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	Yes *1	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	Yes *1	$t_{WCS} \geq t_{WCS}$ (min)
Read–Modify–Write Cycle	L	L	H → L	Valid	Valid	X → Valid	Valid	Yes *1	$t_{CWD} \geq t_{CWD}$ (min)
$\overline{RAS}$–only Refresh Cycle	L	H	X	Valid	—	—	High-Z	Yes	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	X	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H → L	L	X	—	—	—	Valid	Yes	Previous data is kept

Notes:

X : "H" or "L"
*1: It is impossible in Nibble Mode.

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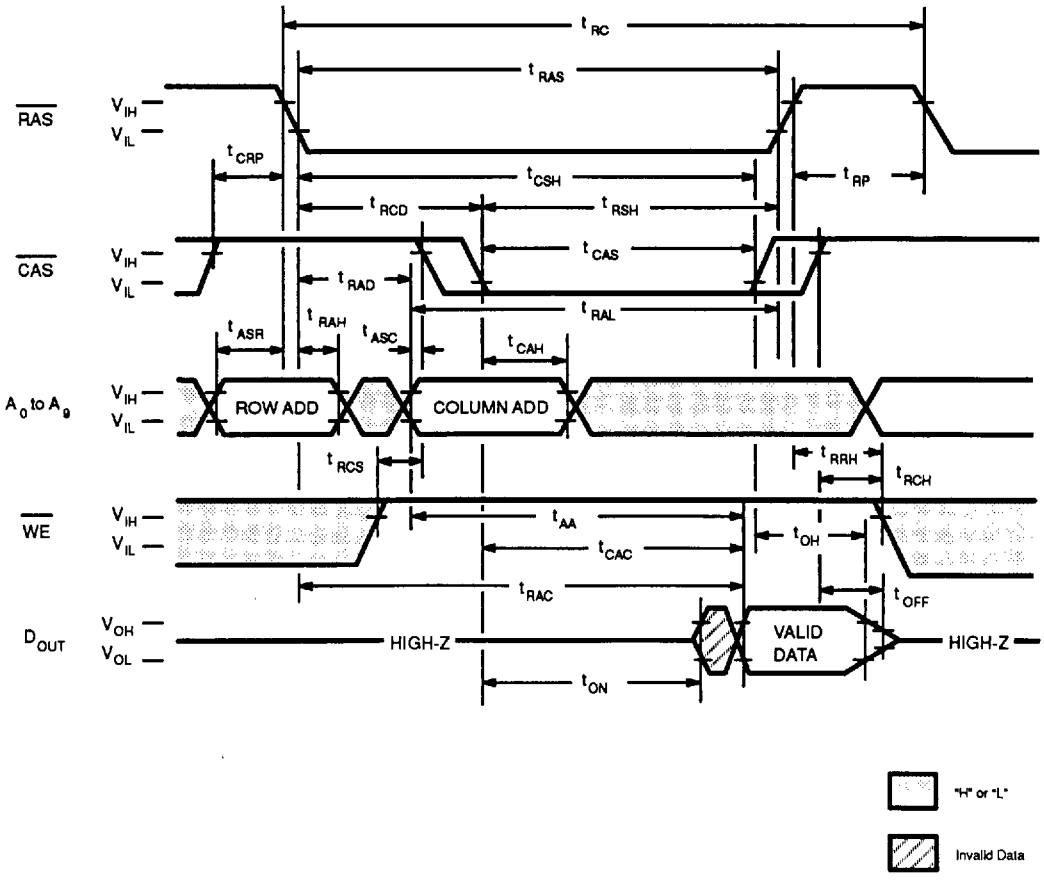
Fig. 4 – READ CYCLE



DESCRIPTION

The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" throughout the cycle. The row and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output remains valid with $\overline{CAS}$ "L", ie., if $\overline{CAS}$ goes "H", the data becomes invalid after tOH is satisfied. The access time is determined by $\overline{RAS}$ (tRAC), $\overline{CAS}$ (tCAC), or Column address input (tAA). If tRCD ($\overline{RAS}$ to $\overline{CAS}$ delay time) is greater than the specification, the access time is tAA.

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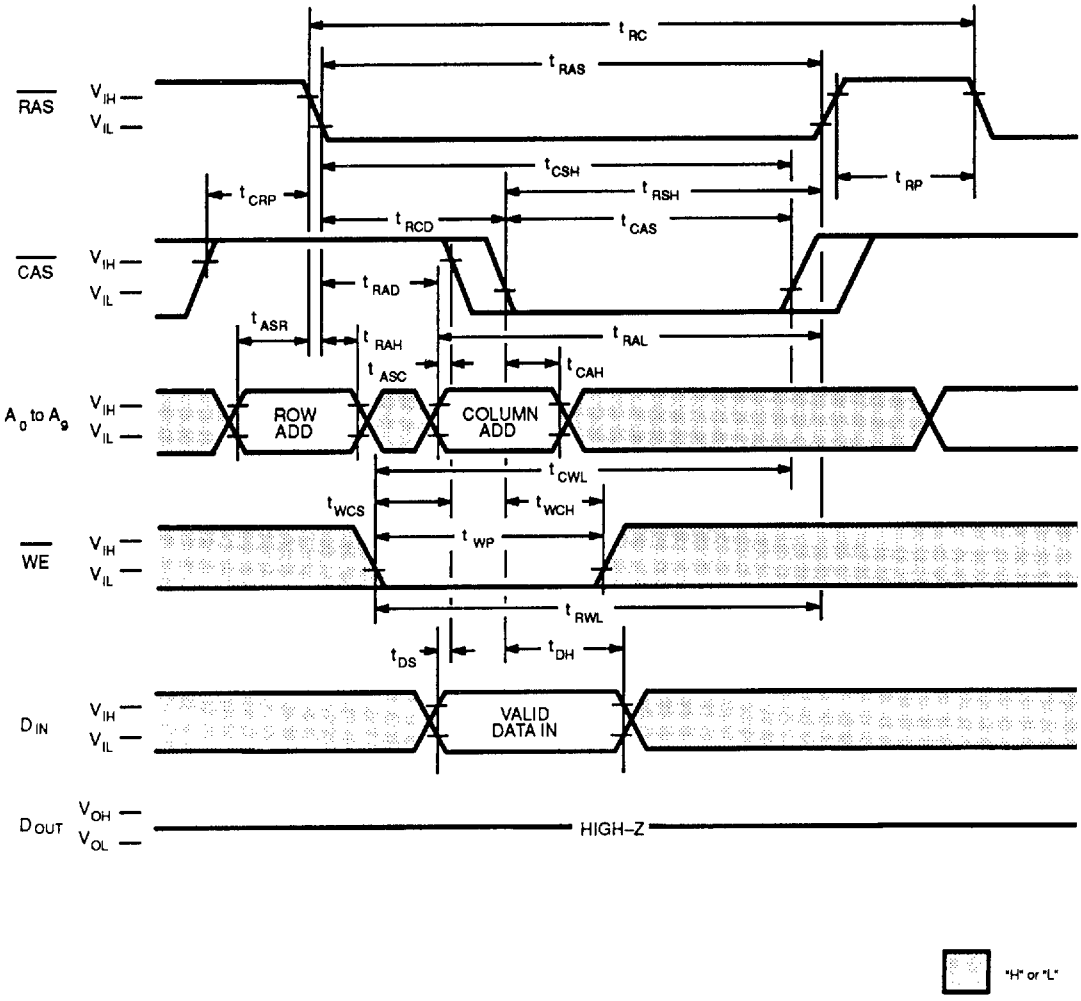
Fig. 5 – WRITE CYCLE (Early Write)



DESCRIPTION

The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and DIN pins. The data on DIN pin is latched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, tRWL and tRAL must be satisfied with the specifications.

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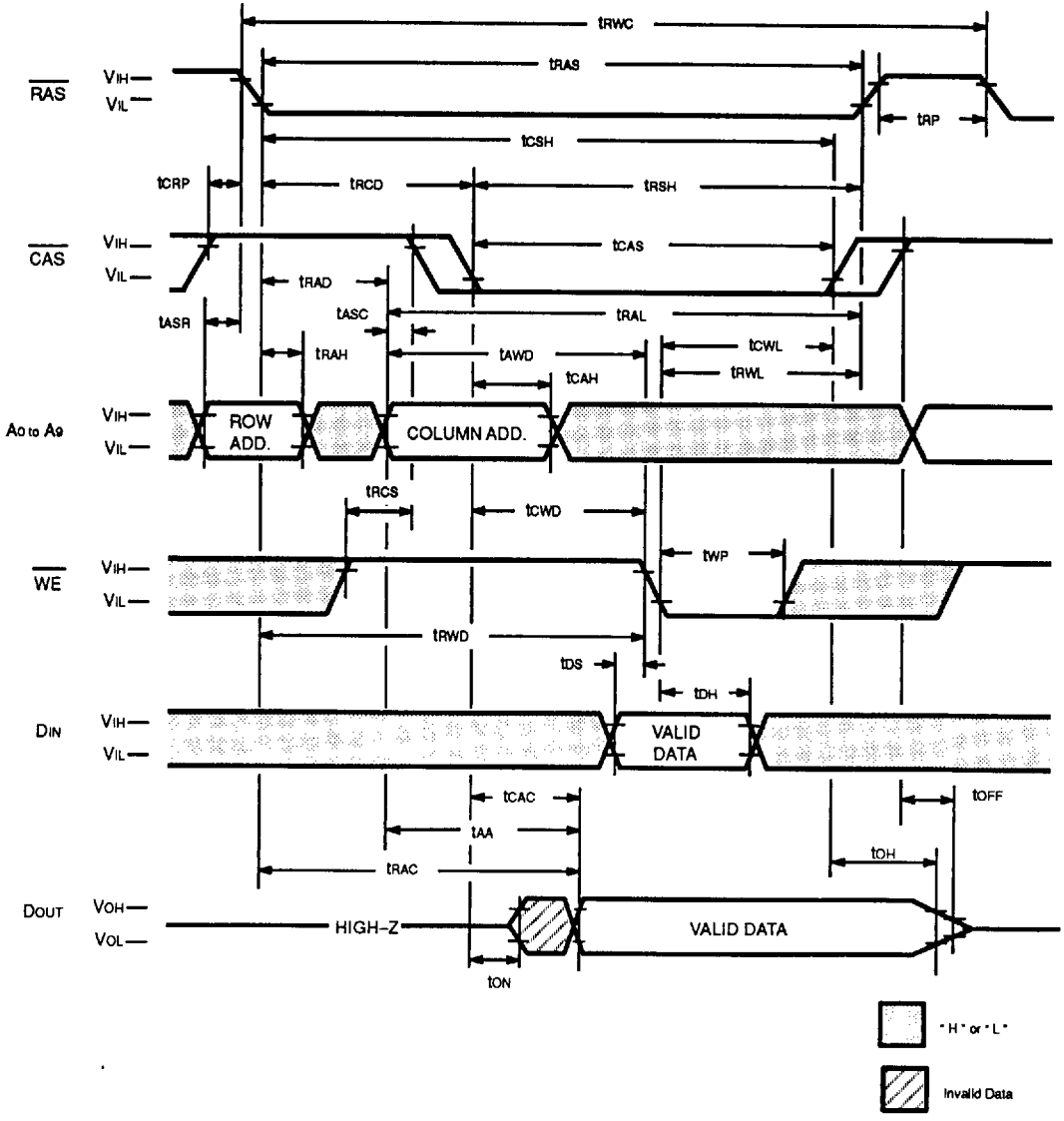
Fig. 6 – READ WRITE/READ–MODIFY–WRITE CYCLE



DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from "H" to "L" after the data appears on the DOUT pin. After the current data is read out, modified data can be rewritten into the same address quickly.

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Fig. 7 – NIBBLE MODE READ CYCLE

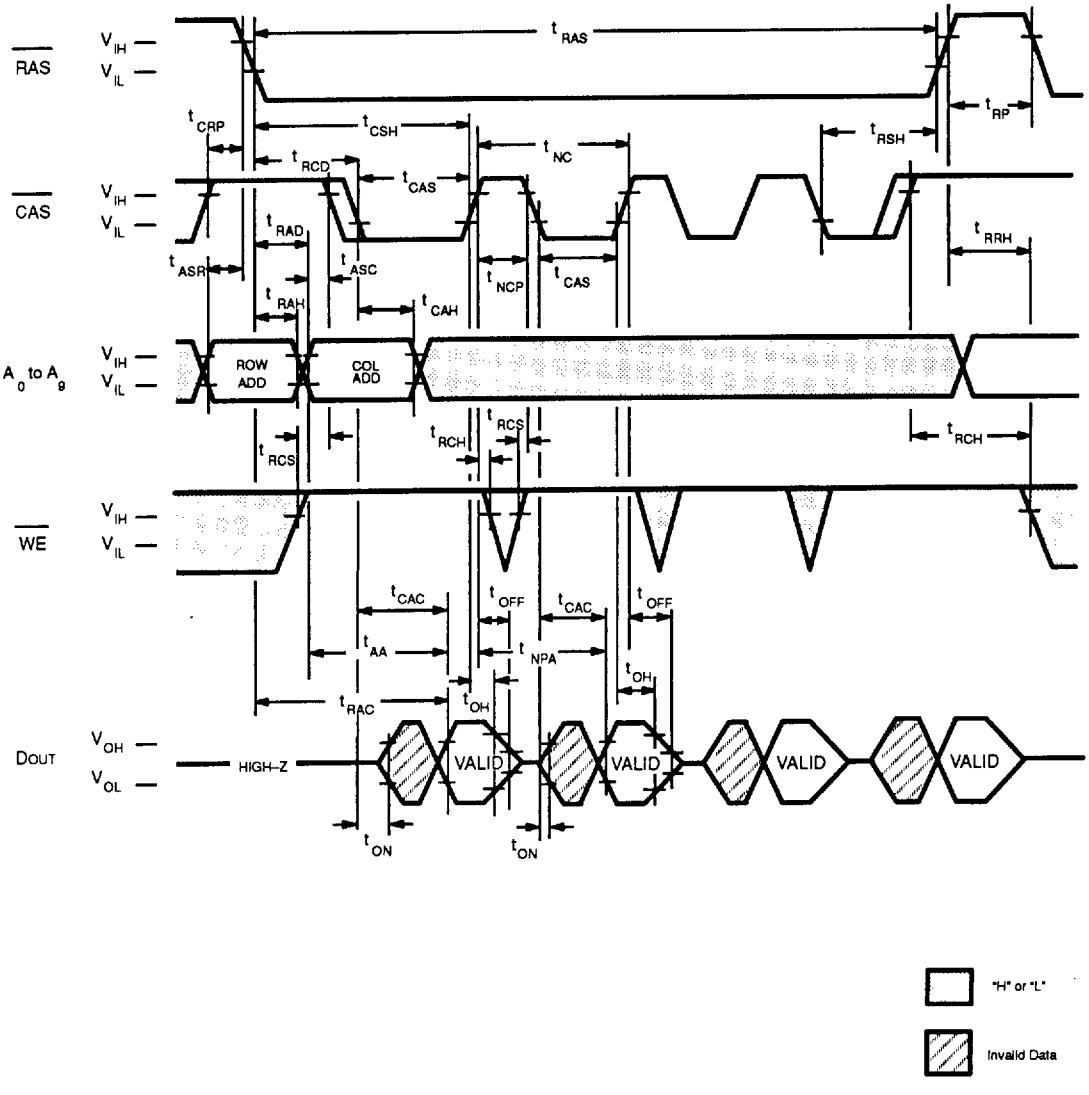

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Fig. 8 – NIBBLE MODE WRITE CYCLE (Early Write)

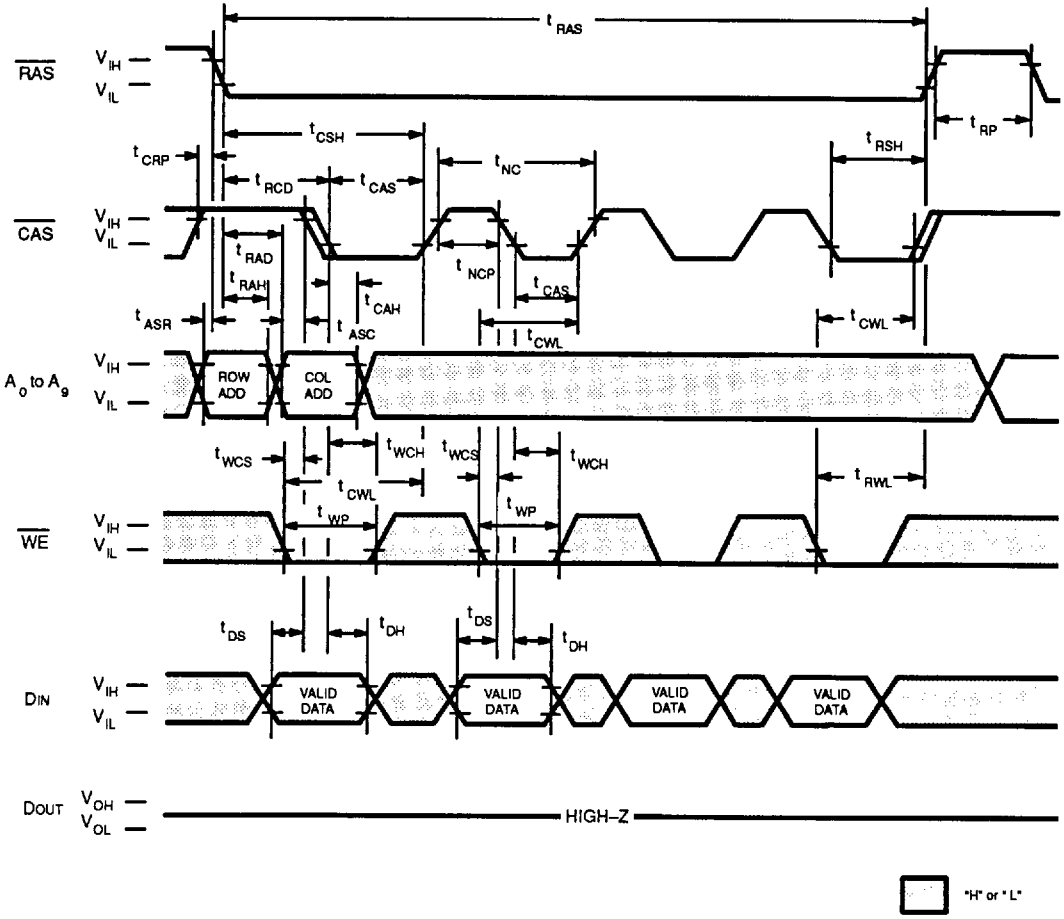

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Fig. 9 – NIBBLE MODE READ–MODIFY–WRITE CYCLE

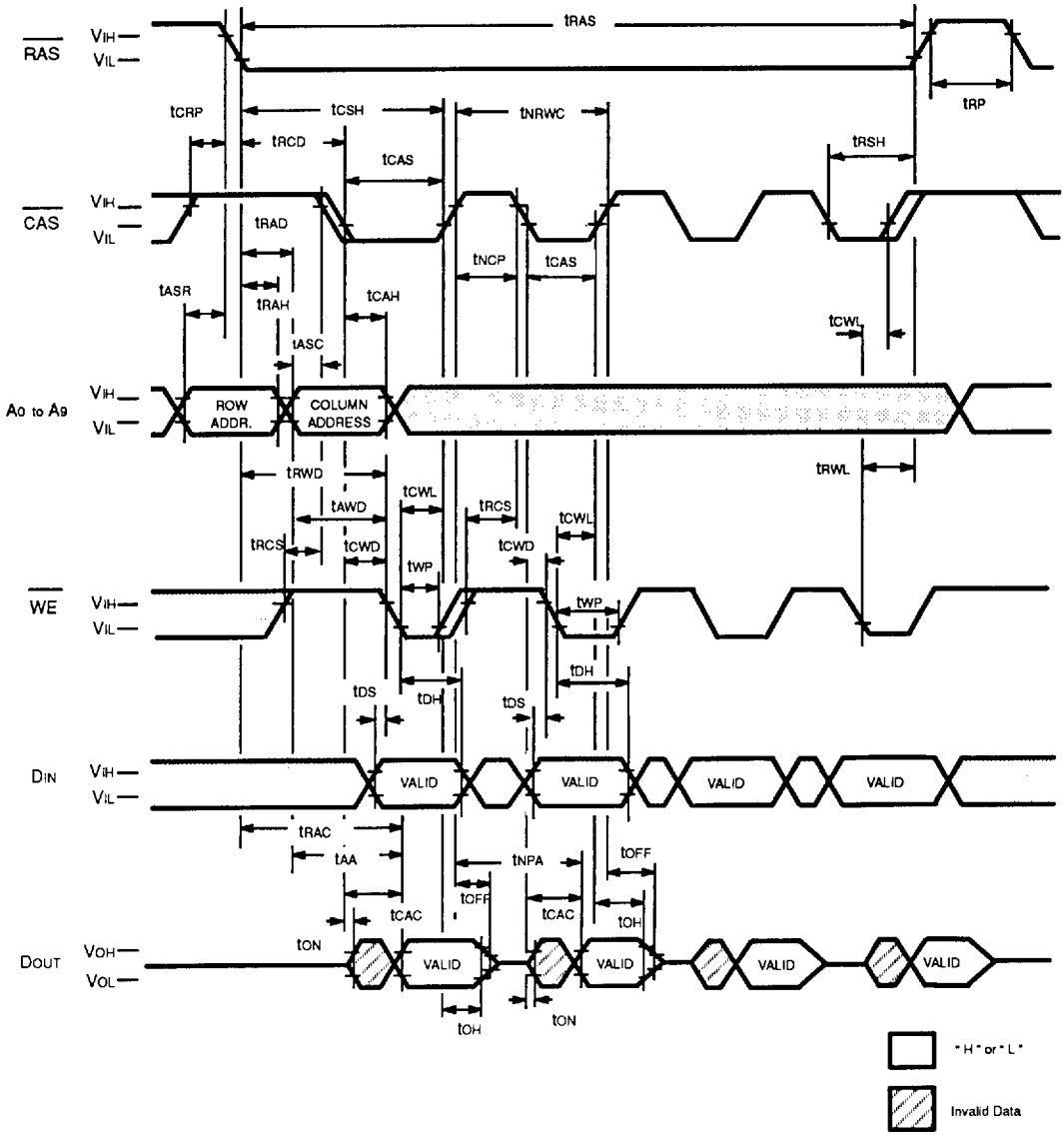
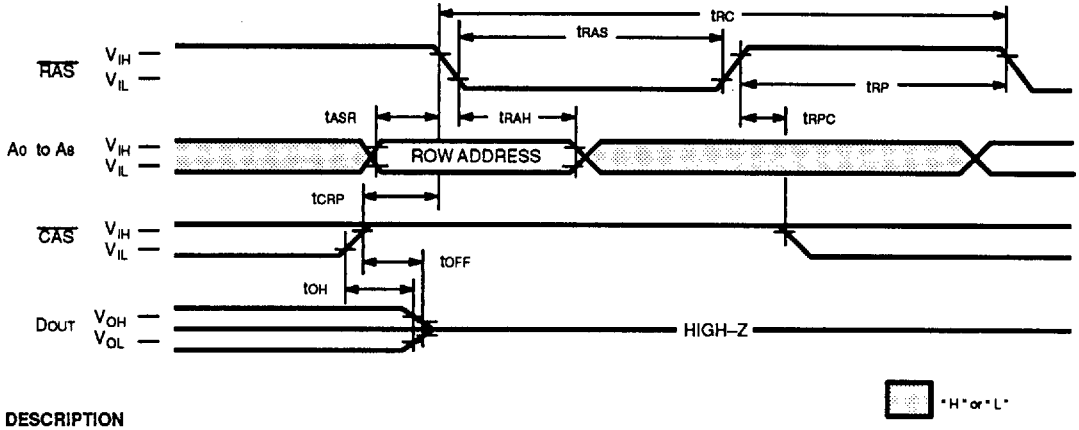


Fig. 10 – $\overline{RAS}$–ONLY REFRESH CYCLE
NOTE: A9, $\overline{WE}$, DIN = " H " or " L "

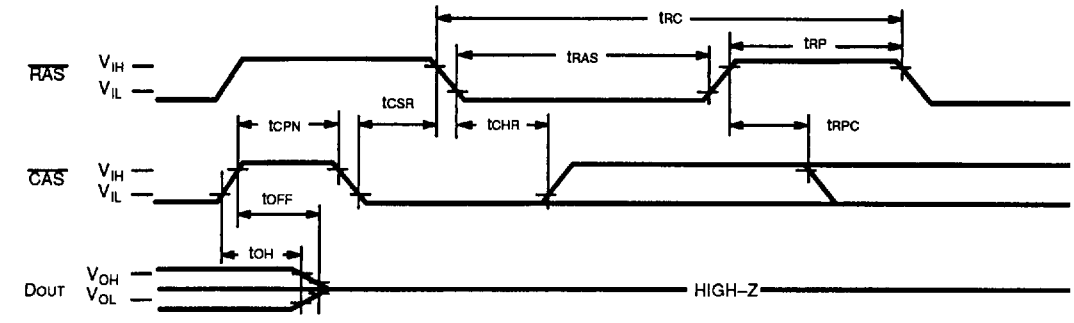


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2–milliseconds. Three refresh modes are available: $\overline{RAS}$–only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, DOUT pin is kept in a high-impedance state.

Fig. 11 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH CYCLE
NOTE: A0 to A9, $\overline{WE}$, DIN = " H " or " L "

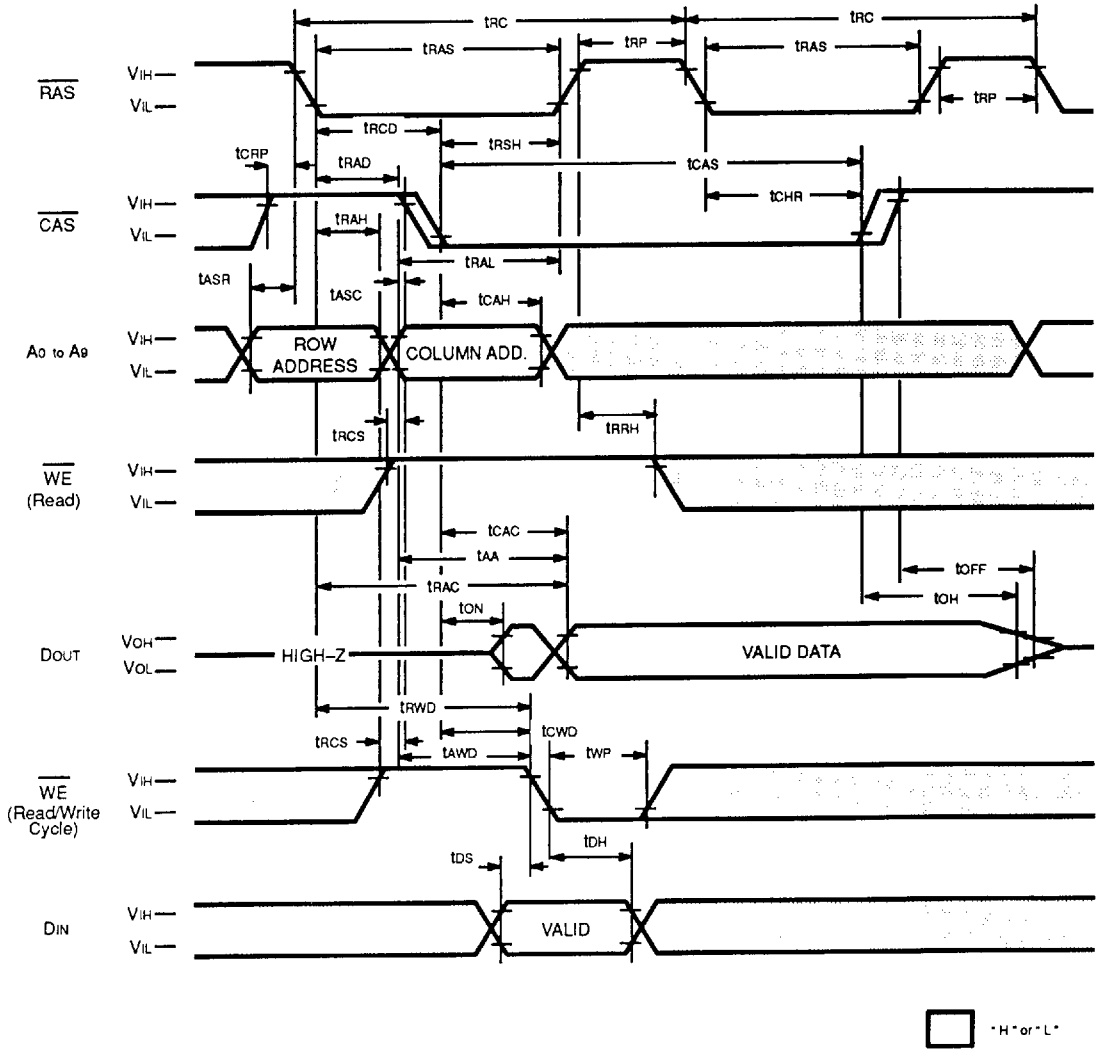


DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (tCSR) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

1

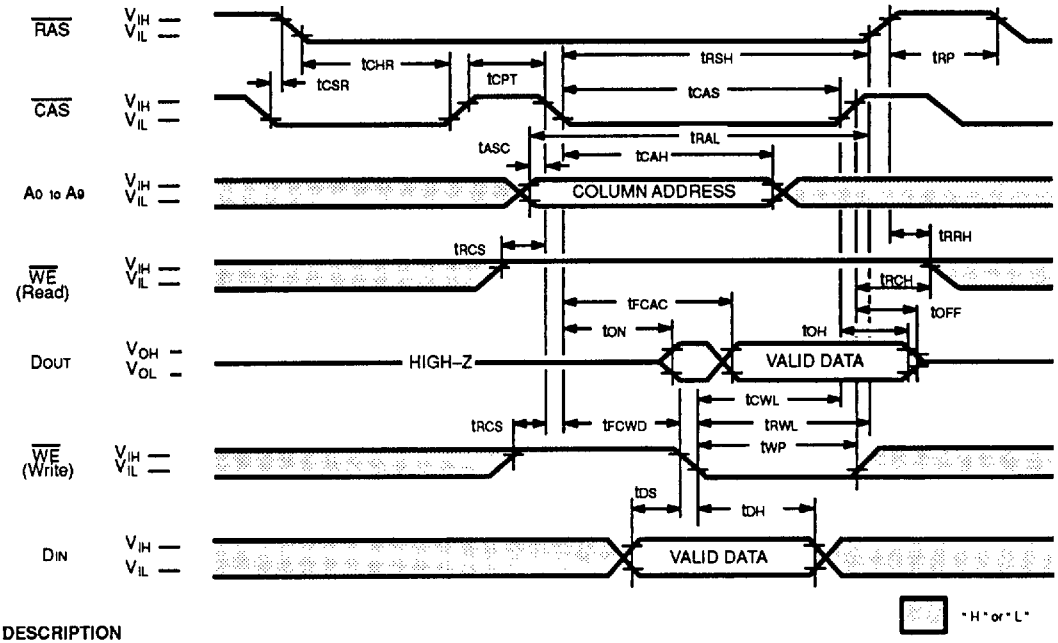
Fig. 12 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig. 13 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If, after a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A9 are defined by the on-chip refresh counter. The bit A9 is set high internally.
Column Address: Bits A0 through A9 are defined by latching levels on A0–A9 at the second falling edge of $\overline{CAS}$.

The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test procedure is as follows ;

1) Initialize the internal refresh address counter by using 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 512 row addresses at the same column address by using normal write cycles.
4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using $\overline{CAS}$–before–$\overline{RAS}$ refresh counter test (read–modify–write cycles). Repeat this procedure 512 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4) by using normal read cycle for all 512 memory locations.
6) Complement test pattern and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

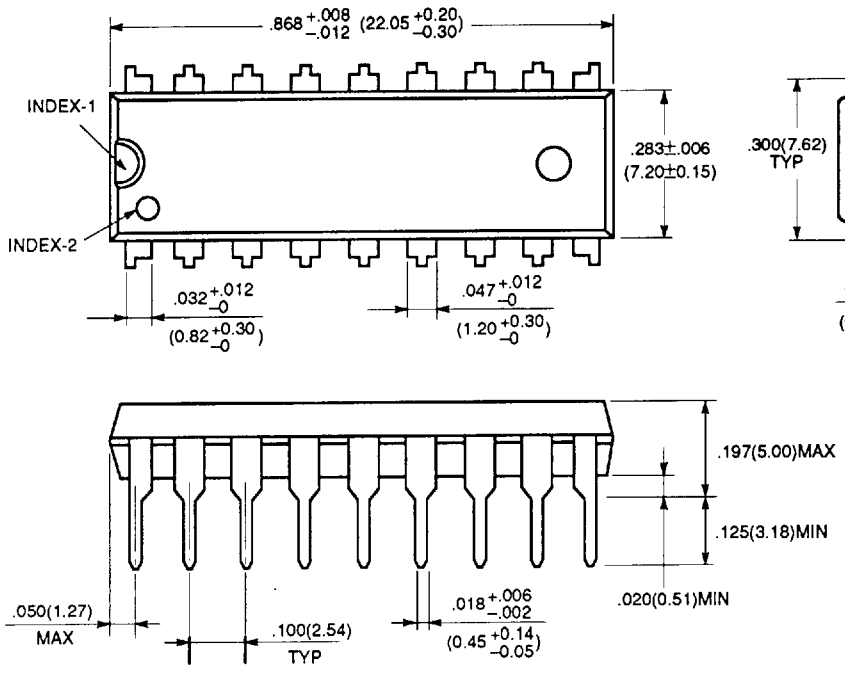
No.	Parameter	Symbol	MB81C1001A -70L		MB81C1001A -80L		MB81C1001A -10L		Unit
			Min	Max	Min	Max	Min	Max	
90	Access Time from $\overline{CAS}$	t_{FCAC}	—	45	—	50	—	60	ns
91	$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{FCWD}	45	—	50	—	60	—	ns
92	$\overline{CAS}$ Precharge Time	t_{CPT}	20	—	20	—	20	—	ns

Note . Assumes that $\overline{CAS}$–before–$\overline{RAS}$ refresh counter test cycle only.

PACKAGE DIMENSIONS

(Suffix: –P)

18-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-18P-M04)

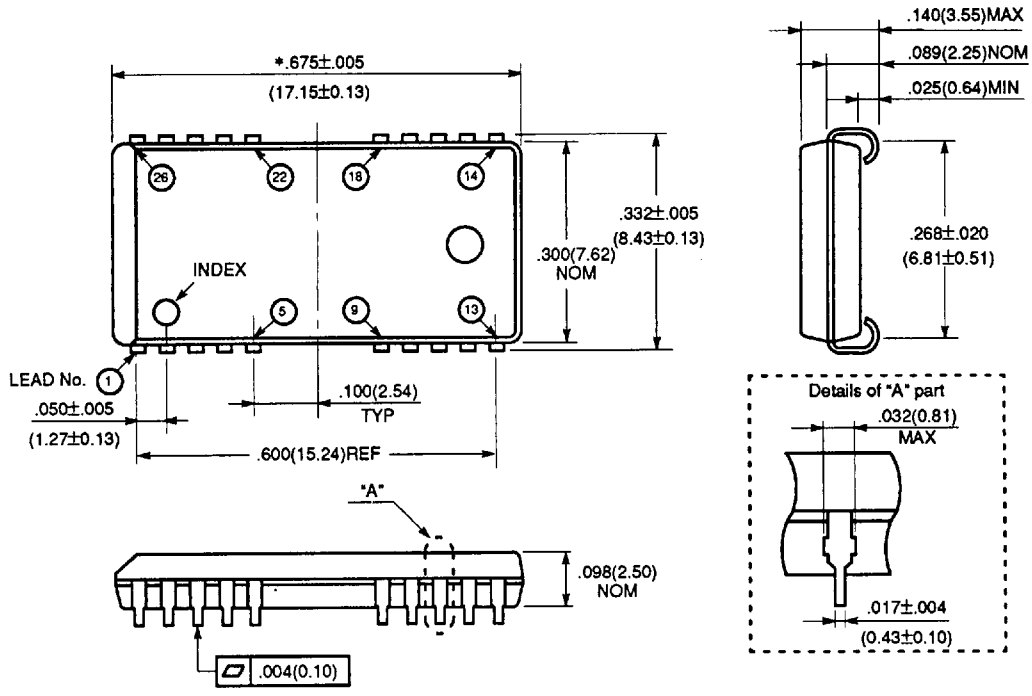


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-26P-M04)

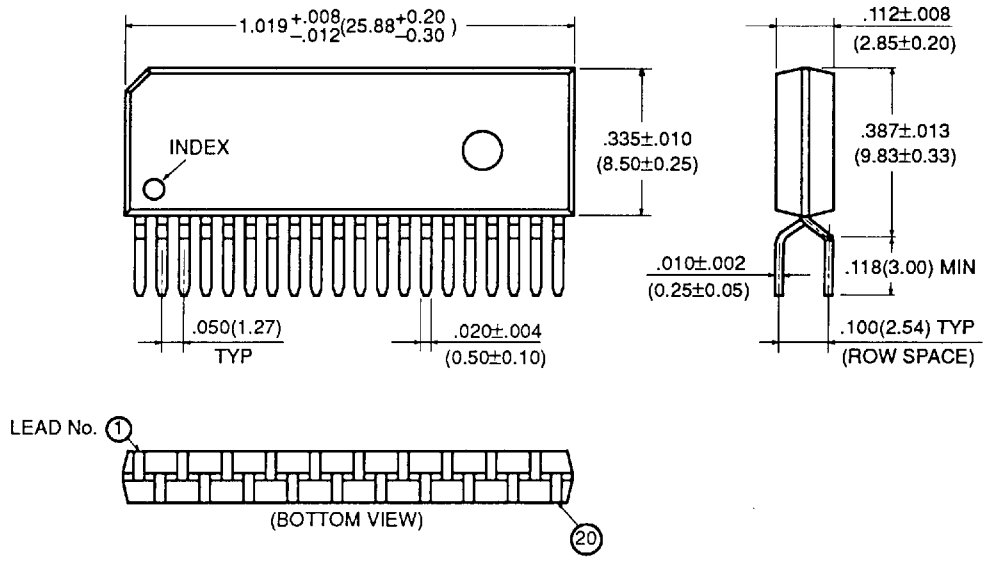


Note: 1. *:This dimension includes resin protrusion. (Each side:.006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.
3. Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –PSZ)

20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE
(CASE No.: ZIP-20P-M02)

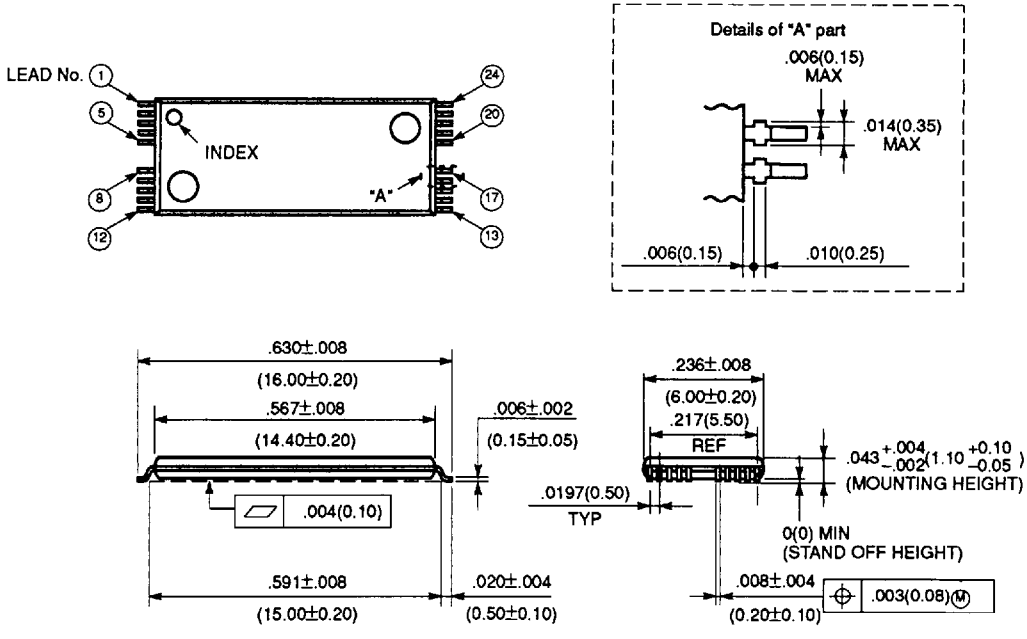


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –PFTN)

24-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-24P-M04)

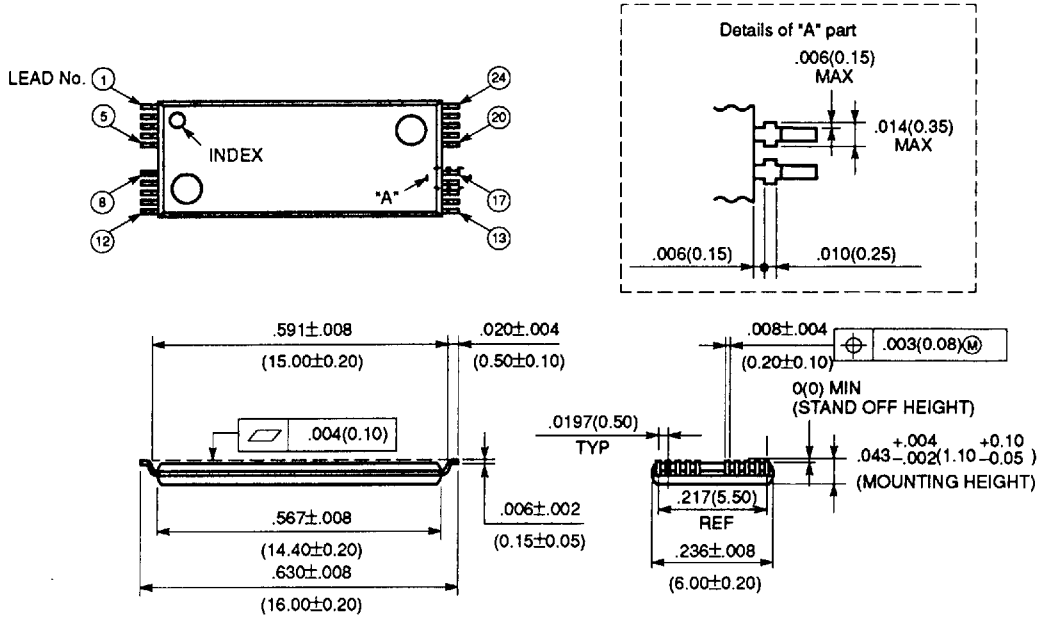


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –PFTR)

24-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-24P-M05)



Dimensions in
inches (millimeters)