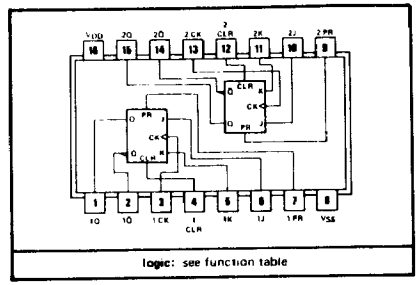
TYPES TF4027A, TP4027A
DUAL J-K FLIP-FLOPS

SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4027A
- Toggle Rate . . . 8 MHz Typical at V_{DD} = 10 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see function table

description

These circuits are dual J-K-type transition-operated master-slave flip-flops with buffered outputs, independent direct overriding preset and clear inputs, and J, K, and clock inputs. While the clock is low, the data at the J and K inputs is entered into the master section, which is isolated from the slave section. On the rising transition of the clock, the J and K inputs are disabled and data previously set up in the master section is transferred to the slave section. Circuit logic for various input configurations is shown in the function table.

Presetting and clearing are independent of the clock and are accomplished by a high-level voltage at the respective input. The $\overline{Q}$ output is complementary to the Q output except for the nonstable situation that exists when both preset and clear inputs are simultaneously high.

FUNCTION TABLE
(EACH FLIP-FLOP)

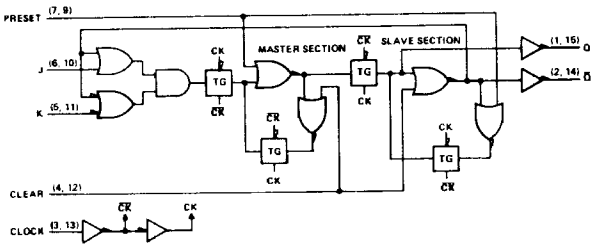
INPUTS					OUTPUTS	
PRESET	CLEAR	CK	J	K	Q	$\overline{Q}$
H	L	X	X	X	H	L
L	H	X	X	X	L	H
H	H	X	X	X	H*	H*
L	L	↑	L	L	Q_0	$\overline{Q}_0$
L	L	↑	H	L	H	L
L	L	↑	L	H	L	H
L	L	↑	H	H	TOGGLE	
L	L	L	X	X	Q_0	$\overline{Q}_0$

See explanation of function tables on pages 16 and 17.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (low) level.

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and on following page	Page 63, Group 2, except as on following page

functional block diagram



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recommended operating conditions

		TF4027A				TP4027A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Pulse width, t_w	Clock high or low	330		110		500		165		ns
	Preset or clear	200		80		300		120		
Setup time, t_{su}		150		50		200		75		ns

electrical characteristics

PARAMETER	TEST CONDITIONS†		TF4027A				TP4027A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{OH} High-level output current	V_{IH} = V_{DD}, V_{IL} = 0, V_O = V_{OH} min	T_A = MIN	-0.65		-0.8		-0.35		-0.4		mA
		T_A = 25°C	-0.5		-0.65		-0.3		-0.35		
		T_A = MAX	-0.35		-0.45		-0.25		-0.3		
I_{OL} Low-level output current	V_{IH} = V_{DD}, V_{IL} = 0, V_O = V_{OL} max	T_A = MIN	0.5		1.25		0.35		0.75		mA
		T_A = 25°C	0.4		1		0.3		0.6		
		T_A = MAX	0.3		0.75		0.25		0.5		

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TF4027A				TP4027A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 50 pF§, R_L = 200 kΩ, See Note 1	1.5		4.5		1		3		MHz
t_{PLH} or t_{PHL}	Clock	Q or $\bar{Q}$			420		185		550		250	ns
t_{PLH} or t_{PHL}	Preset or Clear	Q or $\bar{Q}$			320		185		450		250	ns
t_{TLH} or t_{THL}		Any			235		130		300		175	ns

‡f_{max} = Maximum clock frequency
t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
t_{TLH} = Transition time, low-to-high-level output
t_{THL} = Transition time, high-to-low-level output
§With a 15-pF load, these devices switch with times similar to those of the RCA CD4027A.
NOTE 1: See load circuit and voltage waveforms on page 170.

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