# P-Channel Enhancement-Mode Vertical DMOS FET Quad Array

## Ordering Information

| $BV_{DSS}$ / $BV_{DGS}$ | $R_{DS(ON)}$ (max) | $I_{D(ON)}$ (min) | Order Number / Package |
|---|---|---|---|
| | | | Quad Ceramic DIP* |
| -90V | 5.0Ω | -1.0A | VQ2006P |

* 14-pin side-brazed ceramic DIP.

### High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

## Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low $C_{ISS}$ and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

## Applications

- Motor control
- Convertors
- Amplifiers
- Switches
- Power supply circuits
- Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

## Absolute Maximum Ratings

| | |
|---|---|
| Drain-to-Source Voltage | $BV_{DSS}$ |
| Drain-to-Gate Voltage | $BV_{DGS}$ |
| Gate-to-Source Voltage | ± 30V |
| Operating and Storage Temperature | -55°C to +150°C |
| Soldering Temperature* | 300°C |

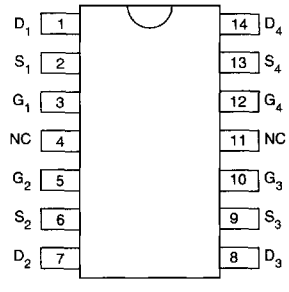
* Distance of 1.6 mm from case for 10 seconds.

## Advanced DMOS Technology

These enhancement-mode (normally-off) DMOS FET arrays utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex quad arrays use four independent DMOS transistors. They are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

## Pin Configuration




top view

14-pin DIP

## Thermal Characteristics ($T_A$ = 25°C)

| Test | Unit | Each Transistor | All Four Transistors |
|---|---|---|---|
| Total Power Dissipation | Watts | 1.3 | 2.0 |
| Thermal Resistance | °C/W | 96.2 | 62.5 |
| Continuous Drain Current | A | -0.41 | — |
| Pulsed Drain Current | A | -3.0 | — |

## Electrical Characteristics (@ 25°C unless otherwise specified)

| Symbol | Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-to-Source Breakdown Voltage | -90 | | | V | $V_{GS}$ = 0V, $V_{DS}$= -10µA |
| $V_{GS(th)}$ | Gate Threshold Voltage | -1.4 | -1.8 | -4.5 | V | $V_{GS}$ = $V_{DS}$, $I_D$ = -1mA |
| $I_{GSS}$ | Gate Body Leakage | | | -100 | nA | $V_{GS}$ = ±30V, $V_{DS}$ = 0V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | | | -10 | µA | $V_{GS}$ = 0V, $V_{DS}$= Max Rating |
| | | | | -500 | | $V_{GS}$ = 0V, $V_{DS}$ = 0.8 Max Rating<br>$T_A$ = 125°C |
| $I_{D(ON)}$ | ON-State Drain Current | -1.0 | | | A | $V_{GS}$ = -10V, $V_{DS}$ = -10V |
| $R_{DS(ON)}$ | Static Drain-to-Source ON-State Resistance | | 2.5 | 5.0 | Ω | $V_{GS}$ = -10V, $I_D$ = -1A |
| $G_{FS}$ | Forward Transconductance | 200 | | | m ℧ | $V_{DS}$ = -10V, $I_D$ = -0.5A |
| $C_{ISS}$ | Input Capacitance | | | 150 | pF | $V_{GS}$ = 0V, $V_{DS}$ = -25V<br>f = 1 MHz |
| $C_{OSS}$ | Common Source Output Capacitance | | | 65 | | |
| $C_{RSS}$ | Reverse Transfer Capacitance | | | 25 | | |
| $t_r$ | Rise Time | | | 15 | ns | $V_{DD}$ = -25V, $I_D$ = -0.5A<br>$R_{GEN}$ = 25Ω |
| $t_{d(ON)}$ | Turn-ON Delay Time | | | 40 | | |
| $t_f$ | Fall Time | | | 30 | | |
| $t_{d(OFF)}$ | Turn-OFF Delay Time | | | 30 | | |
| $V_{SD}$ | Diode Forward Voltage Drop | | | -1.8 | V | $V_{GS}$ = 0, $I_{SD}$ = -1A |

**Notes:**
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit