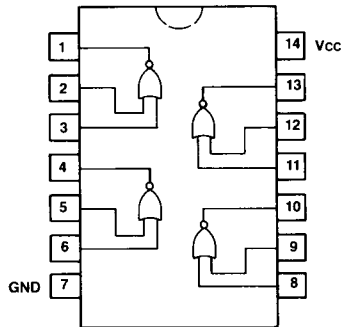


## Quad 2-Input Positive NOR Gate

The LS02 is a bipolar, NPN, sealed-junction, silicon integrated circuit. It is manufactured in low-power Schottky technology and is available in a wire-bonded, 14-pin plastic DIP or surface mount package.



## Electrical Characteristics

$V_{CC} = 5.0 \pm 0.5$  V,  $T_A = -55$  to  $+125^\circ\text{C}$  (WA-LS)

$V_{CC} = 5.0 \pm 0.25$  V,  $T_A = 0$  to  $70^\circ\text{C}$  (WP90222L2)

$V_{CC} = 5.0 \pm 0.5$  V,  $T_A = -40$  to  $+85^\circ\text{C}$  (WA-LSD, WP91397L2)

Parameter	Symbol	WA-LS		WP, WA-LSD		Units
		Min	Max	Min	Max	
Output Voltage, $V_{CC} = 4.5$ V (WA-LS), $4.75$ V (WP, WA-LSD)						
Low, $I_{OL} = 4.0$ mA	$V_{OL}$	—	0.4	—	0.4	V
$I_{OL} = 8.0$ mA	$V_{OL}$	—	0.5	—	0.5	V
High, $I_{OH} = -0.4$ mA	$V_{OH}$	2.5	—	2.7	—	V
Input Voltage, $V_{CC} = 4.5$ V (WA-LS), $4.75$ V (WP, WA-LSD)						
Low	$V_{IL}$	—	0.7	—	0.8*	V
High	$V_{IH}$	2.0	7.5	2.0	5.5	V
Clamp, $I_{IN} = -18.0$ mA	$V_{IK}$	—	-1.5	—	-1.5	V
Input Current, $V_{CC} = 5.5$ V (WA-LS), $5.25$ V (WP, WA-LSD)						
Low, $V_{IL} = 0.4$ V	$I_{IL}$	—	-0.4	—	-0.4	mA
High, $V_{IH} = 2.7$ V	$I_{IH}$	—	20.0	—	20.0	$\mu\text{A}$
@ $V_I$ max, $V_I = 7.0$ V (WA-LS), $5.5$ V (WP, WA-LSD)	$I_I$	—	0.1	—	0.1	mA
Output Current, $V_{CC} = 5.5$ V (WA-LS), $5.25$ V (WP, WA-LSD)						
Short-Circuit	$I_{OS}$	-20.0	-100.0	-20.0	-100.0	mA
Supply Current, $V_{CC} = 5.5$ V (WA-LS), $5.25$ V (WP, WA-LSD)						
Output Low	$I_{CCL}$	—	5.4	—	5.4	mA
Output High	$I_{CCH}$	—	3.2	—	3.2	mA

\* WA-LSD, WP91397L2:  $V_{IL} = 0.7$  V

