FUJITSU

262144×9 BIT DYNAMIC RANDOM ACCESS MEMORY MODULE

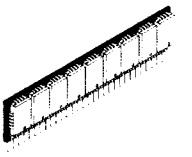
MB85240-10
MB85240-12

December 1987
Edition 1.0

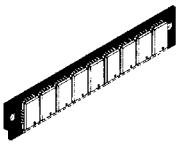
262,144 x 9 BIT CMOS STATIC COLUMN RANDOM ACCESS MEMORY

This Fujitsu MB85240 is a fully decoded, 262,144 words x 9 bits CMOS static column random access memory composed of nine 256k SCRAM chips (MB81C258x9). This module is designed for high speed, high performance applications such as main frame memory, buffer memory, and video memory, and for applications to battery backed-up systems where very low power dissipation and compact layout is required. The electrical characteristics of the MB85240 are quite same as the original MB81C258; each timing requirements are noncritical, and power supply tolerance is very wide. All inputs and outputs are TTL compatible.

- 262,144 x 9 SCRAM MODULE, 30-pin SIP and socket type
- Row Access Time (t_{RAC})
  - 100 ns max. (MB85240-10)
  - 120 ns max. (MB85240-12)
- Random Cycle Time (t_{RC})
  - 200 ns min. (MB85240-10)
  - 230 ns min. (MB85240-12)
- Address Access Time (t_{AA})
  - 45 ns max. (MB85240-10)
  - 55 ns max. (MB85240-12)
- Static Mode Cycle Time (t_{SC})
  - 50 ns min. (MB85240-10)
  - 60 ns min. (MB85240-12)
- Low Power Dissipation
  - 2970 mW max. (MB85240-10)
  - 2475 mW max. (MB85240-12)
  - 99 mW max. standby with TTL level input
  - 15 mW max. standby with CMOS level input
- +5V supply, ±10% tolerance
- 32ms/256 refresh cycles capability
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and Hidden refresh capability

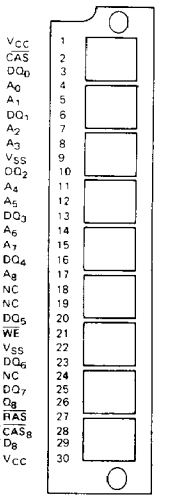


PLASTIC PACKAGE
MSP-30P-P02



PLASTIC PACKAGE
MSS-30P-P01

PIN ASSIGNMENT



* : For parity bit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Storage temperature	T_{STG}	-55 to 125	°C
Power dissipation	P_D	9.0	W
Short circuit output current	–	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Fig. 1 – FUNCTIONAL BLOCK DIAGRAM

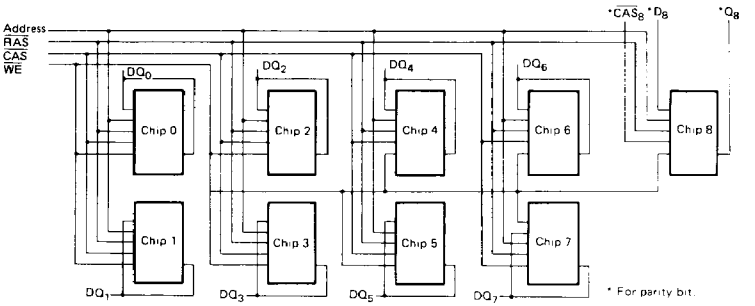
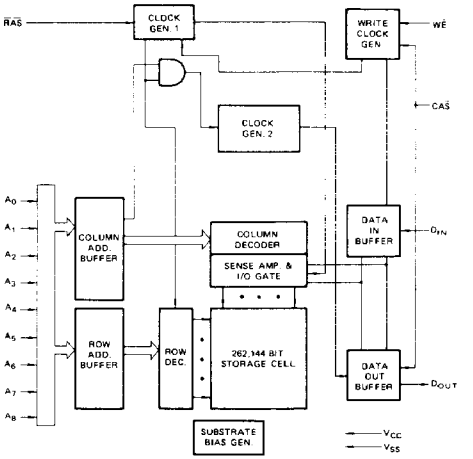


Fig. 2 – BLOCK DIAGRAM FOR EACH CHIP



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A_0 to A_8	C_{IN1}		80	pF
Input Capacitance, $\overline{RAS}$	C_{IN2}		88	pF
Input Capacitance, $\overline{CAS}$	C_{IN3}		70	pF
Input Capacitance, $\overline{WE}$	C_{IN4}		49	pF
Input Capacitance, $\overline{CAS}_8$	C_{IN5}		11	pF
Input Capacitance, D_8	C_{IN6}		7	pF
I/O Capacitance, DQ_0 to DQ_7	C_{DQ}		15	pF
Output Capacitance, Q_8	C_O		11	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V	0°C to +70°C*
Input High Voltage	V_{IH}	2.4	–	6.5	V	
Input Low Voltage	V_{IL}	-1.0	–	0.8	V	

Note *: Ambient temperature is dependent on cycle time and cooling conditions.
See the derating curve Fig. 3 for normal cycle, and Fig. 4 for static mode cycle.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING/REFRESH CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB85240-10	I_{CC1}		540	mA
	MB85240-12			450	
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})	TTL Level	I_{CC2}		18	mA
	CMOS Level			2.7	
STATIC MODE OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IL}, $\overline{WE}$ or Address = cycling; t_{SC} = min)	MB85240-10	I_{CC3}		360	mA
	MB85240-12			315	
$\overline{CAS}$-BEFORE-RAS REFRESH CURRENT* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$ refresh; t_{RC} = min)	MB85240-10	I_{CC4}		495	mA
	MB85240-12			405	
INPUT LEAKAGE CURRENT, ALL INPUTS (V_{IN} = 0V to 5.5V, V_{CC} = 5V, V_{SS} = 0V, all other inputs not under test = 0V)		$I_{I(L)1}$ ($\overline{CAS_8}$, D_8)	-10	10	μA
		$I_{I(L)2}$ (Others)	-30	30	
OUTPUT LEAKAGE CURRENT Each output is high impedance (Data is disable, V_{OUT} = 0V to 5.5V)		$I_{O(L)}$	-10	10	μA
OUTPUT LEVELS Output High Voltage (I_{OH} = -5 mA)		V_{OH}	2.4		V
Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}		0.4	

Note 1): I_{CC} is dependent on the output loading and cycle time. Output pins are open.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2

Parameter NOTE	Symbol	MB85240-10		MB85240-12		Unit
		Min	Max	Min	Max	
Time between Refresh	t_{REF}	–	32	–	32	ms
Random Read/Write Cycle Time	t_{RC}	200	–	230	–	ns
Read-Modify-Write Cycle Time 15	t_{RWC}	245	–	285	–	ns
Access Time from $\overline{RAS}$ 3 5	t_{RAC}	–	100	–	120	ns
Access Time from $\overline{CAS}$	t_{CAC}	–	25	–	30	ns
Output Buffer Turn Off Delay Time	t_{OFF}	0	25	0	25	ns
Transition Time	t_T	3	50	3	50	ns
Column Address Access Time 4 5	t_{AA}	–	45	–	55	ns
Output Hold Time from Column Address Change	t_{AOH}	5	–	5	–	ns
Access Time from $\overline{WE}$ Precharge 15	t_{WPA}	–	25	–	30	ns
Access Time Relative to Last Write 6 15	t_{ALW}	–	90	–	110	ns
Write latched Output Hold Time 15	t_{WOH}	0	–	0	–	ns
$\overline{RAS}$ Precharge Time	t_{RP}	90	–	100	–	ns
$\overline{RAS}$ Pulse Width	t_{RAS}	65	100000	75	100000	ns
$\overline{RAS}$ Hold Time	t_{RSH}	25	–	30	–	ns
$\overline{CAS}$ Pulse Width (Read)	t_{CAS}	25	100000	30	100000	ns
$\overline{CAS}$ Pulse Width (Write)	t_{CAS}	15	100000	20	100000	ns
$\overline{CAS}$ Hold Time (Read)	t_{CSH}	100	–	120	–	ns
$\overline{CAS}$ Hold Time (Write)	t_{CSH}	80	–	95	–	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	75	25	90	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time	t_{CRS}	20	–	25	–	ns
Row Address Set Up Time	t_{ASR}	0	–	0	–	ns
Row Address Hold Time	t_{RAH}	15	–	15	–	ns
Column Address Set Up Time 7	t_{ASC}	0	–	0	–	ns
Column Address Hold Time 7	t_{CAH}	20	–	25	–	ns
$\overline{RAS}$ to Column Address Delay Time 8 9	t_{RAD}	20	55	20	65	ns
Column Address Hold Time Reference to $\overline{RAS}$	t_{AR}	100	–	120	–	ns
Write Address Hold Time Referenced to $\overline{RAS}$	t_{AWR}	80	–	90	–	ns

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AC CHARACTERISTICS (Cont'd)

(Recommended operating conditions unless otherwise noted.) Note 1, 2

Parameter	NOTE	Symbol	MB85240-10		MB85240-12		Unit
			Min	Max	Min	Max	
Read Address to $\overline{RAS}$ Lead Time		t_{RAL}	45	–	55	–	ns
Column Address Hold Time Referenced to $\overline{RAS}$ Rising Time	10	t_{AHR}	15	–	15	–	ns
Last Write to Column Address Delay Time	11 12 15	t_{LWAD}	25	45	30	55	ns
Column Address Hold Time Referenced to Last Write		t_{AHLW}	90	–	110	–	ns
Read Command Set Up Time Referenced to $\overline{CAS}$		t_{RCS}	0	–	0	–	ns
Read Command Hold Time Referenced to $\overline{RAS}$	13	t_{RRH}	10	–	10	–	ns
Read Command Hold Time Referenced to $\overline{CAS}$	13	t_{RCH}	0	–	0	–	ns
$\overline{WE}$ Pulse Width		t_{WP}	15	–	20	–	ns
$\overline{WE}$ Inactive Time		t_{WI}	15	–	20	–	ns
Write Command Hold Time		t_{WCH}	15	–	20	–	ns
Write Command to $\overline{RAS}$ Lead Time	15	t_{RWL}	25	–	30	–	ns
Write Command to $\overline{CAS}$ Lead Time	15	t_{CWL}	25	–	30	–	ns
$\overline{RAS}$ to $\overline{WE}$ Delay Time	14 15	t_{RWD}	100	–	120	–	ns
$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	25	–	30	–	ns
Column Address to $\overline{WE}$ Delay Time	15	t_{AWD}	45	–	55	–	ns
$\overline{RAS}$ to Second Write Delay Time		t_{RSWD}	105	–	125	–	ns
Write Command Hold Time Referenced to $\overline{RAS}$		t_{WCR}	80	–	95	–	ns
Write Set Up Time for Output Disable	14	t_{WS}	0	–	0	–	ns
Write Hold Time for Output Disable	14	t_{WH}	0	–	0	–	ns
D_{IN} Set Up Time		t_{DS}	0	–	0	–	ns
D_{IN} Hold Time		t_{DH}	20	–	25	–	ns
D_{IN} Hold Time Reference to $\overline{RAS}$		t_{DHR}	80	–	90	–	ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCS}	20	–	25	–	ns

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AC CHARACTERISTICS (Cont'd)

(Recommended operating conditions unless otherwise noted.) Note 1, 2

Parameter NOTES	Symbol	MB85240-10		MB85240-12		Unit
		Min	Max	Min	Max	
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{FCH}	20	–	25	–	ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CPR}	20	–	25	–	ns
$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh cycles)	t_{RPC}	20	–	20	–	ns
Static Mode Read/Write Cycle Time	t_{SC}	50	–	60	–	ns
Static Mode Read-Modify-Write Cycle Time 15	t_{SRWC}	95	–	115	–	ns
Static Mode $\overline{CAS}$ Precharge Time	t_{CP}	15	–	20	–	ns

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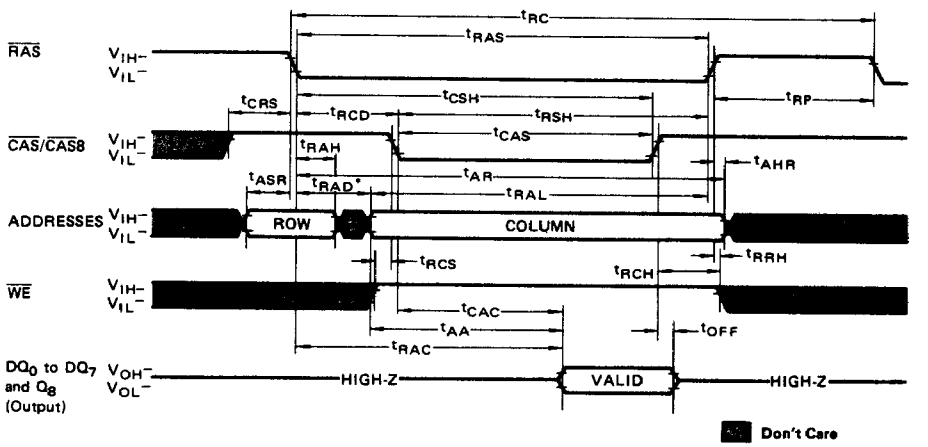
NOTES:

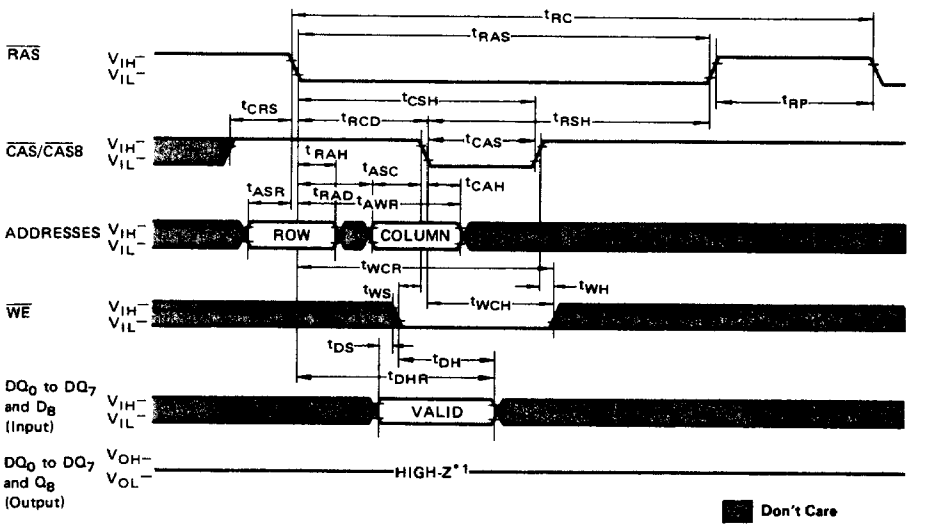
1. An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) of 200 μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T = 5ns, V_{IN} = 0V to 3V, V_{IH} = 2.4V, V_{IL} = 0.8V, V_{OH} = 2.4V, and V_{OL} = 0.4V.
3. Assumes that $t_{RAD} \leq t_{RAD}$ (max). If t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RAD} exceeds the value shown.
4. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
5. Measured with a load equivalent to 2 TTL loads and 100pF.
6. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} will be increased by the amount that t_{LWAD} exceeds the value shown.
7. Write Cycle Only.
8. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
9. t_{RAS} (min) = t_{RAH} (min) + t_T (t_T = 5ns)
10. t_{AHR} is specified to latch column address by the rising edge of $\overline{RAS}$.
11. Operation within the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled by t_{AA}.
12. t_{LWAD} (min) = t_{AHW} (min) + t_T (t_T = 5ns)
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. t_{WS}, t_{WH}, and t_{RWD} are specified as a reference point only. If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), the data output pin will remain High-Z state throughout entire cycle. If $t_{RWD} \geq t_{RWD}$ (min). The data output will contain data read from the selected cell.
15. Parity bit only.

Read Cycle



*; If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{AA}

Write Cycle ($\overline{CAS}$ Controlled)



*; If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), D_{OUT} is high-Z.

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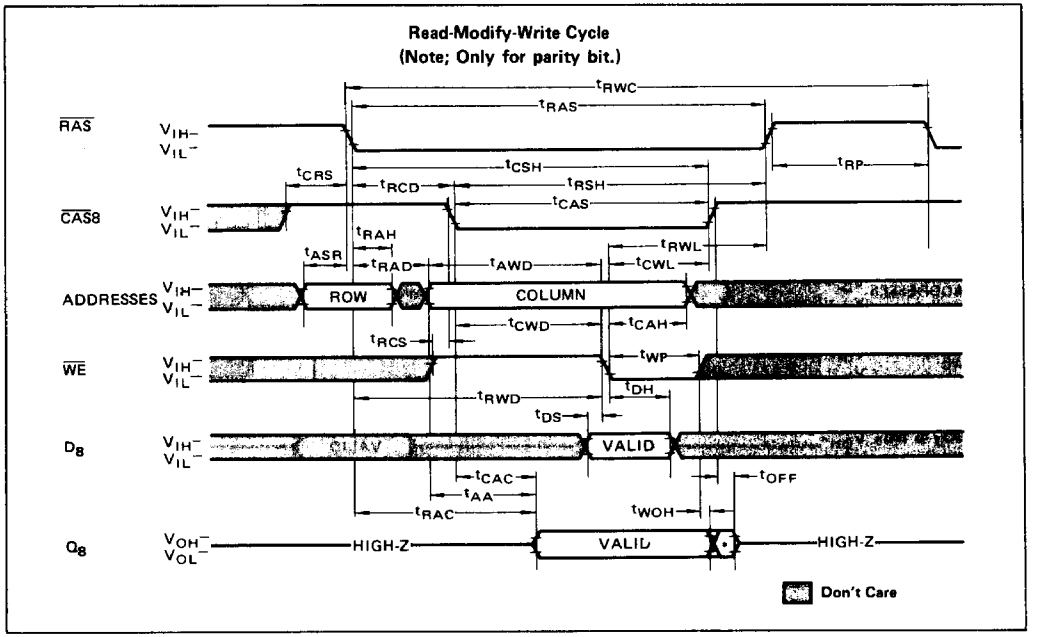
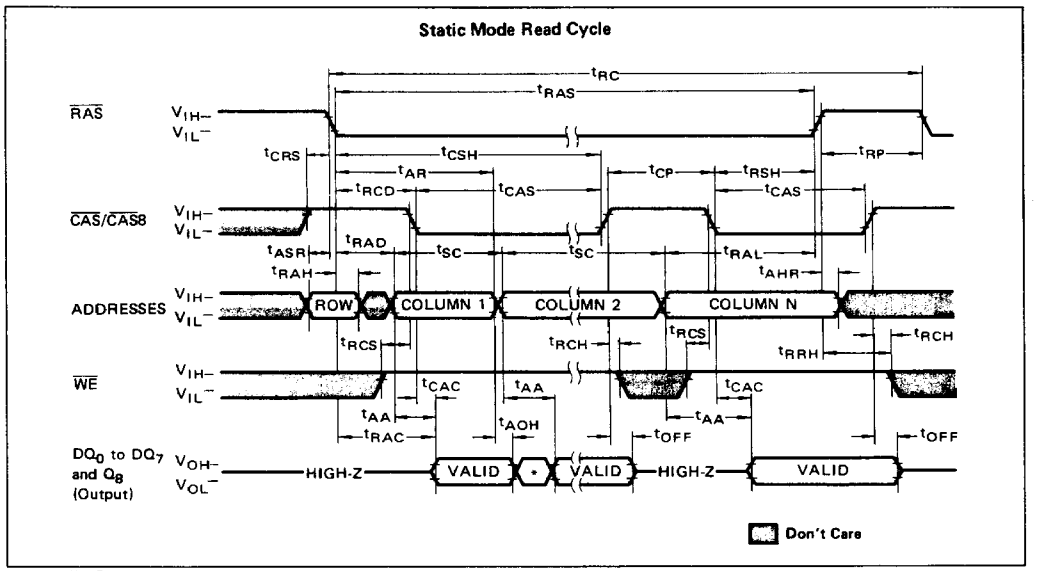
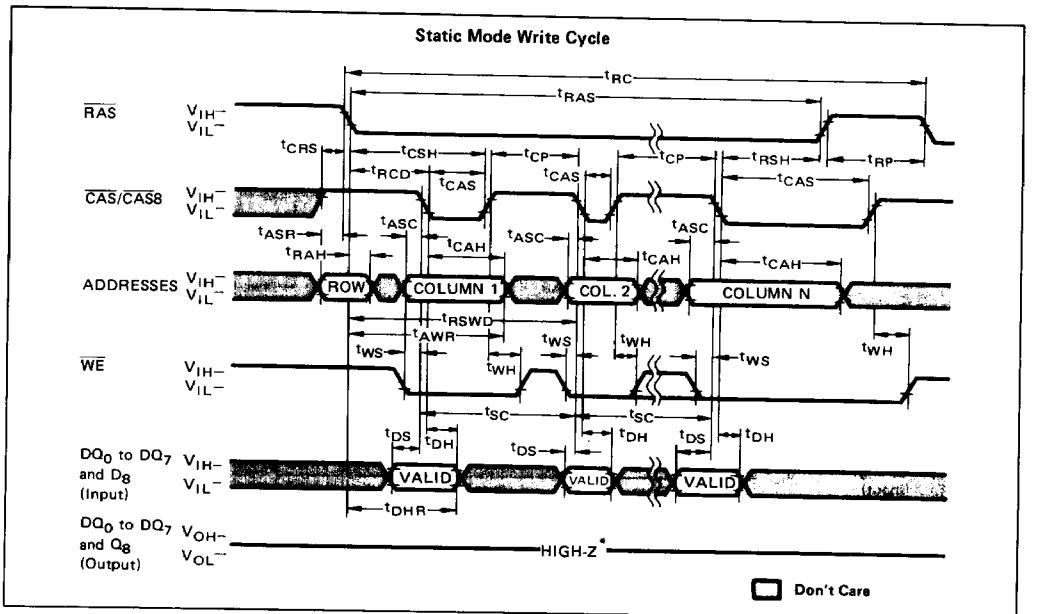


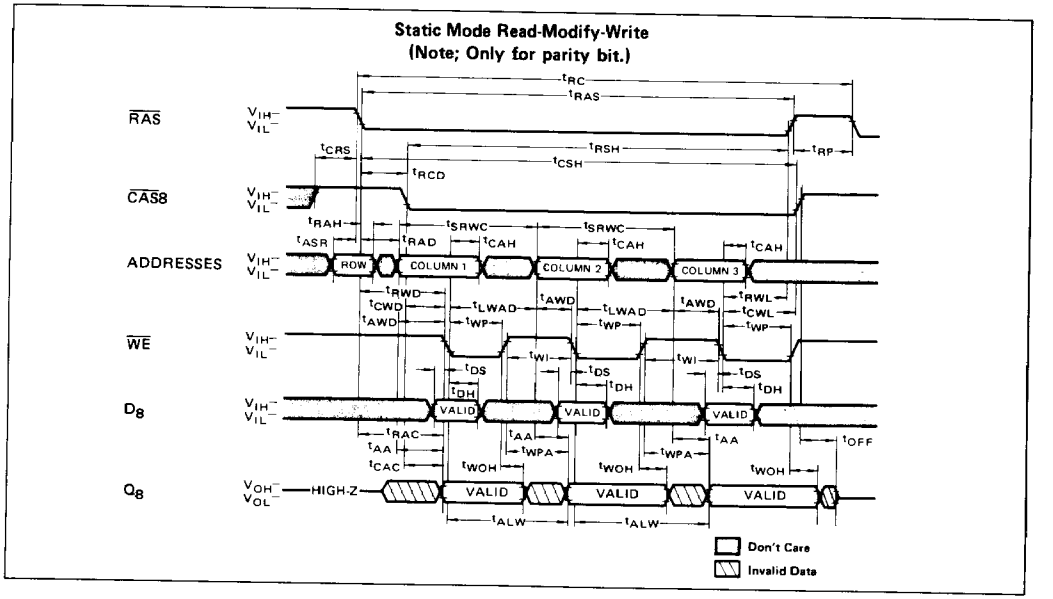
*; Invalid Data



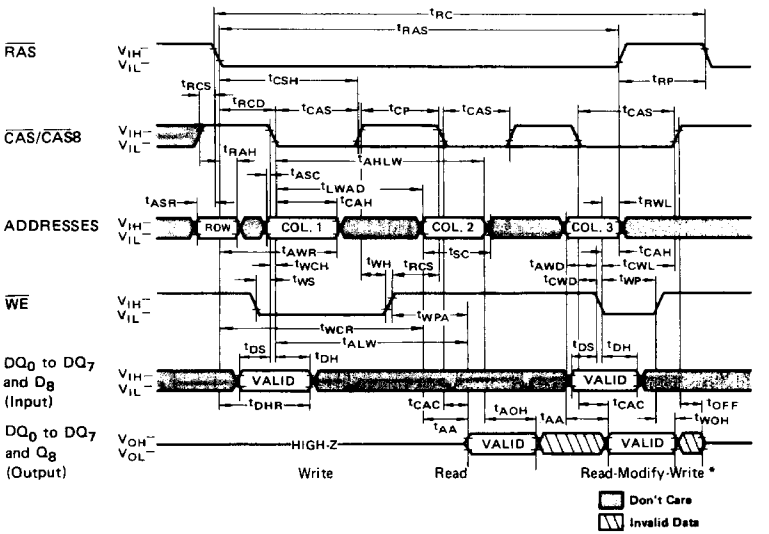
valid Data.



*; If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), D_{OUT} is high-Z.



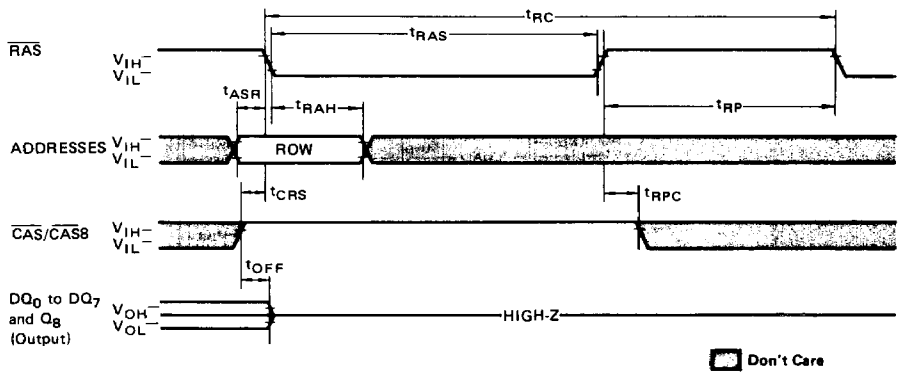
Static Mode Mixed Cycle



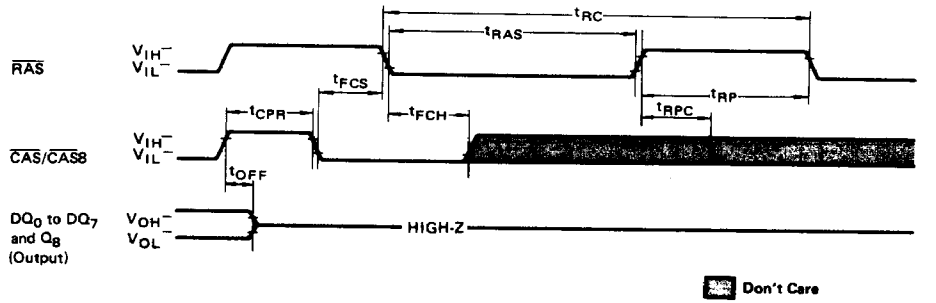
*; Only for parity bit.

RAS-Only Refresh Cycle

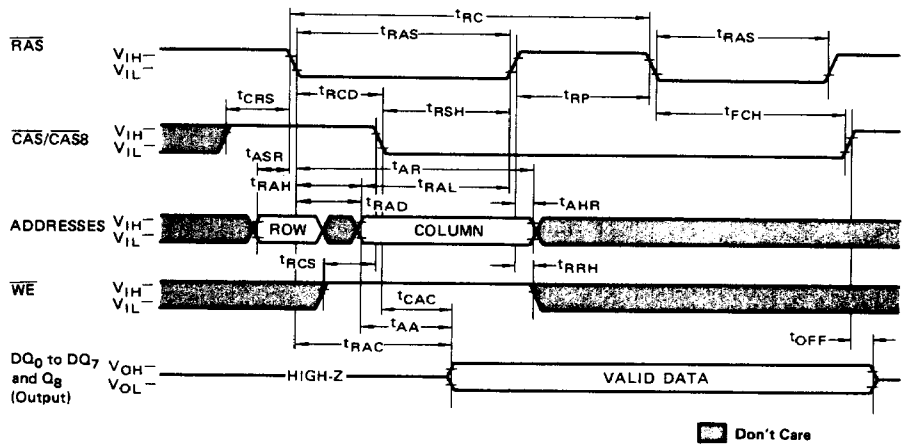
(Note; $\overline{WE}$, D_{IN} = Don't Care, $A_8 = V_{IH}$ or V_{IL})



$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Cycle
(Note; Address, $\overline{\text{WE}}$, D_{IN} = Don't Care)



Hidden Refresh Cycle



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FUNCTIONAL TRUTH TABLE

$\overline{RAS}$	$\overline{CAS}$ and $\overline{CAS_8}$	$\overline{WE}$	DQ_0 to DQ_7, D_8 and Q_8	Function
H	H	Don't Care	High-Z	Standby
L	L	H	Valid Data Out[1)]	Ready cycle
L	L	L	Valid Data In[2)]	Write cycle
L	L[3)]	Don't Care	High-Z	$\overline{CAS}$-before $\overline{RAS}$ Refresh cycle
L	H	Don't Care	High-Z	$\overline{RAS}$-only Refresh cycle
L	H ($\overline{CAS}$) L ($\overline{CAS_8}$)	H → L[4)]	High-Z (DQ_0 to DQ_7) Valid Data In (D_8) Valid Data Out (Q_8)	$\overline{RAS}$-only Refresh cycle (Except for Pairyt bit) Read-Write/Read-Modify-Write (Parity bit)

Notes: 1): DQ Pins are output mode.
2): DQ pins are input mode.
3): $t_{FCS} \geqq t_{FCS}$ (min)
4): $t_{CWD} \geqq t_{CWD}$ (min)

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DESCRIPTION

Address Inputs:
A total of eighteen binary input address bits are required to decode any one of the 262,144 storage cells within each MB81C258. Nine row address bits are established on the address input pins (A_0 to A_8) and latched with the Row Address Strobe ($\overline{RAS}$). The nine column address bits are established on the address input pins (A_0 to A_8) after the Row Address Hold Time (t_{RAH}) has been satisfied. In read cycle, the column address are not latched by the Column Address Strobe ($\overline{CAS}$), so the column address must be stable until the output becomes valid. In write cycle, the column address are latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.

Write Enable:
Read or Write cycle is selected with the $\overline{WE}$ inputs. A high on $\overline{WE}$ selects read cycle and low selects write cycle. The write operation is asserted on the later falling edge of $\overline{CAS}$ or $\overline{WE}$ (Both $\overline{CAS}$ and $\overline{WE}$ are low). The time period of the write operation is determined by internal circuit, thus next write operation will be inhibited during the write operation.

Data Input:
Data is written into the MB85240 during write or read-modify-write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.

Data Output:
Each output buffer is three state TTL compatible with a fan out of two standard TTL loads. Data out has the same porality as data in. Each output is in high impedance state until $\overline{CAS}$ is brought low. In a read cycle, the access time is determined by the following conditions:
1. t_{RAC} from the falling edge of $\overline{RAS}$.
2. t_{AA} from the column address inputs.
3. t_{CAC} from the falling edge of $\overline{CAS}$.

When both t_{RCD} and t_{RAD} satisfy their maximum limits, $t_{RAC} = t_{RCD} + t_{CAC}$ or $t_{RAC} = t_{RAD} + t_{AA}$.
Data outputs remain valid while the column address inputs are kept constant. However, when $\overline{CAS}$ goes high, the output returns to high impedance state.

Static Mode:
The static mode operation allows continuous read, write, or read-modify-write cycle within a row by applying new column address. In the static mode, $\overline{CAS}$ can be kept low throughout static mode operation. The following four cycles are allowed in the static mode.
1. Static mode read cycle;
   In a static mode read cycle, the access time is t_{RAC} from the falling edge of $\overline{RAS}$ or t_{AA} from the column address input. The data remains valid for a time t_{AOH} after the column address is changed.
2. Static mode write cycle;
   In a static mode write cycle, the data is written into the cell triggered by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. If both t_{WS} and t_{WH} are greater than their minimum limits, the data output pin is kept high impedance state through the static mode write cycle.
3. Static mode read-modify-write cycle;
   In the static mode read-modify-write cycle, $\overline{WE}$ goes low after t_{AWD} from the column address inputs and t_{CWD} from the falling edge of $\overline{CAS}$. The data and column address inputs are strobed and latched by the falling edge a of $\overline{WE}$.
4. Static mode mixed cycle;
   In the static mode, read, write, and read-modify-write cycles can be mixed in any order.

In the next read cycle of static mode write cycle or read-modify-write cycle, the access time is determined by the following conditions.
1. t_{ALW} from the later falling edge of $\overline{CAS}$ or $\overline{WE}$ at previous write cycle.
2. t_{AA} from the column address inputs.
3. t_{WPA} from the rising edge of $\overline{WE}$ at the read cycle.
4. t_{CAC} from the falling edge of $\overline{CAS}$.

Refresh:
Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row addresses (A_0 to A_7) at least every 32ms.
The MB85240 offers the following three types of refresh.
1. $\overline{RAS}$-only refresh;
   The $\overline{RAS}$-only refresh avoids any output during refresh because each output buffer is high impedance state due to $\overline{CAS}$ high. Strobing of each 256 row address (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. During $\overline{RAS}$-only refresh cycle, either V_{IH} or V_{IL} is permitted to A_8.
2. CAS-before-RAS refresh;
   $\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB85240 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes low, on chip refresh control clock generator and the internal refresh address counter are enabled, and an internal refresh operation is executed. After the refresh operation, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh.
3. Hidden refresh;
   A hidden refresh cycle will be executed while maintaining latest valid output datas at the DQ pins by extending the $\overline{CAS}$ low time. For the MB85240, a hidden refresh cycle is $\overline{CAS}$-before-$\overline{RAS}$ refresh. The internal refresh address counter provides the refresh address, as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Notice for using MB8520
The MB85240 is a SIP (Single-In-Line-Package) module which is composed of nine MB81C258 DRAMs housed in plastic LCC, and assembled on the epoxy printed circuit board. Generally the multilayer PCB board has large wiring capacitance. This disadvantage causes relatively noise induction between signal lines and power supply lines (V_{SS} or V_{CC}).
Furthermore, as the MB85240 is a very high-speed memory, the timing windows to strobe address $\overline{WE}$ and D_{IN} signals are very short (Approx. 10ns). Therefore, it is very sensitive even to very sharp noise.
From the above reasons, special care should be taken for use the MB85240. The following notices are recommended;

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DESCRIPTION

1. Provide a externally capacitor of approx. a few μF each module, the MB85240 has the nine decoupling capacitors (0.22 μF on each SCRAM 0.22 μF x 9).
2. Remove noise, riging, overshoot and undershoot from the address, clocks and DQ lines, so that the MB85240 won't latch wrong signals due to the noise induction between signal lines and between signal and power supply lines.
3. Keep enough timing margin and remove critical timing in the board design, to avoid the problem mentioned in the above item 2.
4. Provide an appropriate dumping if necessary, to avoid excessive overshoot or undershoot on the TTL input waveforms.

Fig. 3 – MB85240 DERATING CURVE

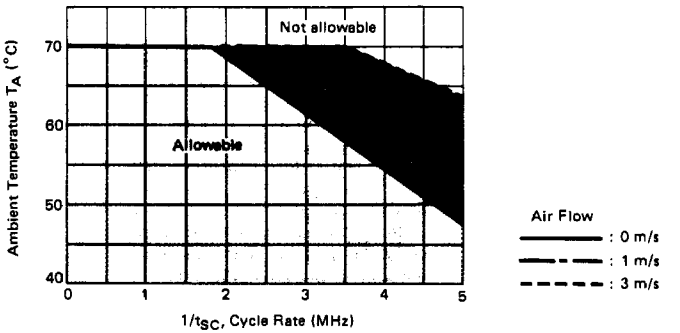
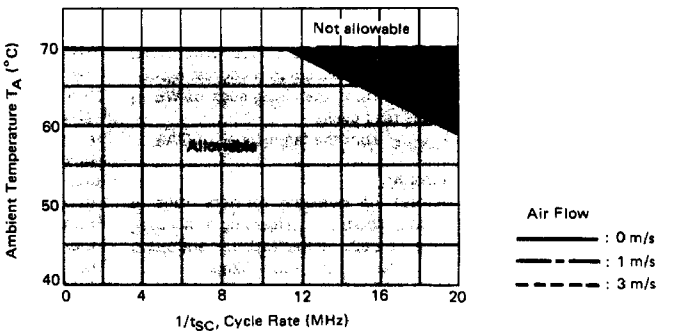
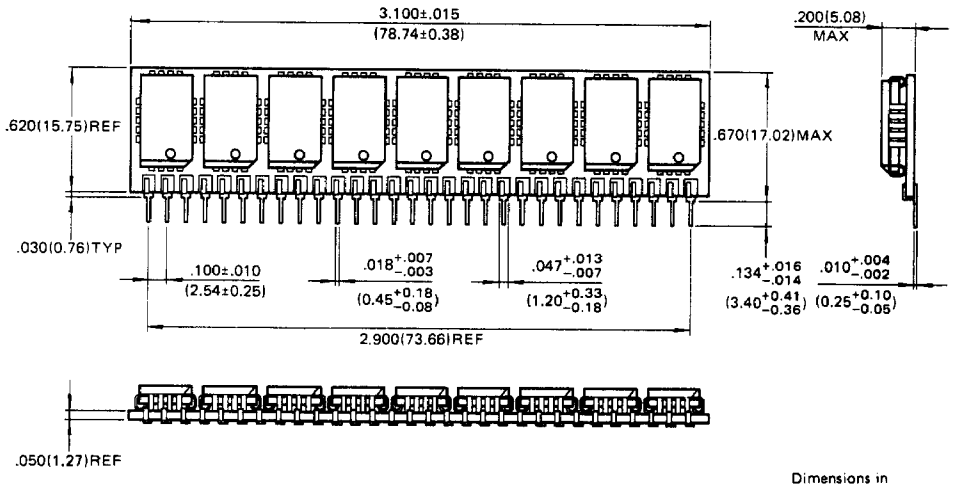


Fig. 4 – MB85240 DERATING CURVE



PACKAGE DIMENSIONS

30-LEAD SINGLE IN-LINE TYPE MODULE
(CASE No.: MSP-30P-P02)



Dimensions in
inches (millimeters)

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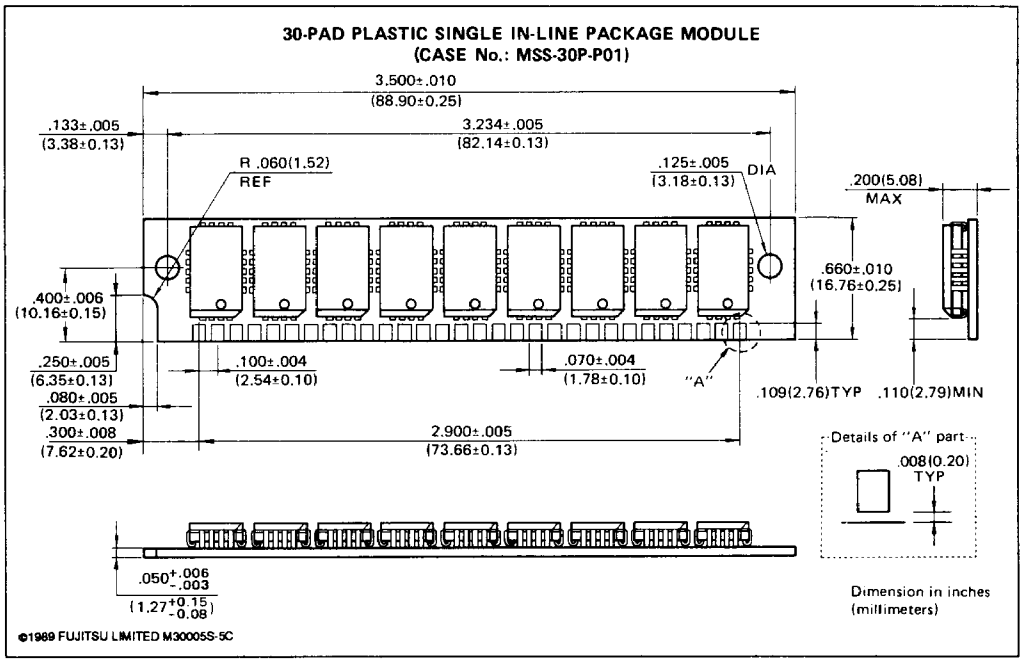
PACKAGE DIMENSIONS



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