Preliminary

SAB 82C37A-5/82C37A-8 High-Performance CMOS Programmable DMA Controller

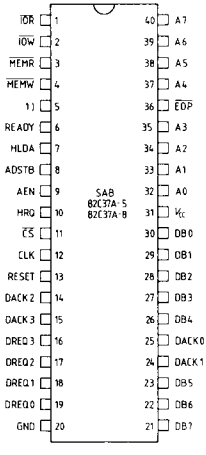
SAB 82C37A-5 5 MHz

- Four independent DMA channels
- Enable/disable control of individual DMA requests
- Memory-to-memory transfers
- Memory block initialization
- Address increment or decrement
- Independent autoinitialization of all channels
- High performance: transfers up to 2.6 Mbytes/s with 8 MHz SAB 82C37A-8

SAB 82C37A-8 8 MHz

- Directly expandable to any number of channels
- End of process input for terminating transfers
- Software DMA requests
- Independent polarity control for DREQ and DACK signals
- Fully static design
- Low standby power dissipation
- Compatible with the industry standard NMOS 9517A/8237A

Pin Configuration



1) Pin always tied high

Pin Names

DB7-DB0	Data Bus (bidirectional)
$\overline{IOR}$, $\overline{IOW}$	I/O Read and Write Input/Output
$\overline{MEMR}$, $\overline{MEMW}$	Memory Read and Write Output
A0-A3	Address Input/Output
A4-A7	Adress Output
$\overline{CS}$	Chip Select Input
CLK	Clock Input
READY	Ready Input
HRQ	Hold Request Output
$\overline{HLDA}$	Hold Acknowledge Input
RESET	Reset Input
DREQ0-DREQ3	DMA Request Input
DACK0-DACK3	DMA Acknowledge Output
AEN	Address Enable Output
ADSTB	Address Strobe Output
$\overline{EOP}$	End of Process Input/Output

The SAB 82C37A Multimode Direct Memory Access (DMA) Controller is designed to improve system performance by allowing external devices to directly transfer information to or from system memory. Memory-to-memory transfer capability is also provided.
The SAB 82C37A contains four independent channels, each with a separate register set, and may be expanded to any number of channels by cascading additional controller chips. The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to autoinitialize to its original state following an end-of-process ($\overline{EOP}$). Each channel has a full 64K address and word count capability.
The SAB 82C37A is fabricated in Siemens ACMOS technology and packaged in a 40-pin DIP. The SAB 82C37A-8 is the 8 MHz version of the 5 MHz SAB 82C37A-5. The SAB 82C37A is compatible with the industry standard 8237A/9517A DMA controllers.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
$\overline{IOR}$	1	I/O	$\overline{I/O\ READ}$ I/O read is a bidirectional active-low tristate line. In the idle cycle, it is an input control signal used by the CPU to read the control registers. In the active cycle, it is an output control signal used by the SAB 82C37A to access data from a peripheral device during a DMA write transfer.
$\overline{IOW}$	2	I/O	$\overline{I/O\ WRITE}$ I/O write is a bidirectional active-low tristate line. In the idle cycle it is an input control signal used by the CPU to load information into the SAB 82C37A. In the active cycle it is an output control signal used by the SAB 82C37A to load data to a peripheral device during a DMA read transfer. Write operations by the CPU to the SAB 82C37A require a rising $\overline{IOW}$ edge following each data byte transfer. It is not sufficient to hold the $\overline{IOW}$ pin low and toggle $\overline{CS}$.
$\overline{MEMR}$	3	O	$\overline{MEMORY\ READ}$ The memory read signal is an active-low tristate output used to access data from the selected memory location during a memory-to-peripheral or a memory-to-memory transfer.
$\overline{MEMW}$	4	O	$\overline{MEMORY\ WRITE}$ The memory write signal is an active-low tristate output used to write data to the selected memory location during a peripheral-to-memory or a memory-to-memory transfer.
–	5	I	Pin 5 must be tied high.
READY	6	I	READY READY is an input used to extend the memory read and write pulses from the SAB 82C37A to accommodate slow memories or I/O peripheral devices. READY must not make transitions during its specified setup/hold time.
HLDA	7	I	HOLD ACKNOWLEDGE The active-high hold acknowledge from the CPU indicates that control of the system buses has been relinquished.
ADSTB	8	O	ADDRESS STROBE The active-high address strobe is used to strobe the upper address byte from DB0-DB7 into an external latch.
AEN	9	O	ADDRESS ENABLE Address enable is an active-high signal used to disable the system bus during DMA cycles and to enable the output of the external latch which holds the upper byte of the address. Note that during DMA transfers HLDA and AEN should be used to deselect all other I/O peripherals which may erroneously be accessed as programmed I/O during the DMA operation. The SAB 82C37A automatically deselects itself by disabling the $\overline{CS}$ input during DMA transfers.

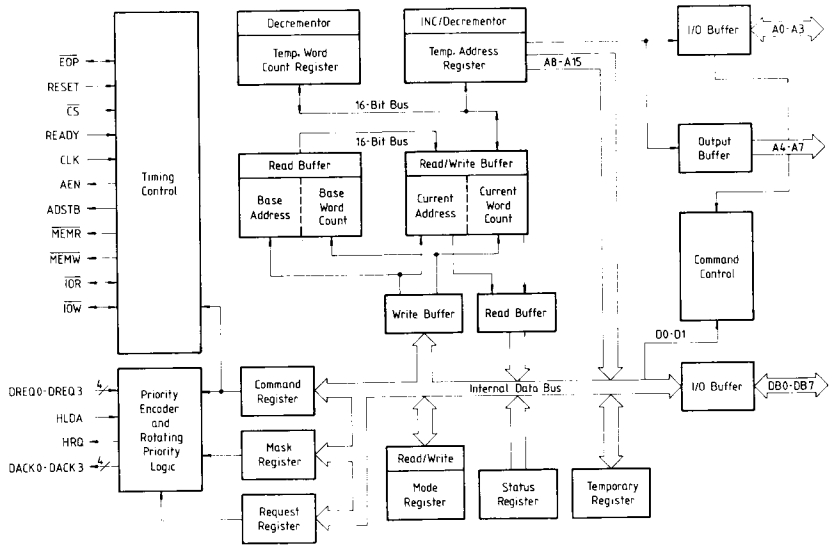
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
HRQ	10	O	HOLD REQUEST The hold request to the CPU is used by the DMA to request control of the system bus. Software requests or unmasked DREQs cause the SAB 82C37A to issue HRQ.
$\overline{CS}$	11	I	$\overline{CHIP\ SELECT}$ Chip select is an active-low input used to select the SAB 82C37A as an I/O device during an I/O read or I/O write by the host CPU. This allows CPU communication on the data bus. During multiple transfers to or from the SAB 82C37A by the host CPU $\overline{CS}$ may be held low providing $\overline{IOR}$ or $\overline{IOW}$ is toggled following each transfer.
CLK	12	I	CLOCK This input controls the internal operations of the SAB 82C37A and its rate of data transfers. The input may be driven at up to 5 MHZ for the standard SAB 82C37A-5 and up to 8 MHz for the SAB 82C37A-8.
RESET	13	I	RESET Reset is an asynchronous active-high input which clears the command, status, request and temporary register. It also clears the first/last flipflop and sets the mask register. Following a reset, the device is in the idle cycle.
DACK0 DACK1 DACK2 DACK3	25 24 14 15	O O O O	DMA ACKNOWLEDGE The DMA acknowledge lines indicate that a channel is active. In many systems they will be used to select a peripheral. Only one DACK will be active at a time and none will be active unless the DMA is in control of the bus. The polarity of these lines is programmable. Reset initializes them to active-low.
DREQ0 DREQ1 DREQ2 DREQ3	19 18 17 16	I I I I	DMA REQUEST The DMA request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In fixed priority, DREQ0 has the highest priority and and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of a DREQ signal. The polarity of DREQ is programmable. Reset initializes these lines to active high.
DB0-DB7	30-26, 23-21	I/O	DATA BUS The data bus lines are bidirectional tristate signals connected to the system data bus. The outputs are enabled during the I/O read by the host CPU, permitting the CPU to examine the contents of an address register, the status register, the temporary register or a word count register. The data bus is enabled to input data during a host CPU I/O write, allowing the CPU to program the SAB 82C37A control registers. During DMA cycles the most significant eight bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations data from the source memory location comes into the SAB 82C37A's temporary register on the read-from-memory half of the operation. On the write-to-memory half of the operation, the data bus outputs the temporary register data into the destination memory location.

Pin Functions and Definitions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
A0–A3	32–35	I/O	ADDRESS 0–3 The four least significant address lines are bidirectional tristate signals. During DMA idle cycles they are inputs and allow the host CPU to load or read control registers. When the DMA is active, they are outputs and provide the lower 4 bits of the output address.
A4–A7	37–40	O	ADDRESS 4–7 The four most significant address lines are tristate outputs and provide four bits of address. These lines are enabled only during DMA service.
$\overline{EOP}$	36	I/O	$\overline{END\ OF\ PROCESS}$ End of process ($\overline{EOP}$) is an active-low bidirectional open-drain signal providing information concerning the completion of DMA service. When a channel's word count goes to zero, the SAB 82C37A pulses $\overline{EOP}$ low to provide the peripheral with a completion signal. $\overline{EOP}$ may also be pulled low by the peripheral to cause premature completion. The reception of $\overline{EOP}$, either internal or external, causes the currently active channel to terminate the service, to set its TC bit in the status register and to reset its request bit. If autoinitialization is selected for the channel, the current registers will be updated from the base registers. Otherwise the channel's mask bit will be set and the register contents will remain unaltered. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. $\overline{EOP}$ always applies to the channel with an active DACK; external $\overline{EOP}$s are disregarded when DACK0-DACK3 are all inactive if the DMA is in state SI. In situations where two or more SAB 82C37A DMA controllers are cascaded, the $\overline{EOP}$ pins should be logically ORed (not wire-ORed). Because $\overline{EOP}$ is an open-drain signal, an external pullup resistor is required. Values of 3.3 kΩ or 4.7 kΩ are recommended.
V_{CC}	31	–	POWER SUPPLY (+5 V)
GND	20	–	GROUND (0 V)

Block Diagram



Functional Description

DMA Operation
The SAB 82C37A is designed to operate in two major cycles. These are called idle and active cycles. Each device cycle is made up of a number of states. State I (SI) is the inactive state. It is entered when the SAB 82C37A has no valid DMA requests pending. While in SI, the DMA controller is inactive but may be in the program condition, being programmed by the processor. State 0 (S0) is the first state of a DMA service. The SAB 82C37A has requested a hold but the processor has not yet returned an acknowledge. An acknowledge from the CPU will signal that transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted before S4 by the use of the READY line on the SAB 82C37A.
Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two digit numbers for identification. Eight states are required for each complete transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half and the last four states (S21, S22, S23 and S24) for the write-to-memory half of the transfer.

Idle Cycle
When no channel is requesting service, the SAB 82C37A will enter the idle cycle and perform "SI" states. In this cycle the SAB 82C37A will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample $\overline{CS}$, looking for an attempt by the microprocessor to write or read the internal registers of the SAB 82C37A.

Active Cycle
When the SAB 82C37A is in the idle cycle and a channel requests a DMA service, the device will output a HRQ to the microprocessor and enter the active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode – In single transfer mode, the SAB 82C37A will make a one-byte transfer during each HRQ/HLDA handshake. When DREQ goes active, HRQ will go active. After the CPU responds by driving HRQ active, a one-byte transfer will take place. Following the transfer, HRQ will go inactive, the word count will be decremented and the address will be either incremented or decremented.

Block Transfer Mode – In block transfer mode, the SAB 82C37A will continue making transfers until a TC (caused by the word count going to zero) or an external end-of-process ($\overline{EOP}$) is encountered.

Demand Transfer Mode – In demand transfer mode the device will continue making transfers until a TC or external $\overline{EOP}$ is encountered or until DREQ goes inactive. Thus, the device requesting service may discontinue transfers by bringing DREQ inactive. Service may be resumed by asserting an active DREQ once again.

Cascade Mode – This mode is used to cascade more than one SAB 82C37A together for simple system expansion. The HRQ and HLDA signals from the additional SAB 82C37A are connected to the DREQ and DACK signals of a channel of the initial SAB 82C37A.

Transfer Types

Each of the three active transfer modes can perform three different types of transfers. These are read, write and verify. Write transfers move data from an I/O device to the memory by activating $\overline{IOR}$ and $\overline{MEMW}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$. Verify transfers are pseudo transfers; the SAB82C37A operates as in read or write transfers generating addresses, responding to $\overline{EOP}$, etc., however, the memory and I/O control lines remain inactive.

Memory-to-Memory – The SAB 82C37A includes a block move capability that allows blocks of data to be moved from one memory adress space to another. Channel 0 forms the source address and channel 1 forms the destination address. The channel 1 word count is used. A memory-to-memory transfer is initiated by setting a software DMA request for channel 0.

Autoinitialize – By programming a bit in the mode register a channel may be set up for an autoinitialize operation. During autoinitialization, the original values of the current address and current word count registers are automatically restored from the base address and base word count registers of that channel following $\overline{EOP}$.

Extended Write – For flyby transactions late write is normally used, as this allows sufficient time for the $\overline{IOR}$ signal to get data from the peripheral onto the bus before $\overline{MEMW}$ is activated. In some systems, performance can be improved by starting the write cycle earlier.

Address Generation – In order to reduce pin count, the SAB 82C37A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of address strobe (ADSTB) is used to load these bits from the data lines to the latch. Address enable (AEN) is used to enable the bits onto the address bus through the tristate enable control signal of the latch. The lower order address bits are output by the SAB 82C37A directly. To save time and speed transfers, the SAB 82C37A executes S1 states only when updating of A8–A15 in the latch is necessary.

Compressed Timing – In order to achieve even greater throughput where system characteristics permit, the SAB 82C37A can compress the transfer time to two clock cycles. By removing state S3 the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write.

Priority – The SAB 82C37A has two types of priority encoding available as software selectable options. The first is fixed priority which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel 0. The second scheme is rotating priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly.

Software Commands
There are two special software commands which can be executed in the program condition.
Clear first/last flipflop: This command may be issued prior to writing or reading SAB 82C37A address or word count information. This initializes the flipflop to a known state so that subsequent accesses to register contents by the microprocessor will address lower and upper bytes in the correct sequence.
Master clear: This software instruction has the same effect as the hardware reset. The command, status, request, temporary and internal first/last flipflop registers are cleared and the mask register is set.

Register Description

Current Address Register
Each channel has a 16-bit current address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the current address register during the transfer.

Current Word Count Register
Each channel has a 16-bit current word count register. This register should be programmed with, and will return on a CPU read, a value one less than the number of words to be transferred. The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes to zero, a TC will be generated.

Base Address and Base Word Count Registers
Each channel has a pair of base address and base word count registers. These 16-bit registers store the original values of their associated current registers. During autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in bytes during DMA programming by the microprocessor.

Command Register
This 8-bit register controls the operation of the SAB 82C37A. It is programmed by the microprocessor in the program condition and is cleared by reset.

Mode Registers
Each channel has a 6-bit mode register associated with it. When the register is being written to by the microprocessor in the program condition, bits 0 and 1 determine which channel mode register is to be written to.

Request Register
The SAB 82C37A can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit request register. These are nonmaskable and subject to prioritization by the priority encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external $\overline{EOP}$. The entire register is cleared by a reset.

Mask Register
Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed for autoinitialize. Each bit of the 4-bit mask register may also be set or cleared separately under software control. The entire register is also set by a reset.

Status Register
The status registers may be read out of the SAB 82C37A by the microprocessor. It indicates which channels have reached a terminal count and which channels have pending DMA requests.

Temporary Register
The temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the program condition.

Absolute Maximum Ratings

Ambient temperature under bias	0° to 70°C
Storage temperature	−65° to + 150°C
Supply voltage	−0.5 to + 7.0 V
Voltage on any pin with respect to ground	−0.5 to V_{CC} + 0.5 V
Power dissipation	1 W

Note:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 10%; GND = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	
V_{IH}	Input high voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output low voltage	–	0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output high voltage	3.0 V_{CC} − 0.4	– –	V V	I_{OH} = −2.5 mA I_{OH} = −100 µA
I_{IL}	Input leakage current	–	±1	µA	0 V < V_{IN} < V_{CC}
I_{OFL}	Output leakage current	–	±10	µA	0 V < V_{OUT} < V_{CC}
I_{CC}	V_{CC} supply current	–	2	mA/MHz	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND Outputs open
I_{CCSB}	V_{CC} supply current – standby	–	10	µA	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND Outputs open CLK = 0 MHz

Capacitance [1]

T_A = 25°C; V_{CC} = GND = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
C_{IN}	Input capacitance	–	5	pF	f_c = 1 MHz
C_{IO}	I/O capacitance	–	20	pF	Unmeasured pins returned to GND
C_{OUT}	Output capacitance	–	15	pF	

[1] This parameter is periodically sampled and not 100% tested.

AC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 10%; GND = 0 V

DMA (Master) Mode

Symbol	Parameter	Limit values				Unit
		82C37A-5		82C37A-8		
		min.	max.	min.	max.	
t_{AEL}	AEN high from CLK low (S1) delay time	–	200	–	105	ns
t_{AET}	AEN low from CLK high (S1) delay time	–	130	–	80	ns
t_{AFAB}	Address active to float delay from CLK high	–	90	–	55	ns
t_{AFC}	$\overline{READ}$ or $\overline{WRITE}$ float from CLK high	–	120	–	75	ns
t_{AFDB}	DB active to float delay from CLK high	–	120	–	80	ns
t_{AHR}	Address from $\overline{READ}$ high hold time	t_{CY}–100	–	t_{CY}–75	–	ns
t_{AHS}	DB from ADSTB low hold time	30	–	25	–	ns
t_{AHW}	Address from $\overline{WRITE}$ high hold time	t_{CY}–50	–	t_{CY}–50	–	ns
t_{AK}	DACK valid from CLK low delay time [1]	–	170	–	105	ns
	$\overline{EOP}$ high from CLK high delay time [2]	–	170	–	105	ns
	$\overline{EOP}$ low to CLK high delay time	–	170	–	60	ns
t_{ASM}	Address stable from CLK high	–	120	–	60	ns
t_{ASS}	DB to ADSTB low setup time	100	–	65	ns	ns
t_{CH}	CLK high time (transitions ≤ 10 ns)	80	–	55	–	ns
t_{CL}	CLK low time (transitions ≤ 10 ns)	68	–	43	–	ns
t_{CY}	CLK cycle time	200	–	125	–	ns
t_{DCL}	CLK high to $\overline{READ}$ or $\overline{WRITE}$ low delay [3]	–	190	–	120	ns
t_{DCTR}	$\overline{READ}$ high from CLK high (S4) delay time [3]	–	190	–	115	ns
t_{DCTW}	$\overline{WRITE}$ high from CLK high (S4) delay time [3]	–	130	–	80	ns
t_{DQ}	HRQ valid from CLK high delay time	–	120	–	75	ns
t_{EPS}	$\overline{EOP}$ low from CLK low setup time	40	–	25	–	ns
t_{EPW}	$\overline{EOP}$ pulse width	220	–	135	–	ns
t_{FAAB}	Address float to active delay from CLK high	–	120	–	60	ns
t_{FAC}	$\overline{READ}$ or $\overline{WRITE}$ active from CLK high	–	150	–	90	ns
t_{FADB}	DB float to active delay from CLK high	–	120	–	60	ns

Notes see next page.

Symbol	Parameter	Limit values				Unit
		82C37A-5		82C37A-8		
		min.	max.	min.	max.	
t_{HS}	HLDA valid to CLK high setup time	75	–	45	–	ns
t_{IDH}	Input data from $\overline{MEMR}$ high hold time	0	–	0	–	ns
t_{IDS}	Input data to $\overline{MEMR}$ high setup time	170	–	90	–	ns
t_{ODH}	Output data from $\overline{MEMW}$ high hold time	10	–	10	–	ns
t_{ODV}	Output data valid to $\overline{MEMW}$ high [4]	125	–	90	–	ns
t_{QS}	DREQ to CLK low (S1, S4) setup time [1]	0	–	0	–	ns
t_{RH}	CLK to READY low hold time	20	–	20	–	ns
t_{RS}	READY to CLK low setup time	60	–	35	–	ns
t_{STL}	ADSTB high from CLK high delay time	–	130	–	70	ns
t_{CLSL}	ADSTB low from CLK low delay time	–	150	–	70	ns
t_{SHSL}	ADSTB high time	70	–	50	–	ns
t_{QH}	DREQ from DACK valid hold time	0	–	0	–	ns
t_{RQHA}	HRQ to HLDA delay time	1	–	1	–	CLK

[1] DREQ and DACK signals may be active high or low. Timing diagrams assume the active high mode.

[2] $\overline{EOP}$ is an open-drain output. This parameter assumes the presence of a 1.6 kΩ pullup to V_{CC}.

[3] The net $\overline{IOW}$ or $\overline{MEMW}$ pulse width for normal write will be t_{CY}–100 ns and for extended write will be $2t_{CY}$–100 ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for normal read will be $2t_{CY}$–50 ns and for compressed read will be t_{CY}–50 ns.

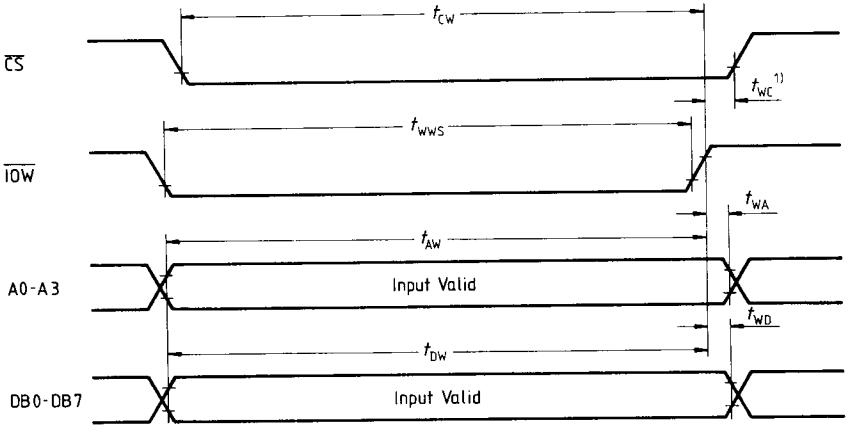
[4] If n wait states are added during the write-to-memory half of a memory-to-memory transfer, this parameter will increase by n (t_{CY}).

Peripheral (Slave) Mode

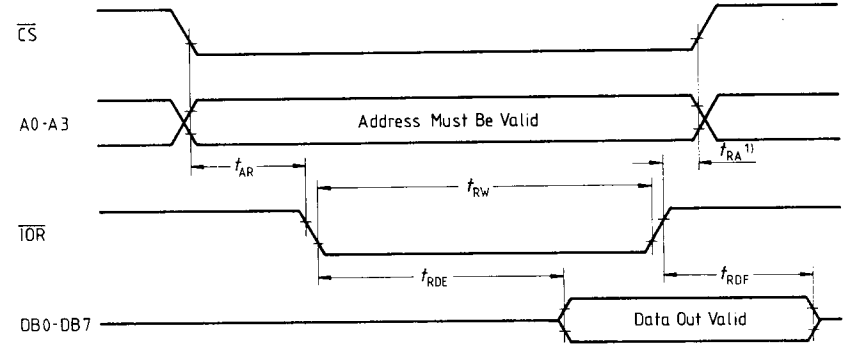
Symbol	Parameter	Limit values				Unit
		82C37A-5		82C37A-8		
		min.	max.	min.	max.	
t_{AR}	Address valid or $\overline{CS}$ low to $\overline{READ}$ low	50	–	10	–	ns
t_{AW}	Address valid to $\overline{WRITE}$ high setup time	130	–	100	–	ns
t_{CW}	$\overline{CS}$ low to $\overline{WRITE}$ high setup time	130	–	100	–	ns
t_{DW}	Data valid to $\overline{WRITE}$ high setup time	130	–	100	–	ns
t_{RA}	Address or $\overline{CS}$ hold from $\overline{READ}$ high	0	–	0	–	ns
t_{RDE}	Data access from $\overline{READ}$ low [1]	–	140	–	120	ns
t_{RDF}	DB float delay from $\overline{READ}$ high	0	70	0	55	ns
t_{RSTD}	Power supply high to RESET low setup time	500	–	500	–	µs
t_{RSTS}	RESET to first $\overline{IOWR}$	$2\,t_{CY}$	–	$2\,t_{CY}$	–	ns
t_{RSTW}	RESET pulse width	300	–	300	–	ns
t_{RW}	$\overline{READ}$ width	200	–	155	–	ns
t_{WA}	Address from $\overline{WRITE}$ high hold time	0	–	0	–	ns
t_{WC}	$\overline{CS}$ high from $\overline{WRITE}$ high hold time	0	–	0	–	ns
t_{WD}	Data from $\overline{WRITE}$ high hold time	30	–	10	–	ns
t_{WWS}	$\overline{WRITE}$ width	160	–	100	–	ns

[1] Output loading is 1 TTL gate plus 150 pF capacitance, unless otherwise noted.

Slave Mode Write Timing

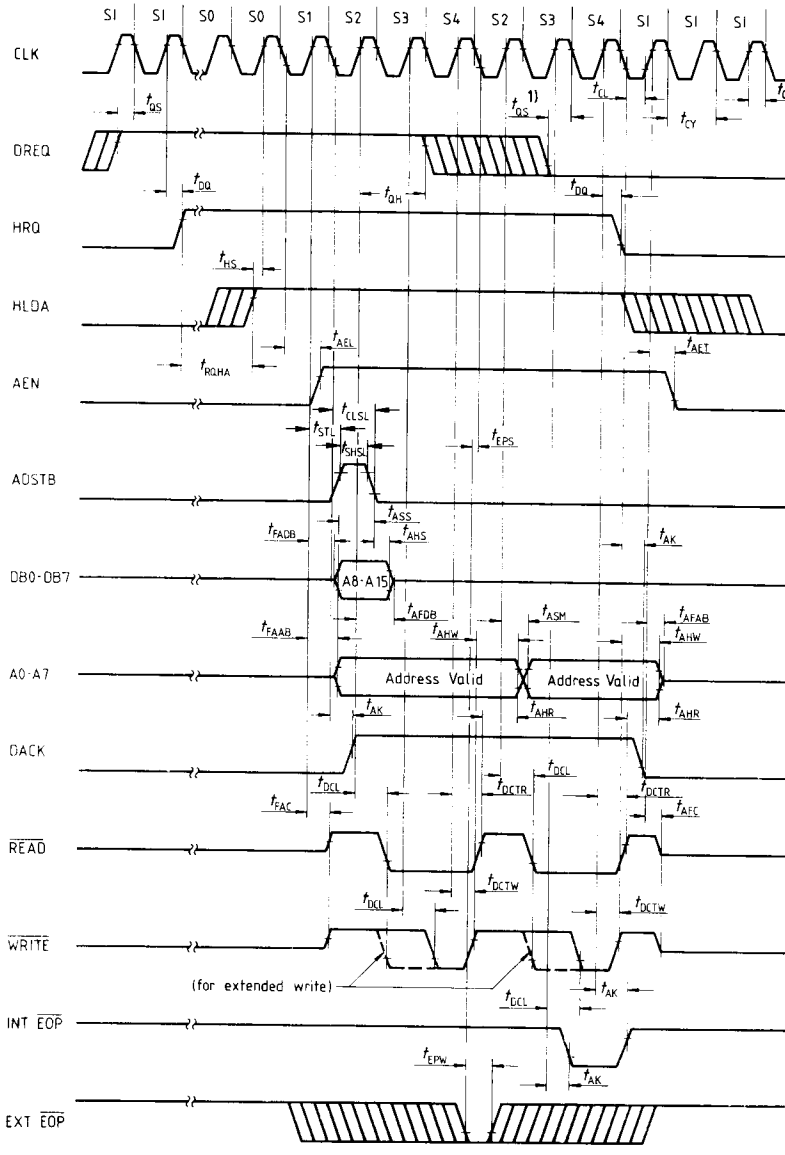


Slave Mode Read Timing



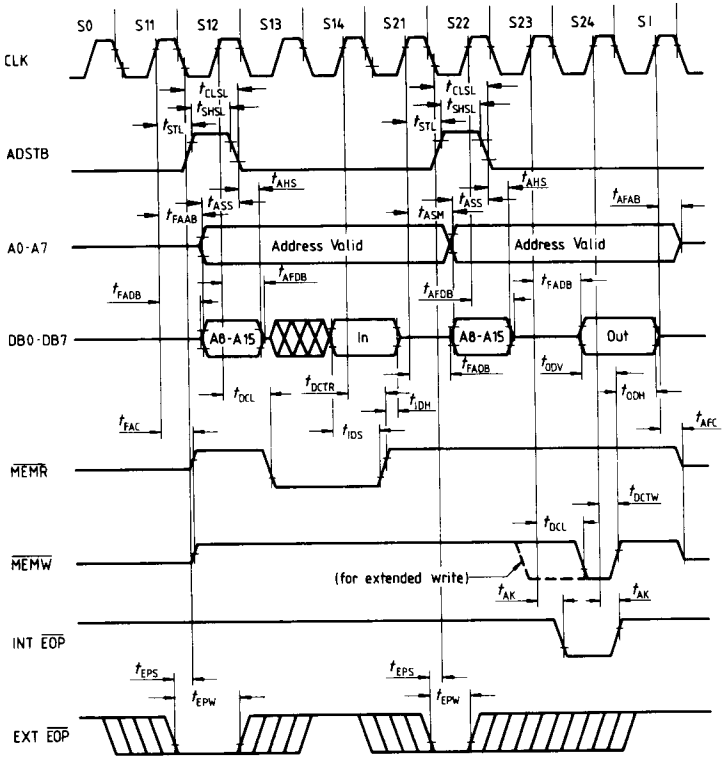
1) Successive read and/or write operation by the CPU to access the SAB 82C37A registers must meet recovery times:
   400 ns at least for the SAB 82C37A-5
   300 ns at least for the SAB 82C37A-8

DMA Transfer Timing

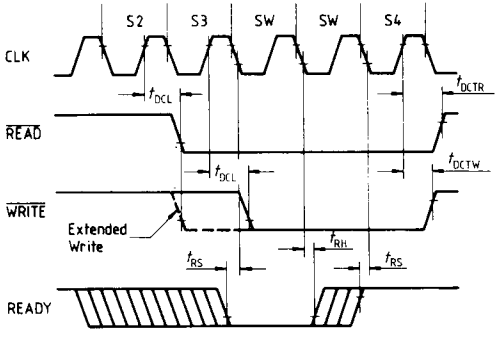


1) DREQ should be held active until DACK is returned.

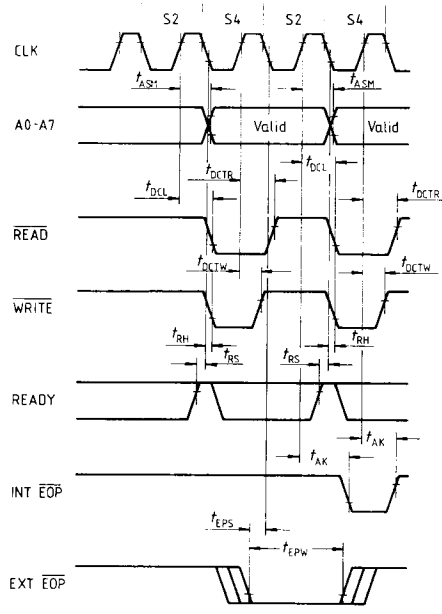
Memory-to-Memory Transfer Timing



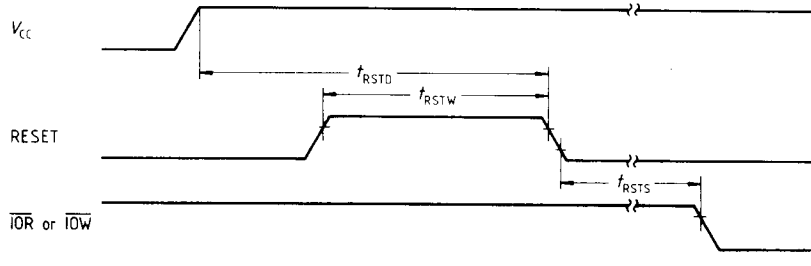
Ready Timing



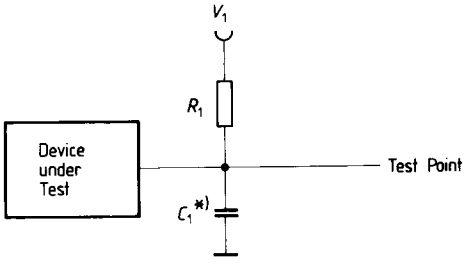
Compressed Transfer Timing



Reset Timing



AC Test Circuits

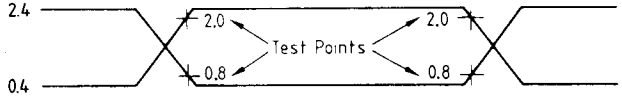


*) Includes stray and jig capacitance

Test Condition Definition

Pins	V_1	R_1	C_1
All Outputs Except $\overline{EOP}$	1.7 V	520 Ω	100 pF
$\overline{EOP}$	V_{CC}	1.6 KΩ	50 pF

Input Waveforms for AC Tests



Ordering Information

Type	Ordering code	Description
SAB 82C37A-5-P	Q 67120-P215	Programmable DMA controller 5 MHz (P-DIP-40)
SAB 82C37A-8-P	Q 67120-P239	Programmable DMA controller 8 MHz (P-DIP-40)