STC9620F Series

CMOS COMMUNICATION PROTOCOL CONTROLLER

- **Compatible with "AT Command" System**
- **Ports for Interface with Modem and Host CPU**
- **On-chip Data Parallel/Serial Conversion Circuit**

■DESCRIPTION

The STC9620F Series asynchronous Communication Protocol Controller runs on a host CPU via an external data memory (registers) and controls a modem LSI or dialer to provide an intelligent communication function. The protocol controller is stored in the program memory of the STC9620F, and can be changed as required to support a specific communication protocol.

In order for the user to understand the functions of the STC9620F Series more realistically, this document focuses on the $STC9620F_{0B}$ that provides programmed intelligent functions compatible with the "AT Command" system.

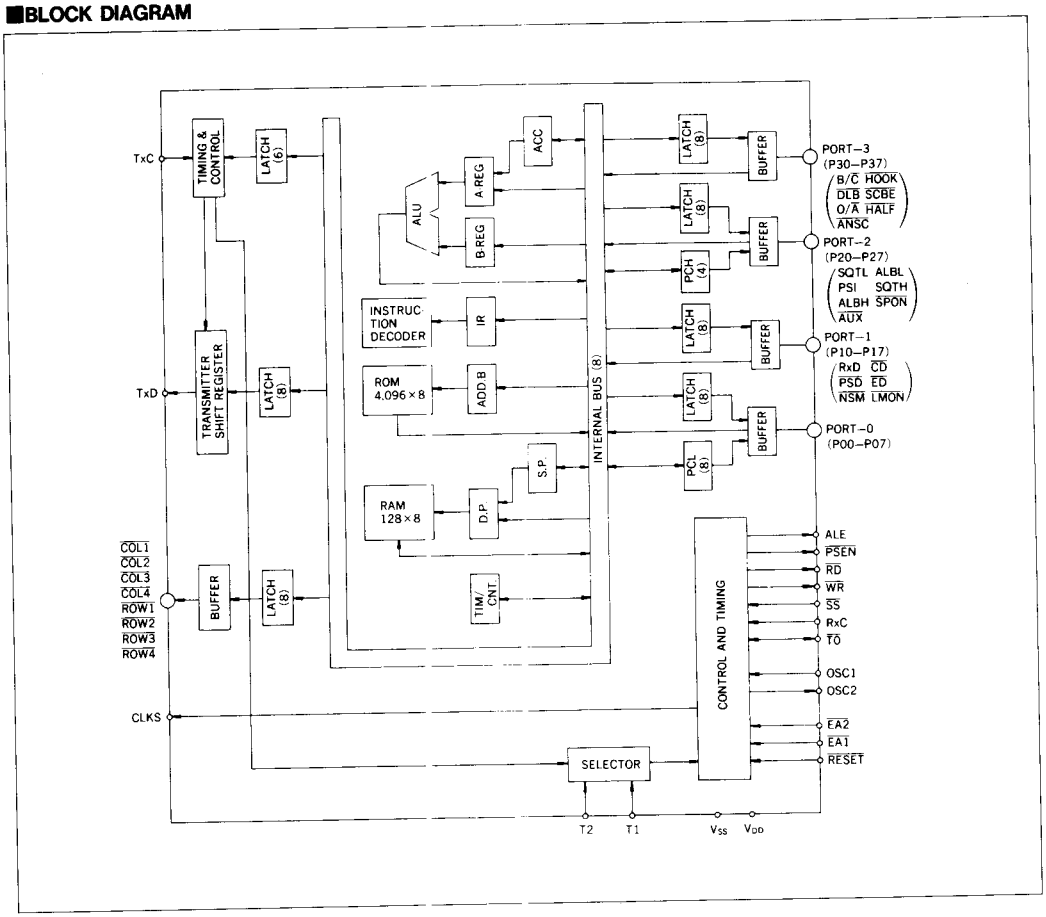
The $STC9620F_{0B}$ contains a parallel/serial data conversion circuit. The $STC9620F_{0B}$ enables the designer to easily configure a system bus interface based intelligent modem when combined with :

1,200 bps PSK full-duplex modem LSI	$STC9492C_{1D}$ ($STC9492M_{1D}$)
300 bps FSK full-duplex modem LSI	$STC9424C_{0A}$ ($STC9424M_{0A}$)
DTMF dialer	$STC2588C_{1B}$ ($STC2588M_{1B}$)
System bus interface LSI (external data memory)	$STC9610F_{0A}$

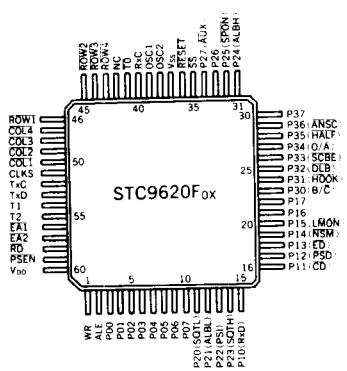
■FEATURES

- Compatible with "AT Command" system
- Can be used with Bell 212A/103 or CCITT V.22/(V.21) protocol (V.21 optional)
- On-chip asynchronous (start-stop synchronous) communication parallel/serial data conversion
- Interface with host CPU ····· Programmable registers
  External data memory : 8 × 8 bits
- Modem control interface ····· Function assignment I/O ports
  Data : Format : Asynchronous serial (Start-stop synchronous)
  Length : 7 or 8 bits
  Parity : None, even, odd, mark, space
  Stop bit length : 1 or 2 bits
  Break signal : Generation/detection function
- Power supply ····· Single 5V
- Package ····· 60-pin QFP (plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



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■PIN DESCRIPTION

Pin name	Pin No.	I/O	Functions
$\overline{WR}$	1	O*1	Provides a timing signal for writing data to external data memory.
ALE	2	O*1	The address of external data memory or external program memory is latched at the falling edge of the output provided at this pin.
P00—P07	3—10	I/O*2	I/O ports for external data memory or external program memory. Each of these pins provides the address of external data memory synchronously with the ALE signal, then reads or writes data synchronously with the $\overline{RD}$ or $\overline{WR}$ signal. Also, it provides the low-order 8 bits of the address of external program memory synchronously with the ALE signal, then fetches the addressed instruction synchronously with the $\overline{PSEN}$ signal.
P20—P23 P24—P27	11—14 31—34	O*2 *3	Output only ports used to control the modem. The P20—P23 provide the high-order 4 bits of the address of external program memory when it is connected.
[SQTL]	[11]		[Controls the squelch transmitter (SQT) pin of STC9430 Series.]
[ALBL]	[12]		[Controls the analog loopback test (ALB) pin of STC9430C Series.]
[PSI]	[13]		[Controls the power save control (PSI) pin of STC9430C Series.]
[SQTH]	[14]		[Controls the squelch transmitter (SQT) pin of STC9492C1D.]
[ALBH]	[31]		[Controls the analog loopback test (ALB) pin of STC9492C1D.]
[$\overline{SPON}$]	[32]		[Turns on/off the speaker to monitor DTMF tone or send/receive signal. Speaker ON···low level Speaker OFF···high level]
	[33]		[For STC9620F0B, this pin must be opened as the device does not use P26.]
[$\overline{AUX}$]	[34]		[Provides an output for driving the relay which determines whether the modem or handset is to be connected to the telephone line. Modem connected···low level Handset connected···high level]
P10—P17	15—22	I*2	Input only ports to control the modem.
[RxD]	[15]		[STC9430C Series or STC9492C1D receive data (RxD) input]
[$\overline{CD}$]	[16]		[STC9430C Series carrier detection signal ($\overline{CD}$) input]
[$\overline{PSD}$]	[17]		[STC9492C1D PSK energy detection signal ($\overline{PSD}$) input]
[$\overline{ED}$]	[18]		[STC9492C1D carrier detection signal ($\overline{ED}$) input]
[$\overline{NSM}$]	[19]		[STC9492C1D non-scramble mark detection signal ($\overline{NSM}$) input]
[$\overline{LMON}$]	[20]		[STC9492C1D call progress tone detection signal ($\overline{LMON}$) input]
	[21] [22]		[For STC9620F0B, these pins must be opened as the device does not use P16/P17.]
P30—P37	23—30	O*2	Output only ports for modem control.
[B/$\overline{C}$]	[23]		[Controls the Bell/CCITT (B/$\overline{C}$) pin of STC9492C1D.]
[$\overline{HOOK}$]	[24]		[Controls the hook switch ($\overline{HS}$) pin of STC2588C1B. Also drives the relay which is used to select on-hook or off-hook for the telephone circuit. Off-hook···low level On-hook···high level]
[$\overline{DLB}$]	[25]		[Controls the digital remote loopback test ($\overline{DLB}$) pin of STC9492C1D.]
[$\overline{SCBE}$]	[26]		[Controls the scramble control ($\overline{SCBE}$) pin of STC9492C1D.]
[O/$\overline{A}$]	[27]		[Controls the originate/answer mode select (O/$\overline{A}$) pin of STC9430C Series or STC9492C1D.]
[$\overline{HALF}$]	[28]		[Controls the 1,200/600 bps data transfer speed select ($\overline{HALF}$) pin of STC9492C1D.]
[$\overline{ANSC}$]	[29]		[Controls the answer tone send control ($\overline{ANSC}$) pin of STC9492C1D.]
	[30]		[For STC9620F0B, this pin must be opened as the device does not use P37.]
$\overline{SS}$	35	I	This signal is used to execute one instruction after another. The pin contains a pull-up resistor (about 100k-ohms), and pulled down (about 10k-ohms) when the device is in stop mode. [For STC9620F0B, the $\overline{SS}$ pin must be opened as the device does not use it.]
$\overline{RESET}$	36	I	Resets the internal CPU into stand-by mode. (A pull-up resistor is incorporated.) Stand-by mode···low level Normal run mode···high level In stand-by mode, the set-up of each function is as follows: • Program counter set to "0" • Stack pointer set to "0" • Program memory area set to addresses 0 through 2047 • Ports P0—P3 set to entry mode • Pin $\overline{T0}$ set to entry mode • External interrupts disabled • Internal interrupts disabled • Pin TxD set to "1" • Timer/counter off

Remarks: The descriptions enclosed in [ ] give functions of the STC9620F0B.

Pin name	Pin No.	I/O	Functions
V_{SS}	37	—	Power supply, 0V
OSC2	38	O	A crystal oscillator (3.579545MHz) is connected between the two pins and capacitors (C_G, C_D) between each of the pins and the power supply pin to make reference signal sources.
OSC1	39	I	
RxC	40	I	Receive clock is entered at this pin. (A pull-up resistor is incorporated.) Data is read from P10 [RxD] synchronously with the falling edge of the receive clock entered.
$\overline{T0}$	41	I	This pin receives the stand-by clear signal. (A pull-up resistor is incorporated.) If at least 2 cycles of low level are applied to this pin with an external interrupt enabled, an interrupt occurs to clear the stand-by mode. [For STC9620F0B, the $\overline{T0}$ pin must be opened as the device does not use it.]
NC	42	—	As this pin is used for special operation verification, it must be held open.
$\overline{ROW4}$–$\overline{ROW1}$ $\overline{COL4}$–$\overline{COL1}$	43—46 47—50	O	Controls key entry for the DTMF dialer. A combination of these outputs enables access to keys 0—9, *, and #. [Controls the STC2588C1B key input ($\overline{ROW4}$–$\overline{ROW1}$, $\overline{COL4}$–$\overline{COL1}$) pins.]
CLKS	51	O	System clock output. In normal run mode, a system clock of 3.579545MHz (the oscillation circuit frequency) is output via the buffer. [The system clock is supplied as the reference signal source for STC9424C0A, STC2588C1B or STC9610F0A.]
TxC	52	I	Transmit clock input. The TxD pin provides transmit data which becomes stable at the falling edge of the transmit clock entered to the TxC pin.
TxD	53	O	Transmit data output Transmit data written into the external data memory according to the format information stored by the host CPU is supplied in serial data form at the baud rate of the transmit clock entered to the TxC pin. [Transmit data is supplied to the STC9430C Series or STC9492C1D transmit data input (TxD) pin.]
T1	54	I	Interrupt control signal input. (A pull-up resistor is incorporated.) When high level is applied to this pin, internal interrupt mode results and the input to pin T2 is nullified. For low level, external interrupt mode results and an interrupt signal entered to pin T2 becomes valid. [For STC9620F0B, the T1 pin must be opened as the device does not use it.]
T2	55	I	External interrupt signal input. (A pull-up resistor is incorporated.) In external interrupt mode, an external interrupt is enabled at the falling edge of the input to pin T2. [For STC9620F0B, the T2 pin must be opened as the device does not use it.]
$\overline{EA1}$	56	I	A combination of these two pin inputs determines control mode. (Pull-up resistors are incorporated.)
$\overline{EA2}$	57	I	
$\overline{RD}$	58	O	Provides a timing signal at which data is read from external data memory.
$\overline{PSEN}$	59	O	Provides a timing signal at which an instruction is taken from external program memory.
V_{DD}	60	—	Power supply, +5V

$\overline{EA2}$	$\overline{EA1}$	Control mode
H	H	Normal run mode
H	L	External program memory mode
L	H	Internal program memory data read mode
L	L	Internal program memory addressing mode

Remarks: The descriptions enclosed in [ ] give functions of the STC9620F0B.

Notes *1 Each control signal holds high level when the device is in the stand-by mode or stop mode, or when the program halts in a single step mode.

*2 In the stand-by mode (system reset), all of P00—P07, P10—P17, P20—P27 and P30—P37 work as input ports.

*3 With external program memory used, no data can be derived from P20—P23.

■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	−0.3 to 7.0	V
Input voltage	V_I	−0.3 to V_{DD}+0.3	V
Output voltage	V_O	−0.3 to V_{DD}+0.3	V
Power Dissipation	P_D	0.5	W
Operating temperature	T_{opr}	−10 to 70	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

■RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V, f_{OSC}=3.579545MHz, Ta=−10 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating voltage	V_{DD}		4.5	5	5.5	V
Operating frequency	f_{OSC}	V_{DD}=5V±10%	50	—	4,000	kHz

■ELECTRICAL CHARACTERISTICS

●DC Characteristics

(V_{DD}=5V±10%, V_{SS}=0V, f_{OSC}=3.579545MHz, Ta=−10 to 70°C)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Low level input voltage	V_{IL}			0	—	0.8	V
High level input voltage	V_{IH1}	Except for $\overline{RESET}$, $\overline{SS}$, OSC1		2.0	—	V_{DD}	V
	V_{IH2}	$\overline{RESET}$, $\overline{SS}$, OSC1		V_{DD}−1	—	V_{DD}	V
Low level output voltage	V_{OL}	I_{OL}=2.0mA		—	—	0.45	V
High level output voltage	V_{OH}	I_{OH}=−1.0mA		2.4	—	—	V
Input current	I_{ILP1}	V_{ILP1}=V_{SS}, Input terminal with pull-up		−250	−100	−30	μA
	I_{ILL}	V_{ILL}=V_{SS}, Latch input terminal		−3	0	3	
	I_{ILP2}	V_{ILP2}=V_{SS}, $\overline{SS}$	RUN	−125	−50	−15	
			STOP	−3	0	3	
Input leakage current	I_{LI1}	V_{LI1}=V_{DD}, Except for $\overline{SS}$		−3	0	3	μA
	I_{LI2}	$\overline{SS}$ terminal open		−3	0	3	
Output leakage current (at High-impedance)	I_{LOP}	V_{LOP}=V_{SS}, I/O port with pull-up		−250	−100	−30	μA
	I_{LOL}	V_{LOL}=V_{SS}, I/O port with latch		−3	0	3	
	I_{LOH}	V_{LOH}=V_{DD}, Output terminal		−3	0	3	
Standby supply current	I_{DDS}	t_{CY}=1μs, Stand-by or stop mode		—	—	20	μA
Operating supply current	I_{DDO}	t_{CY}=1μs, RUN mode		—	6	20	mA
Data retention voltage	V_{DDR}	STOP mode. Without sudden fluctuation of voltage		3.0	—	—	V

●AC Characteristics

(V_{DD}=5V±10%, V_{SS}=0V, f_{OSC}=3.579545MHz, Ta=−10 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Cycle time	t_{CY}		—	1.117	—	μs
ALE pulse width	t_{LL}		200	—	—	ns
Address set up time	t_{AL}		100	—	—	ns
Address hold time	t_{LA}		50	—	—	ns
$\overline{PSEN}$ pulse width	tcc1		300	—	—	ns
$\overline{RD}$ pulse width	tcc2		300	—	—	ns
$\overline{WR}$ pulse width	tcc3		300	—	—	ns
Data-in delay time	t_{RD}		—	—	150	ns
Read data hold time	t_{DR}		0	—	100	ns

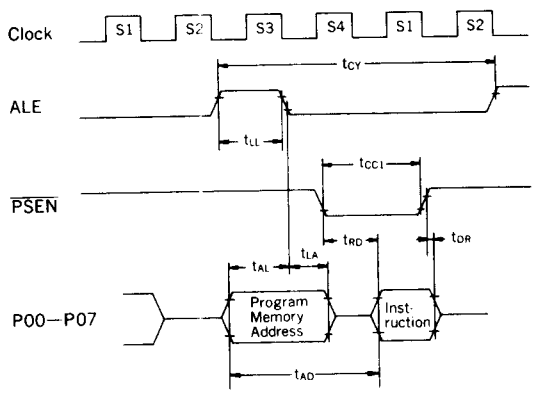
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Write data set up time	t_{DW}		250	—	—	ns
Write data hold time	t_{WD}		5	—	—	ns
$\overline{WR}$ delay time	t_{AW}		200	—	—	ns
Data-in delay time	t_{AD}		—	—	450	ns

Note 1 : The load capacitance of the control pins (ALE, $\overline{PSEN}$, $\overline{RD}$ and $\overline{WR}$) is 80pF.
Note 2 : The load capacitance of port P0 is 150pF.
Note 3 : AC data measuring conditions

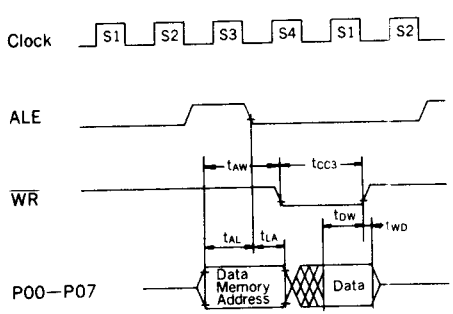
Input : V_{IH}=2.4V, V_{IL}=0.6V
Timing check voltage : Input ····· V_{IH}=2.2V, V_{IL}=0.8V
Output ····· V_{OH}=2.2V, V_{OL}=0.8V
Output load capacitance : Control pins ····· 80pF
Data pins ····· 150pF

●Timing Chart

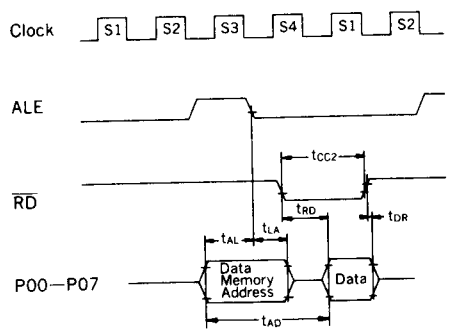
○External Program Memory Fetch Cycle



○External Data Memory Write Cycle

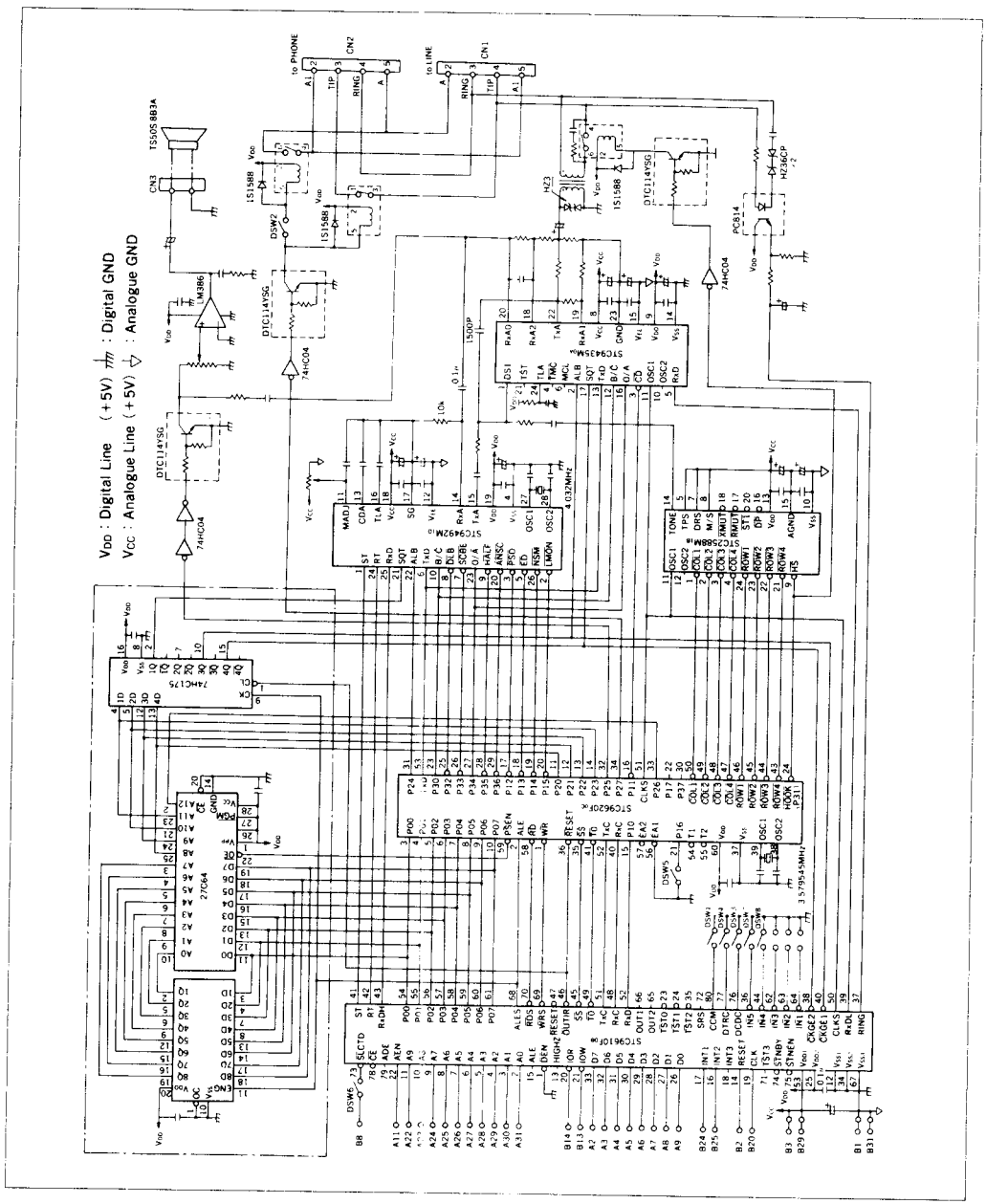


○External Data Memory Read Cycle



■EXAMPLE OF APPLICATIONS

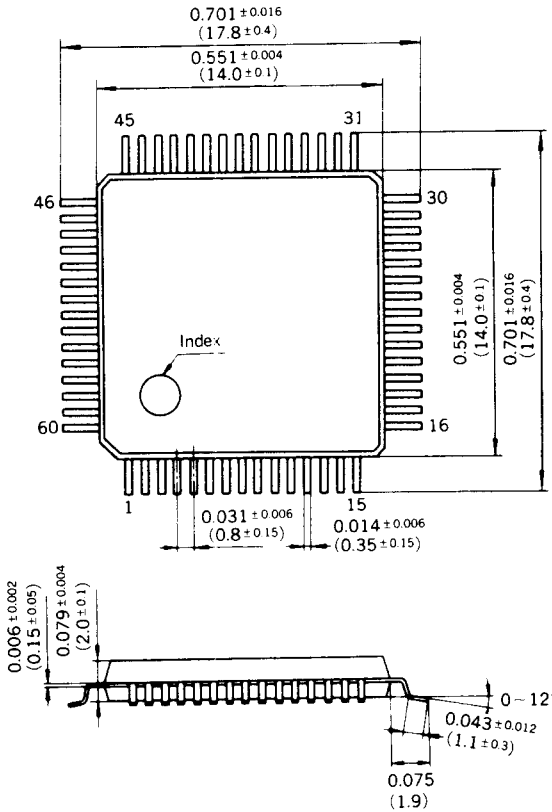
The configuration shown below is a system bus interface based intelligent modem which uses an STC9620F$_{0B}$ in combination with four chips : STC9610F$_{0B}$, STC9492C$_{1D}$ (STC9492M$_{1D}$), STC9435C$_{0A}$ (STC9435M$_{0A}$) and STC2588C$_{1B}$ (STC2588M$_{1B}$).



■PACKAGE DIMENSIONS

F60-2

60-pin QFP



unit : inch
(mm)