Preliminary Datasheet

FUJITSU

MB87Q2040

January 2005
Version 2.0

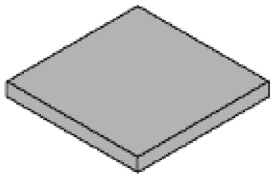
FME/MS/CHEETAH/DS/xxxx

GPS/AGPS Baseband Processor

The MB87Q2040 ("Cheetah") is a GPS/AGPS baseband processor with novel decoding algorithms achieved using 44,000 effective correlators. It is capable of working indoors and receiving signals down to -157.5dBm during acquisition and tracking. The device takes in a single low-IF input from a GPS-RF radio and supplies location measurement data to the host processor. A UART provides a simple 2-wire interface to host applications. The chip is fabricated using Fujitsu's 0.11µm CMOS technology, offering low power consumption from its 1.2V core supply, and small package size. The MB87Q2040 together with a RF radio front-end make up Fujitsu's low cost, high performance GPS/AGPS solution.

PLASTIC PACKAGE

BCC++ 48



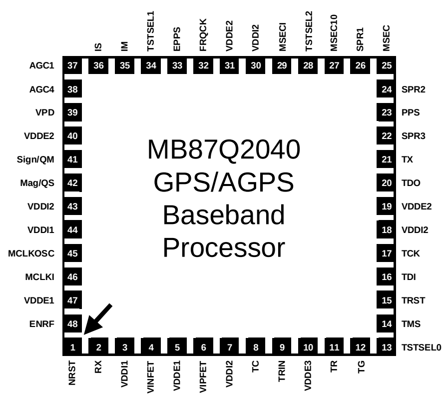
Package Dimensions

7 mm x 7 mm

Features

- GPS L-band C/A code operation
- Supports both autonomous and Assisted-GPS modes
    - MS-based and MS-assisted
- High indoor sensitivity
- 7m outdoor accuracy (CEP 95%) and 20m indoor
- Fast Time To First Fix (TTFF)
    - typically 3s when hot and 40s when cold
- Low power dissipation
    - 15 mW - tracking
    - 69 mW - acquisition
- Control software executes on a host processor
    - requires 4-6 MIPS, run as a background process
- 1 or 2.5 second update rate
- Industrial temperature range operation (-40ºC to +85ºC)

PIN ASSIGNMENT



Not to scale. Viewed from above.

Applications

- Multi-carrier, Multi-standard cellular handsets
- W-CDMA, GSM/EDGE, UMTS, PDC, CDMA, etc.
- Telematics, Navigation/Security and Gaming/Tracking

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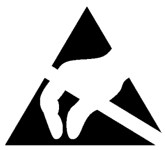

CAUTION

ELECTROSTATIC DISCHARGE SENSITIVE DEVICE

High electrostatic charges can accumulate in the human body and discharge without detection. Ensure proper ESD procedures are followed when handling this device.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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1 Functional Description

The MB87Q2040 GPS/AGPS Baseband Processor is part of a two-chip solution supporting both autonomous and assisted GPS operation. The accompanying RF chip incorporates all the required radio functionality to complete the solution. A system block diagram is shown in Figure 1.

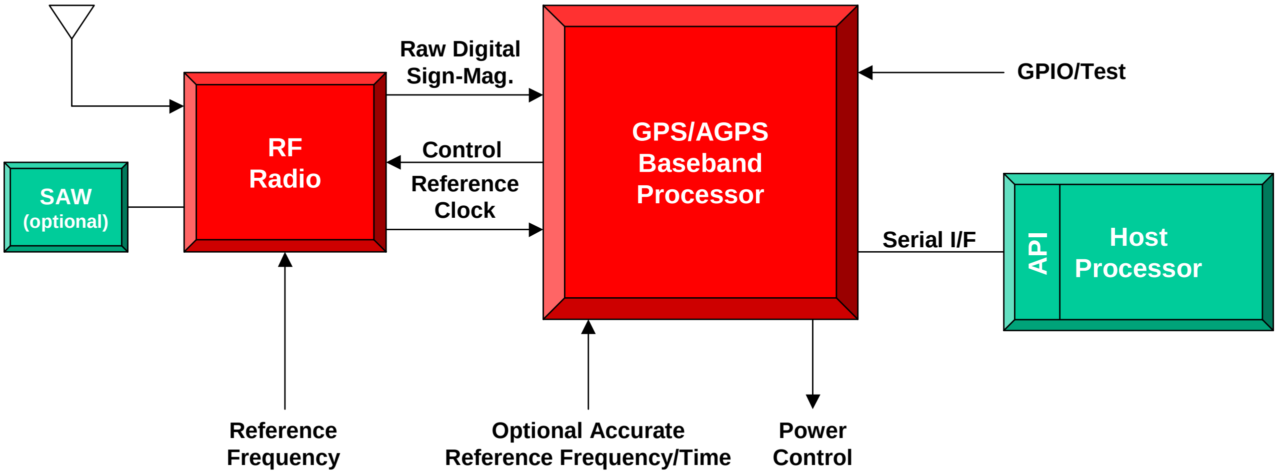

Figure 1 System Block Diagram

System Features include:

- GPS L-band C/A code operation
- High indoor sensitivity down to -157.5dBm for both acquisition and tracking
- Works in both assisted GPS (MS-based and MS-assisted) mode and also autonomous mode
- Fast TTFF, typically 3s when hot and 40s from cold (outdoors). Aided light-Indoor TTFF 5-8 secs
- 7m outdoor accuracy (CEP 95%) and 20m indoor
- 1 second update rate (can also integrate for 2.5 seconds to aid indoor operation)
- UART interface to host processor
- Control software runs on a host processor as a background process, and does not need high MIPS or large RAM
- 3V (2.7-3.6V) I/O and 1.2V (1.1-1.3V) core logic power supplies
- Typical leakage current in deep sleep mode is <100μA (25°C)
- All chips handle Industrial operating temperature range (-40°C to +85°C)
- Interface to MB15H156 BiCMOS RF radio integrating IF-filters, VCO, oscillator & LNA

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1.1 GPS/AGPS Baseband Processor

The MB87Q2040 baseband processor includes a hard-wired engine with 44,000 effective correlators. Input from the RF radio is a single low-IF, and communication with a host processor via a serial UART interface. The control software runs on the host processor and requires around 4-6MIPS of processing capacity, depending on whether an autonomous or assisted mode is being implemented. The software executes as a background process that requires no real-time response to interrupts.

The device is fabricated in 0.11µm CMOS technology, benefiting from a 1.2V internal core voltage to minimise current consumption.

1.2 GPS/AGPS RF Radio

A RF radio is required to complete the chipset and provide the low-IF signal required by the baseband processor. Dependent on the target application, there is a choice of two RF radios. One is a CMOS chip which caters for a wide range (10-40MHz) of reference frequencies, while the other is a lower-cost BiCMOS chip solution requiring a fixed 27.456MHz reference frequency.

Depending on the target application and environment of the product, the reference frequency may be supplied by an external TCXO, directly from an existing reference frequency or from an AT-cut crystal oscillator. The AT-cut crystal oscillator is only suited to environments where temperature changes are slow. In this case, an oscillator circuit integrated on the RF radio may be used. Patented compensation algorithms help to stabilise the frequency and relax the requirements on the crystal.

An RF SAW filter may be required in applications where high level blocking signals must be tolerated. This Fujitsu solution is capable of working indoors and receiving/decoding low sensitivity signals down to -157.5dBm during acquisition and tracking. The solution can operate completely autonomously or in assisted mode (assisted modes can be MS-based or MS-assisted).

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2 GPS/AGPS Baseband Processor

A functional block diagram of the GPS/AGPS Baseband Processor is shown in Figure 2.

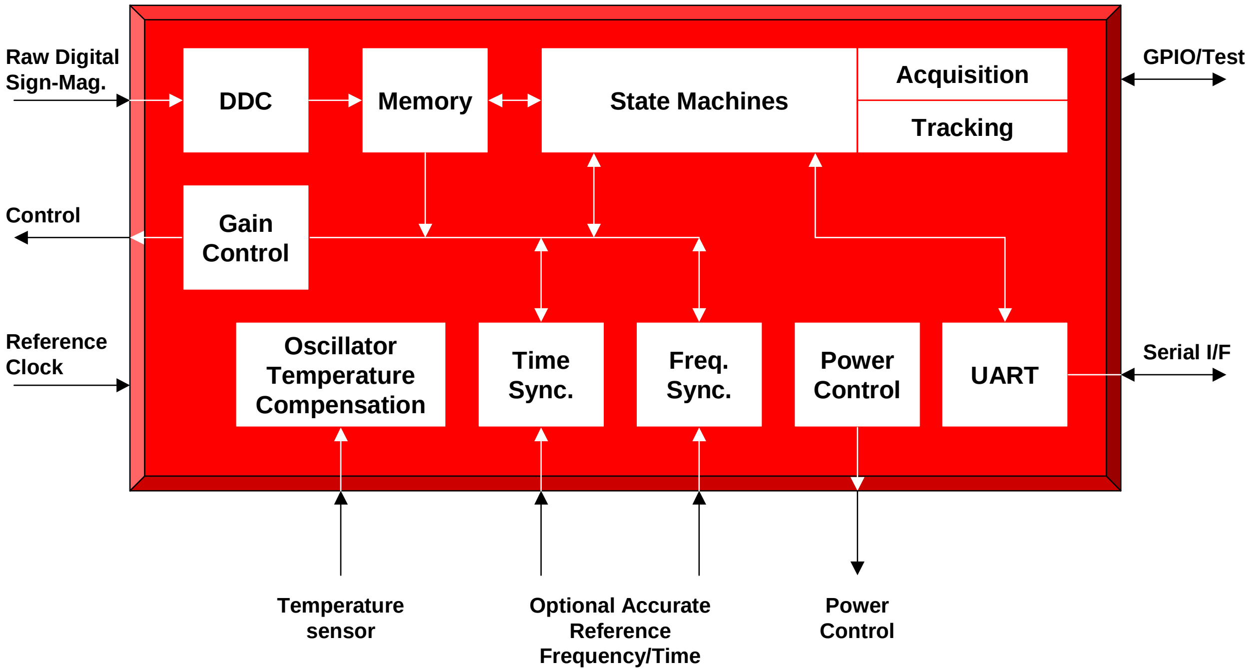

Figure 2 GPS/AGPS Baseband Processor Functional Block Diagram

2.1 Reference Frequency

The MB87Q2040 implements a patented "software compensated crystal oscillator" algorithm that helps tolerate crystal or other reference frequency instability.

A reference frequency clock is supplied from the RF chip and input to MB87Q2040. This is required to be 27.456MHz with ±5ppm accuracy (all causes), and <0.016ppm/s stability (drift + micro-jumps). For environments where the receiver temperature changes slowly (<1^{o}C/minute) an AT-cut crystal will work over the entire temperature range, aided by the software compensation algorithm. For more rapid temperature changes, a TCXO is required.

The Fujitsu GPS/AGPS chipset has a number of options for generation of the reference frequency, depending on the target application/product. The CMOS RF chip may use any modem's existing reference frequency (in the range 10-40MHz) or a dedicated external crystal/TCXO. The BiCMOS RF device requires 27.456MHz. Using a dedicated crystal/TCXO makes this system independent of the application environment around it and allows operation either autonomously or in an assisted mode.

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2.2 Core Engine State Machines

The heart of MB87Q2040 is the GPS Intellectual Property (IP) licensed to Fujitsu from eRide Inc. This IP includes a GPS processing engine and the Control software on the host processor (see section 3).

To achieve a fix, the algorithms on the processing engine employs two different state machines, the Opus State Machine (OSM) and Firmware State Machine (FSM):

2.2.1 Opus State Machine (OSM)

The OSM manages all the code-delays, frequency-offset, correlation as well as interfacing between the hardware and all peripherals.

2.2.2 Firmware State Machine (FSM)

The FSM offers 3 modes of operation:

- An Indoor State Machine (IDSM) mode with a high sensitivity acquisition and tracking block capable of searching and tracking to a sensitivity of -155dBm (1s integration time) and -157.5dBm (2.5s integration time).

- An Outdoor State Machine (ODSM) mode which searches all 32 satellites, with -145dBm sensitivity without intervention from the host processor.

- A Time-Tracking State Machine (TSM) mode which collects navigational data and provides synchronous measurements so that GPS time and navigation data can be decoded and utilized without host processor interrupts.

This GPS processing engine has 44,000 effective correlators available to either search 32 satellites at several time/frequency hypotheses, or search thousands of time/frequency hypotheses for a few satellites that are in view. Search windows (time/frequency hypotheses) can be configured for each satellite.

2.3 Power Supply Regions

MB87Q2040 has two power regions, PowerON and PowerSW. PowerON should remain powered at all times, including when the device is in deep sleep mode when PowerSW would be switched off.

PowerON consists of VDDI1 (1.2V) and VDDE1 (3.0V) and should only be switched off during a full system power down.

PowerSW consists of VDDI2 (1.2V) and VDDE2/3 (3.0V) and can be powered up or down during device operation, but should only be powered while PowerON is on.

To prevent reliability problem VDDE should not be powered whilst VDDI is not.

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2.3.1 Without External PowerSW Control

If external power switching of the PowerSW region is not employed, power up of MB87Q2040 is relatively simple and the following power sequence is recommended.

Power On	VDDI > VDDE > Signal
Power Off	Signal > VDDE > VDDI

All VDDI (1.2V) supplies should be enabled together, followed by all VDDE (3.0V) supplies together.

NRST should be held low until all supplies are stable and MCLKI is receiving a stable clock (running with no glitches).

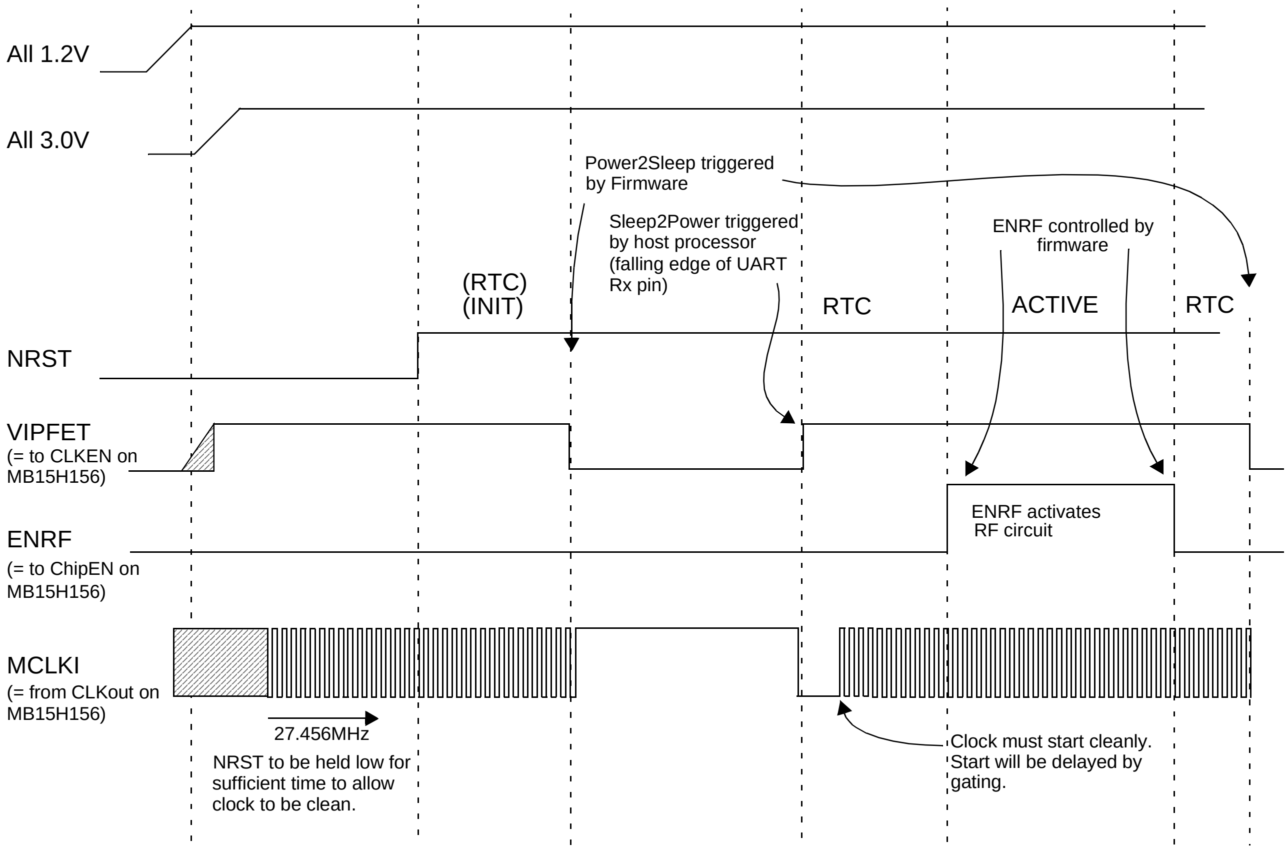

Figure 3 Power sequence without external power switching

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2.3.2 With External PowerSW Control

If external power switching is employed, the power up sequence is more critical. The recommended sequencing is illustrated in Figure 4.

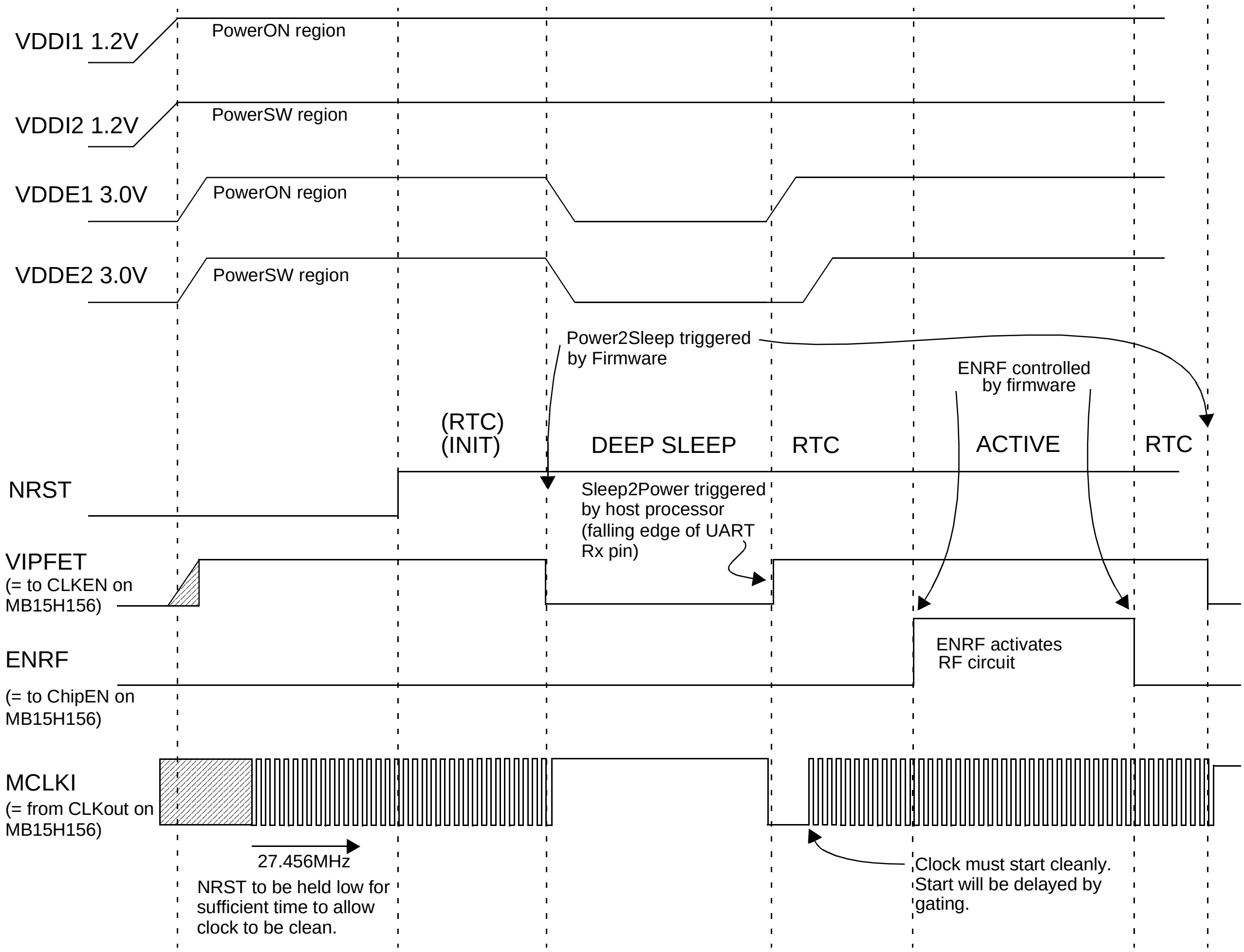

Figure 4 Power sequence with external power switching

2.4 Power Modes

All power modes are selectable via the control software.

2.4.1 Deep Sleep Mode

The deep sleep mode has the lowest power consumption. Use of separate on-chip supply regions allows full power down of most of the chip and stopping of all clocks. Power to the PowerSW region together with its related I/O signals is OFF, and MCLK (the master clock for all internal clocks) is turned OFF as well. Signal ENRF is OFF and signal NRST is in a disabled state. Wake up from deep sleep is invoked by a low transition on the RX pin, which then puts the chip into the RTC mode.

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When the device initiates Deep Sleep mode VINFET is set to ‘1’ and VIPFET to ‘0’, shutting down the externally switched supplies (VDDE2/VDDE3 and VDDI2) if power switching is employed.

VIPFET is linked to the CLKEN of the RF Radio, thus disabling the clock into MCLKI. All internal signals passing between MB87Q2040’s power regions are disabled.

Before a wake-up sequence is started all signals in the powerSW region should be considered unknown, and VDDI2 & VDDE2/VDDE3 will be off if power switching is used. The following events occur at wake up.

A falling edge on RX will trigger the wake-up sequence. VIPFET and VINFET will toggle state and this shall power-up VDDI2 and VDDE2/3. Once the supply is settled, NRST should be held low for at least 10ns after VDDI2/VDDE2 is stable. During power-up the external clock signal fed to MCLKI should be stable (running with no glitches).

2.4.2 Real Time Clock (RTC) Mode

In RTC mode the majority of the logic is not clocked, but power supply is ON for the entire chip. ENRF is OFF and only millisecond (MSECxx) outputs and peripherals are turned ON with clocks running. All other clocks are turned OFF to save power.

2.4.3 Search Mode

In this mode the search is performed, which means highest power dissipation. All the clocks are running, multiple satellites are being searched, and the ENRF is ON.

2.4.4 Track Mode

In Track mode, a certain number of satellites are tracked with fine adjustments in code search. Not all clocks are running, so power dissipation is lower than search mode. ENRF is ON.

2.5 JTAG Boundary SCAN Support

While operating normally, asserting the JTAG reset, TRST, to level “0” for more than 10ns initiates the JTAG scan operation, and the Boundary SCAN registers enter the system test mode.

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3 Host Processor and Control Software

Interfacing the MB87Q2040 to the host processor is via a serial port (UART).

The UART interface can handle Baud rates in the range 9,600-57,600, with 8-bit data, odd parity and 1-stop-bit.

The baseband processor takes its reference frequency and the raw IF sign/magnitude data from the RF radio. After completing the GPS processing measurement results are sent to the host processor where the control software determines the position, velocity, and time (PVT) results. The Control software is written in C and is independent of the target operating system. Figure 5 shows the structure of the control software residing on the host processor.

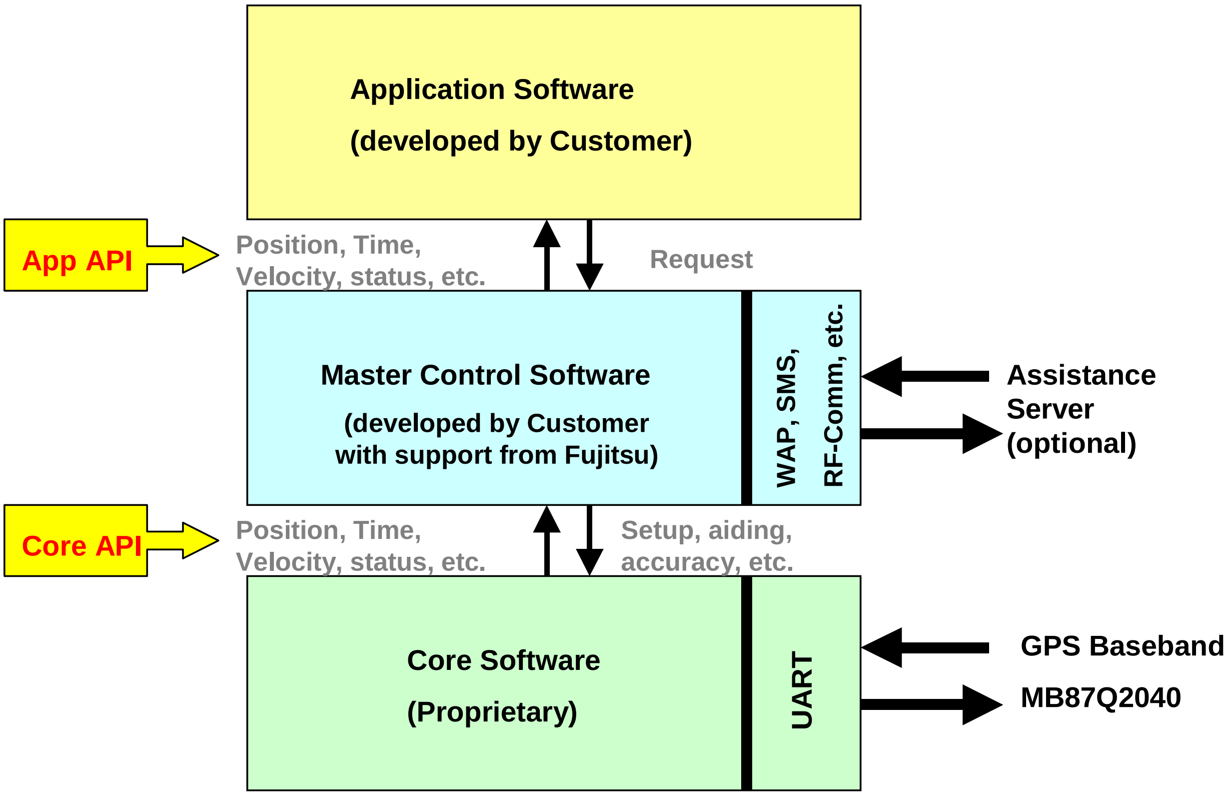

Figure 5 Control Software layers residing on Host Processor

The software is run as a background process on the host processor and requires no real-time interrupts, no host libraries and no RTOS. The processing power required will be dependent on the application and whether GPS-aiding is required; normally some 4-6 MIPS will be required from host processor.

The code footprint varies dependent on the application and efficiency of the application code. For example, an autonomous only implementation on an ARM7TDMI platform resulted in the overall software footprint requiring around 198kB ROM and 70kB RAM on the host processor.

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Two levels of API libraries are available to the customer. The first layer has a “Core API” library that includes functions to perform the basic control decisions for the receiver run mode including setup, aiding availability/type and required minimum accuracy for measurements, see section 3.1.

Customers will tailor the control code based on their requirements, together with Fujitsu’s application engineers. Fujitsu can supply appropriate wire/wireless interface adapters (WAP, RFcomm, TCP/IP, etc.) as well as appropriate aiding-data protocol (3GPP, IS801, NMEA0183 etc.) for communicating with the aiding server hosted by the operator. This layer will also contain and maintain OS specific functions that shall include the standard communication protocols via ports including the UART and TCPIP/WAP/etc.

The second layer of API library will be supplied to customers to assist development of end-user applications such as mapping, directions, boundary areas and security alarms. It also supports/ manages basic location measurement requests for data such as position, velocity, time and GPS status.

Details of the Control software and API libraries are described in a separate document, but an introduction is included in section 3.1. Porting the Control Software to any customer specific platform is eased by having the whole code in the C programming language. Fujitsu will assist with porting and/or the optimisation of this Control software to the customer’s host processor.

MB87Q2040 takes its reference frequency and the raw IF sign/magnitude data from the RF chip, performs the GPS processing and sends the measurements to the host processor, where the control software will provide the final PVT (position, velocity, and time) results.

3.1 Core API Library Introduction

The API library reside on the host processor and controls MB87Q2040. The library consists of three input functions and one output function. The input functions are called by the sample application. The output function is called by the master and must be implemented by the same application. These are:

3.1.1 Input Functions

```
int erStartClient()
```

This function is called to start the client. It will create a thread and return immediately.

```
int erStopClient()
```

This function is called to stop the client. It will not return until all client threads have completed, resources have been freed and MB87Q2040 is in a shutdown state.

```
int erSetAidingOptions(erAidingStruct aiding)
```

This function is called to configure the GPS aiding to be used. It must be called before the call to erStartClient(). If erStartClient() is not preceded with a call to this function, the client will run in autonomous mode.

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3.1.2 Output Function

```
int erProvidePvt(erPvtStruct erPvt)
```

The Master will call this function when it has PVT data available. This function is expected to return immediately. The argument is a structure containing the PVT data and is defined below.
An example application code is shown in Appendix A.

3.1.3 Resulted Measurements

- GPS time of this report
- Time of position fix
- Bit masked flag detailing the type of fix calculated
- Number of SVs in fix
- Indicates source of chosen solution
- If chosen fix is sub solution, indicates SV that removed to calculate fix
- Indicates source of reported altitude
- ECEF position coordinates in meters
- LLA position coordinates in radians, radians, meters
- Filtered ECEF position coordinates in meters
- Filtered LLA position coordinates in radians, radians, meters
- ECEF velocity coordinates in meters per second
- ENU velocity coordinates in meters per second
- Filtered ECEF velocity coordinates in meters per second
- Filtered ENU velocity coordinates in meters per second
- Filtered clock bias in meters
- Filtered clock drift in meters per second
- PDOP of fix
- Accuracy of filtered position in meter
- Accuracy of filtered velocity in meters per second
- Accuracy of filtered bias in meter
- Accuracy of filtered drift in meters per second
- Horizontal accuracy of filtered position in meter per second
- Vertical accuracy of filtered position in meter per second
- Horizontal speed in meter per second
- Vertical speed in meter per second
- Direction of user movement in radians

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4 Performance

4.1 Operating Modes

MB87Q2040 can be set up to perform in three possible modes.

4.1.1 Autonomous mode

In this mode, MB87Q2040 will decode Navigation data from Satellites only. It therefore needs a good signal strength (to as low as -145dBm) while decoding for first fix. TTFF in this mode is slowest as MB87Q2040 downloads the ephemeris data at 50bps (taking ~30s). Once MB87Q2040 has received ephemeris and Almanac data (i.e. its status becomes ‘hot’), then it can go on to supply fix measurements indoors with sensitivity down to -157.5dBm. An application/user may supply some time or location assistance, if available (e.g. handset time or cell location currently in use), resulting in improved TTFF.

4.1.2 Assisted, MS-Based mode

Either on wake up from autonomous mode, or upon a request for a fix after current aiding data has expired (ephemeris is valid for four hours, and refreshed every two hours), MB87Q2040 shall request Navigation data from the aiding server via the implemented interface (SMS, WAP, TCP/IP, RRLP, etc.) using any aiding-data format (3GPP/2, IS801, etc.). MB87Q2040 will continue to supply fixes and update its ephemeris/almanac as time permits and without further resource/help from the aiding server. Therefore assistance can be good for hours.

Assisted, MS-based mode of operation achieves the fastest Time To First Fix.

MB87Q2040 aiding interface is independent of the aiding server. eRide Inc. has a worldwide reference network and can supply the aiding server to any operator and/or infrastructure companies.

4.1.3 Assisted, MS-Assisted Mode

This mode directs MB87Q2040 to request server aiding for every fix every time, and then sends the measurements to the network for computing before then receiving the coordinates. This method can create a lot of network traffic in a continuous application such as tracking/Navigation, and therefore will be slow to fix.

4.2 Sensitivity

The algorithm implemented in MB87Q2040 can acquire and track weak signals down to -155dBm using 1s integration time and -157.5dBm while integrating for 2.5s. MB87Q2040 achieves this sensitivity in both autonomous and assisted modes as well as during both acquisition and tracking of satellites.

4.3 Time To First Fix

The Time To First Fix (TTFF) is as follows:

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- Hot[1] or aided start outdoors take typically 3 seconds
- From Cold[2] on autonomous start, outdoors, takes typically less than 40 seconds
- Warm[3] start takes about 5-30 seconds, outdoors

1. Hot start means that the receiver has full Ephemeris navigation data, Almanac, time to within 10s, and knows its location to within 15km (similar to being aided).
2. Cold start means the receiver has no knowledge of RTC, its location, Almanac or Ephemeris and no aiding is available.
3. Warm start means the receiver has any combination of time, current location, Almanac, and Ephemeris.

4.4 Accuracy

The MB87Q2040 GPS/AGPS baseband processor meets the requirements for FCC-E911 regulations for October 2005.

The results from MB87Q2040 performance shows that it is possible to achieve better than 20m accuracy indoors and in urban canyons. This level of accuracy was previously only achievable in outdoor open spaces.

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5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Parameter	Notes	Symbol	Ratings			Units
			Min.	Typ.	Max.	
Supply voltage						
Internal supply		VDDI	-0.5		1.8	V
External Supply		VDDE	-0.5		4.0	V
Input Voltage			-0.5		VDDE+0.5	V
Storage Temperature		T_{ST}	-40		+85	^oC
Junction Temperature		T_J	-40		+125	^oC
T_A (min) to T_A (max), VSS = 0V						

5.2 Recommended Operating Conditions

Parameter	Notes	Symbol	Ratings			Units
			Min.	Typ.	Max.	
Supply voltage						
Internal supply		VDDI	1.1	1.2	1.3	V
External Supply		VDDE	2.7	3.0	3.6	V
Storage Temperature		T_{ST}	5		+30	^oC
Ambient Temperature		T_A	-40		+85	^oC
T_A (min) to T_A (max), VSS = 0V						

5.3 Clock Specifications

Parameter	Notes	Symbol	Ratings			Units
			Min.	Typ.	Max.	
Clock Input						
Clock frequency	1	F_{clk}		27.456		MHz
Clock input duty cycle			40		60	%
T_A (min) to T_A (max), VDDIx = +1.2V, VDDEx = +3.3V, VSS = 0V						

1. ±5ppm accuracy (all causes) and <0.016ppm/s stability (drift + micro-jumps)

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5.4 DC Characteristics

Parameter	Notes	Symbol	Ratings			Units
			Min.	Typ.	Max.	
CMOS inputs						
High-level input voltage		V_{IH}	2.0		VDDE	V
Low-level input voltage		V_{IL}	0		0.8	V
CMOS outputs						
High-level output voltage	1	V_{OH}	VDDE - 0.2		VDDE	V
Low-level output voltage	2	V_{OL}	0		0.2	V
Internal Pull-up/down Resistance			15	33	70	kΩ

T_A (min) to T_A (max), VSS = 0V
1. I_{OH} = +4mA
2. I_{OL} = -4mA

5.5 Power Consumption

Parameter	Notes	Symbol	Ratings			Units
			Min.	Typ.	Max.	
Power Supply						
PowerON region, core		IDDI1			30	mA
PowerSW region, core		IDDI2			150	mA
PowerON region, external		IDDE1			10	mA
PowerSW region, external		IDDE2			10	mA
Oscillator region, external		IDDE3			TBD	mA
Pad leakage current				10		µA
Power Dissipation	1	P_D				
Real Time Clock mode				2		mW
Tracking after a fix				15		mW
‘Cold’ acquisition (indoor)	2			77		mW
‘Cold’ acquisition (combination)	3			69		mW
‘Hot’ Search (outdoor)				32		mW
Deep Sleep mode				99		µW
Wake-up from Deep Sleep mode				60		mW

T_A (min) to T_A (max), VDDIx = +1.2V, VDDEx = +3.3V, VSS = 0V
1. Current consumption and Power dissipation are data related. Maximum figures are by evaluation.
2. High sensitivity (indoor) search
3. 6 Satellites (outdoor), 2 (indoor)

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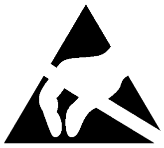

CAUTION

ELECTROSTATIC DISCHARGE SENSITIVE DEVICE

High electrostatic charges can accumulate in the human body and discharge without detection. Ensure proper ESD procedures are followed when handling this device.

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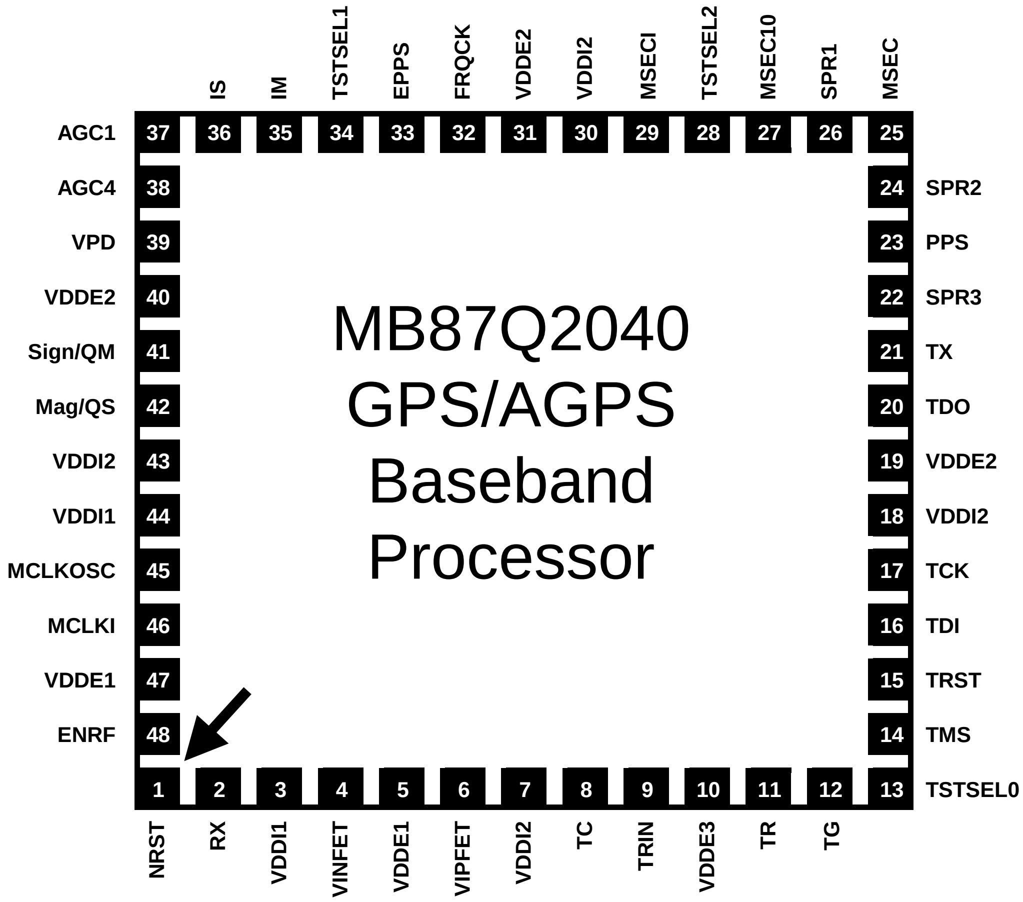
6 Mechanical Data

6.1 Pin Assignment



Not to scale. Viewed from above.

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6.2 Pin Definition

Power & Ground

Pin Nos.	Pin Name	Input/ Output	Description	Note
3, 44	VDDI1	Power	Internal PowerON supply, +1.2V	Decouple to VSS
5, 47	VDDE1	Power	External PowerON supply, +3.0V	Decouple to VSS
7, 18, 30, 43	VDDI2	Power	Internal PowerSW supply, +1.2V	Decouple to VSS
19, 31, 40	VDDE2	Power	External PowerSW supply, +3.0V	Decouple to VSS
10	VDDE3	Power	External supply for oscillator cells, +3.0V	Decouple to VSS
49	VSS	Power	Ground, 0V	Ground pad under package

MOFSET Switches

Pin Nos.	Pin Name	Input/ Output	Description	Note
4	VINFET	O	Gate control of the P-type FET I/O voltage power switch. This switches the 3.3V supply to the VDDE2 and VDDE3 pins in PowerSW region. See Application notes for circuit.	VINFET=1 in Sleep Mode VINFET=0 in RTC/Active modes
6	VIPFET	O	Gate control of the N-type FET Core voltage power switch. This switches the 1.2V supply to all VDDI2 pins located in the PowerSW region. See Application notes for circuit.	VIPFET=0 in Sleep Mode VIPFET=1 in RTC/Active modes

RF Radio Interface

Pin Nos.	Pin Name	Input/ Output	Description	Note
41	Sign/QM	I	IF Sign data input, or Real-part of Magnitude data for I/Q input. Sampled on both edges of 27.456MHz clock.	0=negative signal 1=positive
42	Mag/QS	I	IF Magnitude data input, or Real-part of Sign data for I/Q input. Sampled on both edges of 27.456MHz clock.	0=below threshold 1=above threshold
36	IS	I	Imaginary part of Sign data for I/Q input	Connect to VSS for IF input
35	IM	I	Imaginary part of Magnitude data for I/Q input	Connect to VSS for IF input
46	MCLKI	I	27.456MHz reference clock	Stop high when inactive
48	ENRF	O	Enable/disable RF radio control	0=disable, 1=enable
37	AGC1	O	RF AGC control. If the RF radio has the ability to either control its own gain or be externally controlled, AGC1 can be used to enable/ disable this internal control.	0='internal mode' 1='external mode'
38	AGC4	O	Controls an RF radio AGC in 'external mode'. AGC4 is a PWM output with selectable sign. Linear in dB change between 0V (max gain) and 2V (min gain), and flat gain beyond 2V	

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UART Interface

Pin Nos.	Pin Name	Input/ Output	Description	Note
2	RX	I	Receive data from host processor	
21	TX	O	Transmit data to host processor	

Additional Function Pins

Pin Nos.	Pin Name	Input/ Output	Description	Note
1	NRST	I	Reset	0=reset, 1=active
23	PPS	O	Pulse per second output	
33	EPPS	I	Pulse per second input. Used for accurate reference time if available from host system. The control software will initiate sync of this signal with the RTC.	Internal pull-down
32	FRQCK	I	Accurate reference frequency input. Used to connect an accurate reference source if available from host system. The control software will initiate sync of this signal with the reference frequency.	Internal pull-down
45	MCLKOSC	O	XTAL oscillator cell output	
8	TC	O	TCO capacitor port	Please refer to Section 7
11	TR	O	TCO thermistor port	Please refer to Section 7
12	TG	I	TCO gate port	Please refer to Section 7
9	TR_IN	I	TCO external TR connection	Connect to TR (pin 11)

JTAG & Test

Pin Nos.	Pin Name	Input/ Output	Description	Note
16	TDI	I	JTAG input	Internal pull-up
20	TDO	O	JTAG output	
17	TCK	I	JTAG clock	Connect to VSS
15	TRST	I	JTAG reset	Connect to VSS to disable
14	TMS	I	JTAG	Internal pull-up
39	VPD	I	Fujitsu test pin	Connect to VSS
13	TSTSEL0	I	Fujitsu test pin	Internal pull-down
34	TSTSEL1	I	Fujitsu test pin	Internal pull-down
28	TSTSEL2	I	Fujitsu test pin	Internal pull-down
26	SPR1	I	Fujitsu test pin	Internal pull-down
24	SPR2	I	Fujitsu test pin	Internal pull-down
24	SPR2	I	Fujitsu test pin	Internal pull-down
25	MSEC	O	Test pin - 1msec output	
27	MSEC10	O	Test pin - 10msec output	
29	MSECI	O	Test pin - msec interrupt	

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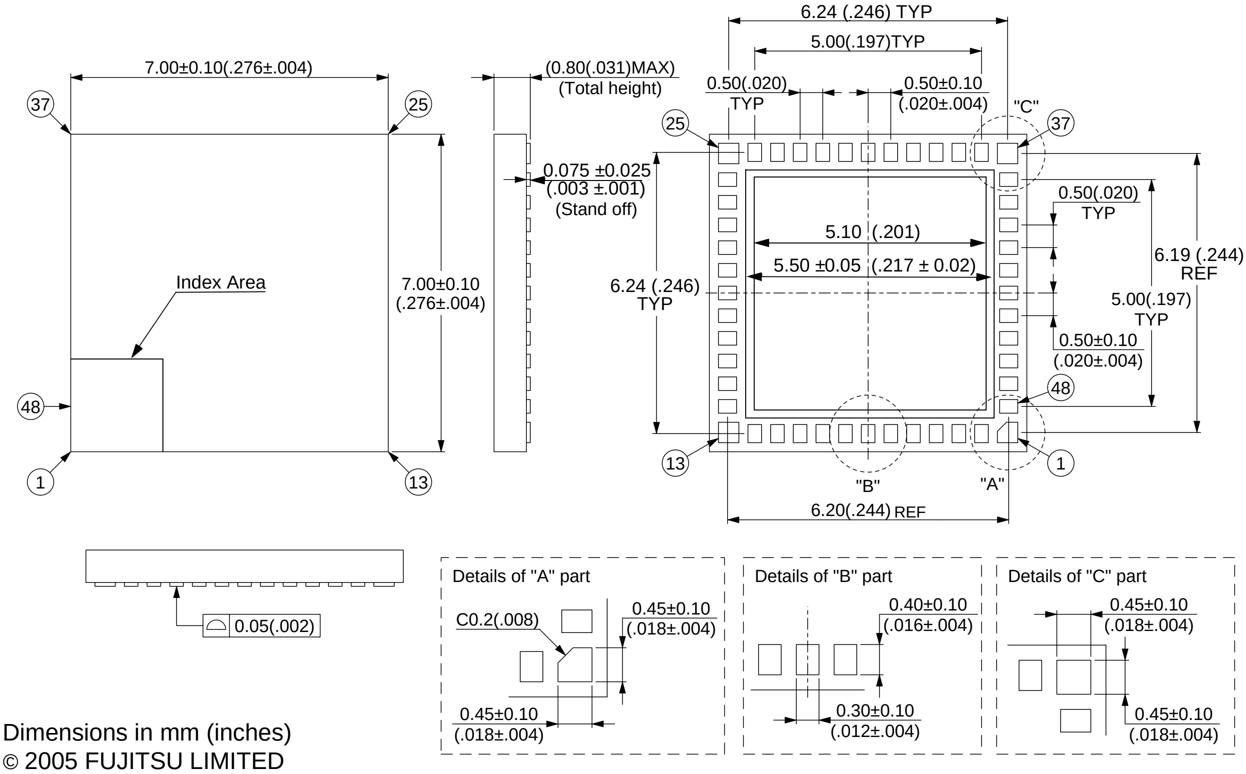
6.3 Package Data

48-pin plastic BCC
(LCC-48P-M06)



Dimensions in mm (inches)

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Mounting Rank H08: After opening the moisture-proof packaging reflow is acceptable twice within 8 days using the Fujitsu H-rank temperature profile.

6.4 Ordering Information

The following reference should be used when ordering devices,

- Tray MB87Q2040PVH-GE1
- Tape & Reel MB87Q2040PVH-G-ERE1

For further assistance please contact your Fujitsu Microelectronics' sales representative.

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7 Applications

For applications information and details of customer development kits please refer to the appropropriate documents.

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Appendix A API Code Application Example

Appendix A.1 Structure Definitions

```
    typedef struct {
    U32 pvtGpsTime;// GPS time of this report.
    U32 pvtFixTime;// Time of position fix.
    U8  pvtFixType;// Bitmasked flag detailing the type of fix calculated.
    U32 pvtFixSVs;// Number of SVs in fix.
    U8  pvtFixSource;// Indicates source of chosen solution.
    U8  pvtSubsolnSv;// If chosenfix is subsolution, indicates SV that
removed to calculate fix.
    U8  pvtAltSource;// Indicates source of reported altitude.
    S32 pvtPos[3];// ECEF position coordinates in meters.
    S32 pvtLla[3]; // LLA position coordinates in radians, radians,
meters.
    S32 pvtPosFilt[3];// Filtered ECEF position coordinates in meters.
    S32 pvtLlaFilt[3]; // Filtered LLA position coordinates in radians,
radians, meters.
    S32 pvtVel[3];// ECEF velocity coordinates in meters per second.
    S32 pvtEnu[3];// ENU velocity coordinates in meters per second.
    S32 pvtVelFilt[3];// Filtered ECEF velocity coordinates in meters per
second.
    S32 pvtEnuFilt[3];// Filtered ENU velocity coordinates in meters per
second.
    S32 pvtBias; // Filtered clock bias in meters.
    S32 pvtDrift;// Filtered clock drift in meters per second.
    S32 pvtPdop; // PDOP of fix.
    U32 pvtSigmaPos;// Accuracy of filtered position in meter.
    U32 pvtSigmaVel; // Accuracy of filtered velocity in meters per
second.
    U32 pvtSigmaBias;// Accuracy of filtered bias in meter.
    U32 pvtSigmaDrift;// Accuracy of filtered drift in meters per second.
    U32 pvtSigmaHoriz;// Horizontal accuracy of filtered position in meter
per second.
    U32 pvtSigmaVert;// Vertical accuracy of filtered position in meter
per second.
    U32 pvtSpeed;// Horizontal speed in meter per second.
    S32 pvtClimb;// Vertical speed in meter per second.
    S32 pvtDirection;// Direction of user movement in radians.
    } erPvtStruct;
```

Appendix A.2 Sample Application

```
static osSerialStruct sioDebug;
osSemaphoreStruct debugSema;
/**
```

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```
 * Program main thread routine.
 */
OS_THREAD_FUNC_RT mainThread(OS_THREAD_FUNC_ARG) {
    osInitSemaphore(&debugSema);
    erStartClient();
    while (1) {
        osSleep(1000);
        if (osGetKey() == 'q') {
            erStopClient();
            break;
        }
    }
   OS_THREAD_FUNC_RTRN(0);
}

/**
 * Program main routine.
 */
void main(int argc, char *argv[]) {
    int comPort;
    erAidingOptionsStruct aid;

    comPort = 1; // Specify COM  port to be used.
    aid.aidProtocol = 0;// Specify aiding protocol to be used,
                          //     0 = autonomous.
    erSetAidingOptions(aid);
    osStartThread(mainThread,0,NULL);
    while(1) osSleep(1000);
}
/**
 * Output data over serial IO / stdout
 */
void bmOutput(char *line) {
    int j;
    osTakeSemaphore(&debugSema);

    for (j = 0; j < (int)strlen(line); j++) {
        osPutSerial(&sioDebug, line[j]);
    }
   osDropSemaphore(&debugSema);
}
/**
 * This function will be called by the Master when
 * PVT data is available.
  */
void erProvidePvt(erPvtStruct pvt) {
    static long startTime = 0;
    long sysTime = (long)((osGetMsecTimer()+500)/1000);
```

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```
    char src[4];
    char rmc[80];
    char out[80];
    if (startTime == 0) startTime = sysTime;
    if (pvt.pvtFixSource == 0) strcpy(src,"EST");
    else strcpy(src,"FIX");

    sprintf(out,"%5u %10u %8u  %10d %10d %10d [%s]\r\n",
       sysTime-startTime,pvt.pvtGpsTime,pvt.pvtFixTime,
       pvt.pvtPosFilt[0],pvt.pvtPosFilt[1],pvt.pvtPosFilt[2],src);
    bmOutput(out);
}
```

Appendix A.3 NMEA Output

The data internally available in the receiver can also be put out in NMEA0183 format. Adding the following lines to erProvidePvt() in the sample code above will put out $GPRMC sentences in addition.

```
    // Format NMEA RMC sentence.
    erGetNmeaRmc(&pvt, rmc);
    bmOutput(rmc);
```

The generated string will look like this

```
$GPRMC,123519,A,4807.038,N,01131.000,E,022.4,084.4,230394,003.1,W*6A
```

Appendix A.4 Server Aiding

The bit mask flag inputType determines the type of input the master is sending to the core. If server aiding data is available, the bit mask flag has to be set accordingly and the aiding values can be put into the appropriate coreInputStruct. Here is an example how this could be done.

```
static coreInputStruct ci;    // Input data for the core.
static void bmFromServer() {
    coreInputStruct local;
    int retval;
    // Check server connection.
    if (saGetSocketStatus() == 0) {
        retval = saOpen();
        if (retval == FALSE) {
            printf("Cannot Open Socket: bmFromServer()\n");
            return;
        }
    }
    // Read data from the server.
    saRead(&local);
```

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```
// Set relevant bit mask flag and put data into core
// input structure.
if (local.inputType & CI_OFFSET) {
    ci.inputType |= CI_OFFSET;
    ci.offset = local.offset;
}
if (local.inputType & CI_OMNIPOS) {
    ci.inputType |= CI_OMNIPOS;
    ci.omniPos = local.omniPos;
}
if (local.inputType & CI_OMNISSF) {
    ci.inputType |= CI_OMNISSF;
    ci.omniSsf = local.omniSsf;
}
if (local.inputType & CI_OMNIEPH) {
    ci.inputType |= CI_OMNIEPH;
    ci.omniEph = local.omniEph;
}
if (local.inputType & CI_OMNIALMPAGE) {
    ci.inputType |= CI_OMNIALMPAGE;
    ci.almPage = local.almPage;
}
if (local.inputType & CI_OMNIMODELS) {
    ci.inputType |= CI_OMNIMODELS;
    ci.omniModels = local.omniModels;
}
// Notify core that data is available.
if (ci.inputType) ccSetData(&ci);
}
```

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