Enpirion® Power Datasheet

EPT4000QI 40A Power Stage High Speed MOSFET with Integrated Current and Temperature Sense

Description

The EPT4000QI is a 40A, high speed, high density, monolithic power stage IC with integrated sensing features in a 5.5mm x 7.5mm x 0.95mm, 46 pin QFN package. It is targeted for low duty cycle operation, supplying low voltages for processor, DDR memory, and GPU core applications. The EPT4000QI offers very high efficiency at operating frequencies of 1MHz or greater. The EPT4000QI enables 35% higher power density by utilizing 50-75% less inductance and significantly less output capacitance than current generation multi-phase power supply solutions. It integrates a current sense and temperature measurement function.

The device has a pin-selectable diode emulation mode to improve efficiency under PS2 and PS3 low power modes.

The EPT4000QI is designed to interface with multi-phase PWM controllers and enables high efficiency delivery of up to 240 Amps for next generation CPU, DDR memory, and GPU core memory applications.

All Altera Enpirion products are RoHS compliant, halogen free and are compatible with lead-free manufacturing environments.

Features

- 40A continuous Operating Current
- 95.1% Peak Efficiency at 600KHz (1.8V at 10A)
- 3MHz Maximum Operating Frequency
- 1.8°C/W Junction-to-Case Thermal Resistance
- 35% Higher Power Density
- No POSCAP or Electrolytic Capacitors Needed
- Thermally Enhanced Low Inductance Package
- Integrated Gate Drive Independent of Drive Voltage
- Integrated Inductorless Current Sense
- Integrated Die Temperature Sense
- Tri-state Control Option
- Diode Emulation Mode for Light Load Efficiency
- Top-side Cooling for Heat-sink Attachment
- RoHS Compliant, MSL Level 3, 260°C Reflow

Applications

- High Density Power Stage in Conjunction with Multi-phase Controllers
- CPU Core, Non-core, Peripheral and DDR Memory Core Power Supplies
- GPU Core Regulation
- Servers, Desktops, Telecommunications, Equipment, Industrial and Embedded computing

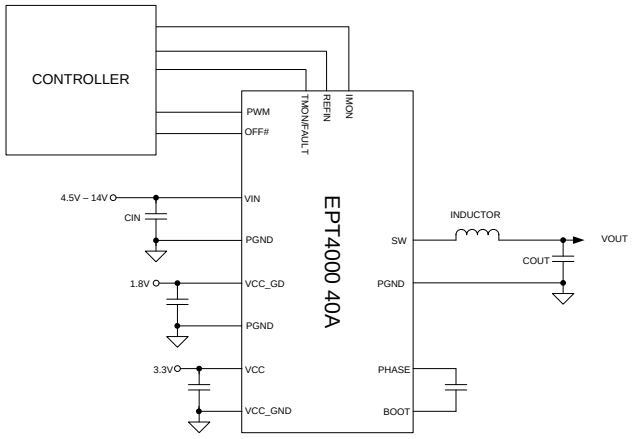

Figure 1. Simplified Applications Circuit

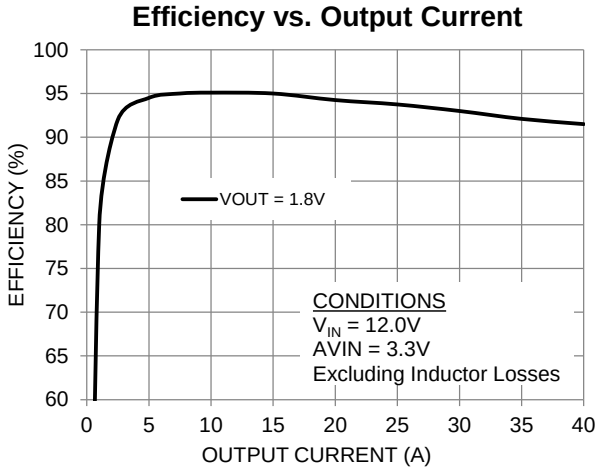

Figure 2. Highest Efficiency in Smallest Solution Size.

Ordering Information

Part Number	Package Markings	$T_{AMBIENT}$ Rating (°C)	Package Description
EPT4000QI	EPT4000QI	-40 to +85	46-pin (5.5mm x 7.5mm x 0.95mm) QFN T&R
EPT4000QI-E	Evaluation Board		

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

Pin Assignments (Top View)

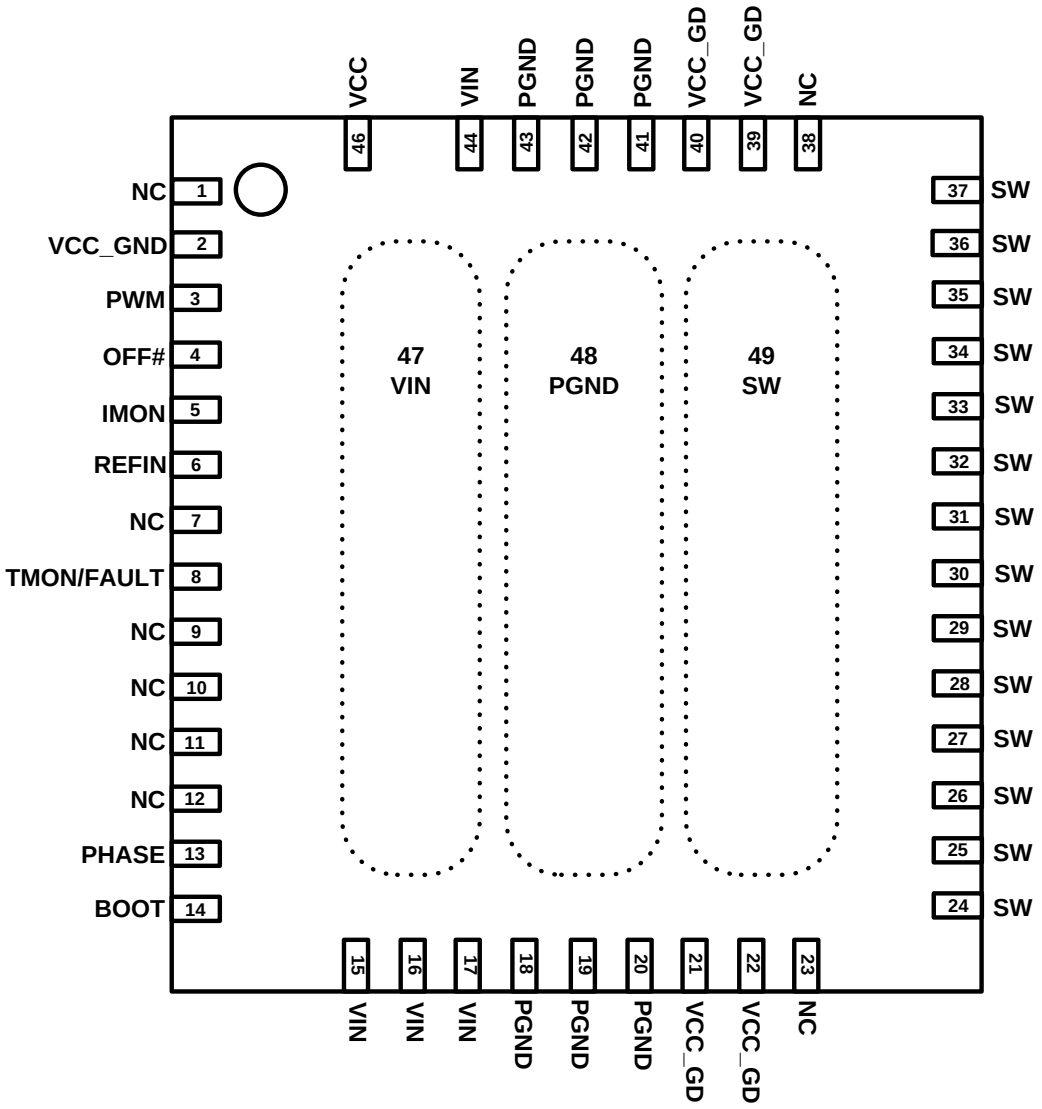

Figure 3: Pin Out Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. All pins including NC pins must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: The dotted outlines in the center of the package represent the exposed pads on the bottom of the package for VIN, PGND, and SW which are required to be soldered to the PCB.

NOTE C: White 'dot' on top left is pin 1 indicator on top of the device package.

Pin Description

I/O Legend: P=Power G=Ground NC=No Connect I=Input O=Output I/O=Input/Output

PIN	NAME	I/O	FUNCTION
			POWER PINS
2	VCC_GND	G	Ground for Analog Control Circuits. This is the ground return for the controller. The VCC_GND pin needs to be connected to a quiet ground.
15-17, 44	VIN	I	Power input supply for drivers.
18-20, 41-43	PGND	G	Input/output power ground. Connect these pins to the ground electrode of the input and output filter capacitors. See VOUT and PVIN pin descriptions for more details.
21, 22, 39, 40	VCC_GD	I	1.8V supply for gate drivers.
46	VCC	I	3.3V supply for analog control circuits.
47	VIN	I	Not a perimeter pin. This VIN is exposed on the package underside. Tie to VIN plane on EVB with buried vias. High-quality connection to VIN plane critical for thermal and electrical performance.
48	PGND	G	Not a perimeter pin. Input/output power ground. This PGND is exposed on package underside. Tie to PGND plane on EVB with buried VIAs. High-quality connection to PGND plane critical for thermal and electrical performance.
49	SW	O	Not a perimeter pin. Driver drain/switch node. This SW is exposed on package underside. Tie to SW node/plane on EVB with wide copper on top layer. High-quality connection to inductor is critical.
			SIGNAL AND CONTROL PINS
3	PWM	I	PWM control signal. Logic LOW = Low-side FET enabled. Logic HIGH = high-side FET enabled. FLOAT = Tri-state, both LS and HS FETs disabled. See PWM Pin Characteristics table for additional details.
4	OFF#	I	Low-side OFF signal. Logic LOW = low-side FET disabled. Logic HIGH = normal PWM operation, LS FET enabled. OFF# is used to turn off the low-side driver during PS2 and PS3 low-power modes, where diode emulation is used to improve efficiency.
5	IMON	O	Current Monitor Output. Provides a bandwidth limited (nominally 3.6 MHz) replica of the current waveform at the SW node. See Current Monitor Characteristics section for more details. Use 5 kΩ low TC resistor between IMON and REFIN.
6	REFIN		Reference level shift voltage for the IMON pin. Provided by the controller. See Current Monitor Characteristics section for more details.
8	TMON/FAULT	O	Temperature monitor output and FAULT indication pin. See Electrical Characteristics table and Functionality and Features section for description.
13	PHASE		Bottom plate of High-Side FET boot capacitor. Use X5R ceramic on top-side of PCB only and critically located very close to device pins (PHASE and BOOT).
14	BOOT		Top plate of High-Side FET boot capacitor. Use X5R ceramic on top-side of PCB only and critically located very close to device pins (PHASE and BOOT).
1,7,9-12,23,38	NC	NC	NO CONNECT – These pins may be internally connected. Do not connect them to each other or to any other electrical signal. Failure to follow this guidance may result in device damage.
24-37	SW		Driver drain/switch node pins. Connect an external inductor from SW to the output.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Voltages on Power MOSFET Input Supply VIN	VIN	-0.3	16	V
VIN Slew Rate	VIN_{SLEW}	0.3	6	V/ms
Voltages on gate drive input supply VCC_GD	VCC_GD	-0.3	2.1	V
Voltages on logic input supply VCC	VCC	-0.3	5.5	V
Voltages on control pin OFF#,	OFF#	-0.3	5.5	V
Voltages on IMON, TMON/FAULT		-0.3	5.5	V
Voltages on BOOT	BOOT	-0.3	16	V
Voltages on PHASE	PHASE	-0.3	2.1	
Voltages on REFIN	REFIN	-0.3	5.5	V
Voltages on PWM input signal	PWM	-0.3	5.5	V
Voltages on PGND	PGND	-0.3	0.3	V
Voltages on logic ground VCC_GND	VCC_GND	-0.3	0.3	V
Voltages on switch (common drain) node	SW	-2.0	VIN+0.3	V
Storage Temperature Range	T_{STG}	-65	150	°C
Maximum Operating Junction temperature	$T_{J\text{-}ABS\ Max}$		150	°C
Reflow Temperature, 10 sec, MSL3 JEDEC J-STD-020A			260	°C
ESD Rating (based on Human Body Model)		2000		V
ESD Rating (based on CDM)		500		V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage to Power MOSFETs	VIN	4.5	12	14.5	V
Supply voltage to the MOSFETs gate driver	VCC_GD	1.6	1.8	2.0	V
Supply voltage to logic circuits	VCC	3.0	3.3	3.6	V
Operating junction temperature		0		+125	^{o}C
Continuous load current	I_{LOAD}			40	A
Operating ambient temperature		0		+85	^{o}C

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Resistance: Junction to Top-side (0 LFM)	θ_{JT}	1.8	°C/W
Thermal Resistance: Junction to Bottom-side (0 LFM)	θ_{JB}	2.0	°C/W

Electrical Characteristics

NOTE: **Boldface** limits apply over the specified range, TA = 0C to 85C.
Typical Operating Conditions unless otherwise noted : TA=25C, VIN=12V, VCC=3.3V, VCC_GD=1.8V.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DEVICE LEVEL CHARACTERISTICS						
Operating VIN Voltage Range	V_{VIN}		4.5		14.5	V
Operating VCC Voltage Range	V_{PVCC}		3.0	3.3	3.6	V
Operating VCC_GD Voltage Range	V_{PVCC_GD}		1.5	1.8	2.2	V
VCC Quiescent Current	I_{QVCC}	PWM = Low	1.4	1.8	2.3	µA
VIN Quiescent Current – No Switching	I_{QVIN_NS}	PWM = Low	2.5	3.3	4.2	mA
VIN Quiescent Current – Switching	I_{QVIN}	Freq(PWM) = 600 kHz, Duty Cycle = 20%	45	60	75	mA
VCC_GD Quiescent Current – No switching	$I_{QVCC\_GD\_NS}$	PWM = Low, VCC_GD = 1.8V	340	450		µA
VCC_GD Quiescent Current – Switching	I_{QVCC_GD}	Freq(PWM) = 600 kHz VCC_GD = 1.8V	22	30	50	mA
Low-Side Rds_on				1.4	1.6	mΩ
High-Side Rds_on				6.6	8	mΩ
CURRENT MONITORING (IMON) CHARACTERISTICS						
Trans-impedance Gain				5.5		mV/A
IMON Output Resistor	R_IMON	External Resistor between IMON and REFIN pins. 0.1% tolerance recommended.	4.995	5	5.005	kΩ
IMON Output Resistor – Temperature Coefficient	TC_RIMON	Use 0TC Resistor		0		mΩ/°C
IMON External Parasitic or LOAD Capacitance	C_IMON	External parasitic capacitance reduces IMON replica bandwidth			5	pF
IMON – Trans-impedance Bandwidth		ILOAD = 0A, C_IMON=2pF	2	3.6		MHz
IMON – Zero-current DC Output Voltage		ILOAD = 0A, REFIN=1.5V Referenced to AGND		1.5		V
IMON – Maximum Output Voltage			2.5			V
IMON – Output Current (into REFIN)		REFIN = 1.5V REFIN must be capable of sinking or sourcing this current.	-200	0	200	µA
REFIN Allowable Voltage Range		Referenced to VCC_GND	0.8		2.1	V
IMON – REFIN (Differential Voltage)		ILOAD = 100A		0.5		V
IMON – REFIN (Differential Voltage)		ILOAD = -50A		-0.25		V
IMON – REFIN		ILOAD = 40A		0.2		V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
(Differential Voltage)						
OVER-CURRENT DETECTION (OCD) CHARACTERISTICS						
Over-Current Detection Threshold – DC Current Threshold	I_OCD	L=150nH, Fsw=600 kHz, DC Output Current		60		A
OCD Counter – Trip Detection	OCD_CNT	Non-consecutive over-current trips before detection occurs		16		Counts
OCD Counter Reset		Consecutive switching cycles without OCD condition – resets OCD counter to 0x0		4		Counts
OCD Timeout	OCD_TO	Continuous over-current condition>=I_OCD and persisting longer than OCD_TO forces OCD FAULT, independent of OCD_CNT	7.5	15	30	µs
SHORT-CIRCUIT DETECTION CHARACTERISTICS						
SC Detection Threshold – DC Current Threshold	I_SC	L=150nH, Fsw=600 kHz, DC Output Current		+/-80		A
SC Detection Timer	t_SC	SC Fault must persist longer than t_SC to trigger FAULT assertion	60	120	240	ns
THERMAL MONITORING (TMON) AND FAULT INDICATION						
Thermal Gain			7.8	8	8.2	mV/C
0C Output Voltage		Temp = 0C	0.582	0.6	0.618	V
150C Output Voltage		Temp = 150C	1.746	1.8	1.854	V
VCC Reset Threshold		FAULT triggered VCC Reset occurs below this supply threshold			0.3	V
Logic High		FAULT indication condition	2.4			V
Input Capacitance					10	pF
Output Resistance, Sourcing					100	Ω
Source Current			1			mA
Sink Current			100			µA
Maximum Number of ORed Phases					7	Phases
Maximum Load Capacitance					1000	pF
PWM PIN CHARACTERISTICS						
Equivalent Input Resistance				6		kΩ
Input Capacitance					10	pF
Input Current		VPWM = VCC = 3.3V		250	330	µA
Logic Low Level		VCC = 3.3V, Relative to VCC_GND	-0.3		+0.8	V
Logic High Level		VCC = 3.3V	2.4V		3.6	V
Logic Low Hysteresis		VCC = 3.3V		110		mV
Logic High Hysteresis		VCC = 3.3V		180		mV
Tri-State Thresholds		VCC = 3.3V	1.2		2	V
Floating Tri-State Voltage		PWM floated/driven with high impedance (>10 MΩ)		VCC/2		V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Rise Time					5	ns
Input Fall Time					5	ns
Turn-off Propagation Delay		Delay from PWM input HIGH to LOW to beginning of SW transition		24		ns
Turn-on Propagation Delay		Delay from PWM input LOW to HIGH to beginning of SW transition		22		ns
Tri-state Hold-Off Time		Delay from Tri-State active level transition on PWM to beginning of transition to tri-state on SW		50		ns
Tri-state to Active High - SW Rising Propagation Delay		Delay - PWM transitions to high state from tri-state mode to start of high-side assertion		22		ns
Tri-state to Active Low – SW Assertion Low Propagation Delay		Delay - PWM transitions to low state from tri-state mode to start of low-side assertion		22		ns
OFF# PIN CHARACTERISTICS						
Logic Low		Relative to VCC_GND	-0.3		0.8	V
Logic High		VCC=3.3V	2.3		VCC + 0.3	V
Hysteresis				800		mV
Input Resistance		(pull-up to VCC)	150	300	450	kΩ
Input Capacitance					10	pF
Input Rise Time					5	ns
Input Fall Time					5	ns
Delay – Logic LOW to NFET OFF				30		ns
Delay – Logic HIGH to NFET ON		PWM=0		30		ns
VCC_GD UVLO CHARACTERISTICS						
Operating VCC_GD Voltage Range	V_{PVCC_GD}		1.6		2.0	V
UVLO Falling Threshold	UVLO_FALL		0.9			V
UVLO Rising Threshold	UVLO_RISE				1.55	V
UVLO Hysteresis				150		mV

Typical Performance Charts

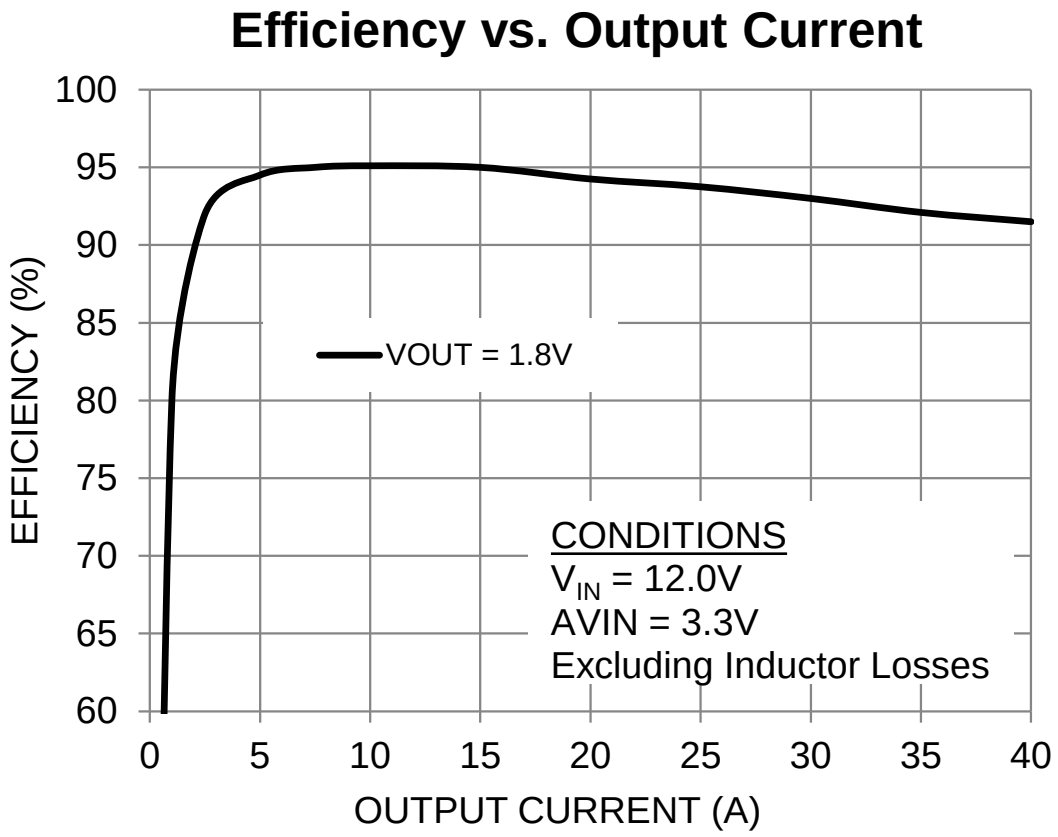

Figure 4: Measured Efficiency (%) vs Load Current (A)

Typical Performance Charts (Continued)

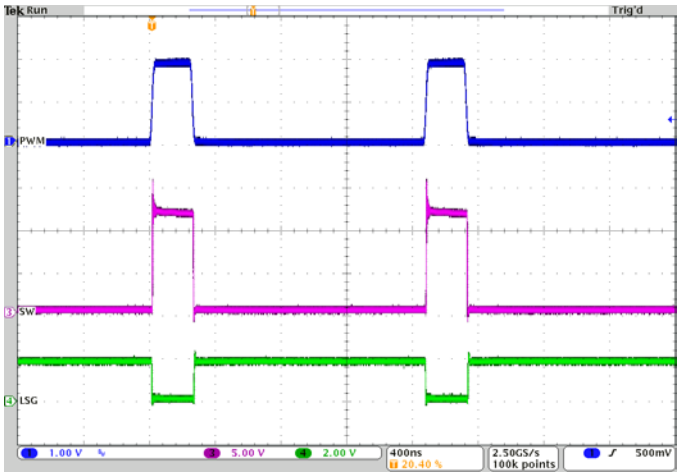

Figure 5: Switching waveform. PWM (top), Switch (middle), and low side gate (bottom) waveforms: VIN=12V, VOUT=1.8V, Fswitch=600KHz, load=0A.

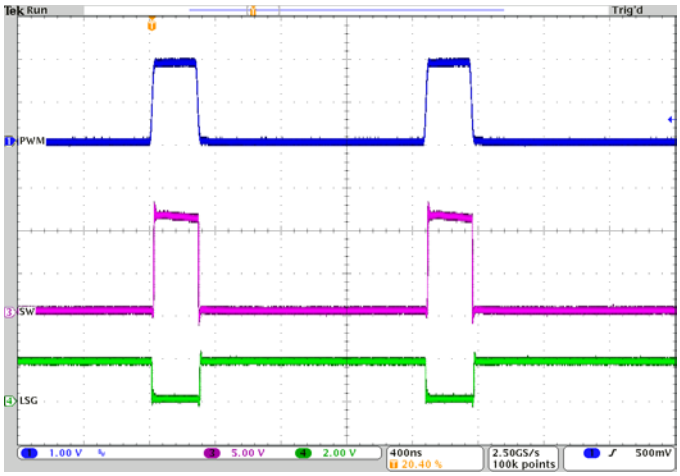

Figure 6: Switching waveform. PWM (top), Switch (middle), and low side gate (bottom) waveforms; VIN=12V, VOUT=1.8V, Fswitch = 600KHz, load = 40A.

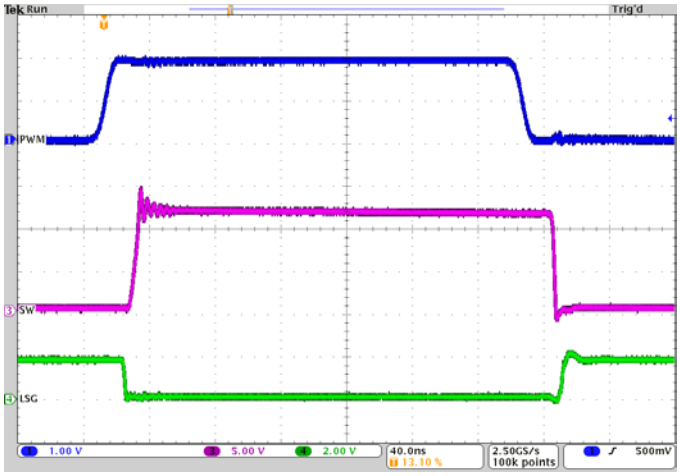

Figure 7: Switching waveform close up. PWM (top), Switch (middle), and low side gate (bottom) waveforms; VIN=12V, VOUT=1.8V, Fswitch = 600KHz, load = 10A.

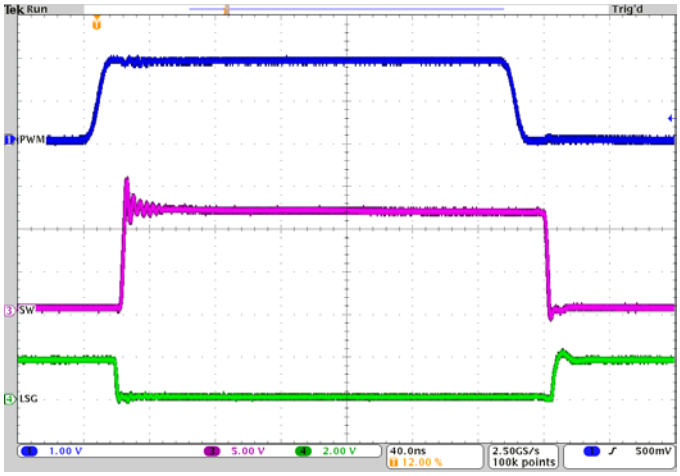

Figure 8: Switching waveform close up. PWM (top), Switch (middle), and low side gate (bottom) waveforms; VIN=12V, VOUT=1.8V, Fswitch = 600KHz, load = 0A.

Functional Block Diagram

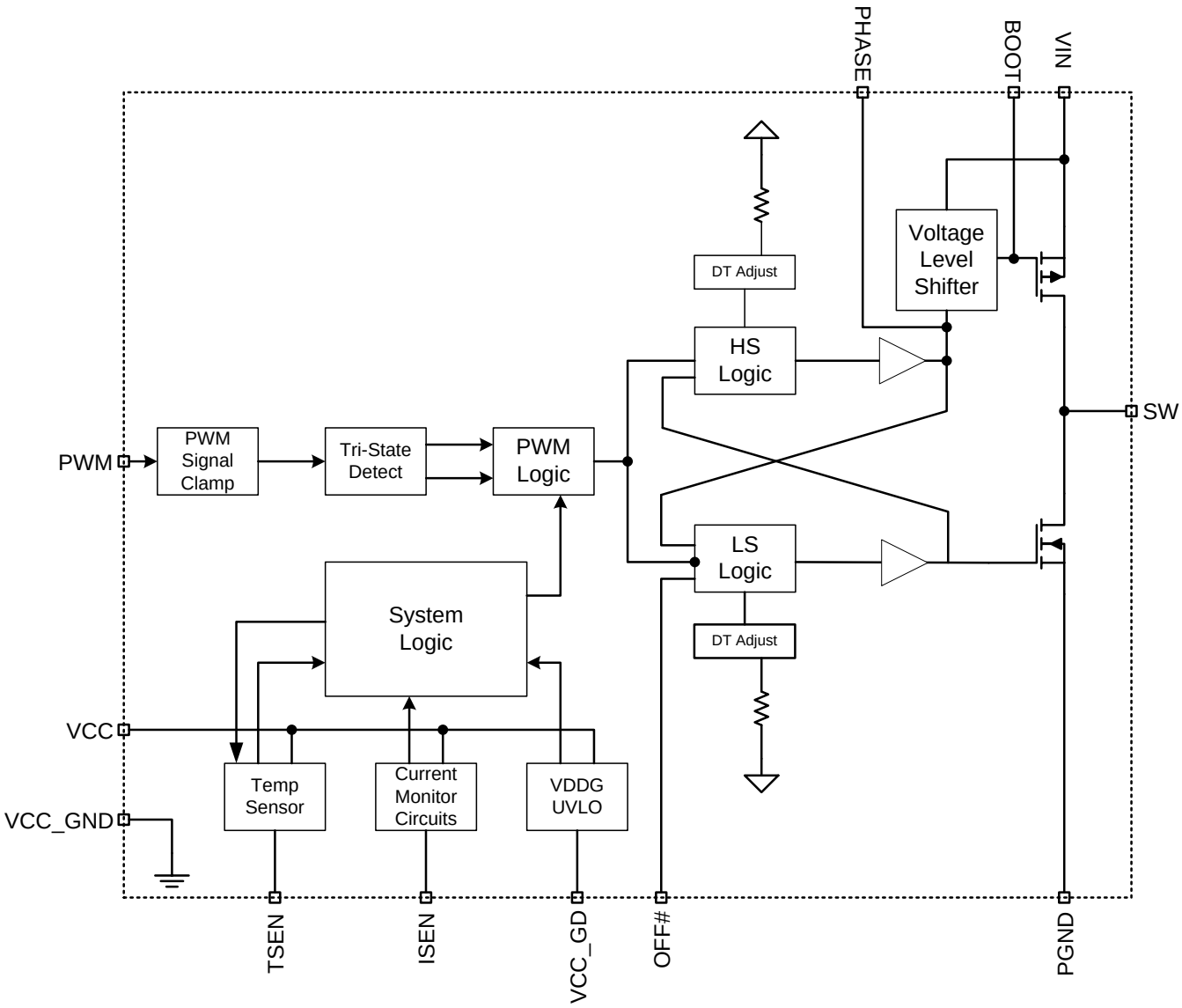

Figure 9: Functional Block Diagram

Theory of Operation

Introduction

The EPT4000QI is a monolithic 40A driver stage that integrates P-Channel high side power MOSFET, N-Channel low side power MOSFET and an optimized high speed gate driver. The device also includes die temperature monitoring, current sensing, and high side MOSFET short circuit detection circuitry. The EPT4000QI also has a pin-selectable diode emulation mode for improved efficiency under light load conditions.

The EPT4000QI utilizes Enpirion's advanced high frequency LDMOS process to enable high switching frequency and high efficiency. The EPT4000QI has industry leading figure of merit (FOM) providing for very low switching loss

hence enabling high switching frequency for small external inductor and capacitors.

Configured properly, the EPT4000QI does not require any bulk electrolytic or POSCAPs. Only low cost Ceramic MLCC capacitors are required.

PWM Input

Pulse Width Modulator (PWM) pin is a Tri-state input signal. Floating or "tri-stating" this pin will turn off both high side and low side MOSFETs. PWM pin levels conform to HP-MOS specifications.

When PWM is placed in tri-state mode, the PWM signal is internally pulled to 1.6V. This simplifies the tri-state operation and prevents indeterminate states from occurring.

Table 1. PWM Logic state table.

PWM	High Side MOSFET	Low Side MOSFET
Low	OFF	ON
High	ON	OFF
Float	OFF	OFF

Shoot Through Protection

The EPT4000QIQI employs an advanced shoot through protection scheme. Feedback is used from each gate to ensure that both MOSFETs are never on simultaneously.

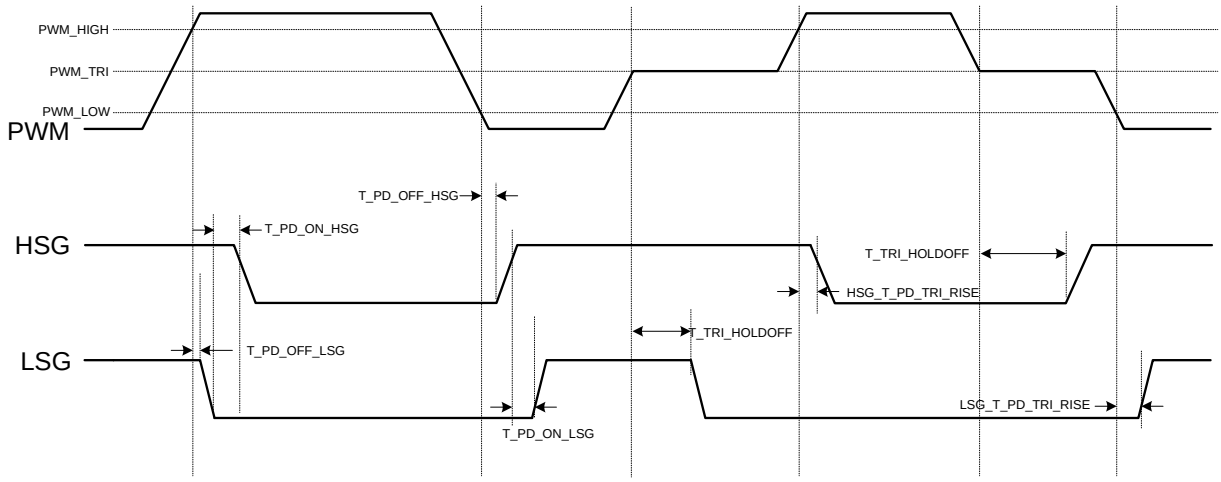

Figure 10. PWM, LSG and HSG timing. Note: HSG is active low, LSG is active high.

IMON Current Sense Output

The current monitoring function provides a voltage based replica of the dynamic inductor current waveform, including both static output current and dynamic ripple current contributions. The nominal replication bandwidth is 3.6 MHz – given the nominal output resistance of 5kΩ, parasitic loading on this pin should be minimized. The voltage on IMON is the sum of the current monitoring output voltage and the REFIN pin, allowing IMON to be summed with REFIN. The IMON control and sensing circuits are internally temperature compensated, allowing the IMON indication to correctly track output current even as internal junction temperature changes due to self-heating and due to changes in ambient temperature.

TMON/FAULT Temperature Monitor and Fault Detection

The EPT4000QI provides a thermal monitor that indicates the internal junction temperature of the device with a conversion factor of ~8 mV/°C – this indication occurs on the TMON/FAULT pin. Additional specifications relative to TMON are provided in the corresponding Electrical Characteristics section. The TMON pin of multiple

devices/phases can be wired-ORed together, allowing the hottest phase with the highest temperature to control the temperature indication. The maximum number of phases that can be ORed together is seven.

If the junction temperature of the EPT4000 exceeds recommended limits by a sufficient margin, an Over-Temperature Detection (OTD) indication will occur. The over-temperature detection threshold is nominally 150°C, or 25°C above the maximum allowed operating junction temperature of 125°C. The detection comparator includes 25°C of hysteresis to prevent thermal shutdown oscillation around the 150°C trip point. When an OTD even occurs, the OTD monitor will immediately trigger FAULT and disable the output drivers.

The secondary purpose of the TMON/FAULT pin is to indicate a fault condition to the VRM controller. The FAULT conditions include:

1) Over-current detection (OCD)
2) Over-temperature detection (OTD)
3) Short-circuit detection (SCD)

The FAULT condition is latched by the internal FAULT latch and can only be reset by toggling the VCC pin below 0.3V. When VCC is toggled low, the supply sequencing requirements in the next section should be followed. VDDQ and VIN should be removed at the same time as VCC, or prior to VCC toggle.

Over-Current Detection (OCD):

Over-current conditions are monitored internally, using monitor circuits that observe and act on the voltage based current replica at IMON. Current is monitored in a bipolar fashion, allowing both sink and source currents beyond the trip threshold to be detected and flagged. Nominal trip current is set at 1.5x rated current, or 60A for the EPT4000. Because the IMON output is wide bandwidth, the OCD trip current is internally compensated for an anticipated inductor ripple current of 10Apeak, allowing the OCD trip detection to occur at ~+/-60A output current. The OCD control circuit counts 16 OCD events (cycles above +/-60A) before triggering – the OCD events do not need to be consecutive. If, however, 4 consecutive switching cycles are completed without an OCD event, the OCD counter is reset to zero and the OCD detection sequence begins anew. The OCD control circuitry will also detect an extended high-side or low-side ON cycle that allows the total inductor current to exceed the OCD threshold. This OCD timeout period is nominally 15 µSec. When an OCD event is successfully detected, the OCD control circuitry immediately drives the TMON/FAULT pin high and sets the FAULT latch. The FAULT latch can only be reset by toggling the VCC supply below 0.3V. The EPT4000 will continue to respond to PWM commands during the OCD/FAULT indication.

Short Circuit Detection

High-side short-circuit detection is also monitored internally, and as per the OCD monitor, the SCD uses monitor circuits that observe and act on the voltage based current replica at IMON. Nominal trip current is set at 2x rated current, or 80A for the EPT4000. If the SCD monitor observes >=80A at the driver stage – a value well beyond expected during normal operation - it assumes a short is present. Because the IMON output is wide bandwidth, the SCD trip current is internally compensated for an anticipated inductor ripple current of 10Apeak, allowing the SCD trip detection to occur at ~+/-80A output current. The SCD control circuitry places a timeout limit of ~250 nSec on the short-circuit condition – i.e. the fault condition must last at least 150 nSec for a successful SCD indication to occur. The SCD timer ensures that the SCD circuit is not tripped by switching noise. If a short-circuit event is detected and validated, the SCD circuit will immediately pull TMON/FAULT high, notifying the VRM controller that a FAULT has occurred. During this fault, the EPT4000 will continue to respond to activity on the PWM pin. The SCD event is latched in the FAULT latch and can only be reset by dropping VCC below 0.3V.

Application Information

Power Up Sequencing

The preferred supply sequence for the EPT4000 during power up is as follows :

1) VCC (3.3V)
2) VCC_GD (1.8V)
3) VIN (12V)

VCC and VCC_GD can be applied simultaneously; however, both should precede the application of VIN. Recommended power-up supply slew rates are less than 5V/mSec. During power-down, the recommended sequence is the inverse of above:

1) VIN (12V)
2) VCC_GD (1.8V)
3) VCC (3.3V)

Under Voltage Lock Out

The gate driver supply rail, VCC_GD, is monitored to ensure a valid supply voltage is present that allows the gate driver control and driver circuitry to properly function. If the VCC_GD supply drops below UVLO_FALL or fails to rise above UVLO_RISE, the UVLO monitor counts 3 PWM pulses or a nominal maximum persistence of 15 uSec, at which point switching is disabled at the next immediate ON cycle. When the UVLO condition clears, the driver allows switching to continue. An UVLO event is NOT indicated fault and therefore does not toggle the TMON/FAULT pin or latch into the FAULT latch.

Diode Emulation Mode

The EPT4000QI diode emulation mode enables increased light load efficiency by preventing negative inductor current from flowing through the low-side (synchronous) MOSFET. Diode emulation mode is controlled with the active low OFF# signal. When the OFF# pin is asserted low, the low side MOSFET will be turned off. The high side MOSFET will be continue to follow the PWM signal commands.

Engineering Schematic

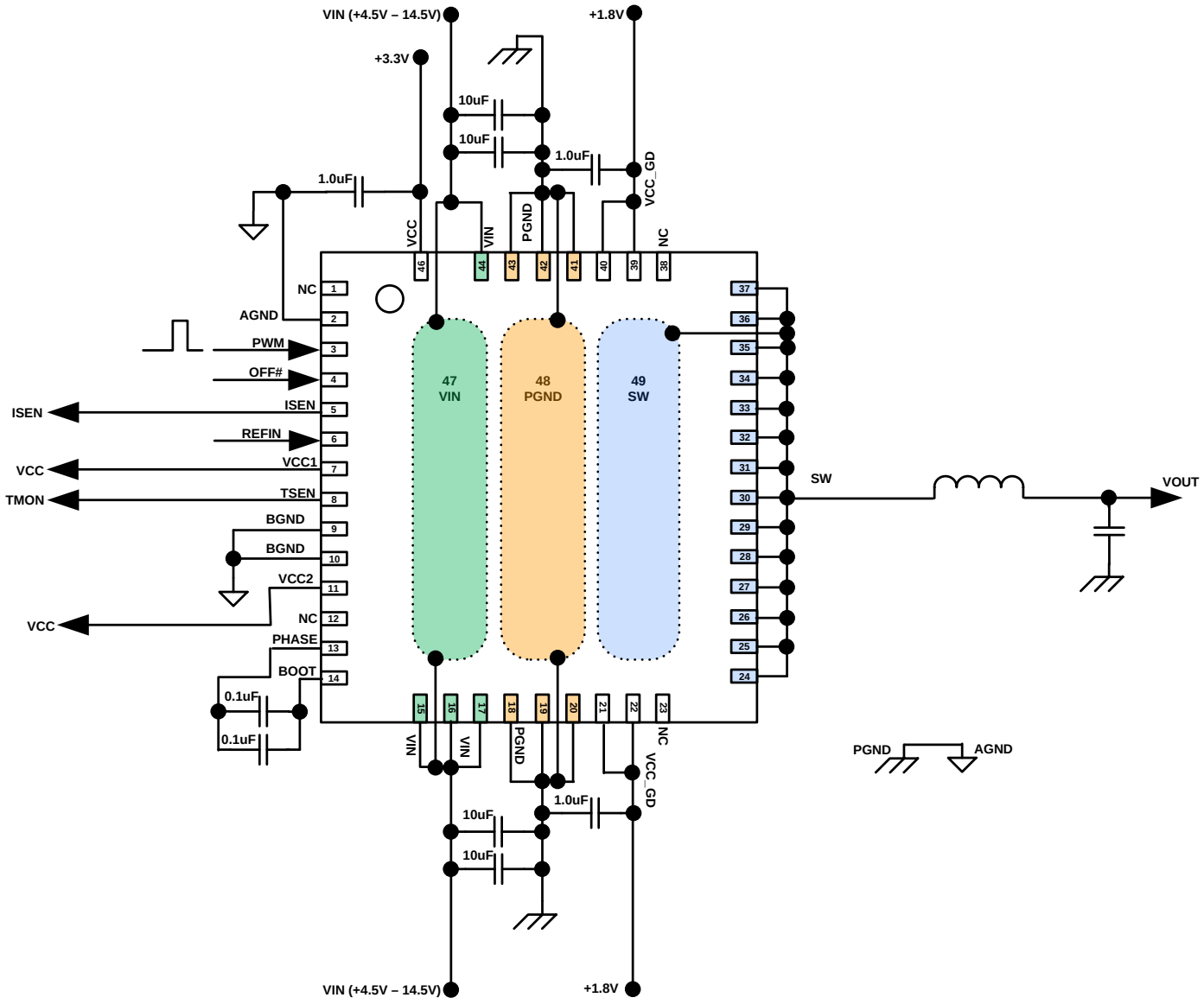

Figure12. Pin interconnection diagram.

Application Diagram

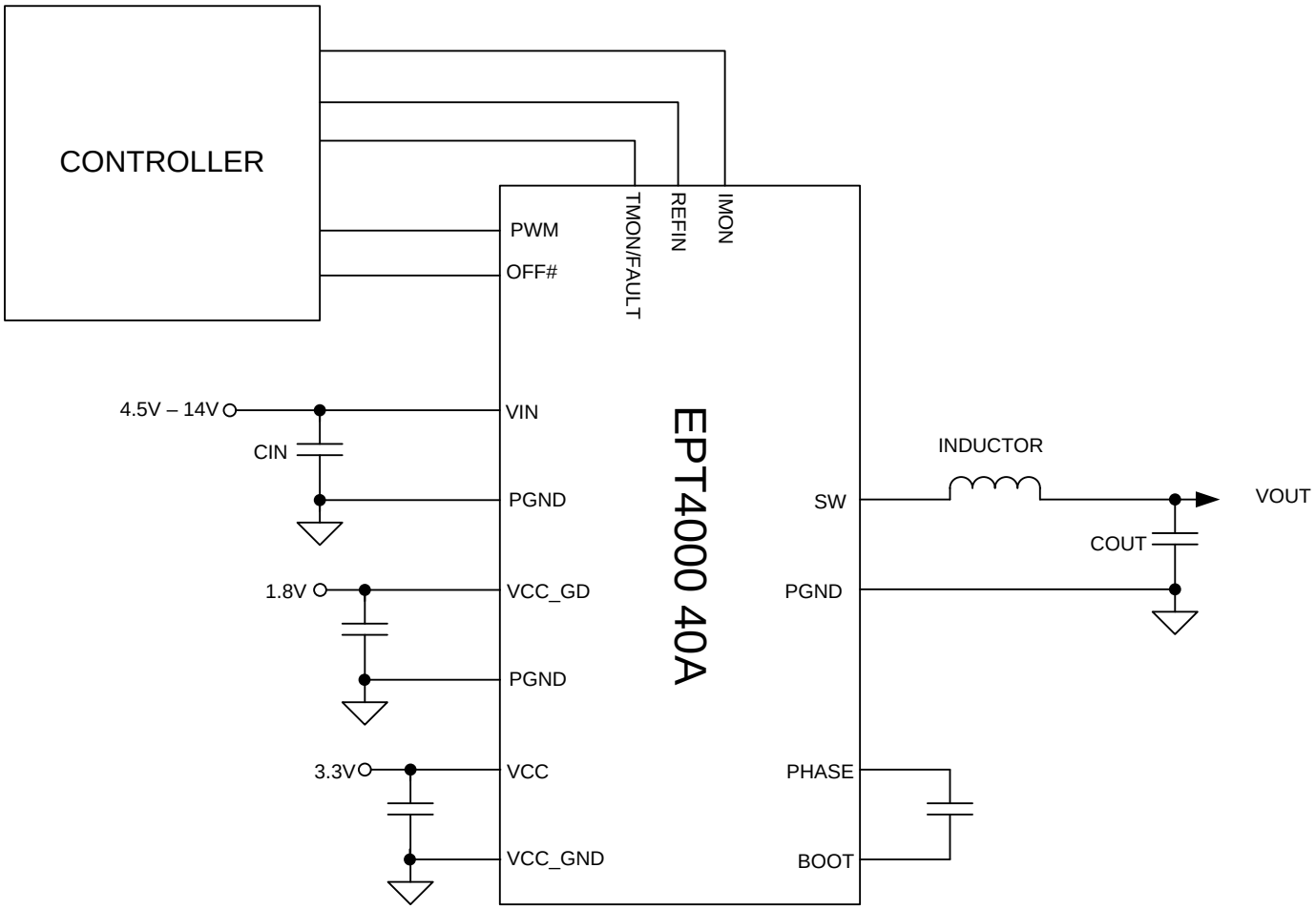

Figure 13: Typical Application Diagram for a single EPT4000QI implimentation.

Recommended PCB Footprint

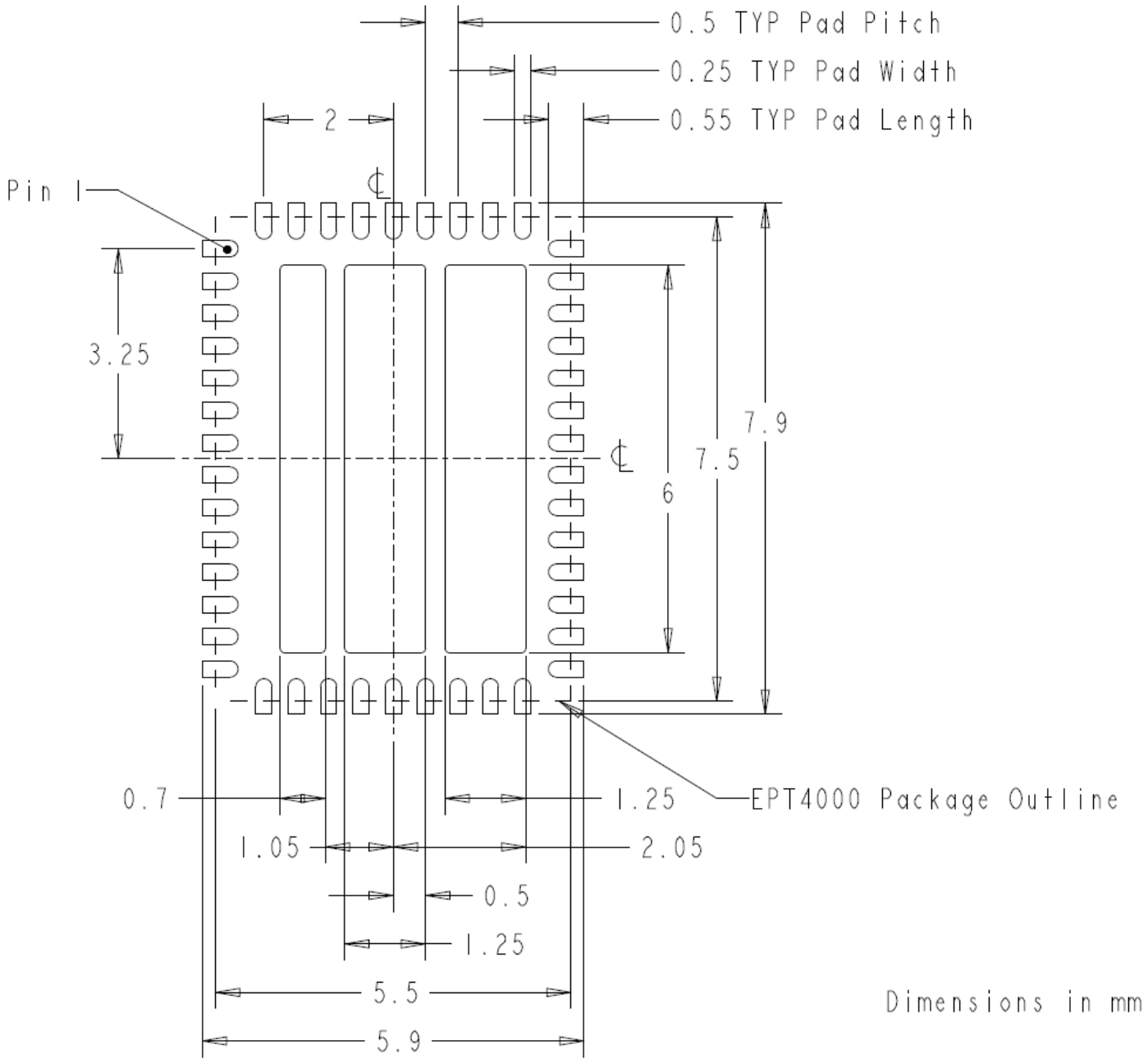

Figure 14: EPT4000QI Recommended PCB Footprint (Top View).

Recommended Solder Stencil Openings

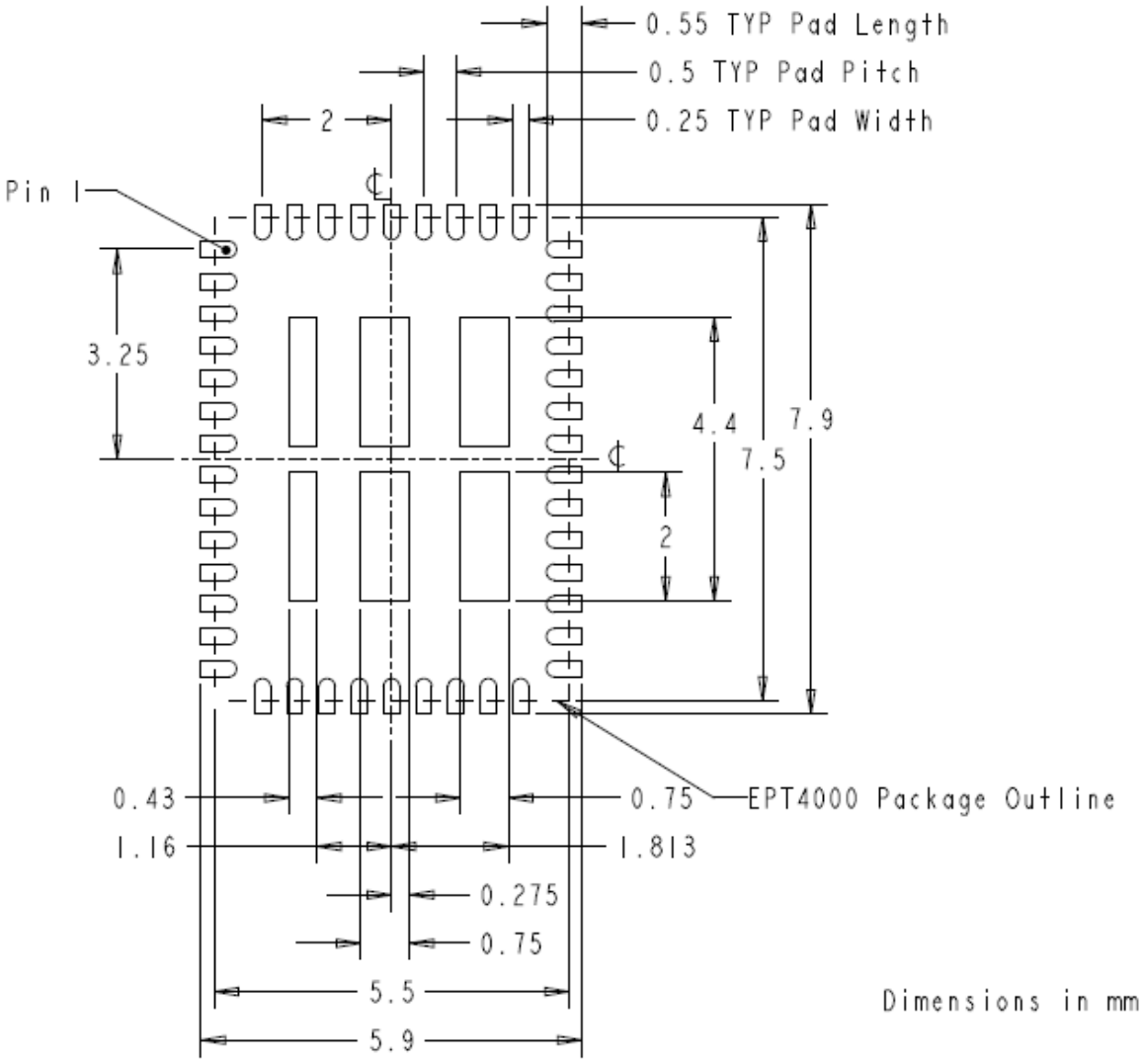

Figure 15: Recommended solder stencil openings.

Package and Mechanical

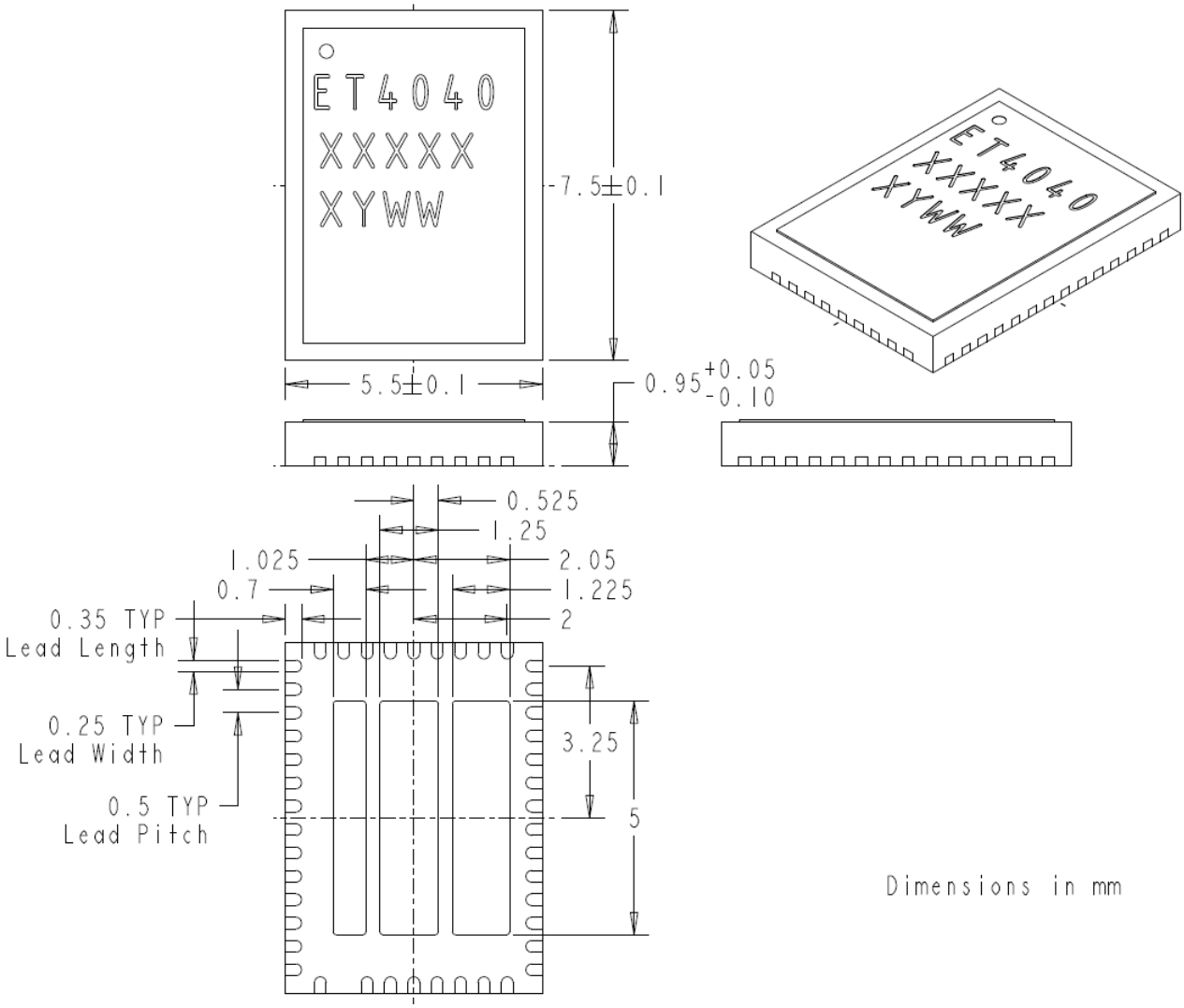

Figure 16: EPT4000QI Package Dimensions (Bottom View)

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

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