

Quad Two-Input AND Gate

Product Specification

Military Logic Products

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54F08/BCA
14-Pin Ceramic Flat Pack	54F08/BDA
20-Pin Ceramic LLCC	54F08/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

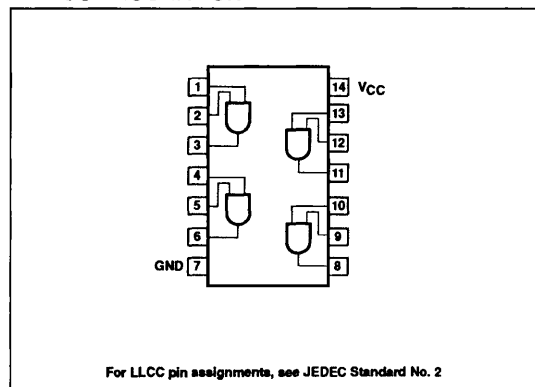
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/1.0	20 μ A/0.6mA
Y	Outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20 μ A in the High state and 0.6mA in the Low state.

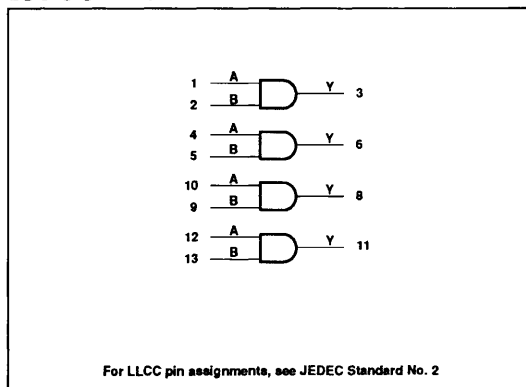
ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage range	-0.5 to +7.0	V
V _I	Input voltage range	-0.5 to +7.0	V
I _I	Input current range	-30 to +5	mA
V _O	Voltage applied to output in High output state range	-0.5 to +V _{CC}	V
I _O	Current applied to output in Low output state	40	mA
T _{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



LOGIC SYMBOL



Gate

54F08

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current			-1	mA
I _{OL}	Low-level output current			20	mA
T _A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT	
			Min	Typ ²	Max		
V _{OH}	High-level output voltage	V _{CC} = Min, V _{IL} = Max, I _{OH} = Max, V _{IH} = Min	2.5			V	
V _{OL}	Low-level output voltage	V _{CC} = Min, V _{IL} = Max, I _{OL} = Max, V _{IH} = Min		0.35	0.50	V	
V _{IK}	Input clamp voltage	V _{CC} = Min, I _I = I _{IK}		-0.73	-1.2	V	
I _{IH2}	Input current at maximum input voltage	V _{CC} = Max, V _I = 7.0V		5	100	μA	
I _{IH1}	High-level input current	V _{CC} = Max, V _I = 2.7V		1	20	μA	
I _{IL}	Low-level input current	V _{CC} = Max, V _I = 0.5V		-0.4	-0.6	mA	
I _{OS}	Short-circuit output current ³	V _{CC} = Max, V _O = 0.0V	-60	-90	-150	mA	
I _{CC}	Supply current (total)	I _{CCCH}	V _{CC} = Max	V _I ≥ 4.0V	5.5	8.3	mA
		I _{CCCL}		V _I = GND	8.6	12.9	mA

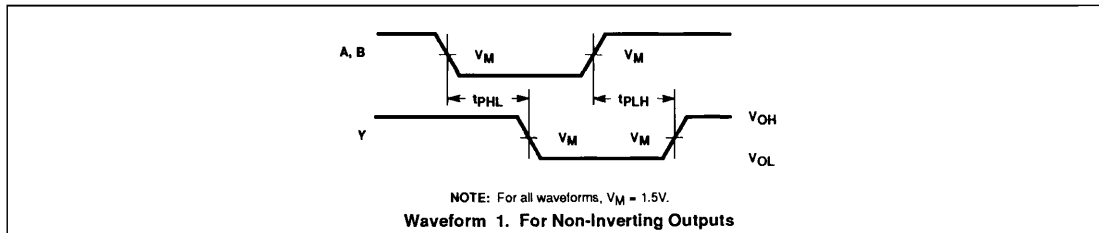
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _A = +25°C, V _{CC} = +5.0V			T _A = -55°C to +125°C		
			Min	Type	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay A, B to Y	Waveform 1	C _L = 50pF R _L = 500Ω			V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		ns
			3.0	4.2	5.6	2.5	7.5	
			2.5	4.0	5.3	2.0	7.5	ns

NOTES:

- For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

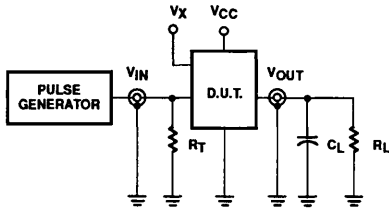
AC WAVEFORM



Gate

54F08

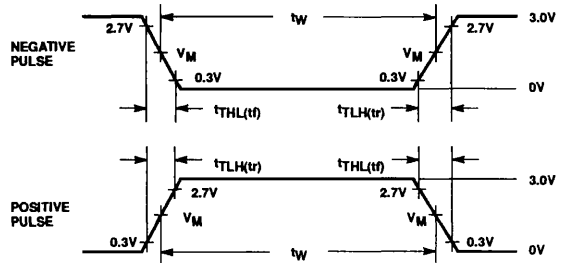
TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs

DEFINITIONS:

- R_L = Load Resistor; see AC Characteristics for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
- V_X = Unclocked pins must be held at: $\leq 0.8V$, $\geq 2.7V$ or open per Function Table.



$V_M = 1.5V$

Input Pulse Definition

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	$\leq 2.5ns$	$\leq 2.5ns$