

Designer's Data Sheet
Power Field Effect Transistor
N-Channel Enhancement-Mode
Silicon Gate TMOS

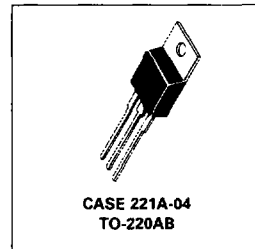
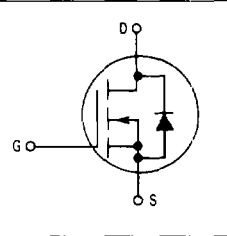
This TMOS Power FET is designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MTP2N25

TMOS POWER FET
2 AMPERES
 $r_{DS(on)} = 2.8 \text{ OHMS}$
250 VOLTS



MAXIMUM RATINGS

Rating	Symbol	MTP2N25	Unit
Drain-Source Voltage	V_{DSS}	250	Vdc
Drain-Gate Voltage ($R_{GS} = 1 \text{ M}\Omega$)	V_{DGR}	250	Vdc
Gate-Source Voltage — Continuous	V_{GS}	± 20	Vdc
— Non-repetitive ($t_p \leq 50 \mu\text{s}$)	V_{GSM}	± 40	Vpk
Drain Current — Continuous	I_D	2	Adc
— Pulsed	I_{DM}	10	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	50	Watts
Derate above 25°C		0.4	W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	2.5	°C/W
— Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1:8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MTP2N25

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 0.25 mA)	V _{(BR)DSS}	250	—	V _{dc}
Zero Gate Voltage Drain Current (V _{DS} = Rated V _{DSS} , V _{GS} = 0) (V _{DS} = 0.8 Rated V _{DSS} , V _{GS} = 0, T _J = 125°C)	I _{DSS}	—	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V _{GSF} = 20 V _{dc} , V _{DS} = 0)	I _{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V _{GSR} = 20 V _{dc} , V _{DS} = 0)	I _{GSSR}	—	100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C	V _{GS(th)}	2 1.5	4.5 4	V _{dc}
Static Drain-Source On-Resistance (V _{GS} = 10 V _{dc} , I _D = 1 Adc)	r _{DS(on)}	—	2.8	Ohms
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 2 Adc) (I _D = 1 Adc, T _J = 100°C)	V _{DS(on)}	—	5.6 4	V _{dc}
Forward Transconductance (V _{DS} = 15 V, I _D = 1 A)	g _{FS}	0.8	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz) See Figure 10	C _{iss}	—	400	pF
Output Capacitance		C _{oss}	—	150	
Reverse Transfer Capacitance		C _{rss}	—	65	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Turn-On Delay Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D R _{gen} = 50 ohms) See Figures 12 and 13	t _{d(on)}	—	25	ns
Rise Time		t _r	—	20	
Turn-Off Delay Time		t _{d(off)}	—	35	
Fall Time		t _f	—	30	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V) See Figure 11	Q _g	6.5 (Typ)	9	nC
Gate-Source Charge		Q _{gs}	3.5 (Typ)	—	
Gate-Drain Charge		Q _{gd}	3 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	I _S = Rated I _D V _{GS} = 0)	V _{SD}	2 (Typ)	—	V _{dc}
Forward Turn-On Time		t _{on}	Limited by stray inductance		
Reverse Recovery Time		t _{rr}	190 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L _d	3.5 (Typ) 4.5 (Typ)	—	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L _s	7.5 (Typ)	—	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.



TYPICAL ELECTRICAL CHARACTERISTICS

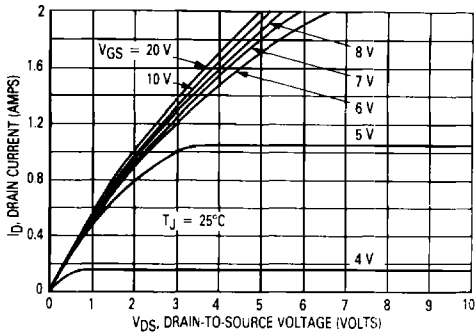


Figure 1. On-Region Characteristics

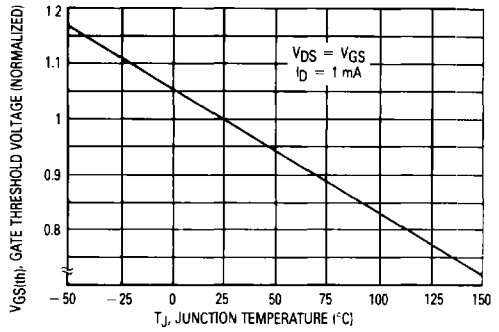


Figure 2. Gate-Threshold Voltage Variation With Temperature

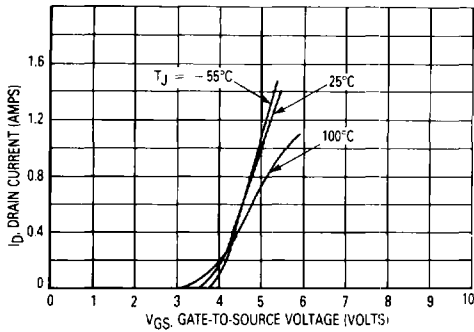


Figure 3. Transfer Characteristics

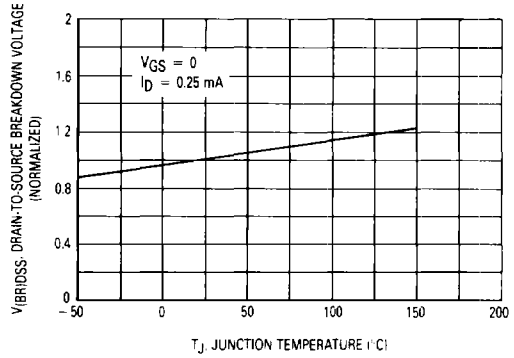


Figure 4. Breakdown Voltage Variation With Temperature

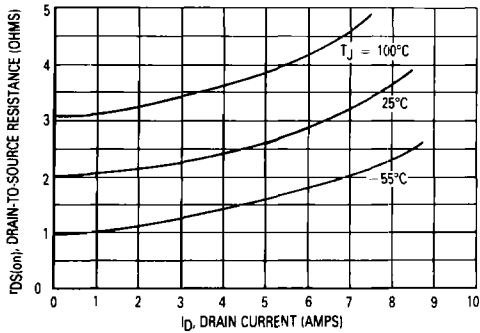


Figure 5. On-Resistance versus Drain Current

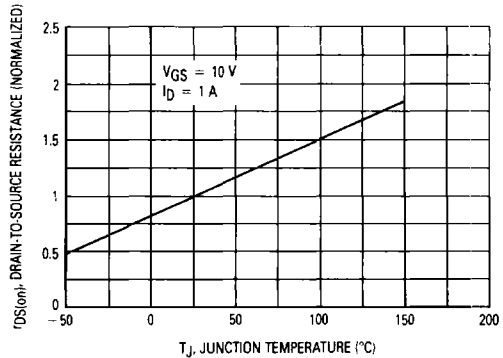


Figure 6. On-Resistance Variation With Temperature

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SAFE OPERATING AREA INFORMATION

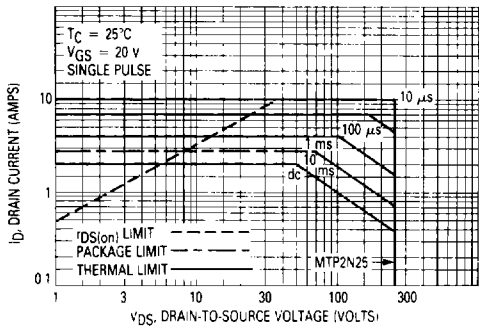


Figure 7. Maximum Rated Forward Biased Safe Operating Area

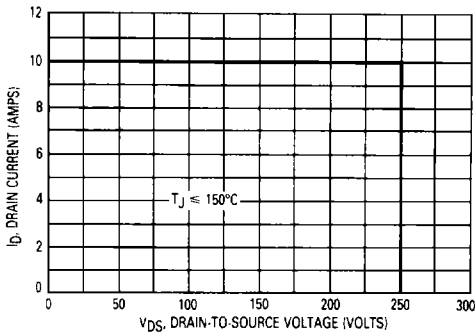


Figure 8. Maximum Rated Switching Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

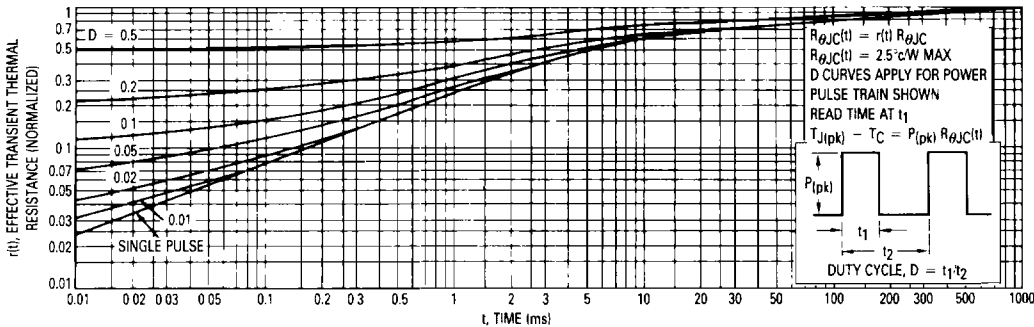


Figure 9. Thermal Response

MTP2N25

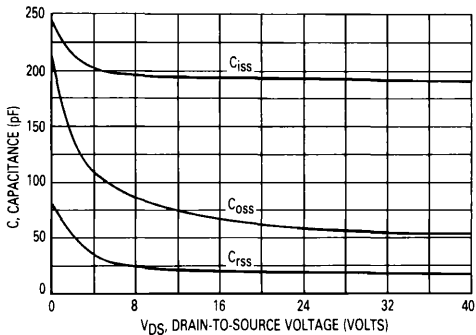


Figure 10. Capacitance Variation

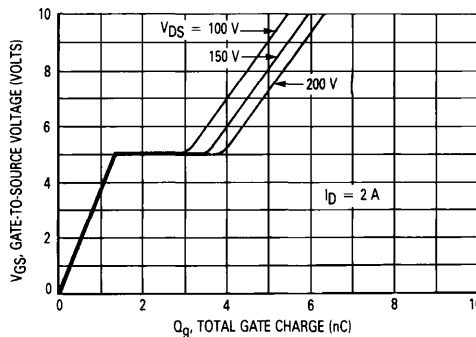


Figure 11. Gate Charge versus Gate-to-Source Voltage

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RESISTIVE SWITCHING

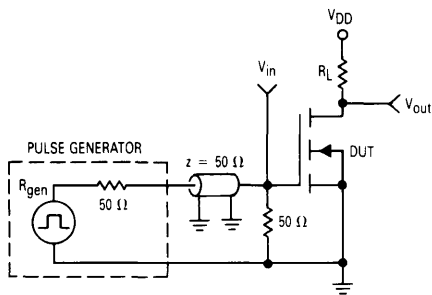


Figure 12. Switching Test Circuit

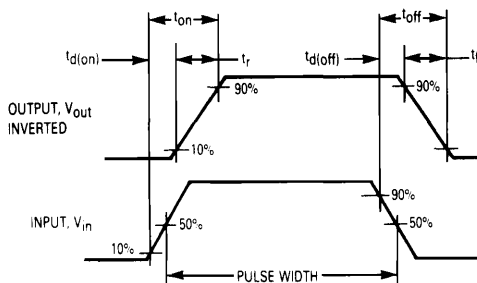
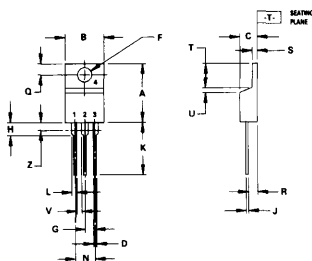


Figure 13. Switching Waveforms

OUTLINE DIMENSIONS

CASE 221A-04 TO-220AB



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.25	0.570	0.602
B	9.60	10.28	0.380	0.405
C	4.07	4.87	0.160	0.190
D	5.64	5.88	0.222	0.231
F	3.51	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.03	0.110	0.120
J	5.28	5.55	0.208	0.220
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.20	0.190	0.205
Q	2.54	3.04	0.100	0.120
R	2.04	2.74	0.080	0.110
S	1.15	1.39	0.045	0.055
T	3.87	4.47	0.152	0.175
U	0.90	1.27	0.035	0.050
V	1.15	—	0.045	—
Z	—	2.54	—	0.100

STYLE 5
PIN 1 GATE
2 DRAIN
3 SOURCE
4 DRAIN

NOTES
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2 CONTROLLING DIMENSION: INCH
3 DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED