# HORIZONTAL COMBINATION

The TBA920 is a monolithic integrated circuit intended for television receivers with transistor, thyristor, or tube-equipped output stages.
It combines the following functions:
- noise gated sync separator
- line oscillator
- phase comparison between sync pulse and oscillator
- loop gain and time constant switching (also for video recorder applications)
- phase comparison between line-flyback pulse and oscillator
- output stage for drive a variety of line output stages

## QUICK REFERENCE DATA

| | | | |
|---|---|---|---|
| Supply voltage | $V_{1-16}$ | nom. | 12 V |
| Ambient temperature | $T_{amb}$ | | 25 °C |
| **Input signals** | | | |
| Video input voltage (positive-going sync) top sync to white value | $V_{8-16(p-p)}$ | typ. | 3 V<br>1 to 7 V |
| Noise gate input current (peak value) | $I_{9M}$ | > | 30 μA |
| Input resistance of noise gate | $R_{9-16}$ | typ. | 200 Ω |
| Flyback signal input voltage (peak value) | $V_{5-16M}$ | typ. | ±1 V |
| Flyback signal input current (peak value) | $I_{5M}$ | typ. | 1 mA |
| **Output signals** | | | |
| Line driver output voltage (peak-to-peak value) | $V_{2-16(p-p)}$ | typ. | 10 V |
| Line driver output current (average value) | $I_{2(AV)}$ | max. | 20 mA |
| Line driver output current (peak value) | $I_{2M}$ | max. | 200 mA |
| Composite sync output voltage (peak value) | $V_{7-16M}$ | typ. | 10 V |

## PACKAGE OUTLINE

16-lead dual in-line; plastic (SOT38).

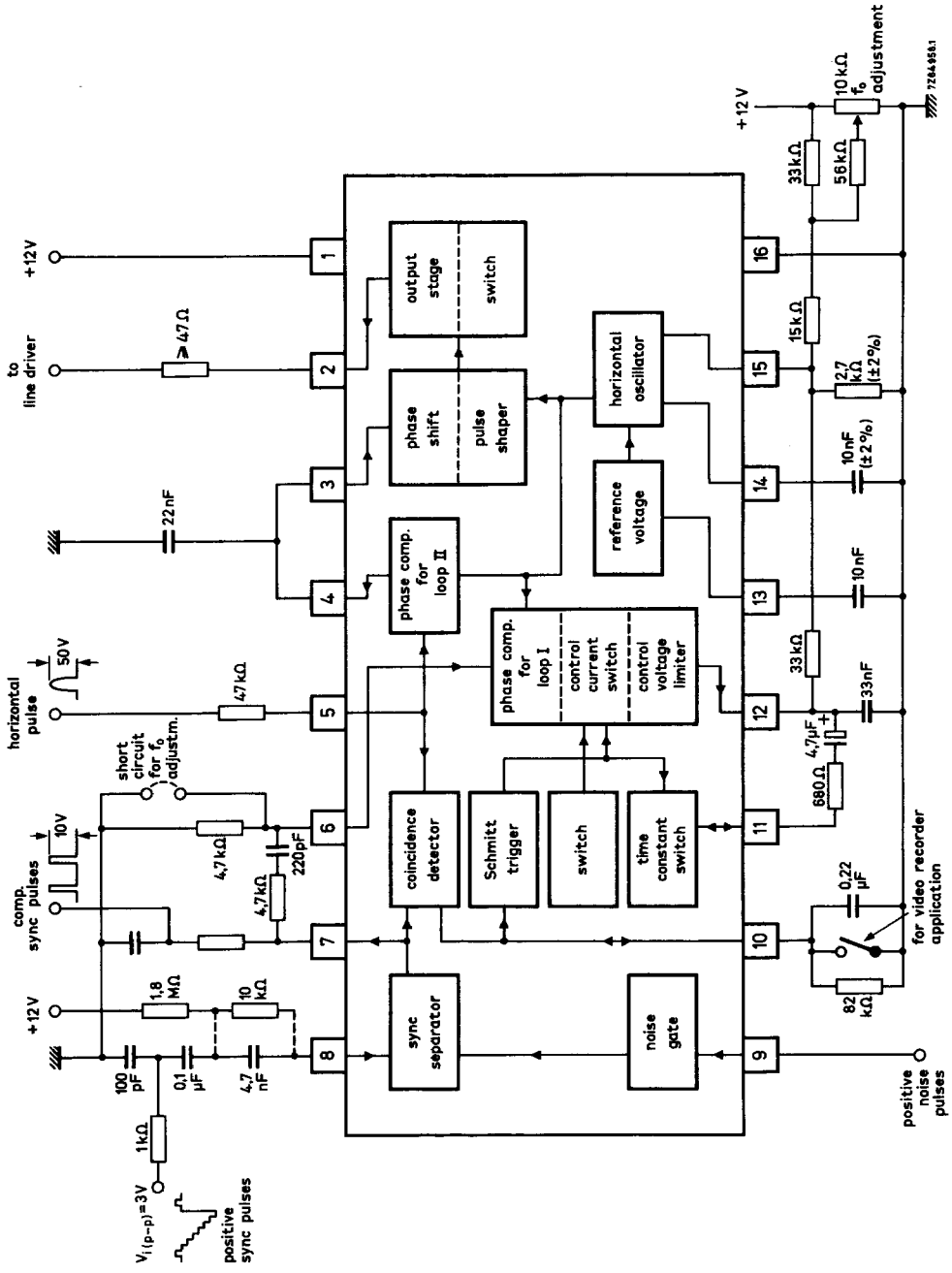


Fig. 1 Block diagram and application information.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (Vp) | $V_{1-16}$ | max. | 13,2 V |
| Phase shift voltage | $V_{3-16}$ | | 0 to 13,2 V |
| Video input voltage | $-V_{8-16}$ | max. | 12 V |
| Coincidence detector voltage | $V_{10-16}$ | | −0,5 to +5 V |
| Line driver output current (average value) | $I_{2(AV)}$ | max. | 20 mA |
| (peak value) | $I_{2M}$ | max. | 200 mA |
| Horizontal pulse current (peak value) | $I_{5M}$ | max. | 10 mA |
| Composite sync current (peak value) | $I_{7M}$ | max. | 10 mA |
| Pos. sync pulse current (peak value) | $I_{8M}$ | max. | 10 mA |
| Noise gate current (peak value) | $I_{9M}$ | max. | 10 mA |
| Total power dissipation | $P_{tot}$ | max. | 600 mW* |
| Storage temperature | $T_{stg}$ | | −55 to +125 °C |
| Operating ambient temperature | $T_{amb}$ | | 0 to + 70 °C |

## CHARACTERISTICS

At $V_{1-16}$ = 12 V; $T_{amb}$ = 25 °C. Measured in circuit of Fig. 1 (CCIR standard).

| | | | |
|---|---|---|---|
| Current consumption at $I_2 = 0$ | $I_1$ | typ. | 36 mA |

**Required input signals**

*Video signal*

| | | | |
|---|---|---|---|
| Input voltage (positive going sync) peak-to-peak value | $V_{i(p-p)}$ | typ. | 3 V<br>1 to 7 V |
| Input current during sync pulse (peak value) | $I_{8M}$ | typ. | 100 μA |

*Noise gating* (pin 9)

| | | | |
|---|---|---|---|
| Input voltage (peak value) | $V_{9-16M}$ | > | 0,7 V |
| Input current (peak value) | $I_{9M}$ | ><br>< | 30 μA<br>10 mA |
| Input resistance | $R_{9-16}$ | typ. | 200 Ω |

*Flyback pulse* (pin 5)

| | | | |
|---|---|---|---|
| Input voltage (peak value) | $V_{5-16M}$ | typ. | ±1 V |
| Input current (peak value) | $I_{5M}$ | ><br>typ. | 50 μA<br>1 mA |
| Input resistance | $R_{5-16}$ | typ. | 400 Ω |
| Pulse duration at 15 625 Hz | $t_5$ | > | 10 μs |

* 800 mW permissible while tubes are heating up.

**CHARACTERISTICS** (continued)

**Delivered output signals**

| | | | |
|---|---|---|---|
| *Composite sync pulses* (positive; pin 7) | | | |
| Output voltage (peak-to-peak value) | $V_{7\text{-}16(p\text{-}p)}$ | typ. | 10 V |
| Output resistance | | | |
| at leading edge of pulse (emitter follower) | $R_{7\text{-}16}$ | ≈ | 50 Ω |
| at trailing edge | $R_{7\text{-}16}$ | typ. | 2,2 kΩ |
| Additional external load resistance | $R_{7\text{-}16(ext)}$ | > | 2 kΩ |
| *Driver pulse* (pin 2) | | | |
| Output voltage (peak-to-peak value) | $V_{2\text{-}16(p\text{-}p)}$ | typ. | 10 V |
| Average output current | $I_{2(AV)}$ | < | 20 mA |
| Peak output current | $I_{2M}$ | < | 200 mA |
| Output resistance (low ohmic) | $R_{2\text{-}16}$ | typ. | 2,5 or 15 Ω * |
| Output pulse duration when synchronized | $t_2$ | | 12 to 32 μs ** |
| Permissible delay between leading edge of output pulse and flyback pulse at $t_5 = 12$ μs | $t_{o\ tot}$ | | 0 to 15 μs |
| Supply voltage at which output pulses are obtained | $V_{1\text{-}16}$ | > | 4 V |

* Depends on switch position and polarity output current. $R_{2\text{-}16} = 2{,}5\ \Omega$ is valid for $V_{2\text{-}16} = +10{,}5$ V and a load between pins 2 and 16 (e.g. an external resistor).

** The output pulse duration is adjusted by shifting the leading edge ($V_{3\text{-}16}$ from 6 V to 8 V). The pulse duration is a result of delay in the line output device and the action of the second control loop in the TBA920S.
For a line output stage with a BU108 high-voltage transistor the resulting duration is about 22 μs, and in such a way that the line output transistor is switched on again about 8 μs after the middle of the line-flyback pulse. This pulse duration must be taken into account when designing the driver stage and driver transformer as this way of driving the line output device differs from the usual, i.e. a driver duty cycle of about 50%.

| | | | | |
|---|---|---|---|---|
| *Oscillator* | | | | |
| Frequency; free running ($R_{15\text{-}16}$ = 3,3 kΩ) | $f_o$ | | 15 625 Hz | * |
| Spread of frequency at $R_{15\text{-}16}$ = 3,3 kΩ; $C_{14\text{-}16}$ = 10 nF | $\frac{\Delta f_o}{f_o}$ | < | 1,5 % | ** |
| Frequency change when decreasing the supply down to minimum 4 V | $\left\lvert\frac{\Delta f_o}{f_o}\right\rvert$ | < | 10 % | |
| Frequency control sensitivity | $\frac{\Delta f_o}{\Delta I_{15}}$ | typ. | 16,5 Hz/μA | |
| Adjustment range of frequency (in Fig. 2) | $\frac{\Delta f_o}{f_o}$ | typ. | ±5 % | |
| Influence of supply voltage on frequency at $V_P$ = 12 V | $\frac{\delta f_o}{f_o} / \frac{\delta V_P}{V_{Pnom}}$ | < | 5 % | |
| *Control loop 1* (between sync pulse and oscillator) | | | | |
| Control voltage range | $V_{12\text{-}16}$ | | 0,8 to 5,5 V | |
| Control current (peak values) | | | | |
| at $V_{10\text{-}16} > 4{,}5$ V; $V_{6\text{-}16} > 1{,}5$ V | $I_{12M}$ | typ. | ±2 mA | |
| at $V_{10\text{-}16} < 2$ V; $V_{6\text{-}16} > 1{,}5$ V | $I_{12M}$ | typ. | ±6 mA | |
| Loopgain of APC system | | | | |
| a. Time coincidence between sync pulse and flyback pulse or $V_{10\text{-}16} > 4{,}5$ V | $\frac{\Delta f}{\Delta t}$ | typ. | 1 kHz/μs | |
| b. No time coincidence or $V_{10\text{-}16} < 2$ V | $\frac{\Delta f}{\Delta t}$ | typ. | 3 kHz/μs | |
| Catching and holding range | $\Delta f$ | typ. | ±1 kHz | ▲ |

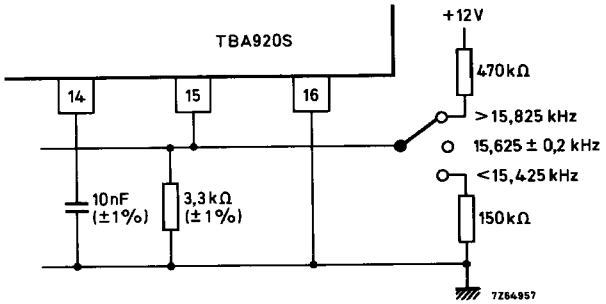


Fig. 2 Possibilities for oscillator frequency adjustment.

* The oscillator frequency can be changed for other TV standards by an appropriate value of $C_{14\text{-}16}$.

** Exclusive external components tolerances.

▲ Adjustable with $R_{12\text{-}15}$.

**CHARACTERISTICS** (continued)

| | | | | | |
|---|---|---|---|---|---|
| Pull-in time for $\Delta f/f_o = \pm 3\%(\Delta f = 470$ Hz) | $t$ | $\approx$ | 20 | ms | (note 1) |
| Switch-over from large control sensitivity to small control sensitivity after catching | $t$ | $\approx$ | 20 | ms | (note 1) |
| *Control loop II* (between flyback pulse and oscillator) | | | | | |
| Permissible delay between leading edge of output pulse (pin 2) and leading edge of flyback pulse | $t_{d\,tot}$ | | 0 to 15 | µs | |
| Static control error | $\frac{\Delta t}{\Delta t_d}$ | $<$ | 0,5 | % | (note 2) |
| Output current during flyback pulse (peak value) | $I_{4M}$ | typ. | ±0,7 | mA | |
| *Overall phase relation* | | | | | |
| Phase relation between leading edge of sync pulse and middle of flyback pulse | $t$ | typ. | 4,9 | µs | (note 3) |
| Tolerance of phase relation | $\lvert\Delta t\rvert$ | $<$ | 0,4 | µs | (note 4) |
| Voltage for $T_2 = 12$ to 32 µs | $V_{3\text{-}16}$ | | 6 to 8 | V | |
| Adjustment sensitivity | $\frac{\Delta T_2}{\Delta V_{3\text{-}16}}$ | typ. | 10 | µs/V | |
| Input current | $I_3$ | $<$ | 2 | µA | |

*External switch-over of parameters* (loop filter and loop gain) of control loop I (e.g. for video recorder application) see note 5.

| | | | | | |
|---|---|---|---|---|---|
| Required switch-over voltage | | | | | |
| at $R_{11\text{-}16} = 150\ \Omega$ | $V_{10\text{-}16}$ | $>$ | 4,5 | V | |
| at $R_{11\text{-}16} = 2$ kΩ | $V_{10\text{-}16}$ | $<$ | 2 | V | |
| Required switch-over current | | | | | |
| at $R_{11\text{-}16} = 150\ \Omega$; $V_{10\text{-}16} = 4,5$ V | $I_{10}$ | typ. | 80 | µA | (note 6) |
| at $R_{11\text{-}16} = 2$ kΩ; $V_{10\text{-}16} = 2$ V | $I_{10}$ | typ. | 120 | µA | |

1. See Fig. 1.
2. The control error is the remaining error in reference to the nominal phase position between leading edge of the sync pulse and the middle of the flyback pulse caused by a variation in delay of the line output stage.
3. This phase relation assumes a luminance delay line with a delay of 500 ns between the input of the sync separator and the drive to the picuture tube. If the sync separator is inserted after the luminance delay line or if there is no delay line at all (black-and-white sets), then the phase relation is achieved at $C_{5\text{-}16} = 560$ pF.
4. The adjustment of the overall phase relation and consequently the leading edge of the output pulse at pin 2 occurs automatically by the control loop II or by applying a d.c. voltage to pin 3.
5. With sync pulses at pin 7 and 8; without RC network at pin 10.