VTC Inc.
Value the Customer™

VM54100

COMPLETE 100 MBITS/SEC PEAK-DETECTION READ CHANNEL

950801

ADVANCE INFORMATION

August,1995

FEATURES

- Compatible with 100 MBits/sec NRZ Data Rate Operation
- Dual Mode VGA Supports AGC and PGC Modes
- Low Z and Fast AGC Modes for Quick Write Recovery
- Programmable Filter with Pulse Slimming
- Multiplexed Filter Tuning Supports Servo and Data Fields
- Demodulation of Servo Bursts
- Low Power (Standby) Mode Along with a Very Low Power (Sleep) Mode

DESCRIPTION

The VM54100 is a PolarMOS2 integrated circuit that provides all of the data processing for detection and qualification of read signals from a head preamplifier. This device can handle NRZ data rates of 100Mbits/sec. This device along with its companion chip, the VM53100 comprises a complete 100Mbits/sec read channel.

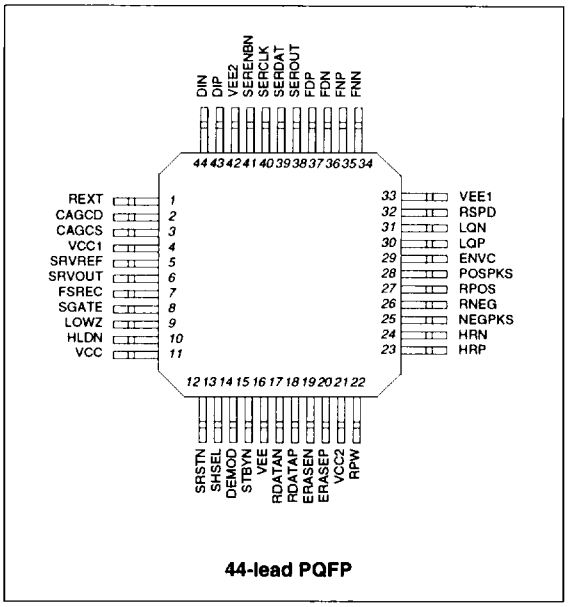
ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage:
V_{CC} ..... -0.3V to 7.0V
Input Voltages:
Digital Input Voltage V_{IN} ..... -0.3V to V_{CC} +0.3V
Analog Input Voltage V_{IN} ..... -0.3V to V_{CC} +0.3V
Junction Temperature T_J ..... 150°C
Storage Temperature T_{stg} ..... -65° to 150°C
Thermal Impedance Θ_{JA}:
44-lead PQFP ..... 60°C/W

RECOMENDED OPERATING CONDITIONS

Supply Voltage:
V_{CC} .....+5V ±10%
Junction Temperature ..... 0° to 125°C

CONNECTION DIAGRAM



44-lead PQFP

READ CHANNEL CIRCUITS

Functional Description

The VM54100 consists of a variable gain amplifier (VGA) with an automatic gain control circuit. The automatic gain control (AGC) circuit can be disabled, which allows the VGA to be operated in programmable gain control (PGC) mode.

A seven pole linear phase 0.05 degree equiripple low pass filter (LPF) with pulse slimming is included in the VM54100. Normal and differentiated outputs from the filter are provided with matched delays.

The filter provides for programmable unboosted cutoff frequencies from 4.68MHz to 37.5MHz. Likewise, the pulse slimming is programmable from 0dB to 13dB.

A pulse detector and qualifier is provided which includes an envelope detector, adjustable dV/dt sensitivity, programmable threshold and independent qualification of negative and positive threshold to suppress error propagation.

A peak detecting servo demodulator with an array of sample and hold amplifiers provides for the demodulation of up to four servo fields.

A low power mode is available through the use of the STBYN pin. In standby mode (STBYN = 0) the VGA, sections of the filter, the PDQ, and the demodulator sections are powered down.

The majority of the chip functionality is controlled via a serial digital interface

Gain Control (GC)

The Gain Control section of the VM54100 consists of a wide band variable gain amplifier (VGA) with a charge pump, amplitude detector, and exponentiator. The Gain Control has two modes: Automatic (AGC), and Programmable (PGC) gain control. The mode of the Gain Control is controlled by the PGC control bit (Addr = 1001,bit = 7).

The read back signal is externally AC coupled into the VGA amplifier on the DIP/DIN pins (see Diagram 1). The signal is amplified by the VGA and equalized by the 0.05" equiripple low pass filter. The normal output of the filter, FNP/FNN, is externally AC coupled back into the LQP/LQN inputs where it is amplitude detected by the AGC loop and locked to $1.0V_{ppd}$. With a nominal filter gain of 1 volts/volt, the VGA provides a $1.0V_{ppd}$ signal to the filter for inputs ranging from 24 to 320 mV_{ppd} on the DIP/DIN pins. A test mode is provided (test mode 5) in which the filter is completely bypassed, and the VGA outputs DOP/DON and filter inputs FIP/FIN are multiplexed to the FNP/FNN and FDP/FDN chip outputs respectively.

When in the AGC mode PGC bit is "0", the gain of the VGA is controlled by an amplitude detector, charge pump, exponentiator, and CAGCx capacitor, either CAGCD or CAGCS. The amplitude detector determines if the signal level (V_{LQ}) at the LQP/LQN inputs is above or below the target amplitude of $1.0V_{ppd}$. If the amplitude is below $1.0V_{ppd}$, the normal charging current (I_{QCN}) charges the CAGCx capacitor to increase the gain of the VGA. If the amplitude is greater than $1.0V_{ppd}$ but below $1.25V_{ppd}$, the normal discharging current (I_{QDN}) discharges the CAGCx capacitor to reduce the gain of the VGA. And if the amplitude exceeds $1.25V_{ppd}$, a fast discharging current (I_{QDF}) that is 7X the normal discharging current, quickly discharges the CAGCx capacitor until the signal level is back below $1.25V_{ppd}$. The magnitude of the normal discharging current (I_{QDN}) is set by an external resistor connected between the REXT pin and ground and is given by the following equation

$$I_{QDN} = \frac{1.2V}{REXT} \qquad \textit{(eq. 9)}$$

where REXT should set to 4.8kΩ. **This value should not be altered to adjust the loop response** because this current is also used as a reference to the DAC's. Adjust the loop responses by altering the AGC caps discussed below. The normal discharging current is 40X the normal charging current, resulting in an asymmetrical loop response.

A fast recovery from small input signals is provided with a '0'-to-'1' transition on the FSREC input. A fast charging current (I_{QCF}) that is 7X the normal discharging current quickly charges the CAGCx capacitor until the $1.0V_{ppd}$ signal level is reached, after which the loop resumes normal operation.

There are two AGC capacitors, the CAGCD pin capacitor which is used for the data field when SGATE = 0, and the CAGCS pin capacitor which is used for the servo field when SGATE = 1. This allows the data and servo fields to have independent discharging and charging rates. It also avoids reacquisition of gain at the beginning of the servo and data fields. When HLDN = 0 the discharging and charging currents are disabled, and the AGC action is halted to allow for servo burst measurement.

In the AGC mode, the VGA has an exponential characteristic of gain versus control voltage in order to minimize response time over the entire range of input voltages. Equation (2) expresses the VGA normal mode gain (A_V), in volts/volts, as an exponential function of the control voltage on the selected CAGCx pin.

$$A_V = A_{V(max)} \bullet e^{\left(\frac{2.8V - V_{CAGCX}}{0.53V}\right)} \qquad \textit{(eq. 10)}$$

where $A_{V(max)}$ is 56 volts/volt and V_{CAGCx} nominally ranges from1.4V to 2.8V.

When in the PGC mode (Addr = 1001, bit7 = "1"), the amplitude detector, charge pump, and exponentiator are disabled, and the gain of the VGA is controlled by the "VGA Gain" DAC. The control word for the DAC is read from the Data VGA Gain register (Addr = 1011, bits[4:0]) when SGATE = 0 otherwise its read for Servo VGA GAIN register (Addr = 1100, bits[4:0]). In PGC mode, the VGA has a linear gain versus binary control word characteristic to insure predictable controlled input response. Equation (3) expresses the VGA gain as a linear function of the control word.

$$A_V = 4 + \frac{46}{31} \times N \qquad \textit{(eq. 11)}$$

where N ranges between 0 and 31decimal or 00000 to 11111 binary (bit 4 is the MSB).

For fast write to read recovery a low input impedance mode is provided. When LOWZ = 1, the gain of the VGA goes to zero, the input impedance is reduced to $1/60^{th}$ of its normal value, and the charge pump currents are disabled to retain the gain values set by the CAGCx capacitors. Also, a low impedance is initiated for the on-chip AC coupling capacitors between the VGA output and the filter input. Upon releasing the LOWZ mode, the on-chip

coupling capacitors are held in the low impedance mode for an extra 200ns while the VGA restores its gain. This eliminates any transient offset effects that may occur while the loop is locking.

While the VM54100 is idle (STBYN = 0) or in SLEEP mode (Addr = 1000, bit7 = "0"), the VGA amplifier is powered down.

Programmable Low Pass Filter (LPF) / Equalizer

The filter is implemented as a 7-pole 0.05 degree linear phase equiripple low pass filter with matched normal and differential outputs. The cutoff frequency and boost equalization are programmable.

The basic building block for the filter is the integrator (g_m-C) stage which consists of a transconductance amplifier driving on-chip capacitors. Figure 2 shows how g_m-C stages are connected to form a bi-quad, which realizes a second-order transfer function. The equation below is the expression for the transfer function of such a bi-quad. In Diagram 3, three of these bi-quads and a single g_m-C stage are cascaded to form a seven-pole low pass filter. In parallel with the final g_m-C stage is a nearly identical single g_m-C stage configured as a high-pass, or differentiator section. The various sections supply normal or differentiated low-pass outputs with matched group delays. The normal output goes to the AGC and servo sections. The differentiated output, along with the normal output, is used by the PDQ block to provide data and servo peak position information. Because the high-pass differentiator stage tracks the other g_m-C stages, the relative gain AO_D of the differentiated output to the normal output is nearly constant (at two-thirds the unboosted cutoff frequency) over the range of the cutoff frequency and boost level of the filter, as depicted in Graph 1.

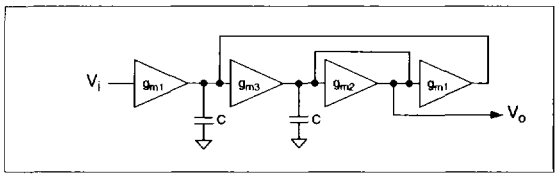


Figure 2: State-Variable Biquad

$$\frac{V_o}{V_i} = \frac{\omega_o^2}{s^2 + s(\omega_o/Q_o) + \omega_o^2} \qquad \textit{(eq. 12)}$$

where $\omega_o = \frac{\sqrt{g_{m1} \cdot g_{m2}}}{C}$ and $Q_o = \frac{\sqrt{g_{m1} \cdot g_{m3}}}{g_{m2}}$

The filter utilizes transconductor-capacitor (g_m-C) techniques to provide a cutoff frequency (f_C) that is directly proportional to g_m/C. An accurate g_m is derived from the Frequency Cutoff (Fc) DAC input current and an on-chip bandgap voltage using a feedback circuit. The parts are trimmed during wafer probe to compensate for on-chip capacitance variations.

Cutoff frequency is controlled by the "Frequency Cutoff" DAC. The control word for the DAC is read from the Data Frequency Cutoff register (Addr = 1000, bits[6:0]) when SGATE=0 otherwise its read from the Servo Frequency Cutoff register (Addr = 1001, bits[6:0]). Cutoff frequency (f_C), in MHz, is related to the binary control word by the following equation

$$f_c = (0.256 \times N) + 4.68 \qquad \textit{(eq. 13)}$$

where N ranges between 0 and 127decimal or 0000000 to 1111111 binary (bit 6 is the MSB).

The gain (g_m) of each g_m-C stage is established using MOSFET input devices. These devices are operated in the triode region, resulting in a transconductance of:

$$g_m \approx \mu \bullet C_{ox} \bullet \frac{W}{L} \bullet V_{ds} \qquad \textit{(eq. 14)}$$

where μ is the MOSFET channel mobility, C_{ox} is the MOSFET gate oxide capacitance per unit area, W and L are the MOSFET channel width and length respectively, and V_{ds} is the MOSFET drain-to-source voltage. The magnitude of the g_m of each stage is set to the desired cutoff frequency by adjusting V_{ds}. Stage-to-stage g_m ratios determine the shape of the filter transfer function and are achieved by rationing the MOSFET widths (W).

The filter gm reference is generated using an external resistor on the REXT pin and on-chip bandgap references.

The amount of boost equalization depends on the output of the BOOST DAC. Boost is programmable from 0 to 13dB as measured from the low-frequency gain portion of the frequency domain transfer function to the peak in the transfer function. Graph 1 shows normalized filter response curves with maximum boost for both the normal and differentiated outputs. Graph 2 shows the nominal relationship between the BOOST control word and the resulting boost level. Notice the absence of boost when BOOST is below 4. In this region the bandwidth is being pushed out but the gain doesn't peak above the DC level.

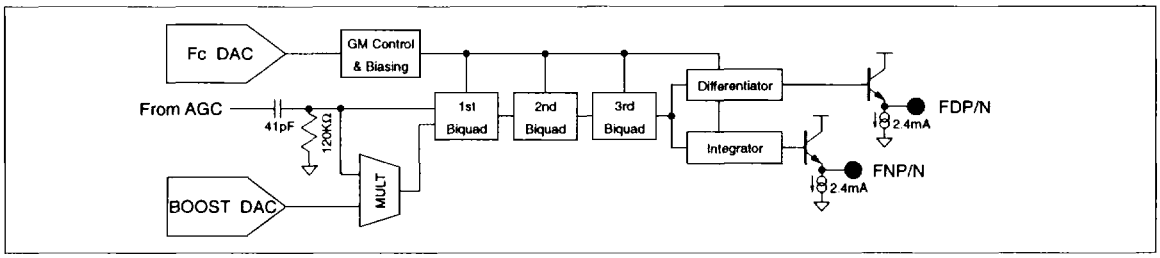
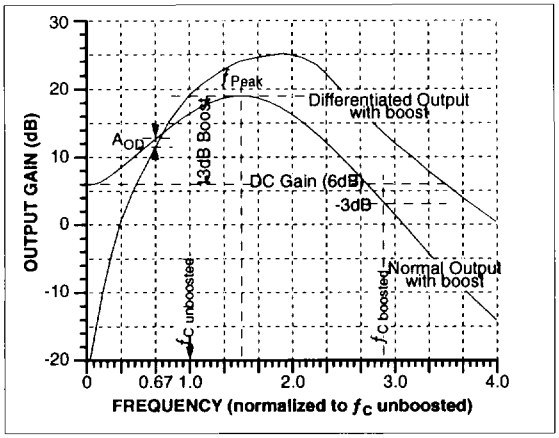
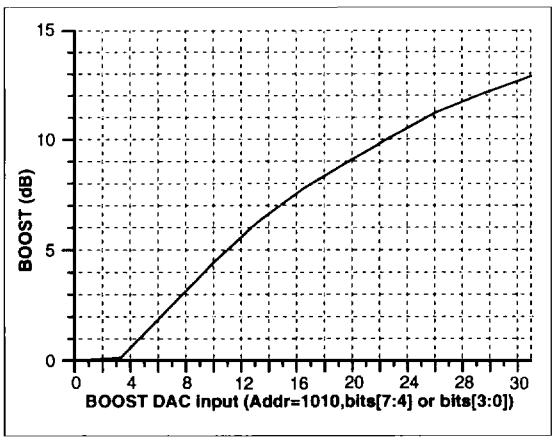


Figure 1: Filter Block Diagram



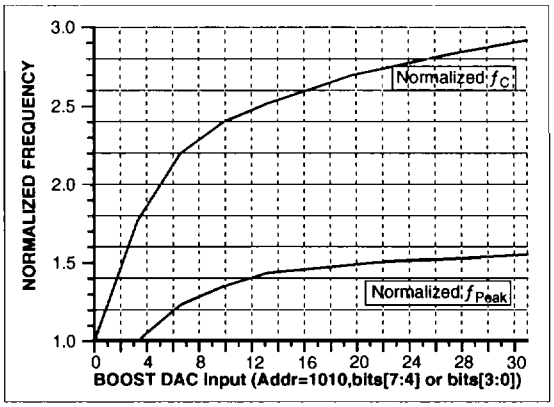
Graph 1: Normal and Differentiated Output Gains

Graph 3 shows the effect of boost on the cutoff frequency. With maximum boost the cutoff frequency is nearly triple the unboosted value. Also shown is gain peak frequency, which for maximum boost achieves a value of over 1.5. Thus, as an example, if the unboosted cutoff frequency is programmed to 30MHz, with maximum boost the peak gain of 13dB will occur at approximately 46MHz, and the net cutoff frequency will be 88MHz.



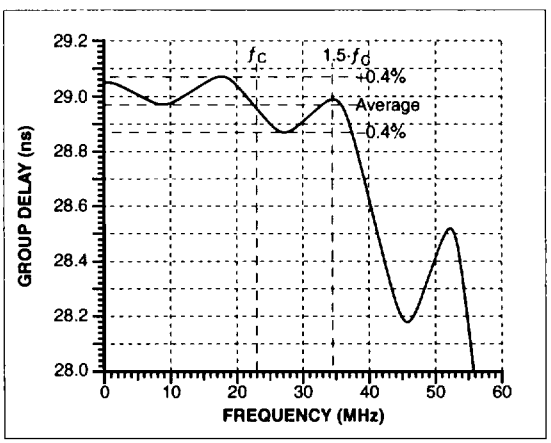
Graph 2: Ideal Boost (in dB) versus BOOST DAC Input

Boost, or pulse slimming, is implemented by feeding the filter input through a variable gain stage to the normally grounded terminals of the capacitors in the first bi-quad. This yields a pair of programmable symmetric zeros on the real axis. Because the resulting transfer function has an added $K \cdot s^2$ in the numerator, the group delay is unaffected by the amount of boost.



Graph 3: Normalized f_C and f_{Peak} versus BOOST DAC Input

Group delay for an ideal 0.05 degree equiripple filter is flat within 1% out to twice the unboosted cutoff frequency. Because group delay is extremely sensitive to device mismatches and parasitic effects, a "real" filter will have variations of several percent. Group delay flatness is defined as the variation about an average value out to the specified frequency. The VM54100 group delay flatness is specified to be less then ±2% out to 1.5 times the unboosted cutoff frequency. It is expressed in percent because the group delay is inversely related to the unboosted cutoff frequency, and is about 24ns at a cutoff of 30MHz. Thus at this cutoff frequency, the group delay varies by less than±0.5ns out to 45MHz. A typical group delay is shown in Graph 4 with measurements displayed.



Graph 4: Typical Group Delay of AGC and Filter (with f_C = 23MHz)

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The absolute group delay through the Gain Control block and the filter consists of both a fixed delay and a delay that varies inversely with cutoff frequency. The group delay (T_{GD}), in nanoseconds, is expressed below as a function of the cutoff frequency.

$$T_{GD} = 6ns + \frac{0.53}{f_C} \qquad \textit{(eq. 15)}$$

where f_C is the unboosted cutoff frequency in Hz.

Because the filter is AC-coupled from the Gain Control output, a zero occurs at DC and a pole occurs at about 60KHz. This pole-zero pair distorts the frequency response of the filter below frequencies of about 1.3MHz. Test Mode 0 bypasses the Gain Control circuit and AC-coupling network, which allows direct filter measurements from the DIP/DIN pins.

Pulse Detector and Qualifier (PDQ)

The PDQ receives filtered analog readback signals from the Read/Write Preamp and delivers qualified logic pulses to the Read Data Separator. Errors due to false peaks are detected in the PDQ and erased in the Data Separator prior to decoding of the data. A block diagram of the PDQ section is shown in Diagram 4 below.

Two analog input channels are processed by the PDQ. The timing channel inputs HRP/HRN (HR) are AC coupled from the differentiated output of the filter FDP/FDN. The level qualification channel inputs LQP/LQN (LQ) are AC coupled from the normal outputs of the filter FNP/FNN.

The high resolution signal is converted to digital pulses using a zero-crossing comparator and self-resetting one-shot circuit having a nominal pulse width of 3.5ns. The timing channel clocks a D-type Flip-Flop on either positive or negative transitions of the HR input. Visibility into the timing channel signals HRCOMP and HRCLK are provided in test mode (see Test Mode description).

The HR pulses are qualified by signals which are derived from the LQ channel. Two comparators indicate when the positive (LP) and negative (LN) extents of the LQ signal exceed a certain percentage of the average peak amplitude of the LQ signal. In addition, two peak detectors qualify consecutive same polarity peaks, if the subsequent peaks are of higher amplitude and have sufficient slope. All subsequent lower amplitude peaks are ignored. The first opposite polarity peak following a valid RDATA pulse is not slope qualified. The digital logic stores the polarity of the peak and qualifies consecutive peaks based on the sensitivity level threshold V_{TH}(detect) set by the PEAK Threshold DAC. If a second peak is qualified, an RDATA pulse is generated with a coincident Erase pulse. Two comparators indicate when the positive (POSPK) and negative (NEGPK) slope detectors exceed the sensitivity level threshold.

The average peak amplitude of the LQ signal is determined by an envelope follower circuit consisting of an input buffer ($A_V = 2$), a rectifier/peak detector, and a unity gain transconductance amplifier (g_m). The buffer stage drives a precision rectifier circuit combining the differential outputs such that the most positive extent of the signal is stored (peak detected) on an internal capacitor (10pF). The storage capacitor charges quickly from its common mode value ($V_{LQ} = 0$) to approximately $V_{LQ}/2$. It's rate of discharge is set by the current I_D, related to the charge pump normal discharging current (I_{QDN}) by the expression

$$I_D = \frac{I_{QDN}}{20} \qquad \textit{(eq. 16)}$$

The envelope follower output voltage (V_{ENVC}) on the ENVC pin 'follows' the peak detector voltage at a rate fixed by the transconductors output currents and the external capacitor ENVC. The transconductors charge and discharge currents, I_{EC} and I_{ED}, are also related to the charge pump normal discharging current (I_{QDN}) by the expressions

$$I_{EC} = 3.32 \cdot I_{QDN} \quad \text{and} \quad I_{ED} = \frac{I_{QND}}{8} \qquad \textit{(eq. 17)}$$

The charge current is 26.6X the discharge current resulting in an asymmetric response.

The product of the envelope follower is the output (V_{ENVC}), which is equal to one-half the average peak amplitude of the LQ signal. The envelope follower output voltage is combined with the dc control voltage, provided by the LVLQ DAC, to create the threshold for "level" qualification ($V_{TH(LQ)}$). The control word for the DAC is read from the LVLQ THRESHOLD register (Addr = 1101, bits[4:0]). The threshold voltage is set proportional to the average peak amplitude of the LQ signal (V_{LQ}) as specified by the DAC input according to following relationship:

$$V_{TH(LQ)}(qual) = V_{LQ} \times \left(\frac{1.1}{31}\right) \times N \qquad \textit{(eq. 18)}$$

where N ranges between 0 and 31decimal or 00000 to 11111 binary (bit 4 is the MSB).

In addition, the envelope follower output voltage is combined with the dc control voltage, provided by the PEAK DAC, to create the threshold for "peak" detection ($V_{TH(PD)}$). The control word for the DAC is read from the PEAK THRESHOLD register (Addr = 1110, bits[4:0]). The threshold voltage is set proportional to the average peak amplitude of the LQ signal (V_{LQ}) as specified by the DAC input according to following relationship:

$$V_{TH(PD)}(detect) = V_{LQ} \times \left(\frac{1.1}{31}\right) \times N \qquad \textit{(eq. 19)}$$

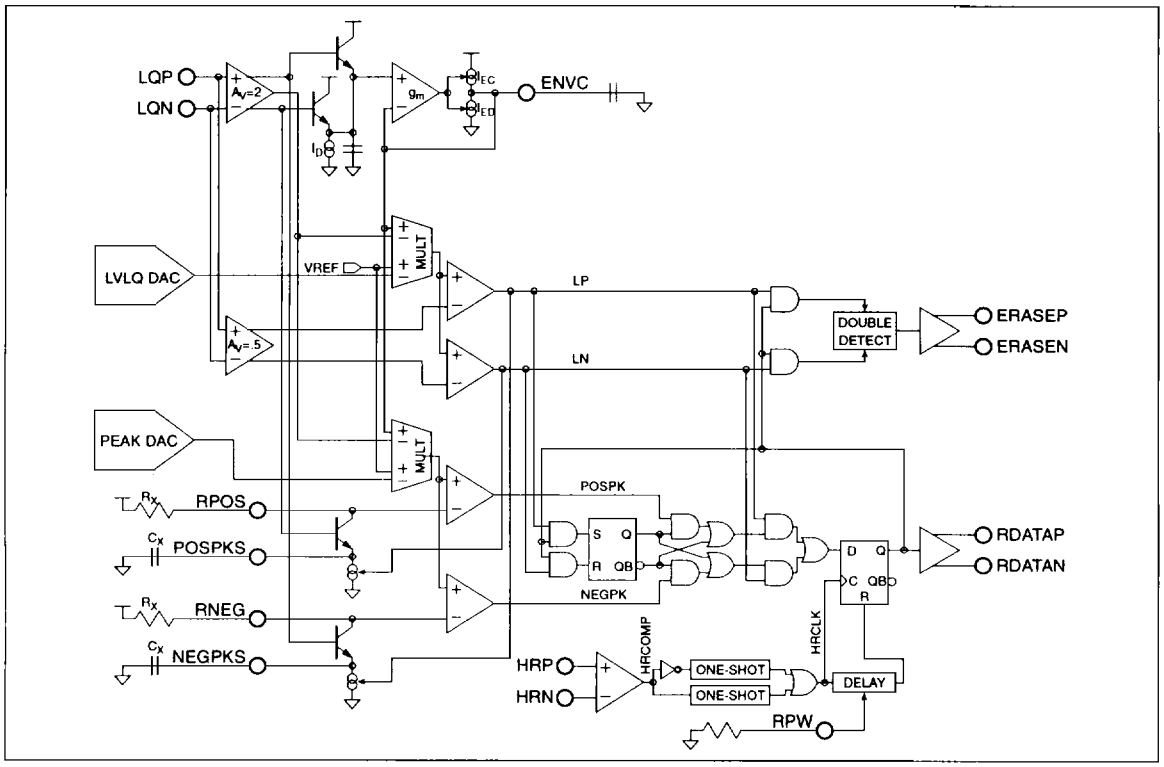
where N ranges between 0 and 31 decimal or 00000 to 11111 binary (bit 4 is the MSB). The slope detector threshold voltage is referenced to V_{CC} and is compared against the pin voltages of RPOS and RNEG, also referenced to V_{CC}. If the most negative extent of either V_{RPOS} or V_{RNEG} exceeds the sensitivity level threshold, comparator outputs POSPK or NEGPK produce a logical '1'. Qualified consecutive same polarity higher amplitude peaks produce both ERASE and RDATA pulses.

The signal voltages on the RPOS and RNEG pins depend on the external components selected. The RC time constant (Rx • Cx) and the LQ signal frequency (f_{LQ}) are both proportional to the magnitude of the voltage (V_{Rx}) across the Rx resistors. The expression for V_{Rx} can be written as

$$V_{Rx} = Rx \cdot Cx \cdot \frac{dV_{LQ}}{dt} = Rx \cdot Cx \cdot 1.0V \cdot \pi \cdot f_{LQ} \cdot \sin(2 \cdot \pi \cdot f_{LQ} \cdot t) \qquad \textit{(eq. 20)}$$

where $V_{LQ} = 0.5V \cdot \sin(2 \cdot \pi \cdot f_{LQ} \cdot t)$. And thus the maximum peak voltage across RPOS and RNEG is

PULSE DETECTOR AND QUALIFEIER (PDQ) BLOCK



$$V_{Rx}(max) = Rx \cdot Cx \cdot 1.0V \cdot \pi \cdot f_{LQ} \quad (eq.\ 21)$$

V_{Rx}(max) is frequency dependent, and hence Rx, Cx, and the slope detector sensitivity level (V_{TH}) must be chosen carefully over the frequency range of interest. For normal operation, $V_{Rx}(max) \geq V_{TH}$ at the minimum signal frequency. The recommended resistance value ranges from 50Ω to 500Ω for Rx, and the capacitance value ranges from 20pF to 200pF for Cx. VTC also recommends using a low threshold of 5% to 30% (high sensitivity). The values chosen should be optimized for system requirements.

The qualified RDATA pulses have provision for external control of the pulse width via an external resistor connected to the RPW pin. The pulse width (PW_{RDATA}) ranges from 3ns to 18ns and is expressed as a function of RPW by the following

$$PW_{RDATA} = 0.5ns/K\Omega \cdot RPW + 1.8ns \quad (eq.\ 22)$$

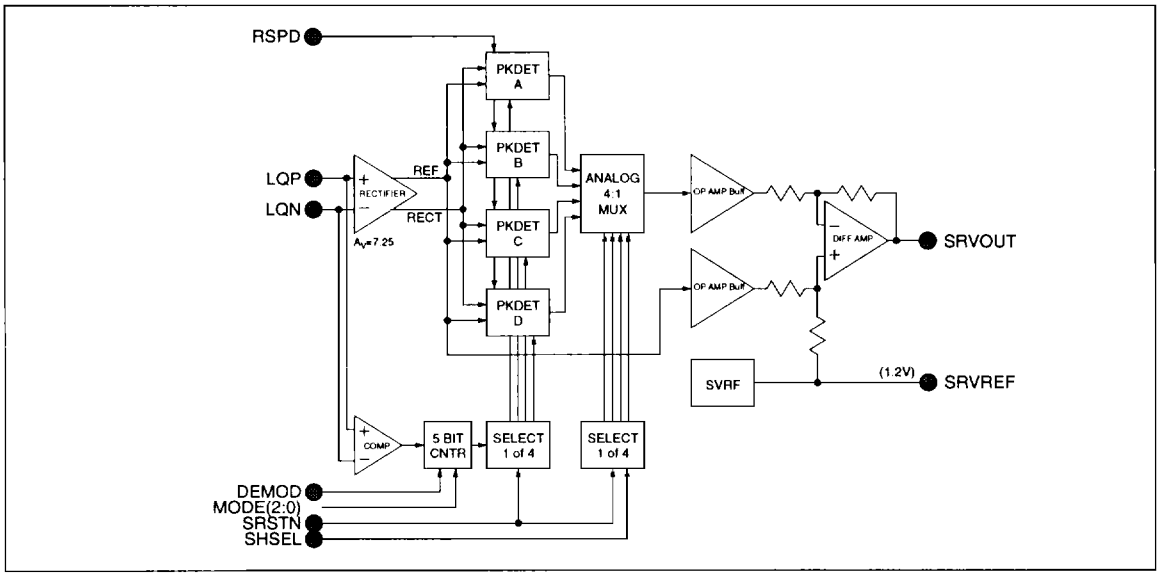
where RPW is given in KΩ and ranges from 4KΩ to 32KΩ.

Servo Demodulator

The servo demodulator supports full quadrature demodulation through the use of an array of four peak detector channels. A block diagram for the servo demodulator is shown above. The filtered servo bursts are AC coupled into the chip through the LQP and LQN inputs. The signal is amplified immediately to maximize the signal amplitude and reduce mismatch effects introduced by subsequent blocks. The amplified signal is full wave rectified and input to an array of four peak detectors. The peak detector consists of an emitter follower and on-chip hold capacitor. Each peak detector is selectively enabled and detects the peak voltage amplitude of the servo burst. After the peak has been detected, the peak detector is disabled and 'holds' the peak voltage for subsequent processing. A 4:1 analog switch allows each peak detector output to be multiplexed to the servo output. The multiplexed peak detector output and its corresponding reference are buffered before feeding into a difference amplifier. The difference amplifier output is the SRVOUT output pin and is referenced to the SRVREF pin (typically 1.2V).

The peak detectors capture the servo burst information under the control of the DEMOD input signal. Both synchronous and asynchronous modes of operation are supported. In asynchronous mode (MODE = 000_b), on the leading (rising) edge of the DEMOD input pin, the peak detectors are enabled and begin tracking the servo signal asynchronously. Likewise, on the falling edge, the peak detectors are disabled and asynchronously stop tracking the servo signal. In synchronous mode (MODE ≠ 000_b), the leading (rising) edge of the DEMOD input pin is synchronized to an internal clock. The clock is generated by a comparator that detects the high to low zero crossings of the input waveform to the peak detector. The comparator has 60mV of input hysteresis which removes low amplitude noise and yields cleaner clock transitions. The synchronized DEMOD signal causes the peak detectors to sample the input waveform synchronously with the incoming waveform to reduce any charge injection nonlinearity. The MODE[2:0] word (Addr = 1011,bits[7:5]) selects the number of cycles counted by a 5-bit

SERVO DEMODULATOR BLOCK DIAGRAM



counter. Note that the full wave rectifier causes both halves of a cycle to be peak detected. The definition of the decoding of the MODE[2:0] word is shown in the normal mode register decode table.

MODE[2:0] word			*MODE*	*NORMAL DEFINITION*
2	*1*	*0*		
0	0	0	0	async mode
0	0	1	1	4 cycles
0	1	0	2	8 cycles
0	1	1	3	12 cycles
1	0	0	4	16 cycles
1	0	1	5	20 cycles
1	1	0	6	24 cycles
1	1	1	7	28 cycles

If the proper number of cycles have not arrived when the trailing edge of the DEMOD input pin occurs, then the peak detectors asynchronously progresses to a Hold mode as a fail safe feature.

Consecutive cycles of the DEMOD pin cause the A, B, C, and D peak detectors to sample the input waveform. The SHSEL input pin is provided to select the various peak detector outputs. The rising edge of SHSEL causes the selection to change to the A peak detector, the second pulse selects B, etc. The servo demodulator control logic and all peak detectors are reset by a low level on the SRSTN input pin. Upon the low level of SRSTN, the SRVOUT pin is reset to the SRVREF voltage. The servo blocks may also be reset automatically by an internal one-shot. The one-shot initiates a reset pulse of ~500ns when SGATE = 1 and STBYN = 0. This automatic reset feature is useful when going back and forth between servo tracking and standby mode.

The RSPD pin gives the user some control of the peak detector bandwidth. A resistor is placed between the RSPD pin and the VCC1 supply. This resistor ties to the collector of each emitter follower in the peak detector. This is shown in Diagram 6.

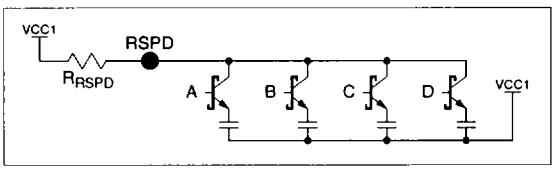


Figure 3: Peak Detector Bandwidth Control Circuitry

When a rising edge comes into the peak detector, the emitter follower charges the capacitor. The charging current flows through the collector and a voltage drop is seen across R_{RSPD}. If $Ic \cdot R_{RSPD}$ becomes large enough, the emitter follower will saturate thus limiting further charging of the capacitor. As R_{RSPD} is increased, the effective bandwidth of the peak detector is reduced and lessens the sensitivity to incoming noise spikes in the servo waveform.

$$\text{BandWidth} \propto \frac{1}{\text{RSPD}} \qquad \textit{(eq. 23)}$$

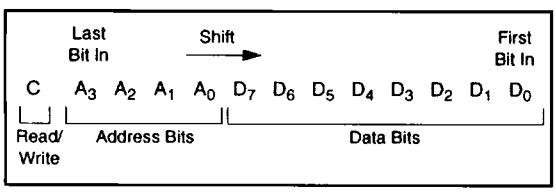
The RSPD Resistor Selection Table gives some typical values for RSPD as a function of servo frequency and the number of cycles used for demodulation. These RSPD values are the maximum resistance that may be used and still guarantee that the demodulated signal will reach 99.75% of the final value, given that servo frequency and number of demodulation cycles.

RSPD Resistor Selection Table

		# OF DEMOD CYCLES	
		4	28
SERVO INPUT FREQUENCY (MHz)	4	4KΩ	300KΩ
	10	1.5KΩ	20KΩ

Digital Control

Control of the chip is performed through a serial digital interface, a 7 byte register file and 5 digital to analog converters. Control information is stored in the register file and used directly as digital control lines or sent to one of the DACs to create analog control signals. The interface consists of four TTL-level signals for input data, output data, clock, and enable. Upon asserting SERENBN, the serial port is enabled and ready for input on SERDAT and SERCLK. The SERDAT line provides the data, address and read/Write control information. During a write cycle the serial control stream is shifted into the input register on the rising edge of the SERCLK starting with the LSB (bit0) of the data byte, after the MSB (bit 7) of the data has been read the four (4) address bits are clocked in starting with the LSB. After all 12 bits have been clocked into the shift register, a "0" must be placed on the SERDAT input (but NOT clocked in by SERCLK) to indicate data is being written to the chip. The data is then latched into the proper register when SERENBN is de-asserted. This process must be performed seven times to load all seven register banks. Refer to the Timing Diagram for Loading Internal Registers with the Serial Interface. The serial interface also has the capability of reading the programmed data back out of the internal registers on the SEROUT(tri-stated serial output) pin. After asserting SERENBN, a 4 bit address must be clocked into the shift register. A "1" must be placed on the SERDAT input (but NOT clocked in by SERCLK) to indicate data is being read from the chip. When the SERENBN line is de-asserted the SEROUT pin is taken out of tri-state mode and put into the active mode. After a short delay the output will settle to the state of bit0 from the selected register. To complete the read operation the SERENBN line must be reasserted and the SERCLK must be strobed to transfer successive bits to the output line. After the SERCLK line is strobed seven times the MSB of the data will be present on the output line. To read the address word the SERCLK must be strobed four additional times, at which time the MSB of the address will reside on the output line. To complete the read cycle the SERDAT line must be put into the "0" state and then the SERENBN can be de-asserted for the second time. After the SERENBN is de-asserted the second time the output buffer is placed into a high impedance tri-state mode. The Refer to the serial interface read timing diagram.



There are 8 control words used to drive the 5 control DACs. There are two control words one for SERVO mode and one for DATA mode for each of the three DACs FREQUENCY CUT-OFF, BOOST and VGA GAIN. The words are selected by the condition of the SGATE pin. The control range and resolution is given in the table below.

DAC Control Range and Resolution Table

DAC	RANGE		RESOLUTION STEP SIZE	UNITS
	MIN (000...)	MAX (111...)		
Frequency Control	3.75	30	0.207	MHz
Boost	0(0)	4.467(13)	0.298	V/V (dB)
VGA Gain	4	50	1.48	V/V
LVLQ Threshold	0	110	3.55	%
Peak Threshold	0	110	3.55	%

COMPONENT PINS

There are a number of different input and output buffers used on this chip. There are CMOS TTL inputs, Bipolar ECL-like differential outputs, Analog differential inputs, and several analog reference input and output pins. Because of pin limitations some pins serve double duty. A table showing the various pin types is provided below.

POWER SUPPLY PINS:

PIN NAME	PIN NO.	DESCRIPTION
VCC	10	Digital CMOS Power
VCC1	3	Analog Power
VCC2	20	Digital Bipolar Power

GROUND SUPPLIES PINS:

PIN NAME	PIN NO.	DESCRIPTION
VEE	15	Digital Ground
VEE1	32	Analog Ground
VEE2	43	Substrate Ground

CMOS TTL INPUT PINS:

PIN NAME	PIN NO.	DESCRIPTION
FSREC (active High)	6	Fast Recovery mode control
SGATE	7	Servo mode control (active High)
LOWZ (active High)	8	Low Impedance mode control
HLDN Low)	9	AGC Hold mode control (active
SRSTN	11	Servo Reset (active Low)

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SHSEL 12 Servo Peak Detector select

DEMOD 13 Demodulation Clock

STBYN 14 Standby mode control (active Low)

SERENBN 40 Serial I/O enable (active low)

SERCLK 39 Serial clock (latch on positive edge)

SERDAT 38 Serial input data

TTL OUTPUT PINS:

PIN NAME	PIN NO.	DESCRIPTION
SEROUT	35	Serial output data (alias stp)

EXTERNAL PINS:

PIN NAME	PIN NO.	DESCRIPTION
RPW	21	RDATA Pulse Width control, Resistor (4KΩ to 32KΩ) to Ground [see equation (14)]
RNEG	25	Negative Slope Detector Gain control, Resistor (50Ω to 500Ω) to VCC [see equation (13)]
RPOS	26	Positive Slope Detector Gain control, Resistor (50Ω to 500Ω) to VCC [see equation (13)]
RSPD	31	Servo Peak Detector Charge limit, Resistor (0 to 5KΩ) to VCC [see equation (15)]
REXT	44	Reference current for the control DACs Resistor (4.8K) to Ground [see equation (1)]
CAGCD	1	AGC Data Field Gain storage, Capacitor (390pF) to Ground
CAGCS	2	AGC Servo Field Gain storage, Capacitor (390pF) to Ground
NEGPKS	24	Negative Peak Voltage Level storage, Capacitor (20pF to 200pF) to Ground [see equation (13)]
POSPKS	27	Positive Peak Voltage Level storage, Capacitor (20pF to 200pF) to Ground [see equation (13)]
ENVC	28	Envelope Tracking Rate control, Capacitor (1200pF) to Ground

ANALOG DIFFERENTIAL INPUT PINS:

PIN NAME	PIN NO.	DESCRIPTION
HRP	22-23	High Resolution Comparator
HRN		
LQP	29-30	Level Qualifier
LQN		
DIP	41-42	Read Data Input
DIN		

BIPOLAR ECL-LIKE DIFFERENTIAL OUTPUT PINS:

PIN NAME	PIN NO.	DESCRIPTION
RDATAN	16-17	Pulse Detector Data Output
RDATAP		
ERASEN	18-19	Pulse Detector Erase Flag
ERASEP		
FDN	36-37	Filter Differentiated Output
FDP		
FNN	33-34	Filter Normal Output
FNP		

ANALOG OUTPUT PINS:

PIN NAME	PIN NO.	DESCRIPTION
SRVREF	4	Servo Reference Voltage
SRVOUT	5	Selected Sample & Hold Amplifier Output

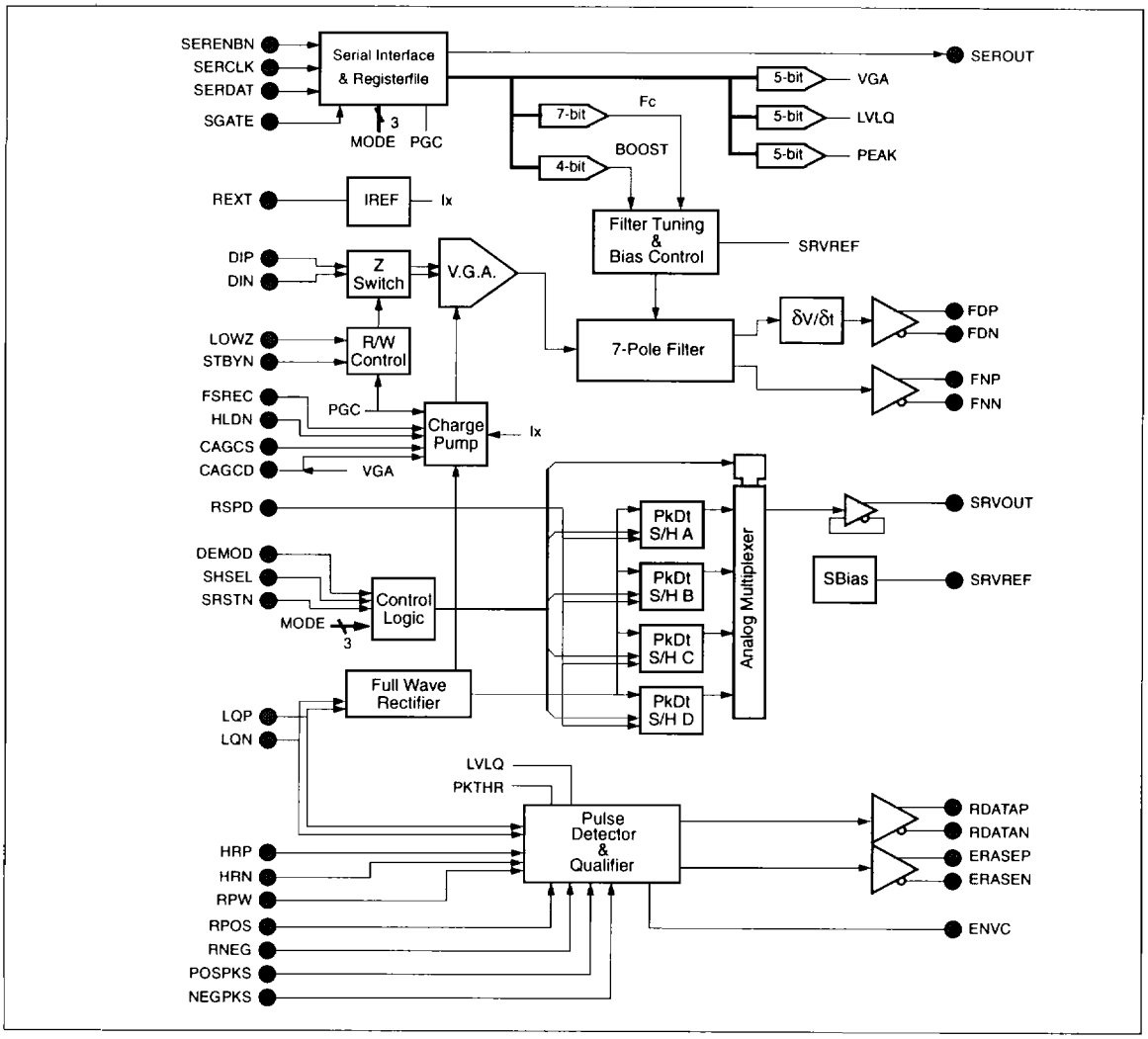
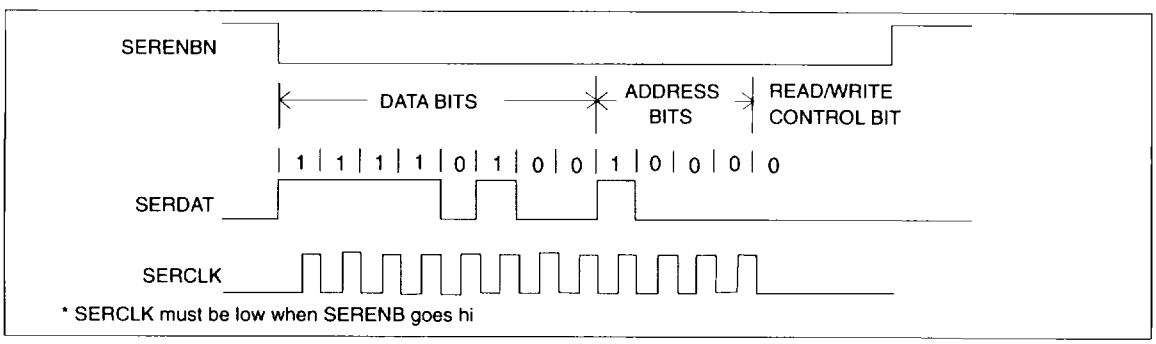
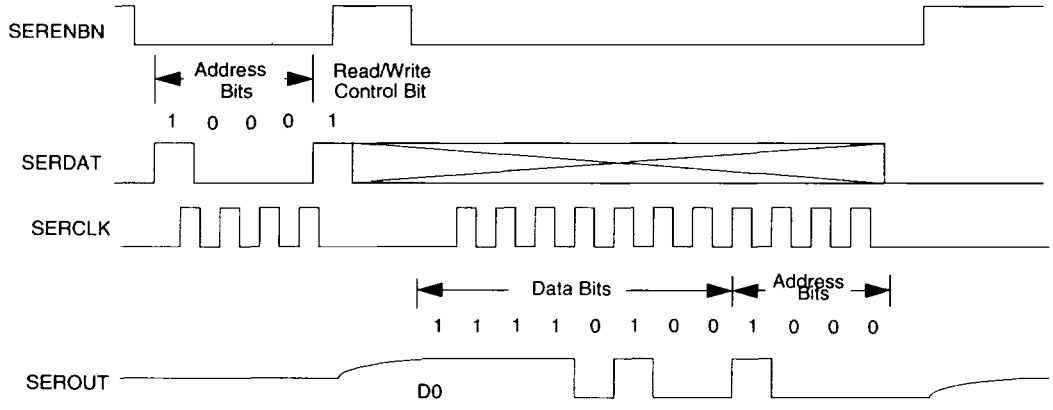


Figure 4: VM54100 Block Diagram



Timing Diagram for Loading Internal Registers with the Serial Interface



The controller should clock the data out of the serial register on the rising edge of SERCLK. The first rising edge clocks D0, etc.

Timing Diagram for Reading Internal Registers with the Serial Interface

Serial Register Table

Register Address	*DATA BIT*							
	7	*6*	*5*	*4*	*3*	*2*	*1*	*0*
1000	SLEEP	DATA "FREQUENCY CUTOFF" DAC						
1001	PGC	SERVO "FREQUENCY CUTOFF" DAC						
1010	DATA "BOOST" DAC				SERVO "BOOST" DAC			
1011	TM2	TM1	TM0	DATA "VGA GAIN" DAC				
1100	TBD	TBD	IQTF	SERVO "VGA GAIN" DAC				
1101	TBD	TBD	TBD	"LVLQ THRESHOLD" DAC				
1110	TBD	TBD	TBD	"PEAK THRESHOLD" DAC				

SLEEP - (Addr1000, bit7). When LO, the chip goes into a sleep mode. The list of powered down blocks includes all those controlled by STBYN, the reference generators and OUTTTLZ

DATA FREQ CUTOFF DAC - (Addr1000, bits[6:0]). Sets the filter cutoff when SGATE is LO.

PGC - (Addr 1001, bit 7). When LO, it disables the AGC loop and enables the VGA gain DAC.

SERVO FREQ CUTOFF DAC - (Addr 1001, bits[6:0]). Sets the filter cutoff when SGATE is HI.

DATA BOOST DAC - (Addr 1010, bits[7:4]). Sets the filter boost when SGATE is LO.

SERVO BOOST DAC - (Addr 1010, bits[3:0]). Sets the filter boost when SGATE is HI.

TM2,TM1,TM0 (Addr 1011, bits[7:5]). Select bits for the test mode options.

DATA VGA GAIN DAC (Addr 1011, bits[4:0]). Set the VGA gain when the PGC bit is LO and SGATE is LO.

SERVO VGA GAIN DAC (Addr1100, bits[4:0]). Sets the VGA gain when hte PGC bit is LO and SGATE is HI.

IQTF - (Addr 1100, bit[5]) set charage pump current to track filter cutoff frequency.

LVLQ THRESHOLD (Addr 1101, bits[4:0]) set the relative threshold for for Pulse data qualification

PEAK THRESHOLD (Addr 1110, bits[4:0]) sets the peak qualification threshold

AC AND DC CHARACTERISTICS Recommended operating conditions apply unless otherwise specified $0°C < T_A < 70°C$, $4.5V < V_{CC} < 5.5V$

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Power Supply Current	I_{CC}	Read Mode, Data Rate = 24Mbps			<TBD>	mA
		Read Mode, Data Rate = 1Gbps		<TBD>	<TBD>	mA
		Standby Mode			<TBD>	mA
Recovery time Standby to fully functional	T_{REC}	AGC within 10% final value, Pulse Detector w/o pulse pairing, Filter cutoff within 10% final value			10	µs

LOGICAL SIGNALS: ALL DIGITAL PINS

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Input High Voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Input Low Voltage	V_{IL}		−0.3		0.8	V
Input Leakage Current	I_{IL}	$V_{IL} = 0.8V$			±10	µA
	I_{IH}	$V_{IH} = 2.0V$			±10	µA
Control Signal rise and fall times	T_{CS}				100	ns
Input Capacitance	C_{IN}				10	pF

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GAIN CONTROL

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Common for both AGC and PGC modes						
Input dynamic range	V_{DI}	$V_{DI} = (V_{DIP} - V_{DIN})$ [THD_S applies for 250 to 320mV_{ppd}]	24		320	mV_{ppd}
Input common mode voltage	V_{CMDI}	$V_{CMDI} = (V_{DIP} + V_{DIN})/2$	V_{CC}-3.1	Vcc-2.7	V_{CC}-2.3	V
Differential input resistance	$R_{in(DA)}$	LOWZ = Low	3.0	6.0	9.0	KΩ
		LOWZ = High	50	100	150	Ω
Single ended input impedance	$R_{in(SA)}$	LOWZ = Low	1.5	3.0	4.5	KΩ
		LOWZ = High	25	50	75	Ω
Output common mode voltage	V_{CMFN}	$V_{CMFN} = (V_{FNP} + V_{FNN})/2$ Test Mode 5	V_{CC}-3.4	Vcc-3.0	V_{CC}-2.6	V
Output common mode voltage	V_{CMFD}	$V_{CMFD} = (V_{FDP} + V_{FDN})/2$ Test Mode 5	Vcc-3.0	Vcc-2.6	Vcc-2.2	V
Output offset voltage	V_{OS}	for V_{FN}, over entire gain range, Test Mode 5	-200		200	mV
Output distortion of V_{FN}	THD	V_{DI} = 250mV_{ppd}, $V_{FN} \leq 1.1V_{ppd}$, Test Mode 5, 1st, 2nd, and 3rd harmonics only			1.0	%
RX pin voltage	V_{RX}	R_{ext} = 6KΩ<TBD>	1.05	1.2	1.35	V
Only for AGC mode (PGC=Low)						
Output dynamic range	V_{FN}	$V_{FN} = (V_{FNP} - V_{FNN})$ $24mV_{ppd} \leq V_{DI} \leq 250mV_{ppd}$ $4MHz < f_{in} < 36MHz$	0.9		1.1	V_{ppd}
AGC minimum Gain	AV_{min}	$AV = V_{FN}/V_{DI}$ V_{CAGCD}=0.8v, Test Mode 5, [0]			4.0	V/V
AGC maximum Gain	AV_{max}	$AV = V_{FN}/V_{DI}$ V_{CAGCD}=3.2v, Test Mode 5, [0]	38	50		V/V
Gain settle from -30% V_{DI} step	T_{GD}	$V_{FN} \geq 0.9 \cdot$(final value)		31	TBD	µs
Gain settle from +30% V_{DI} step	T_{GA}	$V_{FN} \leq 1.1 \cdot$(final value)			2.0	µs
Charge Pump Normal Discharging current	I_{QDN}	0.55v ≤ V_{LQ} ≤ 0.56v (static), R_{ext} = 4.8KΩ	210	250	280	µA
Charge Pump Fast Discharging current	I_{QDF}	$V_{LQ} \geq$ 0.70v (static)	$6.8 \cdot I_{QDN}$		$7.5 \cdot I_{QDN}$	µA
Charge Pump Normal Charging current	I_{QCN}	$V_{LQ} \leq$ 0.40v (static)	I_{QDN}+44		I_{QDN}+36	µA
Charge Pump Fast Charging current	I_{QCF}	$V_{LQ} \leq$ 0.40v (static), FSREC Low to High edge triggered	$6.8 \cdot I_{QDN}$		$7.5 \cdot I_{QDN}$	µA
Charge Pump Leakage current	I_{LK}	HLDN = Low	-10		10	nA
Only for PGC mode (PGC=High)						
PGC minimum Gain	AV_{min}	$AV = V_{FN}/V_{DI}$ VGA_{DAC}=0h, Test Mode 5,			4.0	V/V
PGC maximum Gain	AV_{max}	$AV = V_{FN}/V_{DI}$ VGA_{DAC}=1Fh, Test Mode 5,	38	50	56	V/V

[0] Linearity of 0.5% from 1/8 to 7/8 of 550 mV_{ppd} required.

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PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Common for both AGC and PGC modes						
Special Distortion	THD_S	250 mV ≤ V_{DI} ≤ 320 mV, V_{FN} ≤ 1.1V_{ppd} , Test Mode 5			4	%
Differential input capacitance	$C_{in(DA)}$				10	pF
Input referred noise voltage	V_{IRN}	gain =AV_{max}, BW = 15MHz V_{DIP} = V_{DIN}			10	nV/√Hz
Bandwidth	BW	No AGC action. All gain values.	100			MHz
Common mode rejection ratio	$CMRR_G$	gain = AV_{max}, f_{in} = 5MHz, V_{DIP} = V_{DIN} = 100mV_{pp}	40			dB
Power supply rejection ratio	$PSRR_G$	gain = AV_{max}, f_{in} = 5MHz ΔV_{CC} or ΔV_{EE} =100mV_{pp}	45			dB
Only for AGC mode (PGC=Low)						
AGC Gain Sensitivity to CAGCx voltage	AV_{PV}	(Typical range is 1.4v to 2.8v)		17.5		dB/V
Only for PGC mode (PGC=High)						
Settling time to step change in VGA_{DAC}	T_{PGS}	zero to full scale after completion of the write cycle (SERENBN ↑)			300	ns

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Normal output noise voltage	V_{NN}	BW = 100MHz, f_C = 37.5MHz [1] V_{DIP} = V_{DIN} , Test Mode 4			TBD	mV_{rms}
Differentiated output noise voltage	V_{ND}	BW = 100MHz, f_C = 37.5MHz [1] V_{DIP} = V_{DIN} , Test Mode 4			9.0	mV_{rms}
Common mode rejection ratio	$CMRR_F$	f_{in} = 5MHz, Fc_{DAC}=7Fh , REXT=4.8KΩV_{DIP} = V_{DIN} = 100mV_{pp}	40			dB
Power supply rejection ratio	$PSRR_F$	f_{in} = 5MHz, V_{DI} = 0V, ΔV_{CC} or ΔV_{EE} = 100mV_{pp}	40			dB
Filter settle from step in Fc and BOOST	T_{FS}	Fc_{DAC} or $BOOST_{DAC}$ step to V_{FN} settle			300	ns
Group delay variation (normal or differential)	T_{GD3}	2.3MHz ≤ f_{in} ≤ 1.5f_C, 6MHz ≤ f_C ≤ 37.5MHz, V_{DI} = 250mV_{ppd} , $BOOST_{DAC}$=Fh ,	-3.6		3.6	ns
	T_{GD4}	1.3MHz ≤ f_{in} ≤ 1.5f_C, 6MHz ≤ f_C ≤ 37.5MHz, V_{DI} = 250mV_{ppd} , $BOOST_{DAC}$=Fh,	-5.25		5.25	ns
[1] Fc_{DAC}=7Fh, $BOOST_{DAC}$=Fh (boost level is 8.6dB).						
For Reference Sources and Gain Control Inputs						

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LOW PASS FILTER (7-POLE, 0.05°, EQUIRIPPLE PHASE)

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Filter cutoff frequency (low end)	f_{Cmin}	Fc_{DAC}=00h , REXT=4.8KΩ	3.18	4.68	5.38	MHz
Filter cutoff frequency (middle)	f_{Cmid}	Fc_{DAC}=40h , REXT=4.8KΩ	19	21.12	23.2	MHz
Filter cutoff frequency (high end)	f_{Cmax}	Fc_{DAC}=7Fh , REXT=4.8KΩ	33.75	37.5	41.25	MHz
Normal lowpass gain (V_{FN} vs. V_{DI})	AO_N	no boost, Fc_{DAC}=00h , REXT=4.8KΩ, f_{in} = 4MHz, Test Mode 4	-1.0	0	1.0	dB
Differentiated lowpass gain (V_{FD} vs. V_{FN}))	AO_D	no boost, $f_{in} = 0.67f_C$, Test Mode 4	AO_N-5.0	AO_N-3.5	AO_N-2.3	dB
Filter Boost (low end)	AB_{min}	$BOOST_{DAC}$=0h , REXT=4.8KΩ		0	0.5	dB
Filter Boost (high end)	AB_{max}	$BOOST_{DAC}$=Fh , REXT=4.8KΩ	11.5	13.0	16.0	dB
Normal filter output offset	V_{OSFN}	V_{DI} = 0.0v, Test Mode 4	-200		200	mV
Differentiated filter output offset	V_{OSFD}	V_{DI} = 0.0v, Test Mode 4	-200		200	mV
Total harmonic distortion (V_{FN} or V_{FD} vs. V_{DI})	THD_F	$f_{in} = 0.67f_C$,Fc_{DAC}=7Fh , REXT = 4.8KΩ, $V_{DI} \le 1.0V_{ppd}$, Test Mode 4, 1st, 2nd, and 3rd harmonics only			1.5	%
Filter Input common mode level (V_{DI})	F_{ICM}	Test Mode 4	Vcc-3.1	Vcc-2.7	Vcc-2.3	V
Phase shift from FNP-N to FDP-N (upper)	PS_{FU}	$f_{in} = 0.67f_C$, $f_C \ge$ 20MHz	85	90	95	degree
Phase shift from FNP-N to FDP-N (lower)	PS_{FL}	$f_{in} = 0.67f_C$, $f_C <$ 20MHz	87	90	93	degree
Normal/Diff common mode voltage	V_{CMFx}	Normal Output Differential Output	V_{CC} - 2.6 V_{CC} - 3.0	V_{CC}-2.2 V_{CC}-2.6	V_{CC} - 1.8 V_{CC} - 2.2	V
Normal/Diff output resistance	R_{OFx}				60	Ω
Normal/Diff output current	I_{OFx}		-1.0		1.0	mA
Group Delay	T_{GD}	Fc_{DAC}=7Fh , REXT=4.8KΩ	15	20	25	ns
Group delay variation (normal or differential)	T_{GD1}	$0.1f_C \le f_{in} \le 1.5f_C$, 10MHz ≤ f_C ≤ 38MHz, V_{DI} = 1.0V_{ppd} ,$BOOST_{DAC}$=0h , REXT=4.8KΩ, Test Mode 4	-4		+4	%
	T_{GD2}	$0.1f_C \le f_{in} \le 1.5f_C$, 10MHz ≤ f_C ≤ 38MHz, V_{DI} = 1.0V_{ppd} ,$BOOST_{DAC}$=Fh , REXT=4.8KΩ, Test Mode 4	-5		+5	%

PULSE QUALIFIER (PDQ)

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Input dynamic range	V_{LQ}	$V_{LQ} = (V_{LQP} - V_{LQN})$	0.5		1.5	V_{ppd}
Input common mode voltage	V_{CMLQ}	$V_{CMLQ} = (V_{LQP} + V_{LQN})/2$	V_{CC}–2.6	V_{CC}–2.2	V_{CC}–1.8	V
LQP/N differential input resistance	R_{LQ}		3.0		9.0	KΩ
HRP/N differential input resistance	R_{HR}		3.0		9.0	KΩ
ENVC Common Mode Voltage	V_{ENV0}	V_{LQ} = 0.0v	V_{CC} – 2.5	V_{CC}–2.1	V_{CC} – 1.7	V
Envelope follower offset [2]	N_{EO}	V_{ENVP} for V_{LQ}=+0.25v and V_{ENVN} for V_{LQ}=–0.25v	–3.0		3.0	%
Envelope follower gain	A_{ENV}	$\Delta N_{EO} / \Delta V_{LQ}$, where V_{LQ} is 1.5v and 0.5v	0.4		0.6	V/V
Envelope follower charging current	I_{EC}	$V_{ENV} = V_{ENV0} - 0.5v$, V_{LQ} = 0.0v, R_{EXT}=4.8KΩ	700	875	1050	µA
Envelope follower discharging current	I_{ED}	$V_{ENV} = V_{ENV0} + 0.5v$, V_{LQ} = 0.0v, R_{EXT}=4.8KΩ	30	37.5	45	µA
Envelope follower current tracking	N_{EI}	Variation of I_{EH} to I_{EL} ratio, $[(I_{EC}/I_{ED})(25/660)-1]\cdot 100$	–15		15	%
POSPKS detector gain	A_{PDP}	$\Delta V_{POSPKS} / \Delta V_{LQ}$, where V_{LQ} is 1.5v and 0.5v	0.4		0.6	V/V
NEGPKS detector gain	A_{PDN}	$\Delta V_{NEGPKS} / \Delta V_{LQ}$, where V_{LQ} is 1.5v and 0.5v	0.4		0.6	V/V
xPKS Common Mode Voltage	V_{CMxPKS}	V_{LQ} = 0v	V_{CC} –4.0	V_{CC}–3.5	V_{CC} – 3.0	V
POSPKS leakage current	I_{PL}	$LVLQ_{DAC}$=09h(32%), V_{LQ} = 0.0v, $V_{POSPKS} = V_{CMPPKS} + 0.5v$	–1		1	µA
NEGPKS leakage current	I_{NL}	$LVLQ_{DAC}$=09h(32%), V_{LQ} = 0.0v, $V_{NEGPKS} = V_{CMNPKS} + 0.5v$	–1		1	µA
POSPKS discharge current	I_{PD}	$LVLQ_{DAC}$=09h(32%), V_{LQ} = -0.5v, $V_{POSPKS} = V_{CMPPKS} + 0.5v$	12.5	15	17.5	mA
NEGPKS discharge current	I_{ND}	$V_{SETLV} = V_{REF} - 0.3v$, V_{LQ} = +0.5v, $V_{NEGPKS} = V_{CMNPKS} + 0.5v$	12.5	15	17.5	mA
Input dynamic range	V_{HR}	$V_{HR} = (V_{HRP} - V_{HRN})$	0.2		1.5	V_{ppd}
Input common mode voltage	V_{CMHR}	$V_{CMHR} = (V_{HRP} + V_{HRN})/2$	V_{CC}–3.0	V_{CC}–2.6	V_{CC}–2.2	V
HRP,N input frequency range	$f\Delta_{HR}$		2.3		38	MHz
Level Qual Threshold	TH_{LVLQ}	0.5v ≤ V_{LQ} ≤ 1.5v,(32%) $LVLQ_{DAC}$=09h	22		42	%
		0.5v ≤ V_{LQ} ≤ 1.5v,(81.6%) $LVLQ_{DAC}$=17h	70		95	%
Peak Detect Threshold	TH_{PD}	0.5v ≤ V_{LQ} ≤ 1.5v, (32%) $PEAK_{DAC}$=09h	22		42	%
		0.5v ≤ V_{LQ} ≤ 1.5v,(81.6%) $PEAK_{DAC}$=17h	70		95	%
Pulse pairing, $T_{PP} = 0.03/(16\cdot f_{in})$ $\phi_{HR}=\phi_{LQ}$ – 90° [HR leads LQ in phase]	T_{PP}	$V_{LQ} = V_{HR}$ = 500mV$_{ppd}$, f_{in} = 4 MHz			468	ps
		$V_{LQ} = V_{HR}$ = 500mV$_{ppd}$, f_{in} = 38 MHz			67	ps

[2] where $N_{EO} = (V_{ENVP}-V_{ENVN}) / (V_{ENVP}+V_{ENVN})$

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PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
For both RDATAP/N and ERASEP/N outputs						
Single ended output high level	V_{OHpe}	I_{OHpe} = 4.0mA	V_{CC} - 1.0		V_{CC} - 0.6	V
Single ended output low level	V_{OLpe}	I_{OLpe} = -4.0mA	V_{CC} - 1.9		V_{CC} - .975	V
Single ended output swing	V_{Spe}		375	500	1000	mV
Pulse width	T_{PW1}	Max. pulse width, RPW=24KΩ [3]	11		17	ns
	T_{PW2}	Min. pulse width, RPW=8KΩ [3]	4		8	ns
Idle	T_{PW3}	Relaxation time trailing to leading edge [3]	3		8	ns
[3] Measured from differential cross over points.						

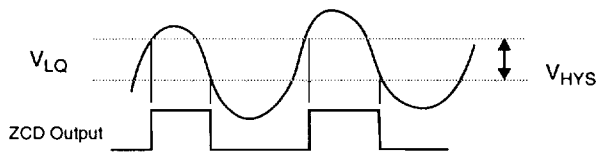
PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Pseudo ECL rise and fall times	T_{RF}	±375mV of Zero cross, C_L=15pF, 220Ω across output			2.0	ns
delay from leading edge RDATA to leading edge ERASE	T_{EF}	[3]			±3.0	ns
peak detect sensitivity (of successive peaks)	Vps	TBD	200			mV
[3] Measured from differential cross over points.						

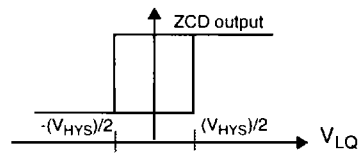
PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
LQ comparator DC gain	A_{LQ}			700		V/V
HR comparator DC gain	A_{HR}			1600		V/V
Internal envelope detector discharge current	I_{ID}	R_{EXT}=4.8KΩ		12.5		µA
Internal envelope detector capacitance	C_{ID}		9		11	pF
LQ comparator input offset	V_{LO}				2	mV
LQ comparator input offset drift	V_{LT}				10	µV/°C
HR comparator input offset	V_{HO}				0.8	mV
Data detection F/F setup time	T_{DS}				1	ns

SERVO PEAK DETECTING DEMODULATOR

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Servo Input frequency	f_{INS}		4		13.5	MHz
Gain [(V_{SVO}–V_{SVR})/V_{LQ}]	AV_S	measured over 1/4 to 3/4 of scale [4]	1.60	1.725	1.85	V/V
Input dynamic range [low end]	V_{DIL}	V_{DIL}=(V_{DIP}-V_{DIN}) 1/8 of 24mVppd min [5]			3	mV_{ppd}
Input dynamic range [high end]	V_{DIH}	V_{DIH}=(V_{DIP}-V_{DIN}) 7/8 of 250mVppd max [5]	218			mV_{ppd}
Linearity of V_{FN} vs. V_{DI}	V_{FL}	measured over 1/8 to 7/8 of scale [6]	–0.5		0.5	%
Linearity of V_{SVO}–V_{SVR} vs. V_{DI}	V_{DL1}	measured over 1/8 to 3/4 of scale [6]	–1.4		1.4	%
	V_{DL2}	measured over 3/4 to 7/8 of scale [6]	–4.5		4.5	%
Output offset (not referred to input)	V_{SO}	intercept of regressed line [6]	–40		40	mV
Output for zero input	V_{ZI}	[6]	0	60	80	mV
Mismatch of sample & holds	V_{MM}	Variation for a common input % of full scale			±1.0	%
SRVREF voltage	V_{SR}		1.14	1.20	1.26	V
Sample and Hold voltage decay rate	V_{DR}	0.1% of full scale droop in 50µs			40	V/sec
ZX comparator differential hysteresis	V_{HYS}	4% to 8% of full scale at LQ pins [7]	40		80	mV_{ppd}

[4] This specification is the slope of the characteristic ratio of a DC voltage to a peak to peak voltage.
[5] V_{DIL} and V_{DIH} specify the input range over which all other specifications must be met.
[6] In addition to the linearity and offset specifications, the output must also be guaranteed monotonic.
[7] Refer to waveshapes below for this specification.





READ CHANNEL CIRCUITS

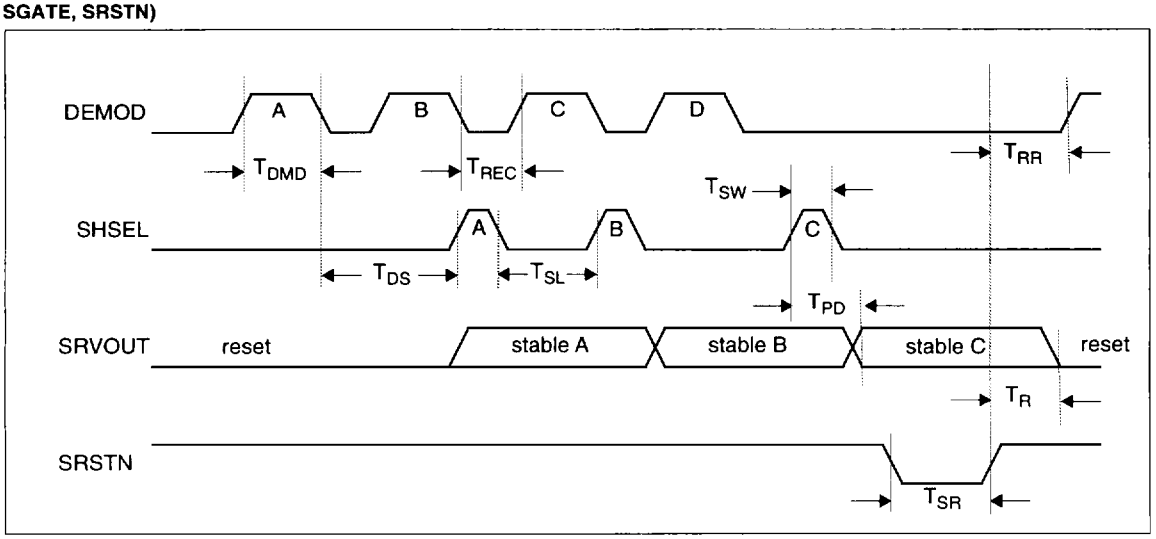
VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Channel to channel cross talk	V_{CT}	Effect of A on B etc. % of full scale			±0.5	%
Output impedance	R_{SO}	SRVREF and SRVOUT pins			50	Ω
Demodulator repeatability (52dB)	N_{DR}	Repeatability without external noise			±5.0	mV
Power supply rejection ratio	$PSRR_S$	f_{in} = 5MHz, V_{DI} = 0V, ΔV_{CC} or ΔV_{EE} = 100mV_{pp} [8]	25			dB
Common mode rejection ratio	$CMRR_S$	0MHz ≤ f_{in} ≤ 1MHz V_{LQP} = V_{LQN} = 100mV_{pp} [8]	25			dB
Total System Gain Variation [(V_{SVO}-V_{SVR})/V_{DI}]	AV_A	over all V_{DI}, 1/4 to 3/4 of scale [4]	1.54	1.725	1.92	V/V

[4] This specification is the slope of the characteristic ratio of a DC voltage to a peak to peak voltage.
[8] The required demodulator output Signal-to-Noise Ratio (SNR) due to external noise is 49dB.

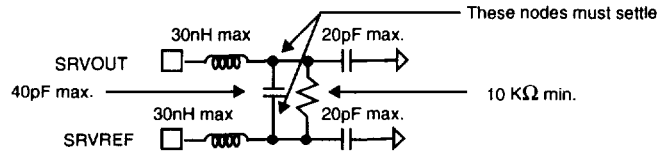
PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Peak Detector Bandwidth	f_{PD}	-3dB roll down of rectifier	68			MHz

DEMODULATOR TIMING (Pins: DEMOD, SHSEL, SRVOUT, SGATE, SRSTN)



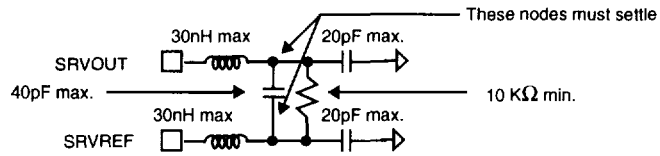
PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Select clock pulse width	T_{SW}		50			ns
Select clock (SHSEL) to stable SRVOUT delay	T_{PD}	0.25% of final value [9]			150	ns
SRSTN pulse width	T_{SR}		600			ns

[9] Load condition for SRVOUT and SRVREF given below.

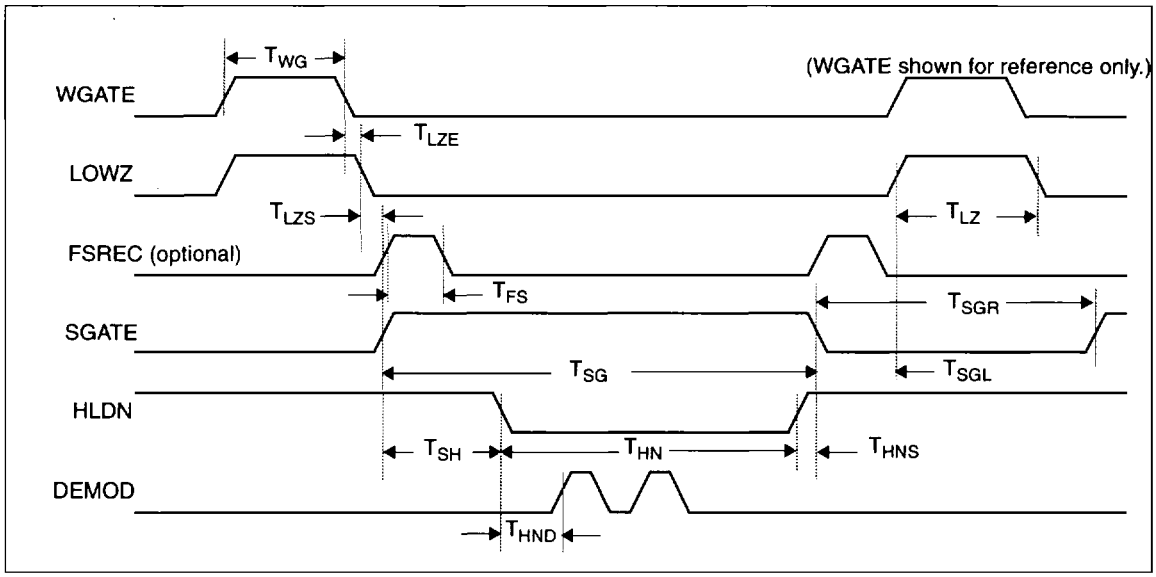


PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
DEMOD pulse width	T_{DMD}		150			ns
DEMOD recovery time	T_{REC}		150			ns
Select clock (SHSEL) inactive time	T_{SL}		50			ns
DEMOD to corresponding select clock delay	T_{DS}		0			ns
Sample and Hold step response	T_{SH}	0.25% of final value [9]			150	ns
Trailing edge SRSTN to SRVOUT reset delay	T_R	0.25% of final value [9]	150			ns
Trailing edge SRSTN to DEMOD recovery	T_{RR}		100			ns

[9] Load condition for SRVOUT and SRVREF given below.



SYSTEM TIMING DIAGRAM (NORMAL MODE) (Pins: LOWZ, FSREC, SGATE, HLDN, DEMOD)

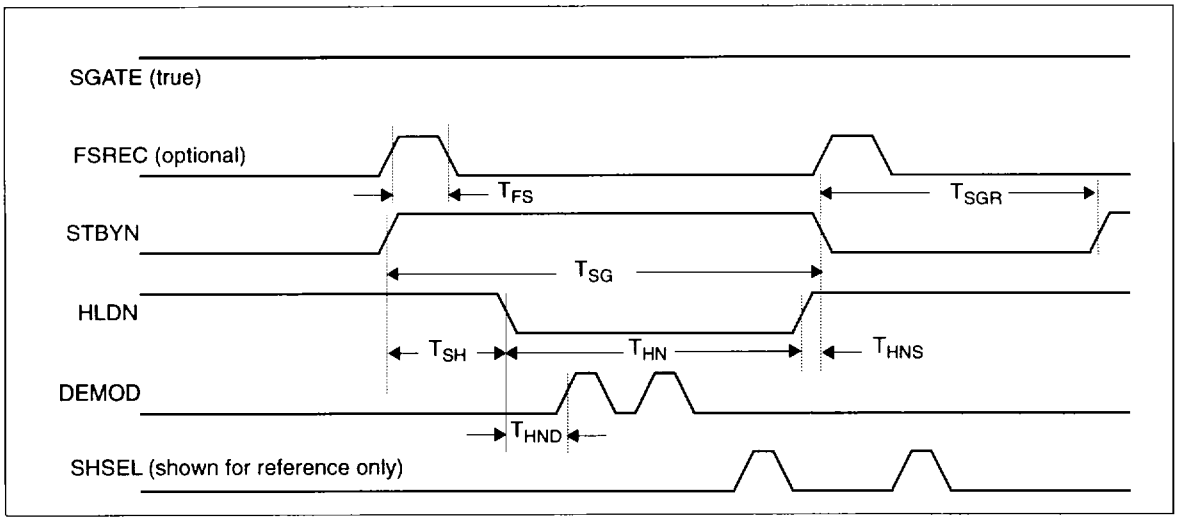


PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
FSREC leading edge to V_{FN} stable	T_{FD}	V_{FN} stable within 10%			2.3	µs
Trailing edge of LOWZ to V_{FN} stable to 10%	T_{WR}	CAGCD value correct			500	ns
Lead, trailing edge SGATE to V_{FN} stable 10%	T_{GS}	CAGCS or D value correct			500	ns

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
LOWZ pulse width	T_{LZ}		1.6			µs
LOWZ to SGATE delay	T_{LZS}		-500			ns
SGATE (or STBYN) pulse width	T_{SG}		5			µs
SGATE (or STBYN) inactive width	T_{SGR}		100			µs
SGATE to LOWZ delay	T_{SGL}		0			ns
HLDN pulse width	T_{HN}		500			ns
HLDN to DEMOD delay	T_{HND}		25			ns
trailing edge of HLDN to SGATE delay	T_{HNS}		0			ns
FSREC pulse width	T_{FSW}		80		250	ns

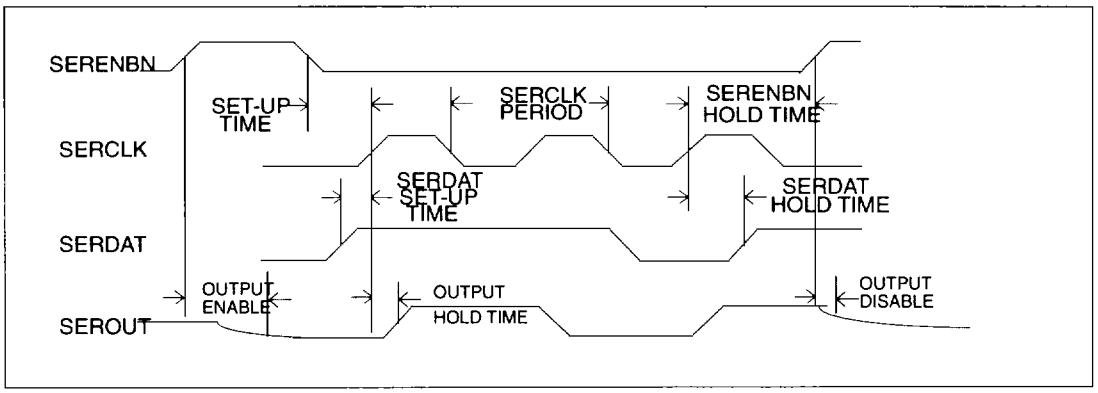
PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
WGATE pulse width (given for reference only)	T_{WG}		1.6			µs
LOWZ extension time	T_{LZE}				500	ns

SYSTEM TIMING DIAGRAM (STANDBY MODE) (Pins: FSREC, SGATE, STBYN, HLDN, DEMOD)



PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
SGATE (or STBYN) pulse width	T_{SG}		5			µs
SGATE (or STBYN) inactive width	T_{SGR}		100			µs
HLDN pulse width	T_{HN}		500			ns
HLDN to DEMOD delay	T_{HND}		25			ns
Trailing edge of HLDN to SGATE delay	T_{HNS}		0			ns
FSREC pulse width	T_{FSW}		100		250	ns
FSREC leading edge to V_{FN} stable	T_{FDT}	V_{FN} stable within 10%			3.8	µs
Lead, trailing edge STBYN to V_{FN} stable 10%	T_{GST}	CAGCS or CAGCD value correct			2	µs

SERIAL INTERFACE DIAGRAM



PARAMETER	*SYM*	*MIN*	*TYP*	*MAX*	*UNITS*
SERENBN pulse width	t_{pwSRE}	200			ns
SERDAT set-up time	t_{sSERD}	20			ns
SERDAT hold time	t_{hSERD}	5			ns
SERENBN set-up time	t_{sSRE}	40			ns
SERENBN hold time	t_{hSRE}	40			ns
SERCLK period	t	50			ns
SERENBN hi to low	t	50			ns
SEROUT enable	t_{OEN}			20	ns
SEROUT disable	t_{ODIS}			30	ns
SEROUT hold time	t_{OUTHLD}	8			ns