

FEATURES

- Controlled Baseline
 - One Assembly/Test Site, One Fabrication Site
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree ⁽¹⁾
- Specified Break-Before-Make Switching
- Low ON-State Resistance (1 Ω)
- Control Inputs Are 5-V Tolerant
- Low Charge Injection
- Excellent ON-State Resistance Matching

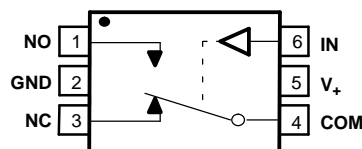
(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- Low Total Harmonic Distortion
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)

APPLICATIONS

- Cell Phones
- PDAs
- Portable Instrumentation

**SOT-23 PACKAGE
(TOP VIEW)**



DESCRIPTION/ORDERING INFORMATION

The TS5A3159-EP is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance and an excellent ON-state resistance matching with the break-before-make feature to prevent signal distortion during the transferring of a signal from one channel to another. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

Summary of Characteristics⁽¹⁾

Configuration	2:1 Multiplexer/ Demultiplexer (1 × SPDT)
Number of channels	1
ON-state resistance (r_{on})	1.1 Ω
ON-state resistance match (Δr_{on})	0.1 Ω
ON-state resistance flatness ($r_{on(Flat)}$)	0.15 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	20 ns/15 ns
Break-before-make time (t_{BBM})	12 ns
Charge injection (Q_C)	36 pC
Bandwidth (BW)	100 MHz
OFF isolation (O_{ISO})	–65 dB at 1 MHz
Crosstalk (X_{TALK})	–66 dB at 1 MHz
Total harmonic distortion (THD)	0.01%
Leakage current ($I_{NO(OFF)}/I_{NC(OFF)}$)	±20 nA
Package option	6-pin DBV

(1) $V_+ = 5\text{ V}$ and $T_A = 25^\circ\text{C}$



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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1-Ω SPDT ANALOG SWITCH

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ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOT (SOT-23) – DBV	Tape and reel	TS5A3159MDBVREP	JA8R

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V ₊	Supply voltage range ⁽²⁾	–0.5	6.5	V
V _{NO} V _{COM}	Analog voltage range ⁽²⁾⁽³⁾⁽⁴⁾	–0.5	V ₊ + 0.5	V
I _{I/O}	Analog port diode current	V _{NO} , V _{COM} < 0 or V _{NO} , V _{COM} > V ₊		±50 mA
I _{NO} I _{COM}	On-state switch current	V _{NO} , V _{COM} = 0 to V ₊		±200 mA
	On-state peak switch current ⁽⁵⁾			±400 mA
V _{IN}	Digital input voltage range ⁽²⁾⁽³⁾	–0.5	6.5	V
I _{IK}	Digital input clamp current	V _{IN} < 0		–50 mA
	Continuous current through V ₊ or GND			±100 mA
θ _{JA}	Package thermal impedance ⁽⁶⁾			165 °C/W
T _{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Electrical Characteristics" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) This value is limited to 5.5 V maximum.
- (5) Pulse at 1-ms duration < 10% duty cycle.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Characteristics for 5-V Supply

$V_+ = 4.5 \text{ V to } 5.5 \text{ V}$ (5 V nominal), $T_A = -55^\circ\text{C to } 125^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
Analog Switch									
Analog signal range	V _{COM} , V _{NC} , V _{NO}					0		V ₊	V
Peak ON resistance	r _{peak}	0 ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = −30 mA,	Switch ON, See Figure 11	25°C	4.5 V	1		1.5	Ω
				Full				1.5	
ON-state resistance	r _{on}	V _{NO} or V _{NC} = 2.5 V, I _{COM} = −30 mA,	Switch ON, See Figure 11	25°C	4.5 V	0.75		1.1	Ω
				Full				1.3	
ON-state resistance match between channels	Δr _{on}	V _{NO} or V _{NC} = 2.5 V, I _{COM} = −30 mA,	Switch ON, See Figure 11	25°C	4.5 V	0.1			Ω
ON-state resistance flatness	r _{on(flat)}	0 ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = −30 mA	Switch ON, See Figure 11	25°C	4.5 V	0.233			Ω
		V _{NO} or V _{NC} = 1 V, 1.5 V, 2.5 V, I _{COM} = −30 mA				0.15			
NC, NO OFF leakage current	I _{NC(OFF)} , I _{NO(OFF)}	V _{NC} or V _{NO} = 4.5 V, V _{COM} = 0,	Switch OFF, See Figure 12	25°C	5.5 V	−6	0.2	4	nA
				Full		−20		60	
NC, NO ON leakage current	I _{NC(ON)} , I _{NO(ON)}	V _{NC} or V _{NO} = 4.5 V, V _{COM} = Open,	Switch ON, See Figure 13	25°C	5.5 V	−6	2.8	4	nA
				Full		−40		70	
COM ON leakage current	I _{COM(ON)}	V _{NC} or V _{NO} = 4.5 V or Open, V _{COM} = 4.5 V,	Switch ON, See Figure 13	25°C	5.5 V	−4	0.47	7	nA
				Full		−40		80	
Digital Control Input (IN)									
Input logic high	V _{IH}			Full		2.4		5.5	V
Input logic low	V _{IL}			Full		0		0.8	V
Input leakage current	I _{IH} , I _{IL}	V _I = 5.5 V or 0		Full	5.5 V	−1		1	μA

(1) $T_A = 25^\circ\text{C}$

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Electrical Characteristics for 5-V Supply (continued)

$V_+ = 4.5 \text{ V to } 5.5 \text{ V}$ (5 V nominal), $T_A = -55^\circ\text{C to } 125^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
Dynamic									
Turn-on time	t _{ON}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 15	25°C	4.5 V to 5.5 V	20	35		ns
				Full		40			
Turn-off time	t _{OFF}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 15	25°C	4.5 V to 5.5 V	15	20		ns
				Full		35			
Break-before-make time	t _{BBM}	V _{NC} = V _{NO} = V ₊ /2, R _L = 50 Ω,	C _L = 35 pF, See Figure 16	25°C	4.5 V to 5.5 V	1	12	14.5	ns
				Full		1			
Charge injection	Q _C	C _L = 1 nF, V _{GEN} = 0 V,	See Figure 20	25°C	5 V	36			pC
NC, NO OFF capacitance	C _{NC(OFF)} , C _{NO(OFF)}	V _{NC} or V _{NO} = V ₊ or GND, Switch OFF,	See Figure 14	25°C	5 V	23			pF
NC, NO ON capacitance	C _{NC(ON)} , C _{NO(ON)}	V _{NC} or V _{NO} = V ₊ or GND, Switch ON,	See Figure 14	25°C	5 V	84			pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND, Switch ON,	See Figure 14	25°C	5 V	84			pF
Digital input capacitance	C _{IN}	V _{IN} = V ₊ or GND,	See Figure 14	25°C	5 V	2.1			pF
Bandwidth	BW	R _L = 50 Ω, Switch ON,	See Figure 17	25°C	5 V	100			MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 18	25°C	5 V	−65			dB
Crosstalk	X _{TALK}	R _L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 19	25°C	5 V	−65			dB
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF,	f = 600 Hz to 20 kHz, See Figure 21	25°C	5 V	0.01			%
Supply									
Positive supply current	I ₊	V _{IN} = V ₊ or GND,	Switch ON or OFF	Full	5.5 V	0.1			μA

Electrical Characteristics for 3.3-V Supply

$V_+ = 3\text{ V}$ to 3.6 V (3.3 V nominal), $T_A = -55^\circ\text{C}$ to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
Analog Switch									
Analog signal range	V _{COM} , V _{NC} , V _{NO}					0		V ₊	V
Peak ON resistance	r _{peak}	0 ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = −24 mA,	Switch ON, See Figure 11	25°C Full	3 V	1.35	2.15	2.15	Ω
ON-state resistance	r _{on}	V _{NO} or V _{NC} = 2 V, I _{COM} = −24 mA,	Switch ON, See Figure 11	25°C Full	3 V	1.15	1.7	1.7	Ω
ON-state resistance match between channels	Δr _{on}	V _{NO} or V _{NC} = 2 V, 0.8 V, I _{COM} = −24 mA,	Switch ON, See Figure 11	25°C	3 V	0.11			Ω
ON-state resistance flatness	r _{on(flat)}	0 ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = −24 mA V _{NO} or V _{NC} = 2 V, 0.8 V, I _{COM} = −24 mA	Switch ON, See Figure 11	25°C	3 V	0.225 0.25			Ω
NC, NO OFF leakage current	I _{NC(OFF)} , I _{NO(OFF)}	V _{NC} or V _{NO} = 3 V, V _{COM} = 0,	Switch OFF, See Figure 12	25°C	3.6 V	0.2			nA
NC, NO ON leakage current	I _{NC(ON)} , I _{NO(ON)}	V _{NC} or V _{NO} = 3 V, V _{COM} = Open,	Switch ON, See Figure 13	25°C	3.6 V	2.8			nA
COM ON leakage current	I _{COM(ON)}	V _{NC} or V _{NO} = 3 V or Open, V _{COM} = 3 V,	Switch ON, See Figure 13	25°C	3.6 V	0.47			nA
Digital Control Input (IN)									
Input logic high	V _{IH}			Full		2		5.5	V
Input logic low	V _{IL}			Full		0	0.6		V
Input leakage current	I _{IH} , I _{IL}	V _I = 5.5 V or 0		Full	3.6 V	−1		1	μA

(1) $T_A = 25^\circ\text{C}$

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Electrical Characteristics for 3.3-V Supply (continued)

$V_+ = 3\text{ V to }3.6\text{ V}$ (3.3 V nominal), $T_A = -55^\circ\text{C to }125^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
Dynamic									
Turn-on time	t _{ON}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 15	25°C	3 V to	30	40		ns
				Full	3.6 V	55			
Turn-off time	t _{OFF}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 15	25°C	3 V to	20	25		ns
				Full	3.6 V	40			
Break-before-make time	t _{BBM}	V _{NC} = V _{NO} = V ₊ /2, R _L = 50 Ω,	C _L = 35 pF, See Figure 16	25°C	3 V to	1	21	29	ns
				Full	3.6 V	1			
Charge injection	Q _C	C _L = 1 nF, V _{GEN} = 0 V,	See Figure 20	25°C	3.3 V	20			pC
NC, NO OFF capacitance	C _{NC(OFF)} , C _{NO(OFF)}	V _{NC} or V _{NO} = V ₊ or GND, Switch OFF,	See Figure 14	25°C	3.3 V	23			pF
NC, NO ON capacitance	C _{NC(ON)} , C _{NO(ON)}	V _{NC} or V _{NO} = V ₊ or GND, Switch ON,	See Figure 14	25°C	3.3 V	84			pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND, Switch ON,	See Figure 14	25°C	3.3 V	84			pF
Digital input capacitance	C _{IN}	V _{IN} = V ₊ or GND,	See Figure 14	25°C	3.3 V	2.1			pF
Bandwidth	BW	R _L = 50 Ω, Switch ON,	See Figure 17	25°C	3.3 V	100			MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 18	25°C	3.3 V	−65			dB
Crosstalk	X _{TALK}	R _L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 19	25°C	3.3 V	−65			dB
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF,	f = 600 Hz to 20 kHz, See Figure 21	25°C	3.3 V	0.015			%
Supply									
Positive supply current	I ₊	V _{IN} = V ₊ or GND,	Switch ON or OFF	Full	3.6 V	0.1			μA

Electrical Characteristics for 2.5-V Supply

$V_+ = 2.3 \text{ V}$ to 2.7 V (2.5 V nominal), $T_A = -55^\circ\text{C}$ to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
Analog Switch									
Analog signal range	V _{COM} , V _{NC} , V _{NO}					0		V ₊	V
Peak ON resistance	r _{peak}	0 ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = −8 mA,	Switch ON, See Figure 11	25°C Full	2.5 V	1.7	2.7	2.9	Ω
ON-state resistance	r _{on}	V _{NO} or V _{NC} = 1.8 V, I _{COM} = −8 mA,	Switch ON, See Figure 11	25°C Full	2.5 V	1.45	2.3	2.5	Ω
ON-state resistance match between channels	Δr _{on}	V _{NO} or V _{NC} = 0.8 V, 1.8 V, I _{COM} = −8 mA,	Switch ON, See Figure 11	25°C	2.5 V	0.7			Ω
ON-state resistance flatness	r _{on(flat)}	0 ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = −8 mA V _{NO} or V _{NC} = 0.8 V, 1.8 V, I _{COM} = −8 mA	Switch ON, See Figure 11	25°C	2.5 V	0.5	0.45		Ω
NC, NO OFF leakage current	I _{NC(OFF)} , I _{NO(OFF)}	V _{NC} or V _{NO} = 2.3 V, V _{COM} = 0,	Switch OFF, See Figure 12	25°C	2.7 V	0.2			nA
NC, NO ON leakage current	I _{NC(ON)} , I _{NO(ON)}	V _{NC} or V _{NO} = 2.3 V, V _{COM} = Open,	Switch ON, See Figure 13	25°C	2.7 V	2.8			nA
COM ON leakage current	I _{COM(ON)}	V _{NC} or V _{NO} = 2.3 V or Open, V _{COM} = 2.3 V,	Switch ON, See Figure 13	25°C	2.7 V	0.47			nA
Digital Control Input (IN)									
Input logic high	V _{IH}			Full		1.8		5.5	V
Input logic low	V _{IL}			Full		0	0.6		V
Input leakage current	I _{IH} , I _{IL}	V _I = 5.5 V or 0		Full	2.7 V	−1		1	μA

(1) $T_A = 25^\circ\text{C}$

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Electrical Characteristics for 2.5-V Supply (continued)

$V_+ = 2.3 \text{ V to } 2.7 \text{ V}$ (2.5 V nominal), $T_A = -55^\circ\text{C to } 125^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
Dynamic									
Turn-on time	t _{ON}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 15	25°C	2.3 V to	40	55		ns
				Full	2.7 V	70			
Turn-off time	t _{OFF}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 15	25°C	2.3 V to	30	40		ns
				Full	2.7 V	55			
Break-before-make time	t _{BBM}	V _{NC} = V _{NO} = V ₊ /2, R _L = 50 Ω,	C _L = 35 pF, See Figure 16	25°C	2.3 V to	1	33	39	ns
				Full	2.7 V	1			
Charge injection	Q _C	C _L = 1 nF, V _{GEN} = 0 V,	See Figure 20	25°C	2.5 V	13			pC
NC, NO OFF capacitance	C _{NC(OFF)} , C _{NO(OFF)}	V _{NC} or V _{NO} = V ₊ or GND, Switch OFF,	See Figure 14	25°C	2.5 V	23			pF
NC, NO ON capacitance	C _{NC(ON)} , C _{NO(ON)}	V _{NC} or V _{NO} = V ₊ or GND, Switch ON,	See Figure 14	25°C	2.5 V	84			pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND, Switch ON,	See Figure 14	25°C	2.5 V	84			pF
Digital input capacitance	C _{IN}	V _{IN} = V ₊ or GND,	See Figure 14	25°C	2.5 V	2.1			pF
Bandwidth	BW	R _L = 50 Ω, Switch ON,	See Figure 17	25°C	2.5 V	100			MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 18	25°C	2.5 V	−64			dB
Crosstalk	X _{TALK}	R _L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 19	25°C	2.5 V	−64			dB
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF,	f = 600 Hz to 20 kHz, See Figure 21	25°C	2.5 V	0.025			%
Supply									
Positive supply current	I ₊	V _{IN} = V ₊ or GND,	Switch ON or OFF	Full	2.7 V	0.1			μA

Electrical Characteristics for 1.8-V Supply

$V_+ = 1.65\text{ V}$ to 1.95 V (1.8 V nominal), $T_A = -55^\circ\text{C}$ to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
Analog Switch									
Analog signal range	V _{COM} , V _{NC} , V _{NO}					0		V ₊	V
Peak ON resistance	r _{peak}	0 ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = −2 mA,	Switch ON, See Figure 11	25°C	1.8 V	4	4.9	Ω	
				Full		7			
ON-state resistance	r _{on}	V _{NO} or V _{NC} = 1.5 V, I _{COM} = −2 mA,	Switch ON, See Figure 11	25°C	1.8 V	1.7	3.2	Ω	
				Full		4.2			
ON-state resistance match between channels	Δr _{on}	V _{NO} or V _{NC} = 0.6 V, 1.5 V, I _{COM} = −2 mA,	Switch ON, See Figure 11	25°C	1.8 V	0.7		Ω	
				Full		0.7			
ON-state resistance flatness	r _{on(flat)}	0 ≤ V _{NO} or V _{NC} ≤ V ₊ , I _{COM} = −2 mA	Switch ON, See Figure 11	25°C	1.8 V	1.85		Ω	
				Full		1.85			
		V _{NO} or V _{NC} = 0.6 V, 1.5 V, I _{COM} = −2 mA		25°C		0.9			
				Full		0.9			
NC, NO OFF leakage current	I _{NC(OFF)} , I _{NO(OFF)}	V _{NC} or V _{NO} = 1.65 V, V _{COM} = 0,	Switch OFF, See Figure 12	25°C	1.95 V	0.2		nA	
NC, NO ON leakage current	I _{NC(ON)} , I _{NO(ON)}	V _{NC} or V _{NO} = 1.65 V, V _{COM} = Open,	Switch ON, See Figure 13	25°C	1.95 V	2.8		nA	
COM ON leakage current	I _{COM(ON)}	V _{NC} or V _{NO} = 1.65 V or Open, V _{COM} = 1.65 V,	Switch ON, See Figure 13	25°C	1.95 V	0.47		nA	
Digital Control Input (IN)									
Input logic high	V _{IH}			Full		1.5		5.5	V
Input logic low	V _{IL}			Full		0	0.6		V
Input leakage current	I _{IH} , I _{IL}	V _I = 5.5 V or 0		Full	1.95 V	−1		1	μA

(1) $T_A = 25^\circ\text{C}$

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Electrical Characteristics for 1.8-V Supply (continued)

$V_+ = 1.65\text{ V to }1.95\text{ V}$ (1.8 V nominal), $T_A = -55^\circ\text{C to }125^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP ⁽¹⁾	MAX	UNIT
Dynamic									
Turn-on time	t _{ON}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 15	25°C	1.65 V to	65	70	ns	
				Full	1.95 V	95			
Turn-off time	t _{OFF}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 15	25°C	1.65 V to	40	55	ns	
				Full	1.95 V	70			
Break-before-make time	t _{BBM}	V _{NC} = V _{NO} = V ₊ /2, R _L = 50 Ω,	C _L = 35 pF, See Figure 16	25°C	1.65 V to	1	60	72	ns
				Full	1.95 V	0.5			
Charge injection	Q _C	C _L = 1 nF, V _{GEN} = 0 V,	See Figure 20	25°C	1.8 V	13			pC
NC, NO OFF capacitance	C _{NC(OFF)} , C _{NO(OFF)}	V _{NC} or V _{NO} = V ₊ or GND, Switch OFF,	See Figure 14	25°C	1.8 V	23			pF
NC, NO ON capacitance	C _{NC(ON)} , C _{NO(ON)}	V _{NC} or V _{NO} = V ₊ or GND, Switch ON,	See Figure 14	25°C	1.8 V	84			pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND, Switch ON,	See Figure 14	25°C	1.8 V	84			pF
Digital input capacitance	C _{IN}	V _{IN} = V ₊ or GND,	See Figure 14	25°C	1.8 V	2.1			pF
Bandwidth	BW	R _L = 50 Ω, Switch ON,	See Figure 17	25°C	1.8 V	100			MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 18	25°C	1.8 V	−63			dB
Crosstalk	X _{TALK}	R _L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 19	25°C	1.8 V	−63			dB
Supply									
Positive supply current	I ₊	V _{IN} = V ₊ or GND,	Switch ON or OFF	Full	1.95 V	0.1			μA

TYPICAL PERFORMANCE

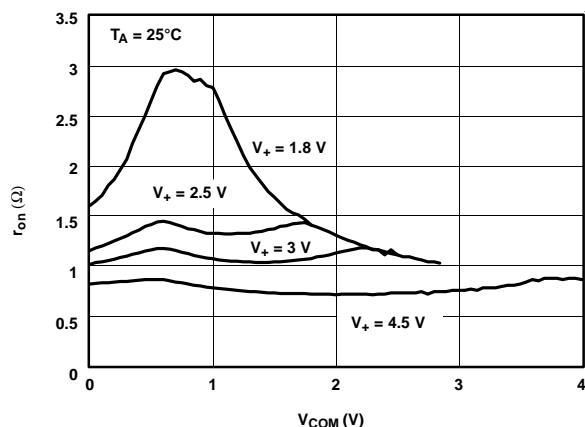


Figure 1. r_{on} vs V_{COM}

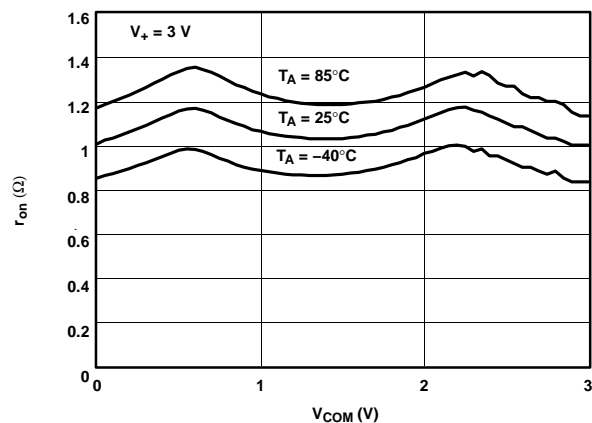


Figure 2. r_{on} vs V_{COM}

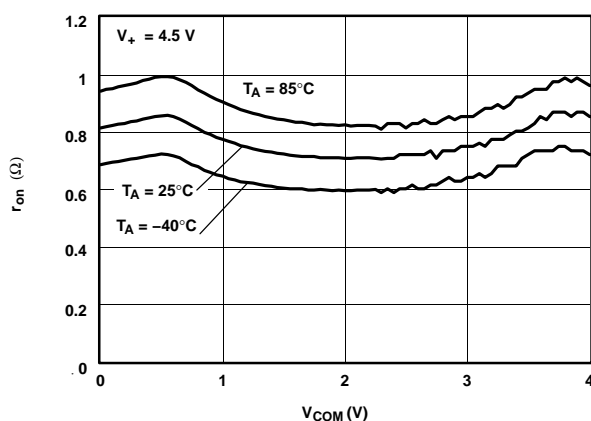


Figure 3. r_{on} vs V_{COM}

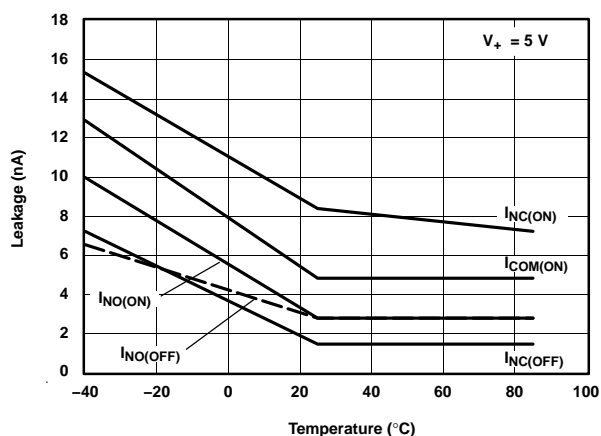


Figure 4. Leakage Current vs Temperature

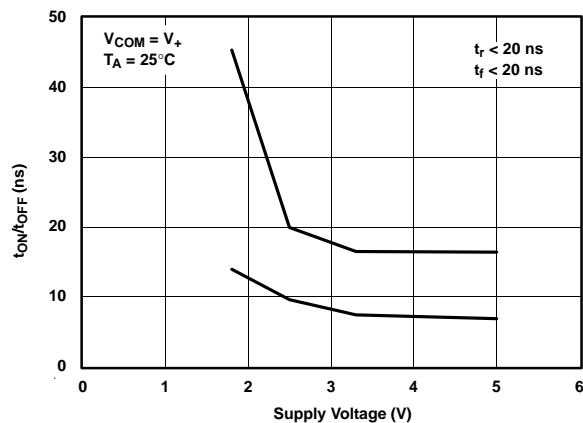


Figure 5. t_{ON}/t_{OFF} vs V_+

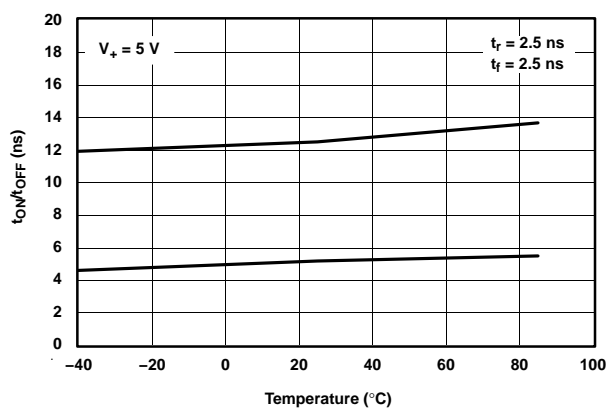


Figure 6. t_{ON}/t_{OFF} vs Temperature

TYPICAL PERFORMANCE (continued)

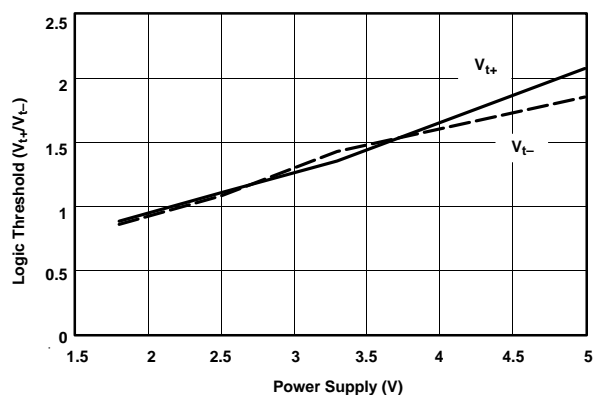


Figure 7. Logic Threshold vs Power Supply

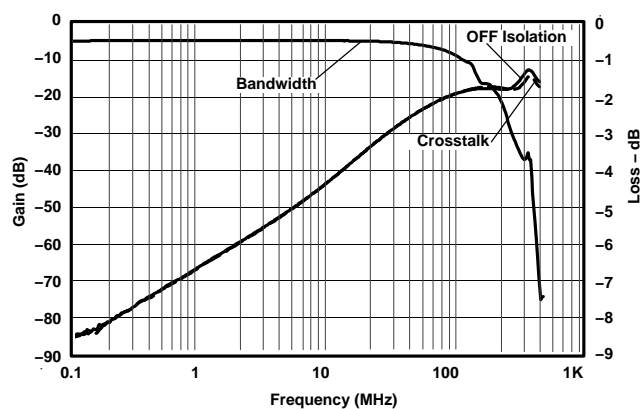


Figure 8. Frequency Response

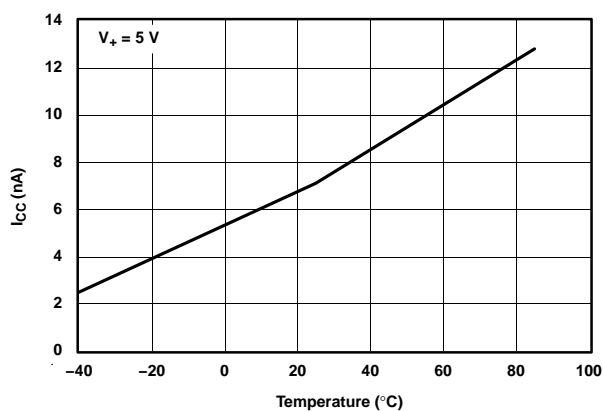


Figure 9. Power-Supply Current vs Temperature

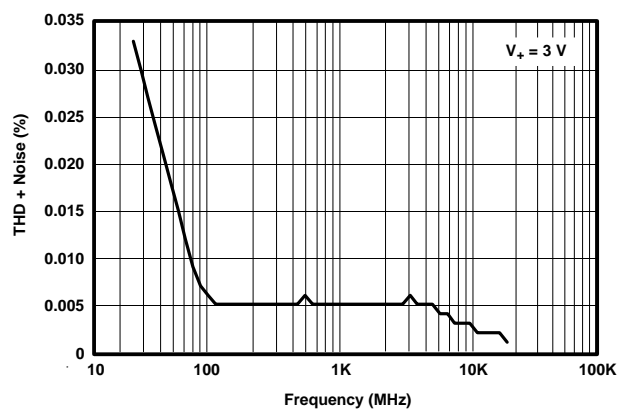


Figure 10. Total Harmonic Distortion (THD) vs Frequency

PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
1	NO	Normally open
2	GND	Digital ground
3	NC	Normally closed
4	COM	Common
5	V ₊	Power supply
6	IN	Digital control to connect COM to NO or NC

PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V _{COM}	Voltage at COM
V _{NC}	Voltage at NC
V _{NO}	Voltage at NO
r _{on}	Resistance between COM and NO ports when the channel is ON
r _{peak}	Peak on-state resistance over a specified voltage range
Δr _{on}	Difference of r _{on} between channels in a specific device
r _{on(flat)}	Difference between the maximum and minimum value of r _{on} in a channel over the specified range of conditions
I _{NC(OFF)}	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
I _{NO(OFF)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
I _{NC(ON)}	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
I _{NO(ON)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
I _{COM(ON)}	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the ON state and the output (NO) open
V _{IH}	Minimum input voltage for logic high for the control input (IN)
V _{IL}	Maximum input voltage for logic low for the control input (IN)
V _{IN}	Voltage at IN
I _{IH} , I _{IL}	Leakage current measured at IN
t _{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t _{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
t _{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO), when the control signal changes state.
Q _C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, Q _C = C _L × ΔV _{COM} , C _L is the load capacitance and ΔV _{COM} is the change in analog output voltage.
C _{NC(OFF)}	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
C _{NO(OFF)}	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
C _{NC(ON)}	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
C _{NO(ON)}	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
C _{COM(ON)}	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
C _{IN}	Capacitance of IN
O _{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NO to COM) in the OFF state.
X _{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an adjacent ON channel (NC1 to NC2). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.

TS5A3159-EP
1-Ω SPDT ANALOG SWITCH

SCDS217B–DECEMBER 2005–REVISED JANUARY 2006

PARAMETER DESCRIPTION (continued)

SYMBOL	DESCRIPTION
I_+	Static power-supply current with the control (IN) pin at V_+ or GND
ΔI_+	This is the increase in I_+ for each control (IN) input that is at the specified voltage, rather than at V_+ or GND.

PARAMETER MEASUREMENT INFORMATION

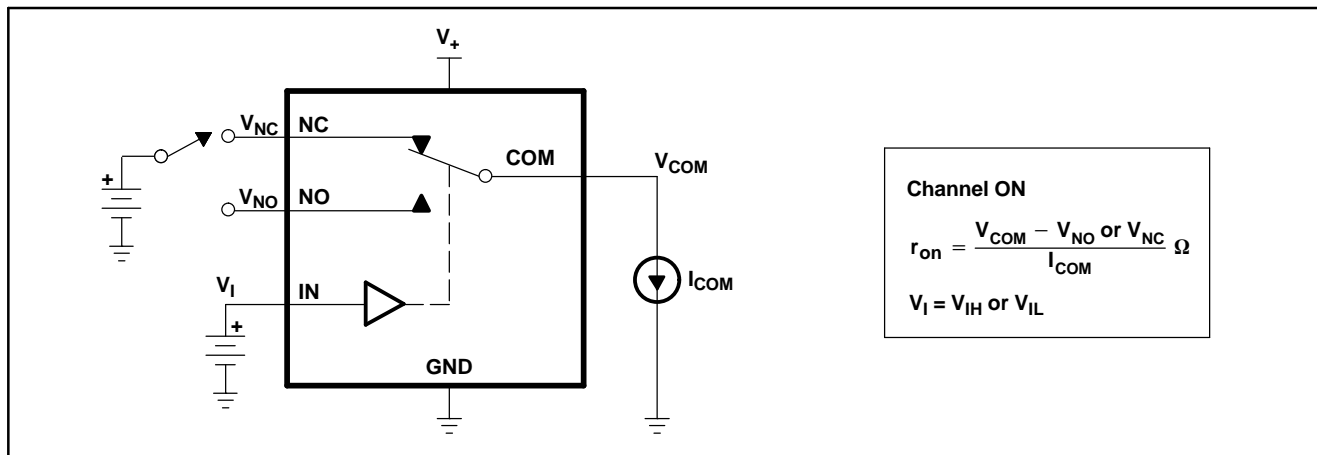


Figure 11. ON-State Resistance (r_{on})

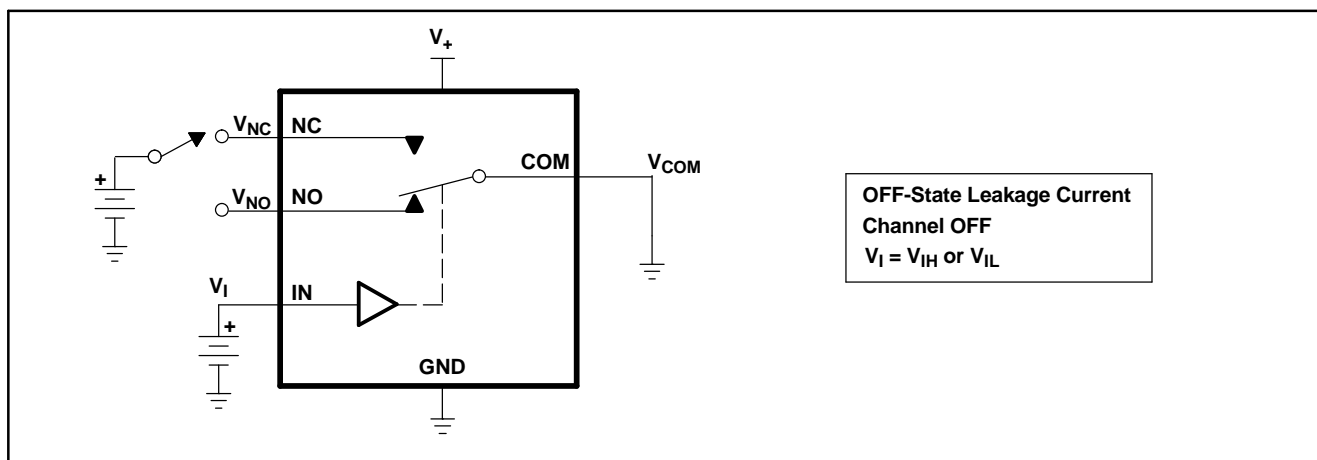


Figure 12. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NO(OFF)}$)

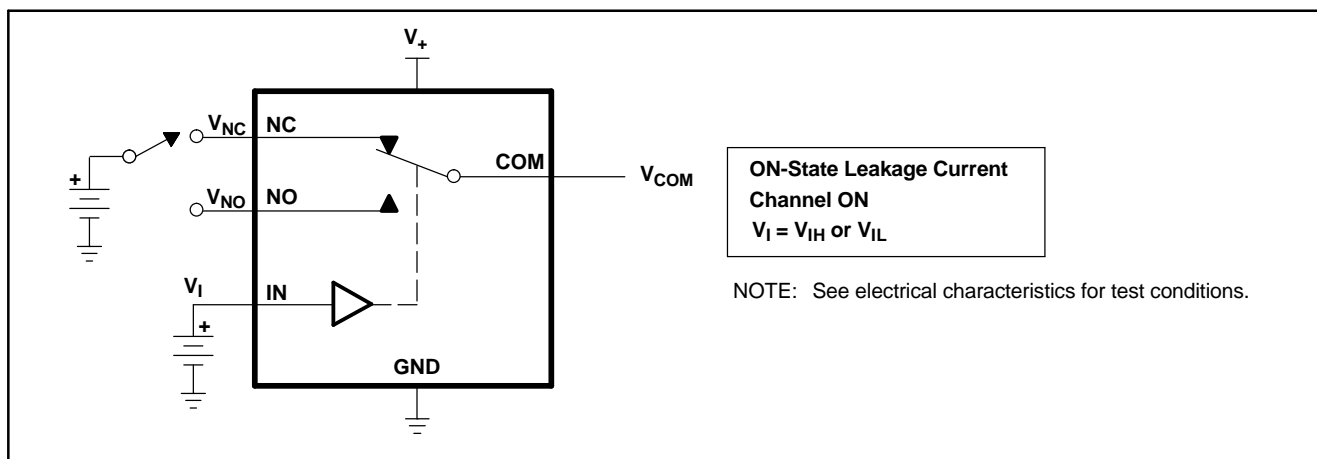


Figure 13. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

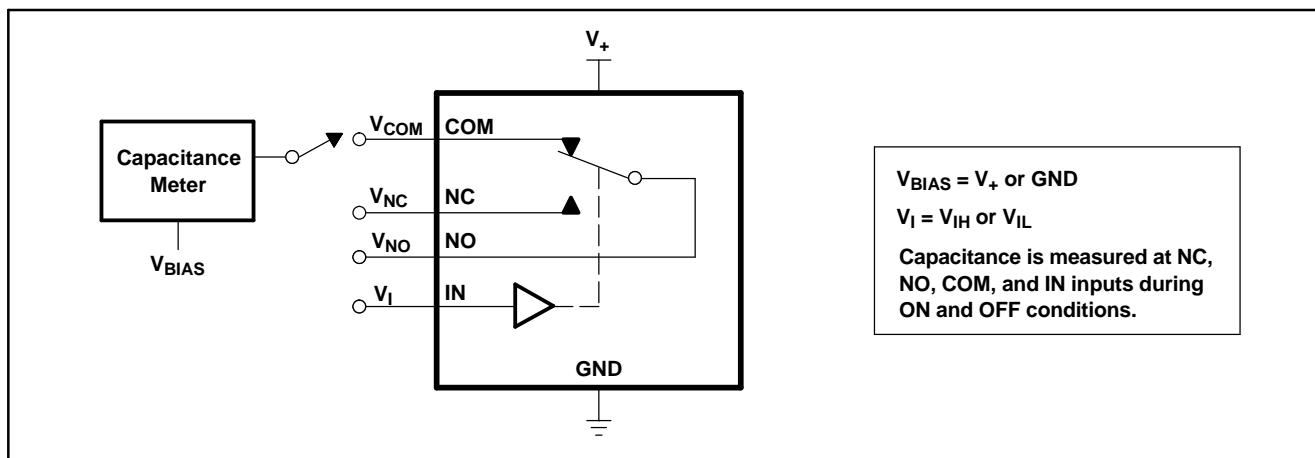
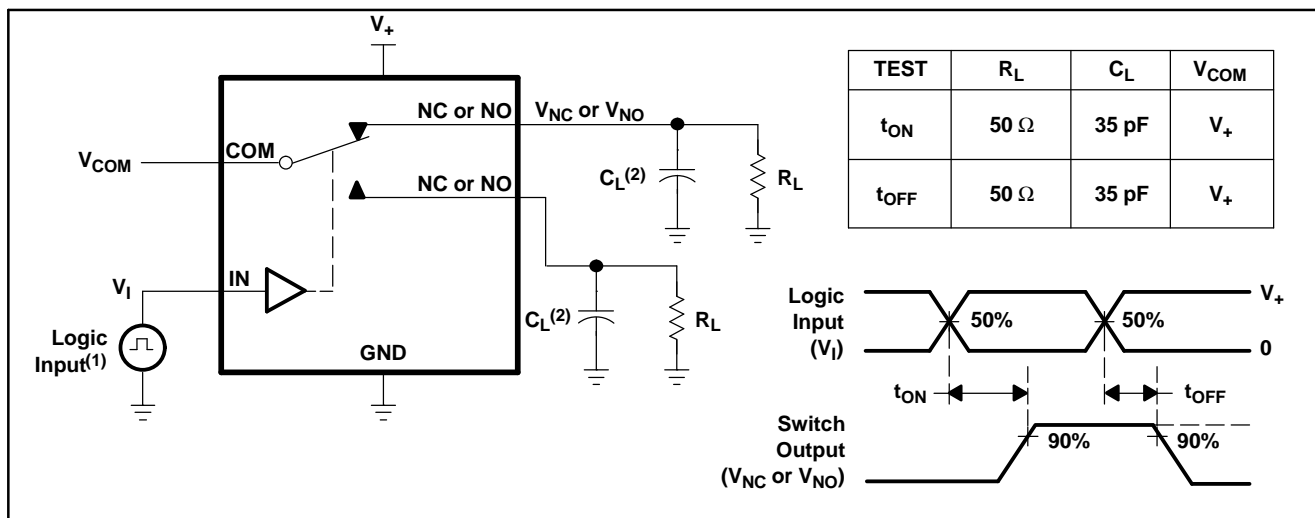


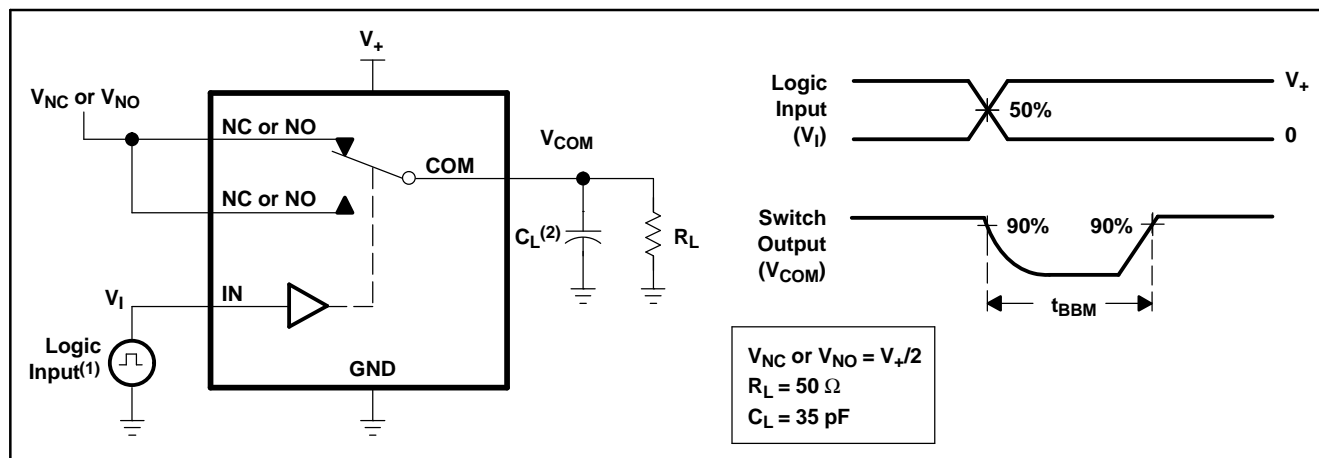
Figure 14. Capacitance (C_I , $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



- (1) All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r < 5 \text{ ns}$, $t_f < 5 \text{ ns}$.
- (2) C_L includes probe and jig capacitance.

Figure 15. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

PARAMETER MEASUREMENT INFORMATION (continued)



- (1) All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\ \text{MHz}$, $Z_O = 50\ \Omega$, $t_r < 5\ \text{ns}$, $t_f < 5\ \text{ns}$.
- (2) C_L includes probe and jig capacitance.

Figure 16. Break-Before-Make Time (t_{BBM})

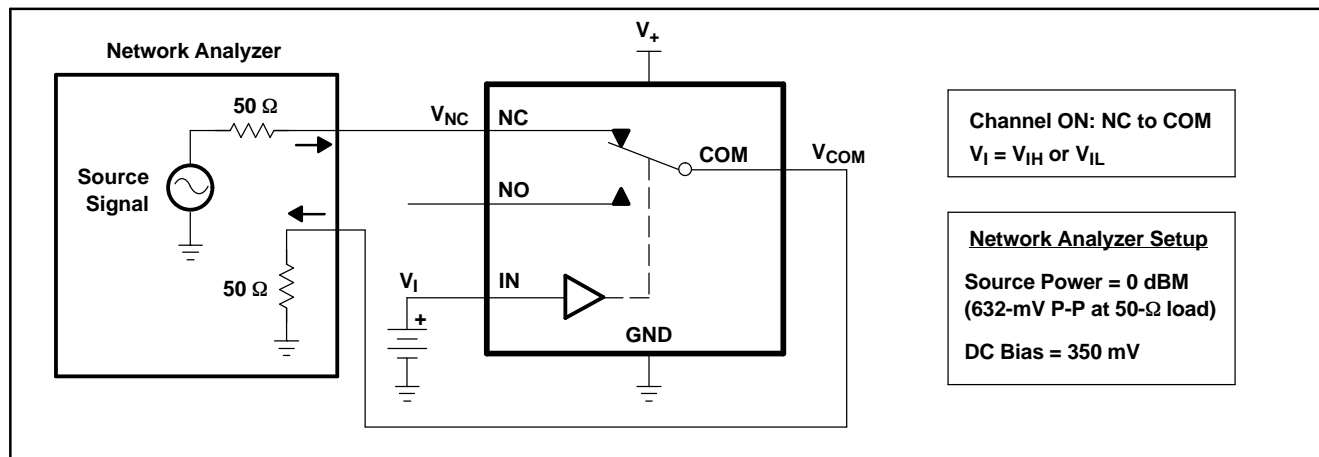


Figure 17. Bandwidth (BW)

PARAMETER MEASUREMENT INFORMATION (continued)

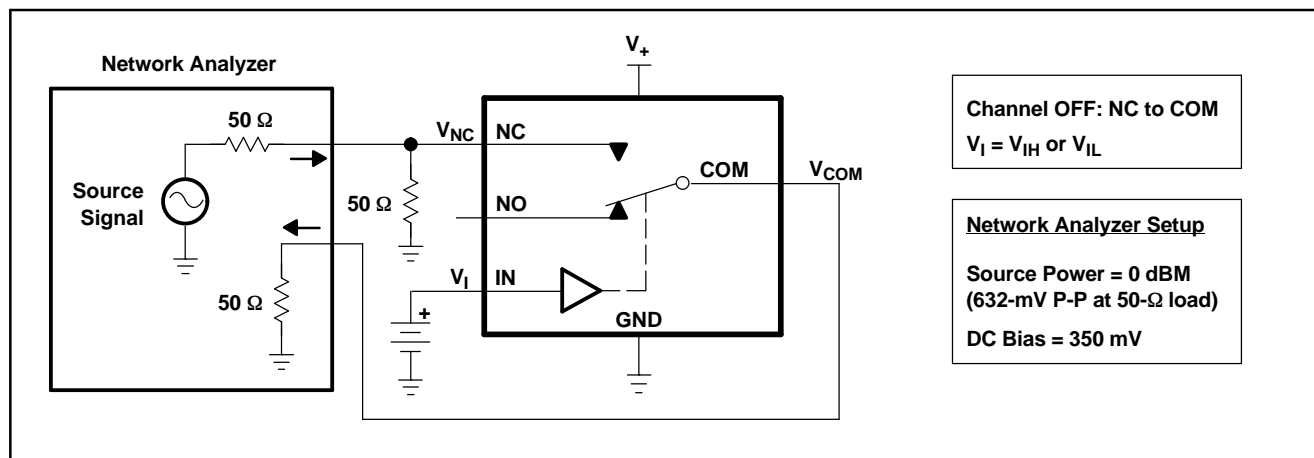


Figure 18. OFF Isolation (O_{ISO})

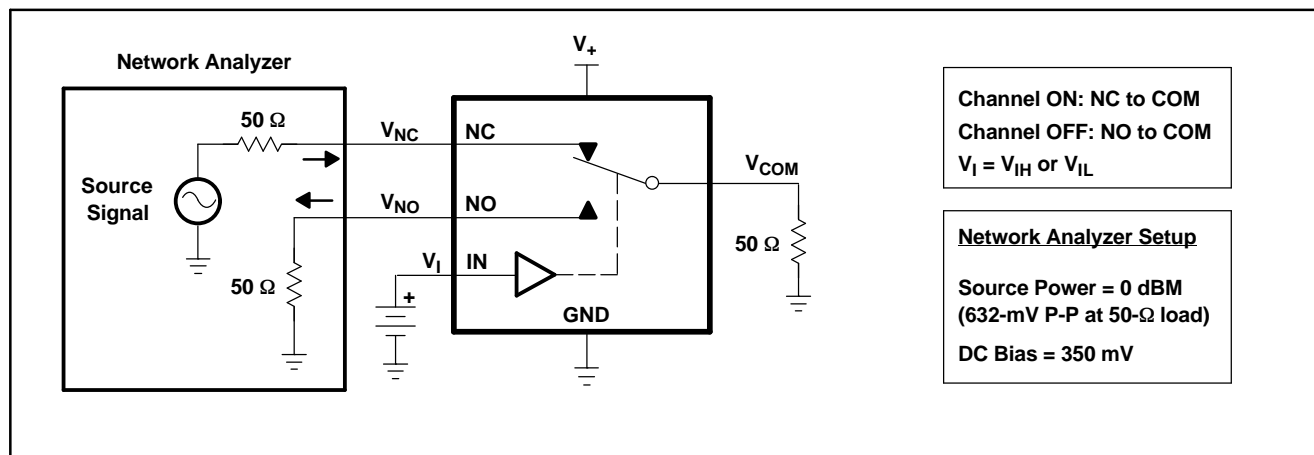
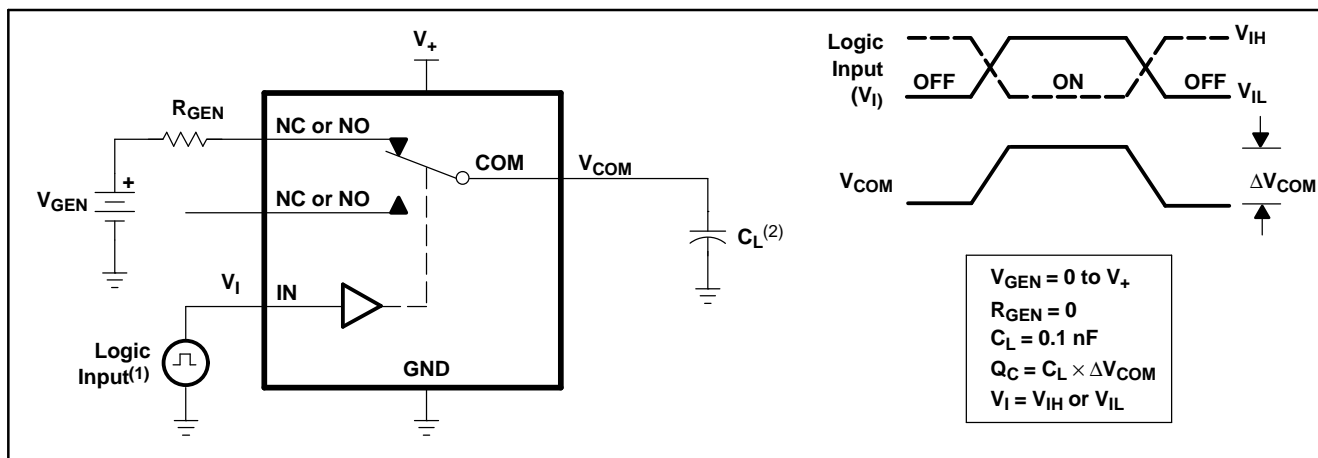


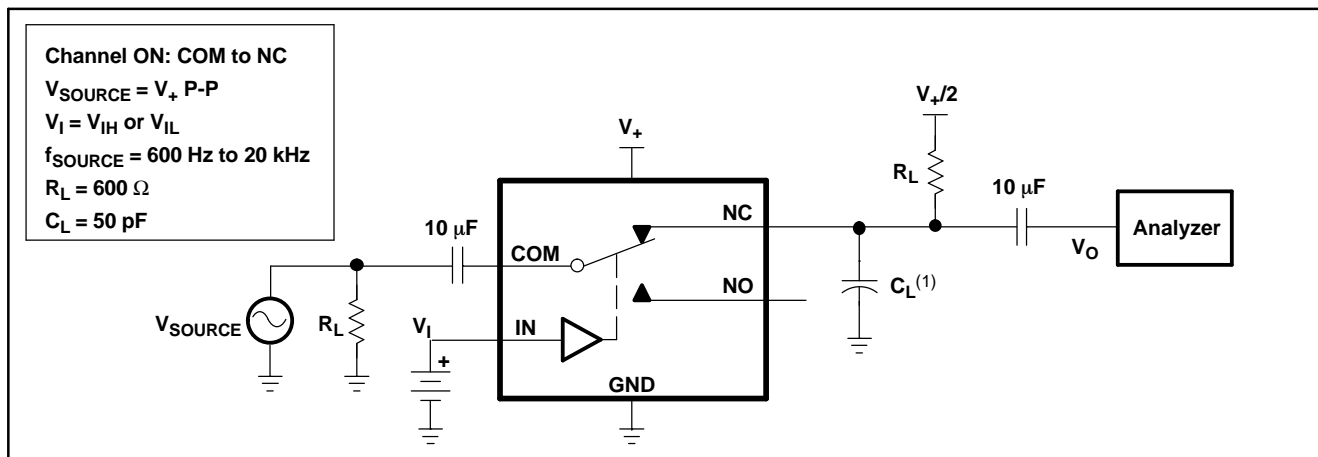
Figure 19. Crosstalk (X_{TALK})

PARAMETER MEASUREMENT INFORMATION (continued)



- (1) All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.
(2) C_L includes probe and jig capacitance.

Figure 20. Charge Injection (Q_C)



- (1) C_L includes probe and jig capacitance.

Figure 21. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A3159MDBVREP	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	JA8R	Samples
V62/06613-01XE	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	JA8R	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TS5A3159-EP :

- Catalog: [TS5A3159](#)
- Automotive: [TS5A3159-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3159MDBVREP	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

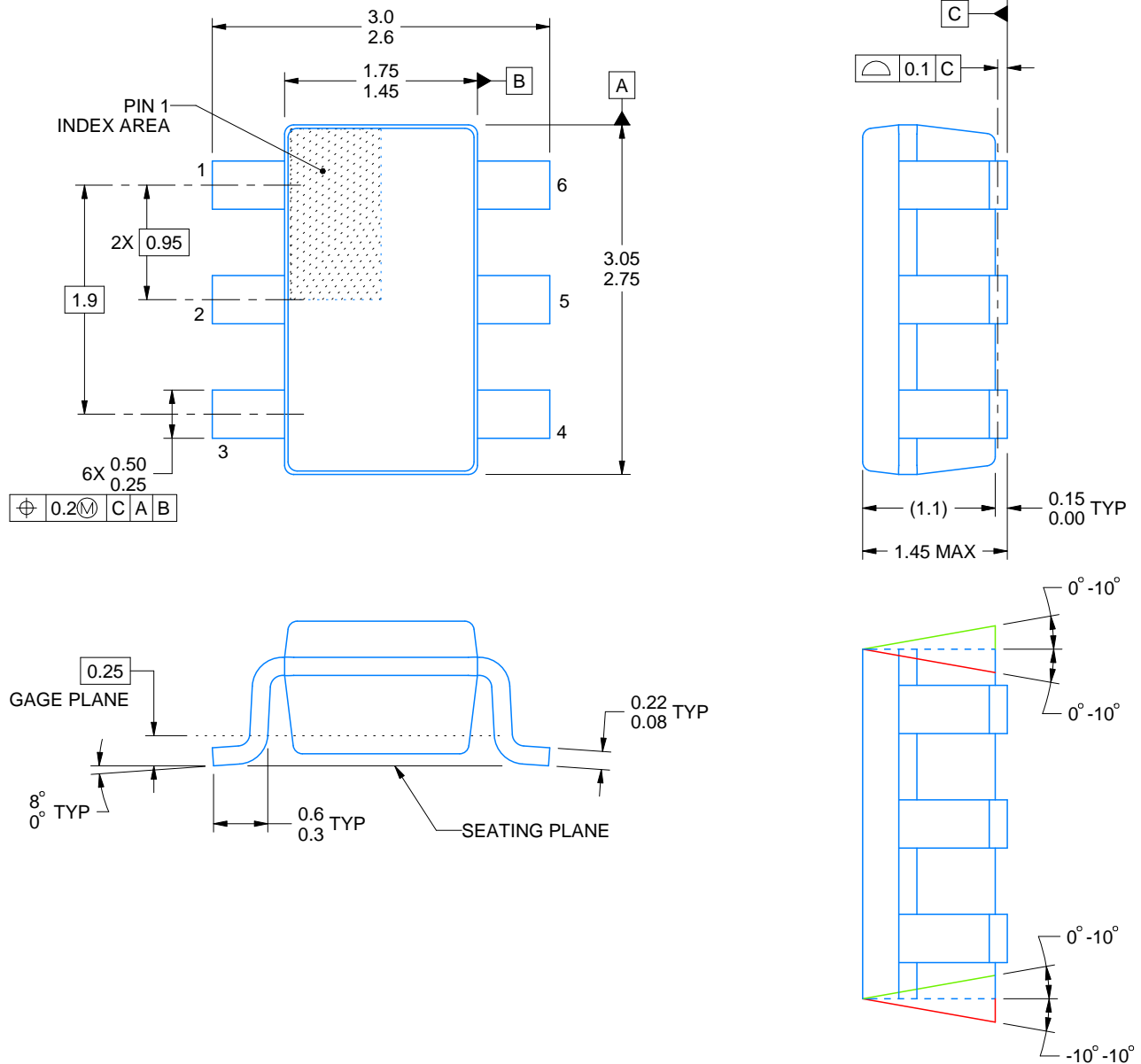


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3159MDBVREP	SOT-23	DBV	6	3000	202.0	201.0	28.0

DBV0006A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

4214840/D 09/2023

NOTES:

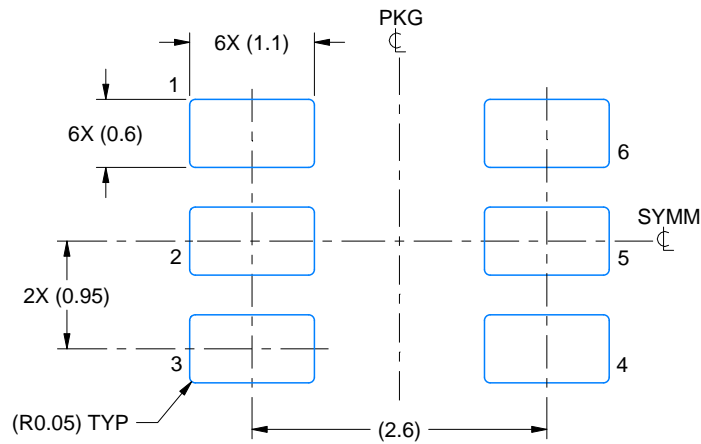
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

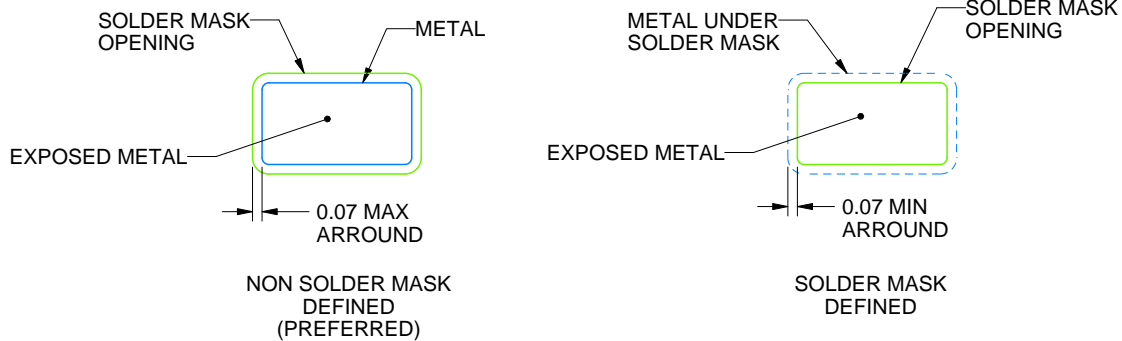
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/D 09/2023

NOTES: (continued)

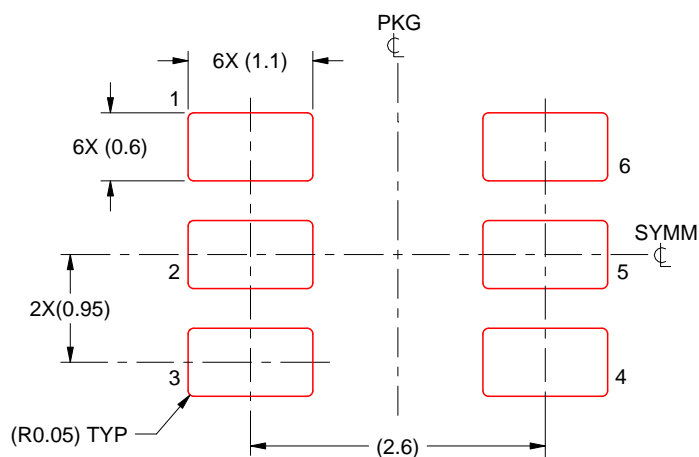
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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