3091-1.3 November 1991

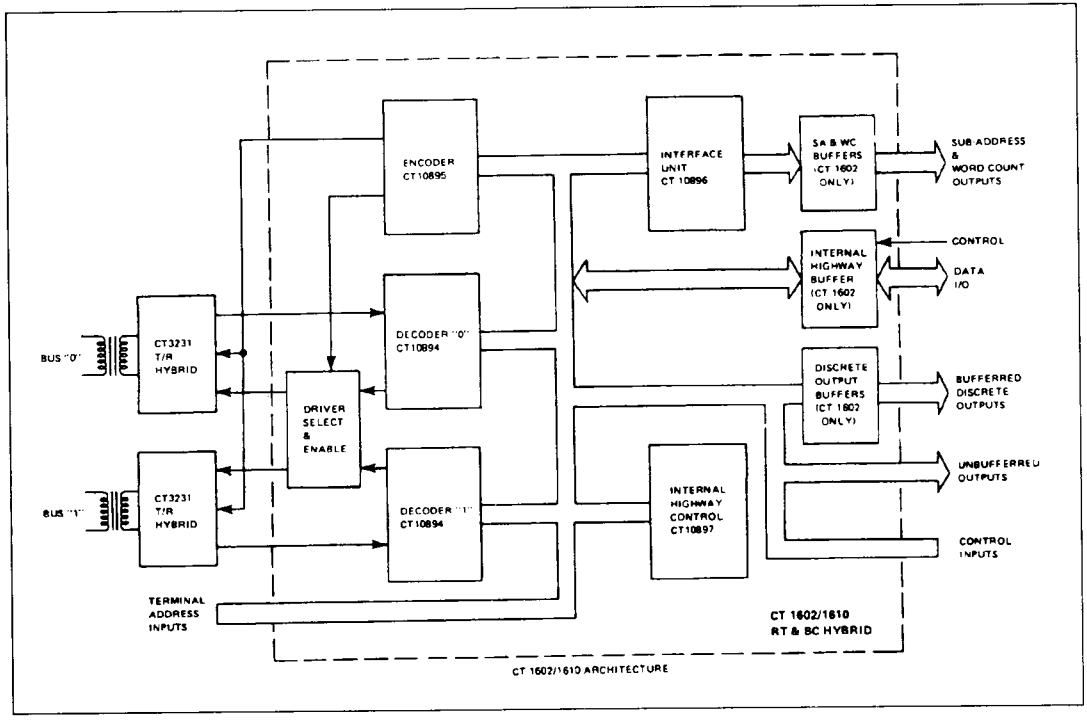
CT1602/10

MIL-STD-1553B REMOTE TERMINAL, BUS CONTROLLER OR PASSIVE MONITOR HYBRIDS

The CT1602/CT1610 design incorporates five LSI chips that accomplish the dual redundant MIL-STD1553B Remote Terminal and/or Bus Controller Protocol Functions. Buffering has been added to the most commonly used output signals on the CT1602, minimizing external hardware requirements. The CT1610 contains no buffers resulting in very low power consumption. The CT1602/CT1610 connects directly to all GPS Driver/Receiver Units.

FEATURES

- Performs the complete dual-redundant Remote Terminal and Bus Controller Protocol Functions of MIL-STD-1553B
- Automatic switchover to superseding input commands
- Screened to applicable portions of MIL-STD-883 Level B
- 750 mW power consumption CT1602
  125 mW power consumption CT1610
- Small Size
- Available in plug-in or flatpack configuration
- Compatible with all GPS Driver/Receiver Units
- 5V DC operation
- -55° to +125°C operation



CT 1602/1610 ARCHITECTURE

REMOTE TERMINAL OPERATION

Receive Data Operation

All valid data words associated with a valid receive data command word for the RT are passed to the subsystem. The RT examines all command words from the bus and will respond to valid (i.e. correct Manchester, parity coding etc.) commands which have the correct RT address (or broadcast address if the RT broadcast option is enabled). When the data words are received, they are decoded and checked by the RT and, if valid, passed to the subsystem on a word by word basis at 20 us intervals. This applies to receive data words in both Bus Controller to RT and RT to RT messages. When the RT detects that the message has finished, it checks that the correct number of words have been received and if the message is fully valid, then a Good Block Received signal is sent to the subsystem, which must be used by the subsystem as permission to use the data just received.

The subsystem must therefore have a temporary buffer store up to 32 words long into which these data words can be placed. The Good Block Received signal will allow use of the buffer store data once the message has been validated.

If a block of data is not validated, then Good Block Received will not be generated. This may be caused by any sort of message error or by a new valid command for the RT being received on another bus to which the RT must switch.

Transmit Data Operation

If the RT receives a valid transmit data command addressed to the RT, then the RT will request the data words from the subsystem for transmission on a word by word basis. To allow maximum time for the subsystem to collect each data word, the next word is requested by the RT as soon as the transmission of the current word has commenced.

It is essential that the subsystem should provide all the data words requested by the RT once a transmit sequence has been accepted. Failure to do so will be classed by the RT as a subsystem failure and reported as such to the Bus Controller.

Control of Data Transfers

This section describes the detailed operation of the data transfer mechanism between RT and subsystems. It covers the operations of the signals $\overline{DTRQ}$, $\overline{DTAK}$, IUSTB, H/$\overline{L}$, $\overline{GBR}$, $\overline{NBGT}$, TX/$\overline{RX}$ during receive data and transmit data transfers.

Figure 7 shows the operation of the data handshaking signals during a receive command with two data words. When the RT has fully checked the command word, $\overline{NBGT}$ is pulsed low, which can be used by the subsystem as an initialization signal. TX/$\overline{RX}$ will be set low indicating a receive command. When the first data word has been fully validated, $\overline{DTRQ}$ is set low. The subsystem must then reply within approximately 1.5 us by setting $\overline{DTAK}$ low. This indicates to the RT that the subsystem is ready to accept data The data word is then passed to the subsystem on the internal highway IH08-IH715 in two bytes using IUSTB as a strobe signal and H/$\overline{L}$ as the byte indicator (high byte first followed by low byte). Data is valid about both edges of IUSTB. Signal timing for this handshaking is shown in Figure 12.

If the subsystem does not declare itself busy, then it must respond to DTRQ going low by setting DTAK low within approximately 1.5 us. Failure to do so will be classed by the RT as a subsystem failure and reported as such to the Bus Controller.

It should be noted that IUSTB is also used for internal working in the RT. DTRQ being low should be used as an enable for clocking data to the subsystem with IUSTB.

Once the receive data block has finished and been checked by the RT, GBR is pulsed low if the block is entirely correct and valid. This is used by the subsystem as permission to make use of the data block If no GBR signal is generated, then an error has been detected by the RT and the entire data block is invalid and no data words in it may be used.

If the RT is receiving data in an RT to RT transfer, the data handshaking signals will operate in an identical fashion but there will be a delay of approx 70 us between $\overline{NBGT}$ going low and $\overline{DTRQ}$ first going low. See Figure 10.

Figure 6 shows the operation of the data handshaking signals during transmit command with three, data words. As with the receive command discussed previously, $\overline{NBGT}$ is pulsed low if the command is valid and for the RT. TX/$\overline{RX}$ will be set high indicating a transmit data command. While the RT is transmitting its status word, it requests the first data word from the subsystem by setting $\overline{DTRQ}$ low. The subsystem must then reply within approximately 13.5 us by setting $\overline{DTAK}$ low. By setting $\overline{DTAK}$ low, the subsystem is indicating that it has the data word ready to pass to the RT. Once $\overline{DTAK}$ is set low by the subsystem, $\overline{DTRQ}$ should be used together with H/$\overline{L}$ and TX/$\overline{RX}$ to enable first the high byte and then the low byte of the data word onto the internal highway IH08-IH715. The RT will latch the data bytes during IUSTB, and will then return $\overline{DTRQ}$ high. Data for each byte must remain stable until IUSTB has returned low. Signal timing for this handshaking is shown in Figure 11.

Additional Data Information Signals

At the same time as data transfers take place, a number of information signals are made available to the subsystem. These are $\overline{INCMD}$, the subaddress lines SA0-4, the word count lines WC0-4 and current word count lines CWC0-4. Use of these signals is optional.

$\overline{INCMD}$ will go active low while the RT is servicing a valid command for the RT. The subaddress, transmit/receive bit. and word count from the command word are all ma a vailable to the subsystem as SA0-4, TX/$\overline{RX}$ and WC0-4 respectively. They may be sampled when $\overline{INCMD}$ goes low and will remain valid while $\overline{INCMD}$ is low.

The subaddress is intended to be used by the subsystem as an address pointer for the data block Subaddress 0 and 31 are mode commands, and there can be no receive or transmit data blocks associated with these. (Any data word associated with a mode command uses different handshaking operations. If the subsystem does not use all the subaddresses available, then some of the subaddress lines may be ignored.

The TX/$\overline{RX}$ signal indicates the direction of data transfer across the RT - subsystem interface. Its use is described in the previous section.

The word count tells the subsystem the number of words to expect to receive or transmit in a message, up to 32 words. A word count of all 0s indicates a count of 32 words.

The current word count is set to 0 at the beginning of a new message and is incremented following each data word transfer across the RT - subsystem interface. (It is clocked on the falling edge of the second IUSTB pulse in each word transfer). It should be noted that there is no need for the subsystem to compare the word count and current word count to validate the number of words in a message. This is done by the RT.

Subsystem Use of Status Bits and Mode Commands

General Description

Use of the status bits and the mode commands is one of the most confusing aspects of MIL-STD-1553B. This is because much of their use is optional, and also because some involve only the RT while others involve both the RT and the subsystem.

The CT1602/CT1610 allows full use to be made of all the status bits, and also implements all the mode commands. The subsystem is given the opportunity to make use of status bits, and is only involved in mode commands which have a direct ir~lpact on the subsystem.

The mode commands in which the subsystem may be involved are Synchronize, Sychronize with data word, Transmit Vector Word, Reset and Dynamic Bus Control Allocation. The status bits to which the subsystem has access are Service Request, Busy, Subsystem Flag and Dynamic Bus Control Acceptance. Operation of each of these mode commands and of the status bits is described in the following sections.

The subsystem designer should note that all other mode commands and status bits are serviced internally by the RT, and the subsystem has no access to them. In particular, the terminal flag and message error status bits and BIT word contents are all controlled internally by the RT.

Synchronize Mode Commands

Once the RT has validated the command word and checked for the correct address, the $\overline{SYNC}$ line is set low. The signal WC4 will be set low for a Synchronize mode command Figure 16, and high for a Synchronize with data word mode command Figure 15. In a Synchronize with data word mode command, $\overline{SYNC}$ remains low during the time that the data word is received. Once the data word has been validated, it is passed to the subsystem on the internal highway IH08-IH715 in two bytes using IUSTB as a strobe signal and H/L as the byte indicator (high byte first followed by low byte). SYNC being low should be used on the enable to allow IUSTB to clock synchronize mode data to the subsystem.

If the subsystem does not need to implement either of these mode commands, the $\overline{SYNC}$ signal can be ignored, since the RT requires no response from the subsystem.

Transmit Vector Word Mode Command

Figure 14 illustrates the relevant signal timings for an RT receiving a valid Transmit Vector Word mode command. The RT requests data by setting $\overline{VECTEN}$ low. The subsystem should use H/L to enable first the high byte and then the low byte of the Vector word onto the internal highway IH08-IH715.

It should be noted that the RT expects the Vector word contents to be already prepared in a latch ready for enabling onto the internal highway when $\overline{VECTEN}$ goes low. If the subsystem has not been designed to handle the Vector word mode command, it will be the fault of the Bus Controller if the RT receives such a command. Since the subsystem is not required to acknowledge the mode command, the RT will not be affected in any way by Vector word circuitry not being implemented in the subsystem. It will however transmit a data word as the Vector word, but this word will have no meaning.

Reset Mode Command

Figure 8 shows the relevant signal timings for an RT receiving a valid reset mode command. Once the command word has been fully validated and serviced, the $\overline{RESET}$ signal is pulsed low. This signal may be used as a reset function for subsystem interface circuitry.

Dynamic Bus Allocation

This mode command is intended for use with a terminal which has the capability of configuring itself into a bus controller on command from the bus. The line $\overline{DBCREQ}$ cannot go true unless the $\overline{DBCACC}$ line was true at the time of the valid command, i.e. tied low. For terminals acting only as RTs, the signal DBCACC should be tied high (inactive), and the signal $\overline{DBCREQ}$ should be ignored and left unconnected.

Use of the Busy Status Bit

The Busy Bit is used by the subsystem to indicate that it is not ready to handle data transfers either to or from the RT.

The RT sets the bit to logic one if the $\overline{BUSY}$ line from the subsystem is active low at the time of the second falling edge of INCLK after $\overline{INCMD}$ goes low. This is shown in Figure 13. Once the Busy bit is set, the RT will stop all receive and transmit data word transfers to and from the subsystem. The data transfers in the Synchronize with data word and Transmit Vector word mode commands are not affected by the Busy bit and will take place even if it has been set.

It should be noted that a minimum of 0.5 us subaddress decoding time is given to the subsystem before sening of status bits. This allows the subsystem to selectively set the Busy bit if for instance one subaddress is busy but others are ready. This option will prove useful when an RT is interfacing with multiple subsystems.

Use of the Service Request Status Bit

The Service Request bit is used by the subsystem to indicate to the Bus Controller that an asynchronous service is requested.

The timing of the setting of this bit is the same as the Busy bit and is shown in Figure 13. Use of $\overline{SERVREQ}$ has no effect on the RT apart from sening the Service Request bit.

It should be noted that certain mode commands require that the last status word be transmitted by the RT instead of the current one, and therefore a currently set status bit will not be seen by the Bus Controller. Therefore the user is advised to hold $\overline{SERVREQ}$ low until the requested service takes place.

Use of the Subsystem Status Bit

This status bit is used by the RT to indicate a subsystem fault condition. If the subsystem sets $\overline{SSERR}$ low at any time, the subsystem fault condition in the RT will be set, and the Subsystem Flag status bit will subsequently be set The fault condition will also be set if a handshaking failure takes place during a data transfer to or from the subsystem. The fault condition is cleared on power-up or by a Reset mode command.

Dynamic Bus Control Acceptance Status Bit

$\overline{DBCACC}$, when set true, enables an RT to configure itself into a Bus Controller, if the subsystem has the capability, by allowing $\overline{DBCREQ}$ to pulse true and BIT TIME 18 to be set in the status response. If Dynamic Bus Control is not required then $\overline{DBCACC}$ must be tied high. $\overline{DBCACC}$ tied high inhibits $\overline{DBCREQ}$ and clears BIT TIME 18 in the status response.

Bus Driver/Receiver Interface

Receive Data

The decoder chip requires two TTL signals (PDIN & NDIN) to represent the data coming in from the bus. PDIN should be driven to a logic level '1' when the bus waveform exceeds a specified positive threshold and NDIN should be driven to a logic level '1' when a specified negative threshold is exceeded. During the quiet period on the bus both signals should be at the same logic level. All the bus receivers must be permanently enabled, the selection if the bus in use is done within the chip set.

Transmit Data

The signals generated by the encoder chip ($\overline{PDOUT}$ & $\overline{NDOUT}$) are of the same format as the receive data The only difference is that the TTL signals are negative logic, e.g. the signal is active when on logic level '0'. This means that when the encoder is quiet both $\overline{PDOUT}$ & $\overline{NDOUT}$ are at logic level '1'. Both the signals should be used in conjunction with $\overline{TXEN}$ and the appropriate driver enable, e.g. (CS0 - enable for bus 0). $\overline{TXEN}$ only enables the driver when it should be transmitting, and the driver enable routes the data on to the bus in use.

Figure 5 shows an example of a typical interface circuit between the CT1602/CT1610 and a driver/receiver unit.

BUS CONTROL OPERATION

To enable its use in a bus controller each chip in the chipset has additional logic within it. This logic can be enabled by pulling the pin labelled RT/$\overline{BC}$ low. Once the chipset is in bus control mode, all data transfers must be initiated by the bus control processor correctly commanding the chipset via the subsystem interface. In bus control mode six inputs are activated which in RT mode are inoperative and four signals with dual functions exercise the second function (the first being for the RT operation).

To use the CT1602 or CT1610 as a 1553B bus control interface, the bus control processor must be able to carry out four basic bus-related functions. Two inputs, BCOPA and BCOPB allow these four options to be selected. The option is then initiated by sending a negative-going strobe on the $\overline{BCOPSTB}$ input. $\overline{BCOPSTB}$ must only be strobed low when $\overline{NDRQ}$ is high. This is particularly important when two options are required during a single transfer.

With these options all message types and lengths can be handled. Normal BC/RT exchanges are carried out in the chipset option zero. This is selected by setting BCOPA and BCOPB to a zero and strobing $\overline{BCOPSTB}$. On receipt of the strobe, the CT1602/CT1610 loads the command word from an external latch using CWEN and H/$\overline{L}$ The command word is transmitted down the bus. The TX/$\overline{RX}$ bit is, however, considered by the chipset as being its inverse and so if a transmit command is sent to a RT, Figure 17, the chipset in BC mode believes it has been given a receive command. As the RT returns the requested number of data words plus its status, the BC chipset carries out a full validation check and passes the data into the subsystem using $\overline{DTRQ}$, $\overline{DTAK}$, H/$\overline{L}$, IUSTB and CWC as in RT operation. It also supplies GBR at the end of a valid transmission. Conversely, a receive command sent down the bus is interpreted by the BC chipset as a transmit command, and so the requisite data words are added to the command word, see Figure 18.

For mode commands, where a single command word is required, option one is selected by strobing $\overline{BCOPSTB}$ when BCOPA is high and BCOPB is low. On receiving the strobe, the command word is loaded from the external latch using $\overline{CWEN}$ and H/$\overline{L}$, the correct sync and parity bits are added and the word transmitted, see Figure 20. Mode commands followed by a data word requires option two. Option two, selected by strobing $\overline{BCOPSTB}$ while BCOPA is low and BCOPB is high, loads a data word via $\overline{DWEN}$ and H/$\overline{L}$, adds sync and parity and transmits them to the bus, see Figure 21. If the mode code transmitted required the RT to return a data word, then selecting option three by strobing $\overline{BCOPSTB}$ when BCOPA and BCOPB are both high will identify that data word and if validated, output it to the subsystem interface using RMDSTB and H/$\overline{L}$ This allows data words resulting from mode codes to be identified differently from ordinary data words and routed accordingly, see Figure 22. All received status words are output to the subsystem interface using STATSTB and H/$\overline{L}$.

In BC option three, if the signal $\overline{PASMON}$ is active, then all data appearing on the selected bus is output to the subsystem using STATSTB for command and status words or RMDSTB for data words.

RT to RT transfers require the transmission of two command words. A receive command to one RT is contiguously followed by a transmit command to the the other RT. This can be achieved by selecting option one followed by option zero for the second command. The strobe ($\overline{BCOPSTB}$) for option zero must be delayed until $\overline{NDRQ}$ has gone low and returned high following the strobe for option one. The RT transmissions are checked and transferred in the subsystem interface to the bus control processor, see Figure 19.

Note: For all BC operations, BCOPA and BCOPB must remain valid and stable for a minimum of 1 us following the leading (negative going) edge of $\overline{BCOPSTB}$.

PIN DESCRIPTION CT1602 AND CT1610

Signal Mnemonic	Hybrid Sink or Source	Signal Description
RX DATA0/1	SINK	**Positive Date In.** This should be a TTL description of the positive, half of the Manchester code data on the bus. It should be driven to a logic level "1" when a predetermined positive threshold is exceeded on the bus.
RX DATA 0/1	SINK	**Negative Data In.** This should be a TTL description of the negative half of the Manchester code data on the bus. It should be driven to a logic level "1" when a predetermined negative threshold is exceeded on the bus.
TX INHIBIT 0/1	SOURCE	**Transmitter Enable.** Goes low when the transmitter is transmitting. Should be used to enable the bus drivers.
TX DATA	SOURCE	**Positive Data Out** - When this signal goes high the bus should be driven positive.
TX DATA	SOURCE	**Negative Data Out** - When this signal goes high the bus should be driven negative.
RTAD 0-4	SINK	**RT address lines** - These should be hardwired by the user. RTAD4 is the most significant bit.
RTADPAR	SINK	**RT address parity line** - This must be hardwired by the user to give odd parity.
BCSTEN 0/1	SINK	**Recognition of Broadcast command enable** - When low the recognition of broadcast command is prevented on the specified bus.
6MCK	SINK	**6 Megahertz master clock.**
IH 08 IH 19 IH 210 IH 311 IH 412 IH 513 IH 614 IH 715	SINK/SOURCE	**Internal Highway** - Bi-directional 8 bit highway on which 16 bit words are passed in two bytes. IH 715 is the most significant bit of each byte, the most significant byte being transferred first. The highway should only be driven by the subsystem when data is to be transferred to the RT.
DTRQ	SOURCE	**Data Transfer Request** - Goes low to request a data transfer between the Chip Set and subsystem. Goes high at the end of the transfer.
DTAK	SINK	**Data Transfer Acknowledge** - Goes low to indicate that the subsystem is ready for the data transfer.
IUSTB	SOURCE	**Interface Unit Strobe** - This is a double pulse strobe used to transfer the two bytes of data

Signal Mnemonic	Hybrid Sink or Source	Signal Description
H/$\overline{L}$	SOURCE	**High/Low** - Indicates which byte of data is on the internal highway. Logic level "0" for least significant byte.
$\overline{GBR}$	SOURCE	**Good Block Received** - Pulses low for 500ns when a block of data has been received by the Chip Set and has passed all the validity and error checks.
$\overline{NBGT}$	SOURCE	**New Bus Grant** - Pulses low whenever a new command is accepted by the Chip Set.
TX/$\overline{RX}$	SOURCE	**Transmit/Receive** - The state of this line informs the subsystem whether it is to transmit or receive data The signal is valid while $\overline{INCMD}$ is low.
$\overline{INCMD}$	SOURCE	**In Command** - Goes low when the RT is servicing a valid command. The subaddress and word count lines are valid while the signal is low.
WC 0-4	SOURCE	**Word Count** - These five lines specify the requested number of data words to be received or transmitted. Valid when $\overline{INCMD}$ is low.
SA 0-4	SOURCE	**Sub Address** - These five lines are a label for the data being transferred. Valid when $\overline{INCMD}$ is low.
CWC 0-4	SOURCE	**Current Word Count** - These five lines define which data word in the message is currently being transferred.
$\overline{SYNC}$	SOURCE	**Synchronize** - Goes lowwwhen a synchronize mode code is being serviced.
$\overline{VECTEN}$/ $\overline{DWEN}$	SOURCE	**Vector Word Enable/DataWord Enable** - In the RT mode, this signal is provided to enable the contents of the vector word latch (which is situated in the subsystem) onto the Chip Set's internal highway. This signal, when in the Bus Controller mode, is used to enable mode code data from the subsystem onto the internal highway.
$\overline{RESET}$	SOURCE	**Reset** - This line pulses low for 500ns on completion of the servicing of a valid and legal mode command to reset remote terminal.
$\overline{SSERR}$	SINK	**Subsystem Error** - By taking this line low, the subsystem can set the Subsystem Flag in the Status Word.
$\overline{BUSY}$	SINK	**Busy** - This signal should be driven low if the subsystem is not ready to perform a data transfer to or from the Chip Set.
$\overline{SERVREQ}$	SINK	**Service Request** - This signal should be driven low to request an asynchronous transfer and left low until the transfer has taken place.

Signal Mnemonic	Hybrid Sink or Source	Signal Description
$\overline{\text{PASMON}}$	SINK	**Passive Monitor** - When functioning as a Bus Controller this line acts as a passive monitor select. The active going edge of this line will cause the REQBUS lines to be latched and that bus, now selected will be monitored so long as $\overline{\text{PASMON}}$ remains low. All traffic on the bus will be handed, after validation, to the subsystem via STATSTB for status and commands words, and RMDSTB for data words.
$\overline{\text{BCOPSTB}}$	SINK	**Bus Controller Operation Strobe** - When functioning as a Bus Controller a low going pulse on this line will initiate the selected bus controller operation on the requested bus, using BCOPA&B and REQBUSA&B.
BCOPA	SINK	**Bus Control Operation A** - Least significant bit of the bus controller operation select lines.
BCOPB	SINK	**Bus Control Operation B** - Most significant bit of the bus controller operation select lines.
REQBUS A	SINK/SOURCE	**Request Bus A** - This line,wwhen in RT mode, is the least significant bit of the bus request lines which specify the origin of the command, ie. they are sources. When in BC mode these lines are sinks and specify which bus is to be used for the next command.
REQBUS B	SINK/SOURCE	**Request Bus B** - Most significant bit of the bus request lines. (See above for description.)
RT/$\overline{\text{BC}}$	SINK	**Remote Terminal/Bus Control** - This line when high causes the chip set to function as a remote terminal. When low the chip set functions as a bus controller or passive monitor.
$\overline{\text{DBCACC}}$	SINK	**Dynamic Bus Control Accept** - This line should be permanently tied low if a subsystem is able to accept control of the bus if offered.
$\overline{\text{LTFAIL}}$	SOURCE	**Loop Test Fail** - This line goes low if any error in the transmitted waveform is detected or if any parity error in the hardwired RT address is detected.
$\overline{\text{ERROR}}$	SOURCE	**Error** - This line latches low if a Manchester or parity error is detected. It is reset by the next $\overline{\text{CMSYNC}}$ (RT mode) and also by $\overline{\text{RTO}}$ in the BC mode.
$\overline{\text{RTO}}$	SOURCE	**Reply Time Out** - This signal will pulse low whenever the reply time for a transmitting terminal has been exceeded. This line is intended for the bus controller use.
$\overline{\text{TXTO}}$	SOURCE	**Transmitter Time Out** - This line goes true if the transmitter time out limits are exceeded.

Signal Mnemonic	Hybrid Sink or Source	Signal Description
INCLK	SOURCE	**Internal Clock (2 MHz)** - This is made available for synchronization use by the subsystem if required. However, many of the outputs to the subsystem are asynchronous.
$\overline{\text{EOT}}$	SOURCE	**End of Transmission** - Goes low if a valid sync plus two data bits do not appear in time to be contiguous with preceding word.
$\overline{\text{RTADER}}$	SOURCE	**Remote Terminal Address Error** - This line goes low if an error is detected in the RT address parity of the selected receiver. Any receiver detecting an error in the RT address will turn itself off.
$\overline{\text{HSFAIL}}$	SOURCE	**Handshake Failure** - This line pulses low if the allowable time for $\overline{\text{DTAK}}$ response has been exceeded during the Chip Set/subsystem data transfer handshaking.
$\overline{\text{LSTCMD}}$/ $\overline{\text{CWEN}}$	SOURCE	**Last Command/Command Word Enable** - This line pulses low when servicing a valid and legal mode command to transmit last command. When in RT mode this line must not be used to enable data from the subsystem. This line also pulses low, when in the Bus Control mode, when a command word is required for transmission.
$\overline{\text{STATEN}}$/ STATSTB	SOURCE	**Status Enable/Status Strobe** - This line pulses low to enable the status word onto the internal highway for transmission. When in RT mode this line must not be used to enable data from the subsystem. This line also pulses high, when in the Bus Control mode, to strobe received status words into the subsystem. When $\overline{\text{PASMON}}$ is true this line pulses high for Command and Status words.
$\overline{\text{BITEN}}$/ RMDSTB	SOURCE	**Built In Test Enable/Receive Mode Data Strobe** - This line pulses low when servicing a valid and legal mode command to transmit the internal BIT word. This signal is for information only and must not be used to enable data from the subsystem. This line also pulses high when in the Bus Control mode when mode data is received to be passed to the subsystem and when data is passed to the subsystem during $\overline{\text{PASMON}}$.
$\overline{\text{DWSYNC}}$	SOURCE	**Data Word Sync** - This line goes low if a data word sync and two Manchester biphase bits are valid.
$\overline{\text{CMSYNC}}$	SOURCE	**Command Word Sync** - This line goes low if a command word sync and two Manchester biphase bits are valid.
$\overline{\text{NDRQ}}$	SOURCE	**No Data Required** - This line goes low if the encoder transmit buffer is full i.e. another word is going to be transmitted. This signal is for information only and must not be used to enable data from the subsystem.

Signal Mnemonic	Hybrid Sink or Source	Signal Description
$\overline{\text{PARER}}$	SOURCE	**Parity Error** - This line will pulse low if a parity error is detected by the decoder.
$\overline{\text{MANER}}$	SOURCE	**Manchester Error** - This line will pulse low if a Manchester error is detected by the decoder.
$\overline{\text{DBCREQ}}$	SOURCE	**Dynamic Bus Control Request** - This line will pulse low when the status reply for a mode code Dynamic Bus Control has finished where the accept bit was set.
$\overline{\text{VALD}}$	SOURCE	**Valid Data** - This line will pulse low when a valid data word is received.
$\overline{\text{BUF INH}}$*	SINK	**Buffer Inhibit** - A low on this line causes the Buffered Signals to assume a high impedance state.
$\overline{\text{IH ENA}}$*	SINK	**Internal Highway Enable** - A low on this line enables the Internal Highway transceiver to transmit or receive data which is controlled by the IH DIR Line.
IH DIR*	SINK	**Internal Highway Direction** - Controls the direction of data through the Internal Highway Transceiver. High = To Subsystem A → B Low = From Subsystem B → A

* NOT USED ON CT1610

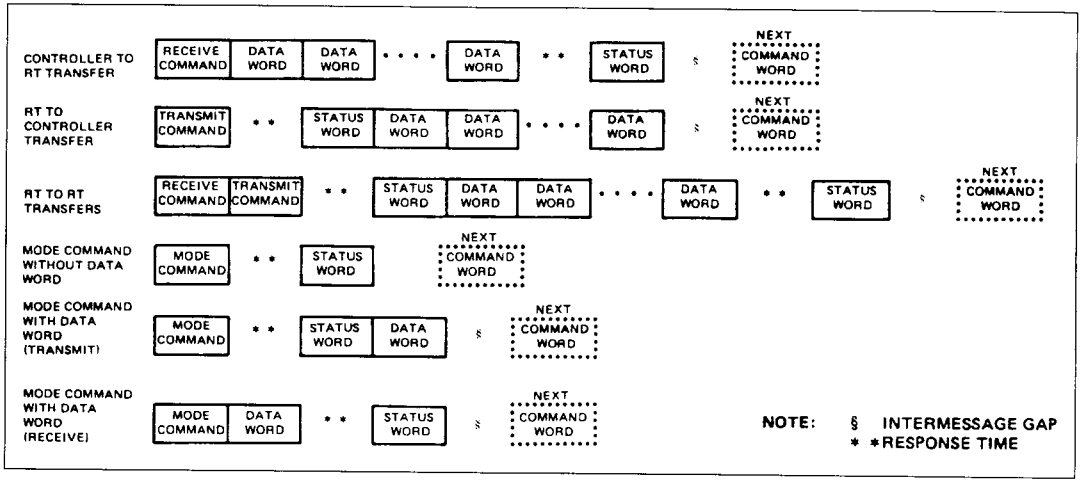


Figure 1: Typical Message Formats

T/R Bit	Mode Code	Function	Associated Data Word	Broadcast Command Allowed
1	00000	Dynamic Bus Control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit Status Word	No	No
1	00011	Initiate Self Test	No	Yes
1	00100	Transmitter Shutdown	No	Yes
1	00101	Override Transmitter Shutdown	No	Yes
1	00110	Inhibit Terminal Flag Bit	No	Yes
1	00111	OverrideInhibitTerminal FlagBit	No	Yes
1	01000	Reset Remote Terminal	No	Yes
1	01001	Reserved	No	TBD
	↓	↓	↓	↓
1	01111	Reserved	No	TBD
1	10000	Transmit Vector Word	Yes	No
0	10001	Synchronize	Yes	Yes
1	10010	Transmit Last Command	Yes	No
1	10011	TransmitBITWord	Yes	No
0	10100	Selected Transmitter Shutdown	Yes	Yes
0	10101	Override Selected Transmitter Shutdown	Yes	Yes
1 or 0	10110	Reserved	Yes	TBD
	↓	↓	↓	↓
1 or 0	11111	Reserved	Yes	TBD

NOTE: To be determined (TBD)

Figure 2: Assigned Mode Codes

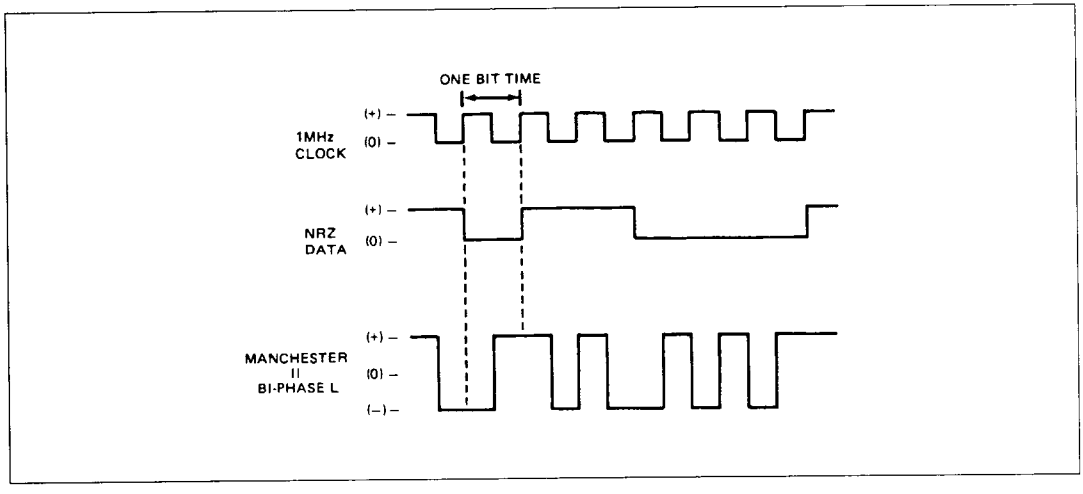


Figure 3: Data Encoding

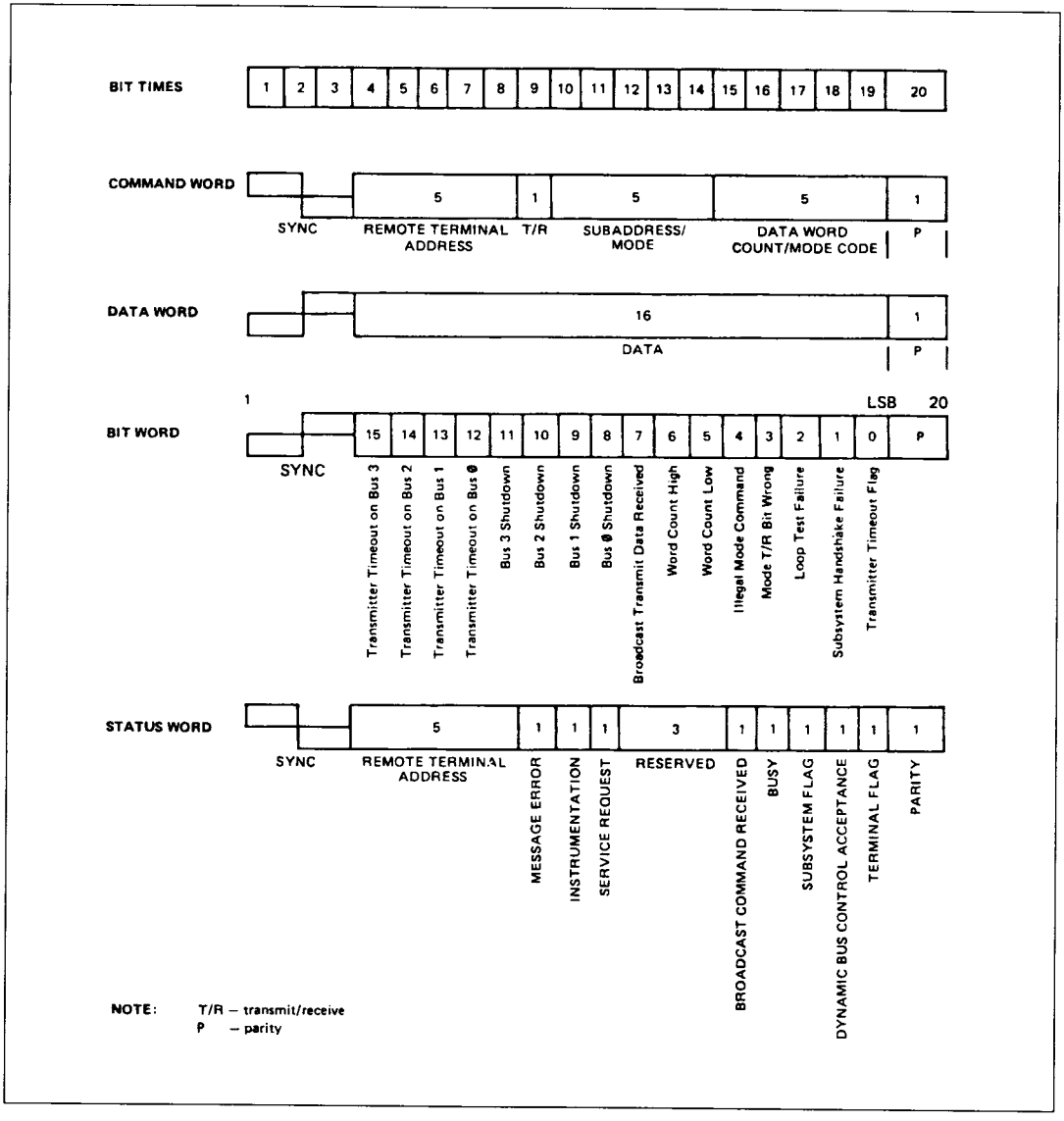


Figure 4: Word Formats

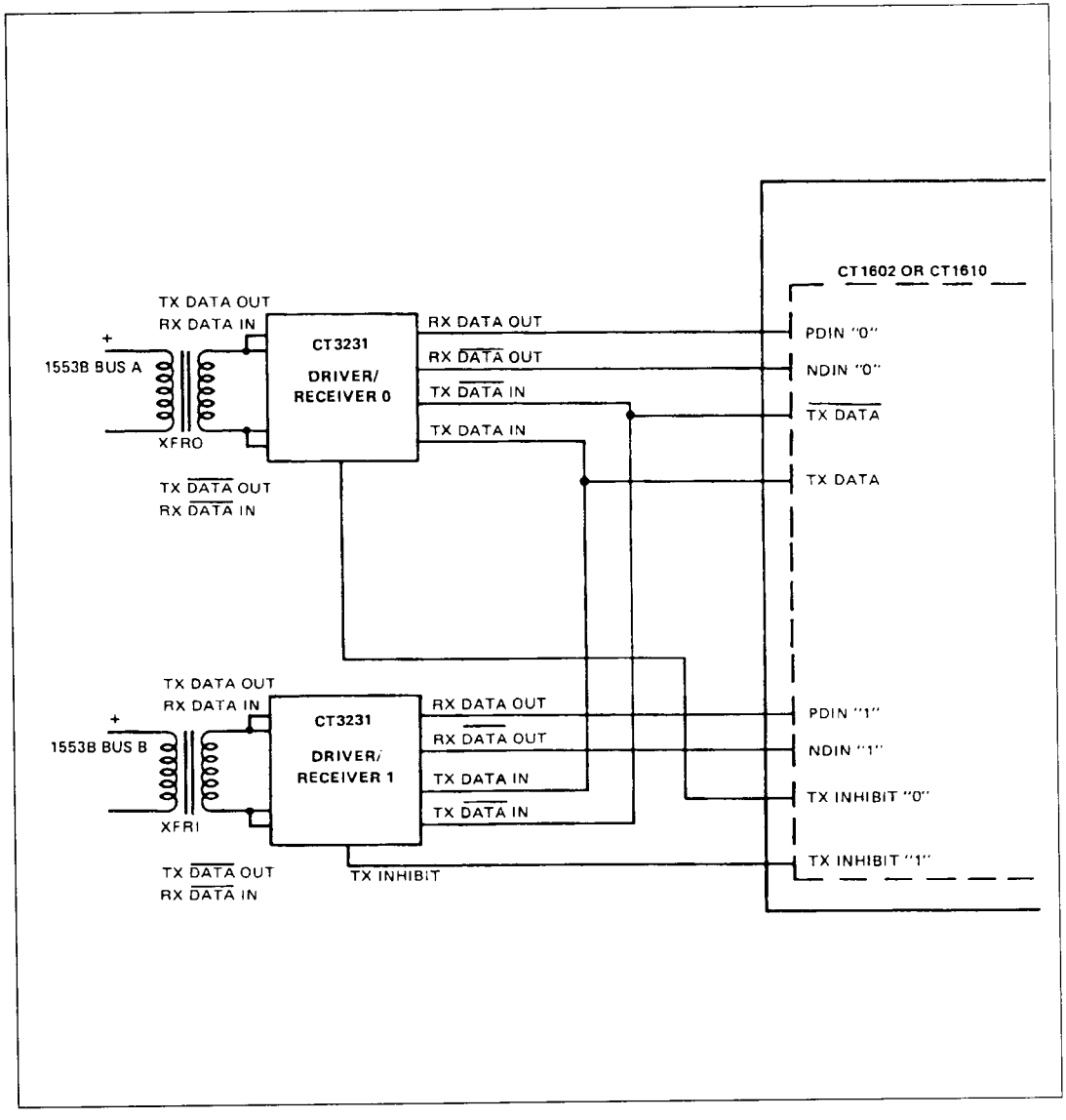


Figure 5: Examples of an interface between CT1602 or CT1610 and Driver/Receiver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Operating free-air temperature	-55°C to +125°C
Storage temperature range	-65°C to +150°C

CLOCK REQUIREMENTS

Frequency	6.0 MHz
Stability -55° to +125°C	±0.01% (100ppm)
Maximum Asymmetry	60-40%
Rise/Fall Time	10 nsec max
Output level TTL	Logic "0" 0.4v max
	Logic "1" 2.4v min

ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT	COMMENTS
V_{CC}		4.5	5.5	V	
V_{IH} High - level input voltage	CMOS TTL	V_{CC}-1 2.0	V_{CC} V_{CC}	V V	
V_{IL} Low - level input voltage	CMOS TTL	0 0	1.0 0.7	V V	
V_{OH} High - level output voltage	V_{CC} = MIN I_{OH} = -800uA I_{OH} = -400 I_{OH} = -3mA	 2.4 2.4 2.4		 V V V	 LS32 LS241-LS244 (CT1602 Only)
V_{OL} Low - leveloutput voltage	V_{CC} = MIN I_{OL} = +2mA I_{OL} = +4mA I_{OL} = +12mA		 0.4 0.4 0.4	 V V V	 LS32 LS241-LS244 (CT1602 Only)
I_{IH} HIgh - level input current	V_{CC} = MAX V_{IH} = 2.4V	 -400 -20 -500	 5.0 20 0.0	 uA uA uA	 IH08-IH715 PULL-UPS
I_{IL} Low - level input current	V_{CC} = MAX V_{IL} = 0.4V	 -500 -200 -800	 0.0 0.0 -350	 uA uA uA	 IH08-IH715 PULL-UPS
I_{CC} Supply Current	V_{CC} = MAX, Fclk = 6MHz Outputs enabled and open CT1602 CT1610		 310 35	 mA mA	

NOTE:

ALL MAX/MIN VALUES SHOWN ARE FOR WORST CASE OPERATING CONDITIONS, WHERE APPROPRIATE, AT -55°C or +125°C.

1. **PULL-UPS** DENOTES: RTADD0-RTADD4, RTADDPAR, BUF_INH/, and IH_INH/
2. **LS32** DENOTES: TXDATA, TXDATA/, TXINH0, and TXINH1
3. **LS241-LS244** DENOTES: CWC0-4, SA0-4, IH08-IH715, SYNC/, IUSTB, TX-RX/, INCMD/, H-L/, STATEN/, EOT/, INCLK, NBGT/, DTRQ/, VECTEN/, and GBR/.

TIMING DIAGRAMS

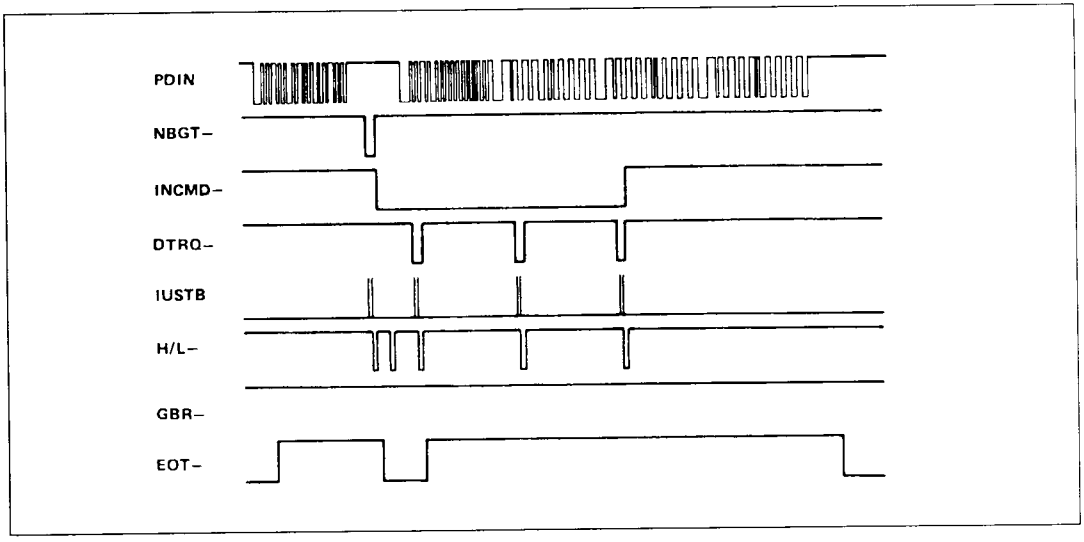


Figure 6: Transfer of Three Data Words from RT 03 to BC

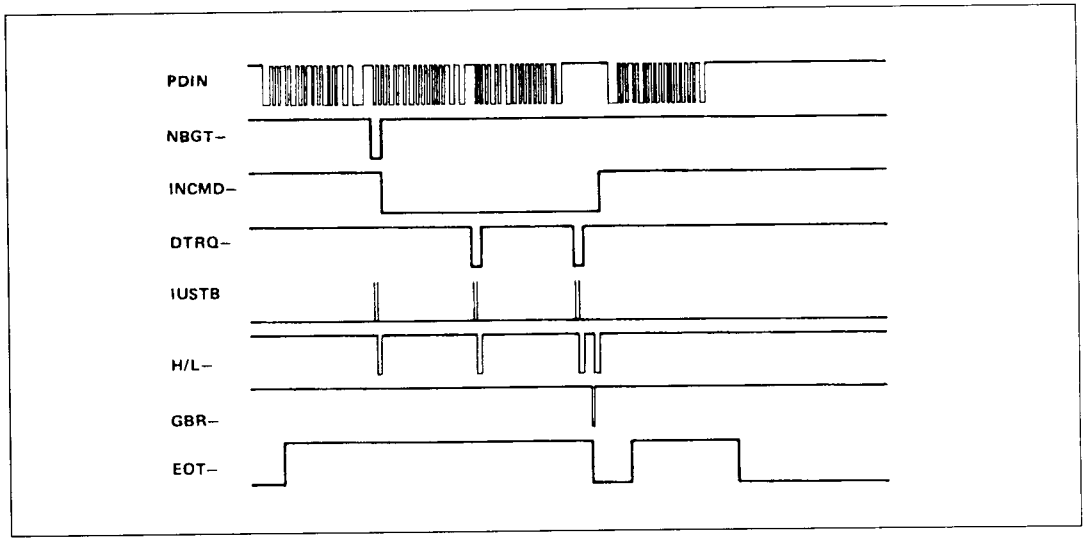


Figure 7: Transfer of Three Data Words from BC to RT 03

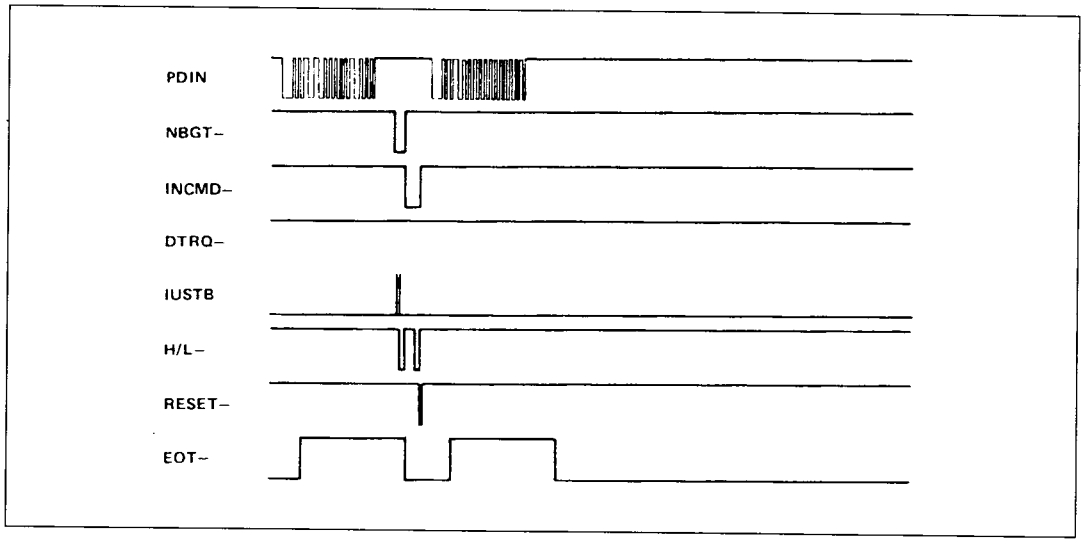


Figure 8: Mode Command Reset Remote Terminal

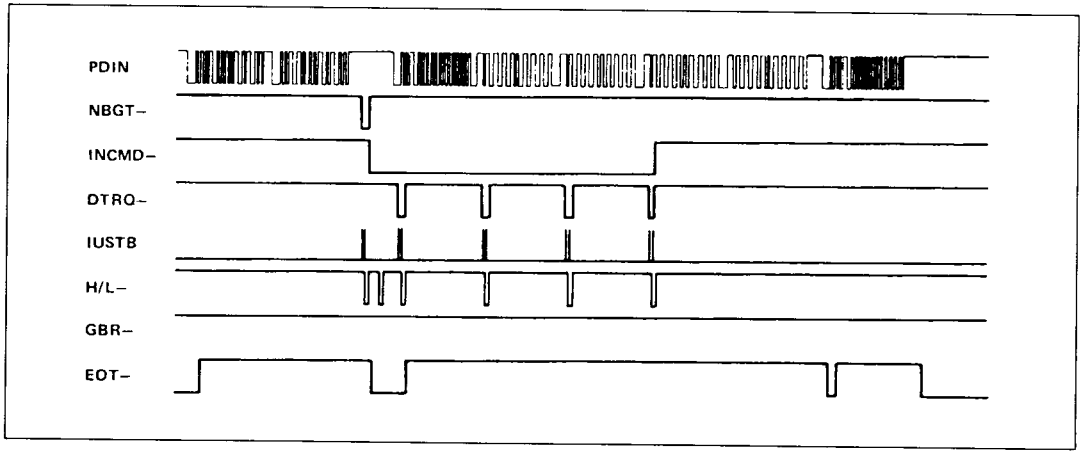


Figure 9: RT to RT Transfer of Four Data Words This RT Sending the Data

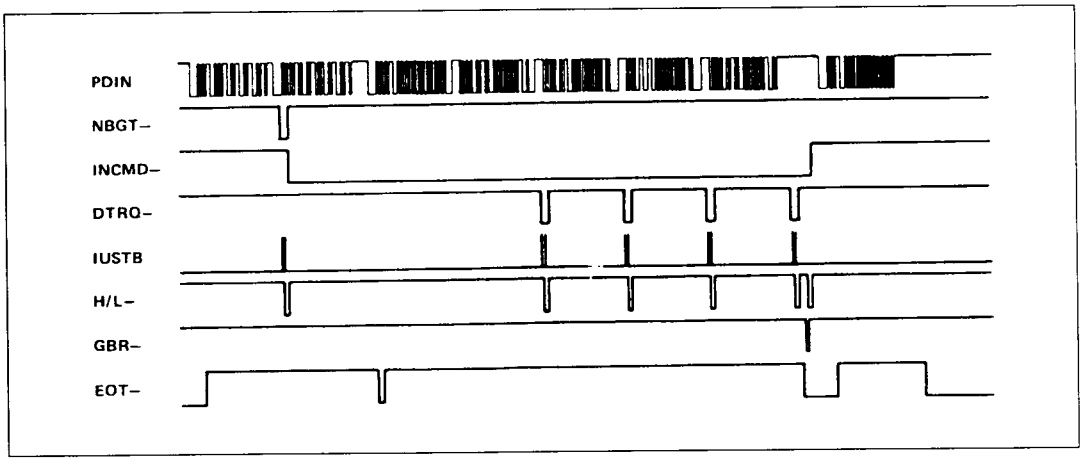


Figure 10: RT to RT Transfer of Four Data Words - This RT Receiving the Data

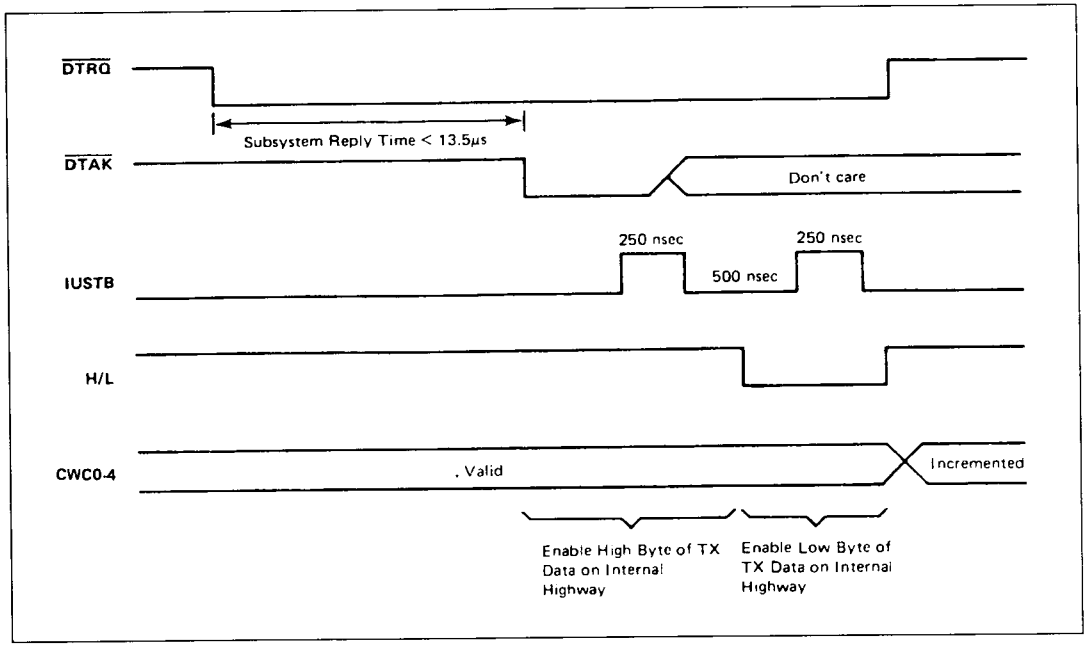


Figure 11: Handshaking for TX Data Transfers

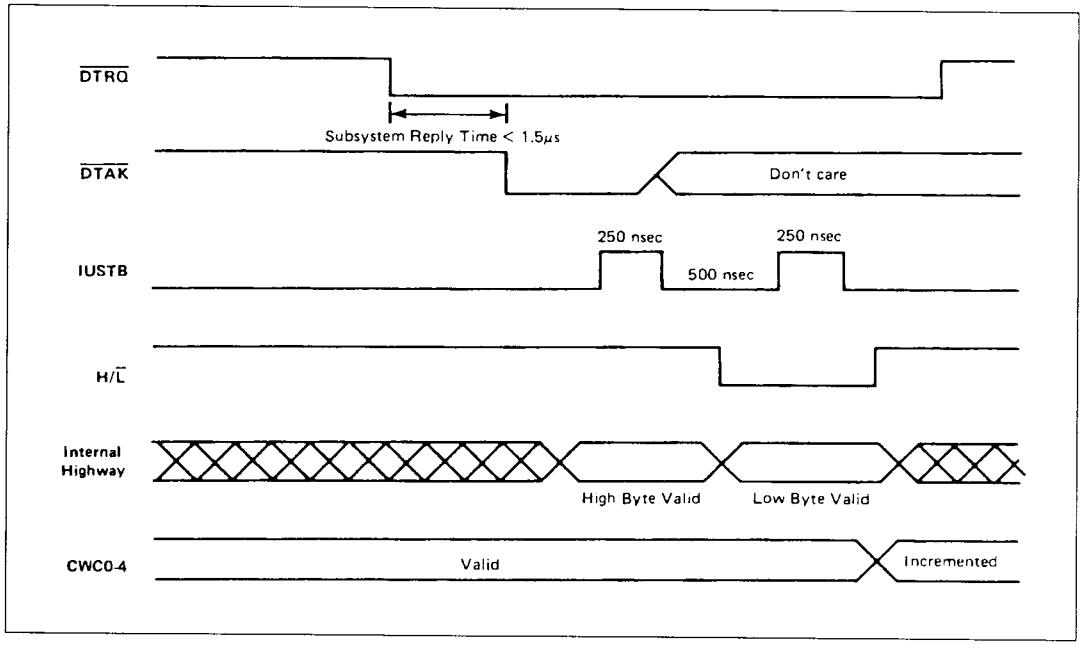


Figure 12: Handshaking for RX Data Transfers

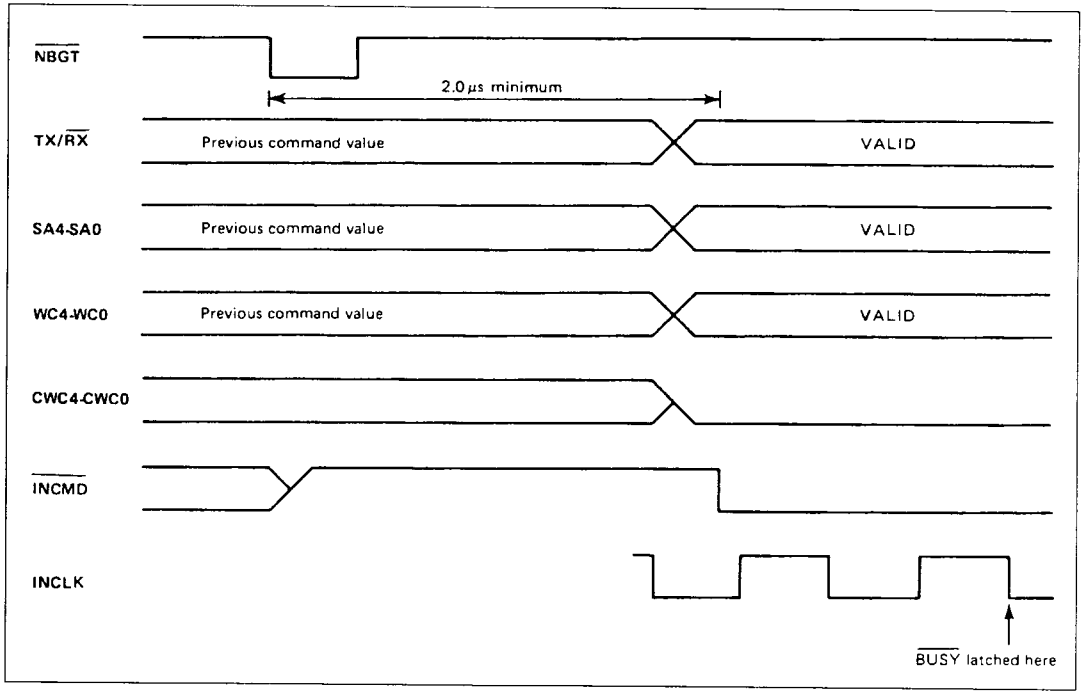


Figure 13: New Command Initialization

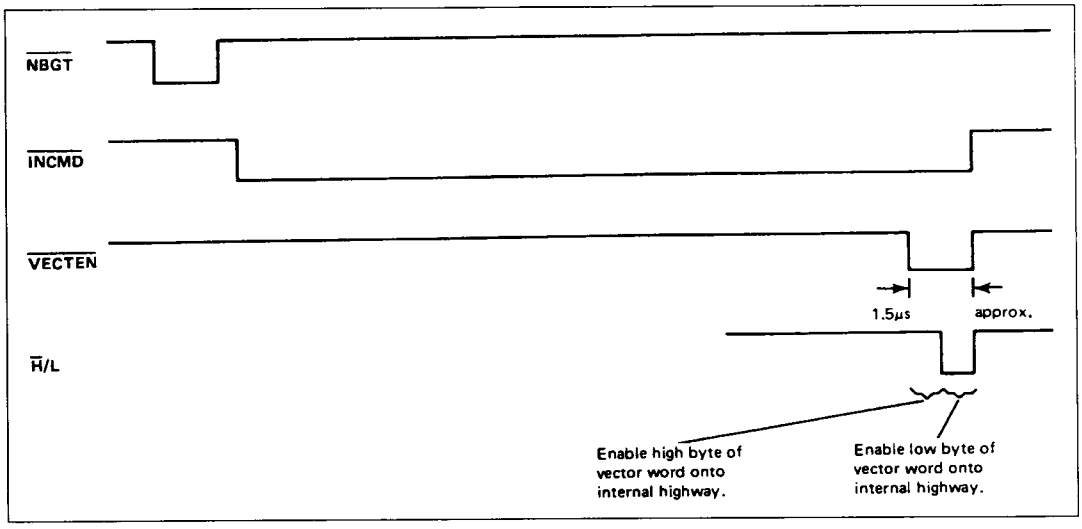


Figure 14: Transmit Vector Word Command

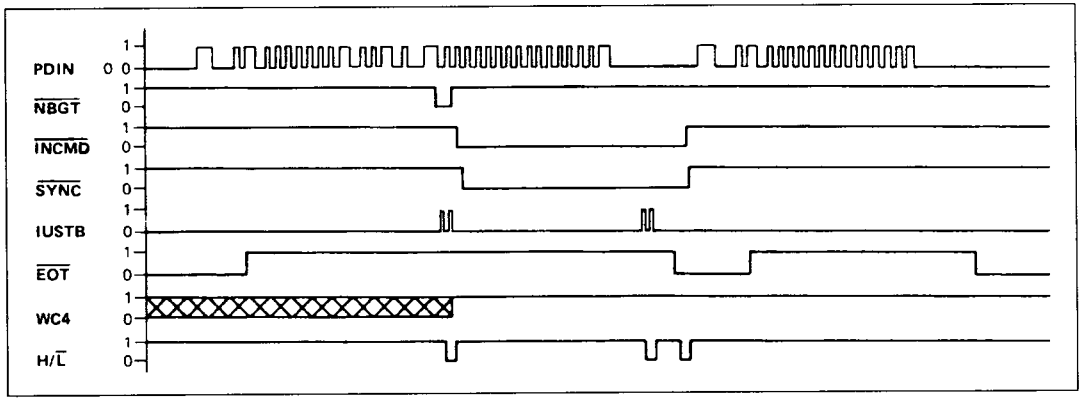


Figure 15: Synchronize (with data) Mode Command

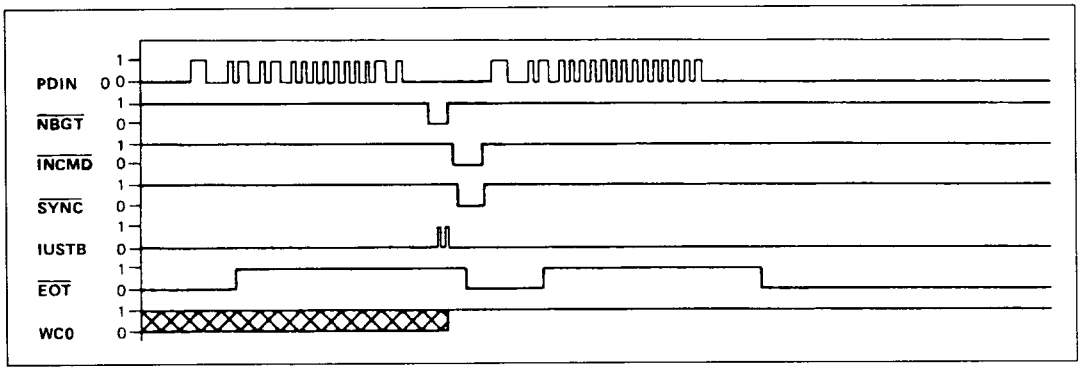


Figure 16: Synchronize (no data) Mode Command

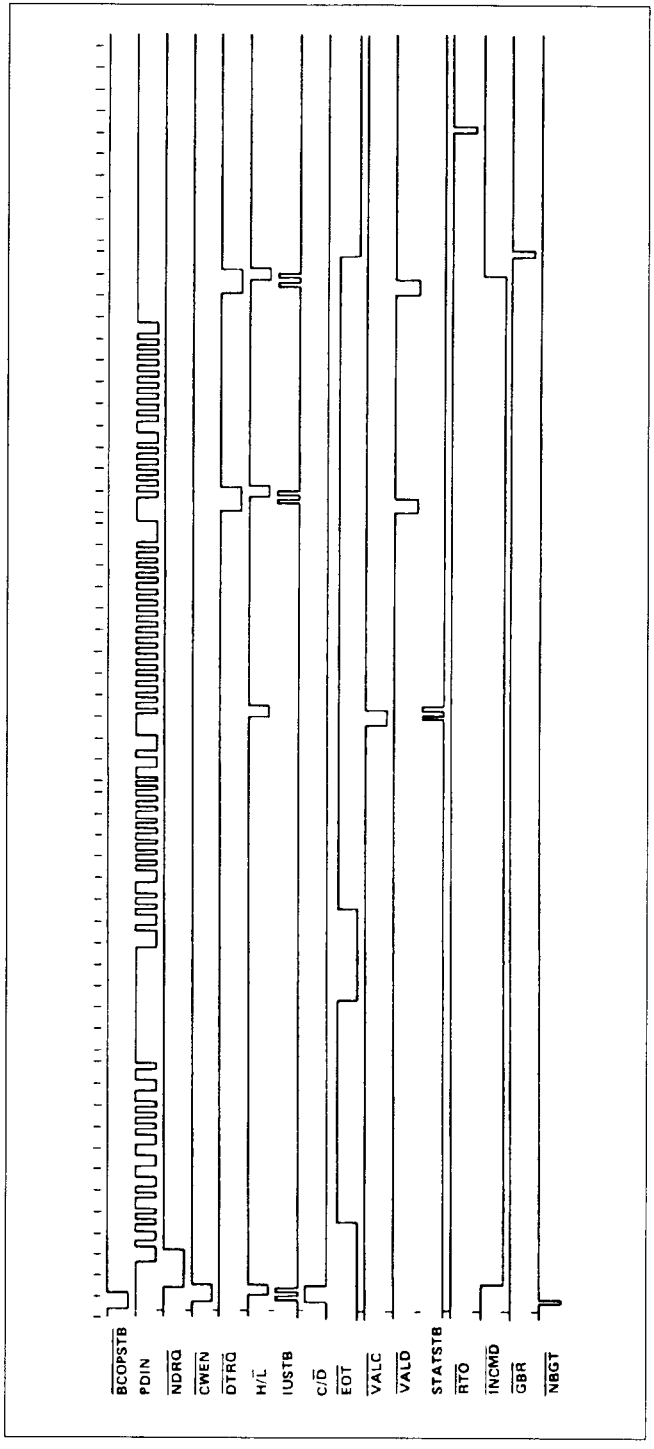


Figure 17: Bus Controller Sending Command to RT 10001 to Transmit Two Data Words

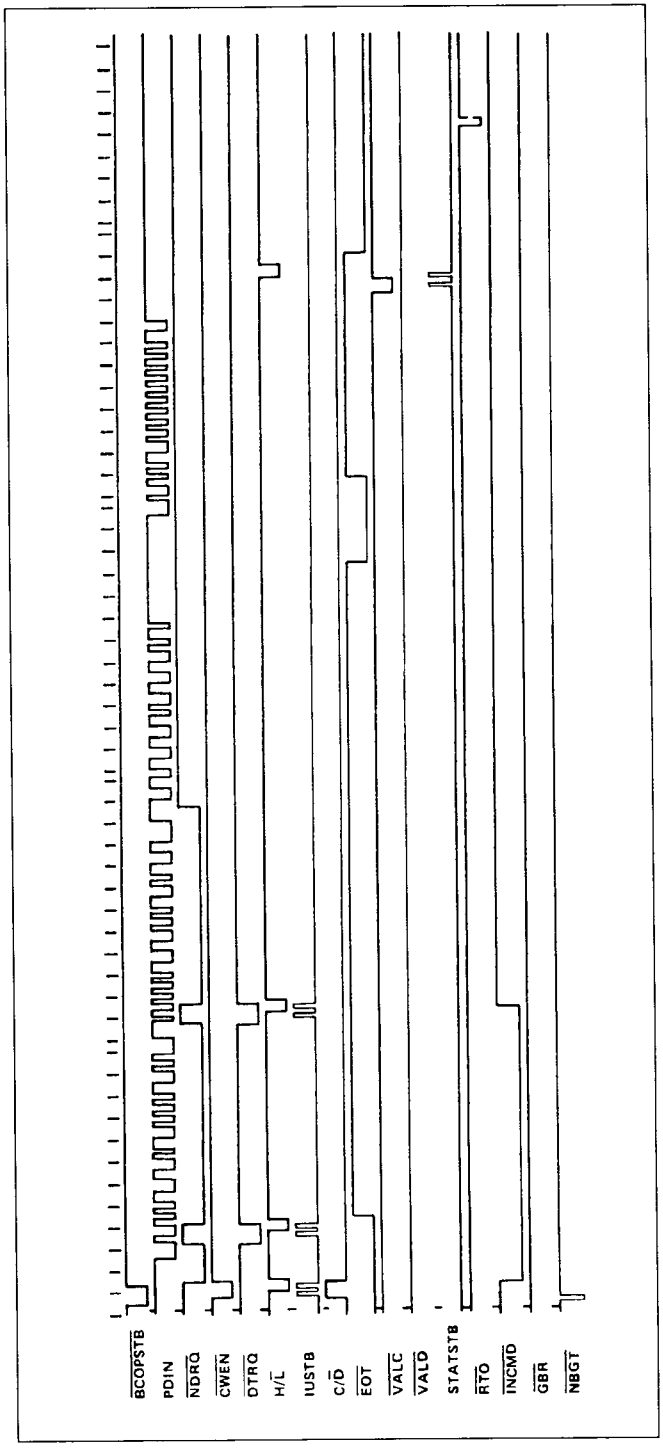


Figure 18: Bus Controller Sending Command to RT 10001 to Receive Two Data Words

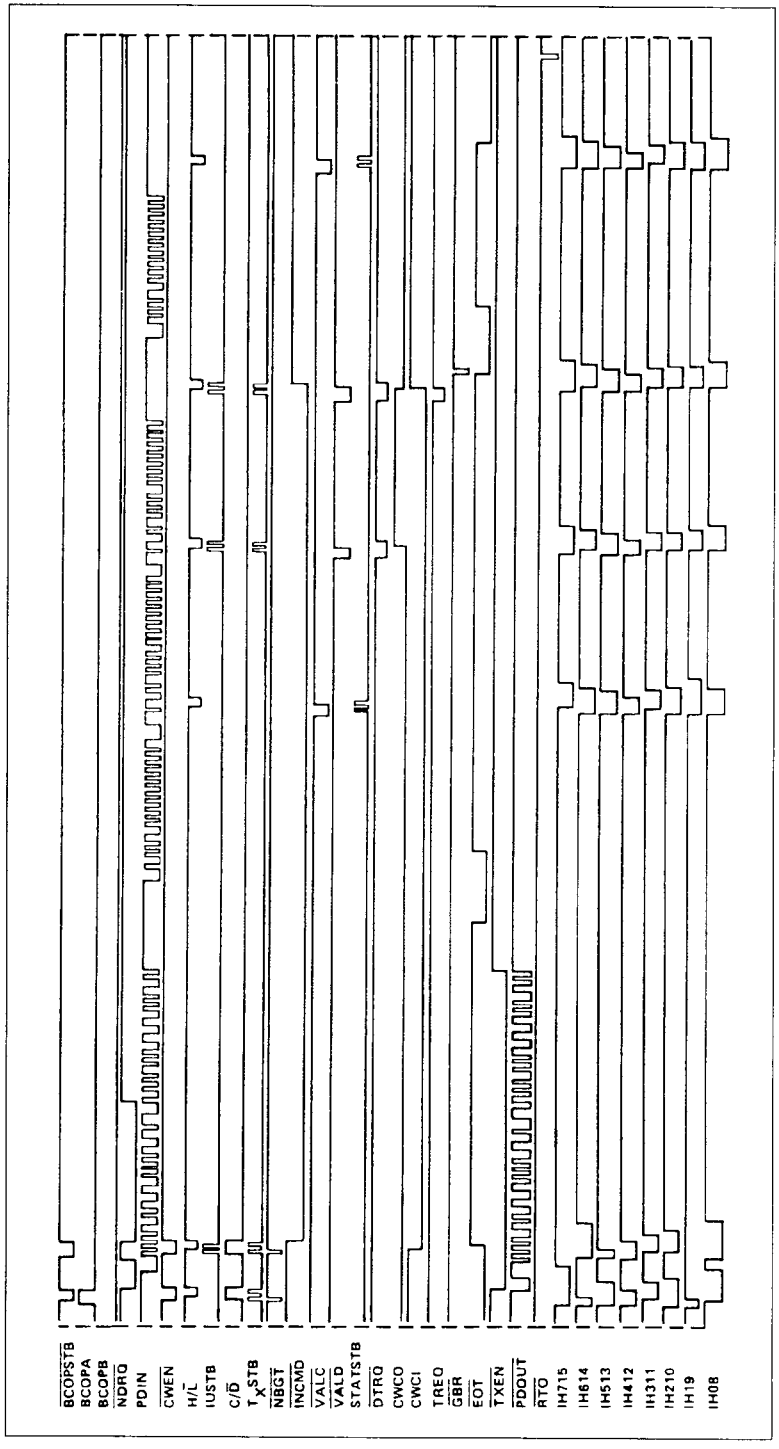


Figure 19: Bus Controller Commanding RT 10001 to Transmit Two Data Words to RTT 00001

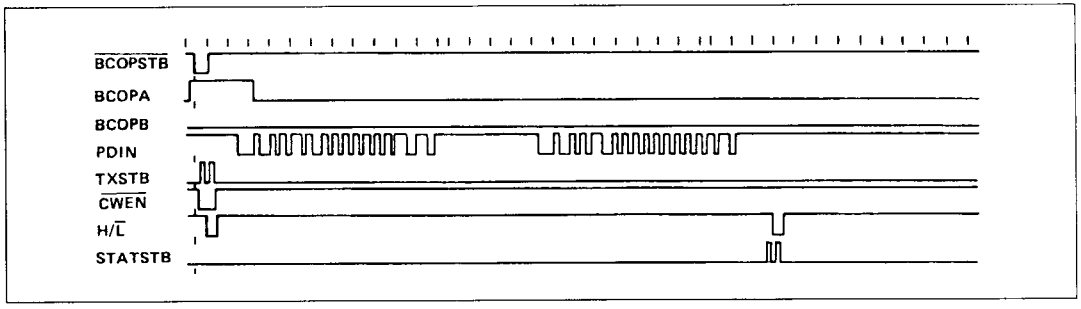


Figure 20: Bus Controller Sending Mode Command Transmit Status Word Mode Code 00010

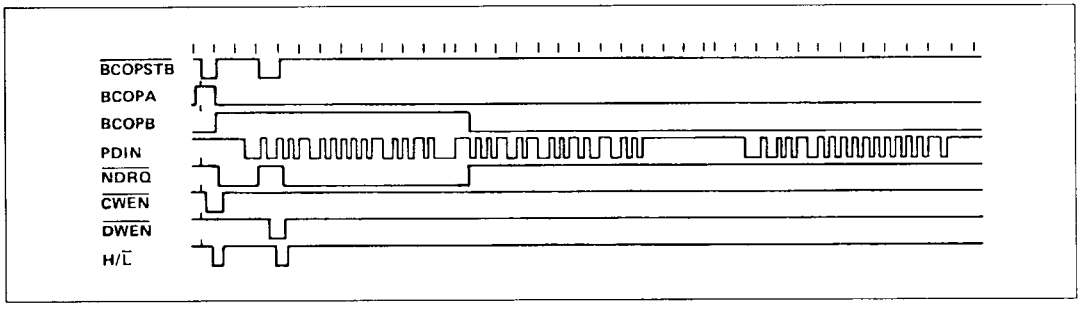


Figure 21: Bus Controller Sending Mode Command Synchronize Mode Code 1001

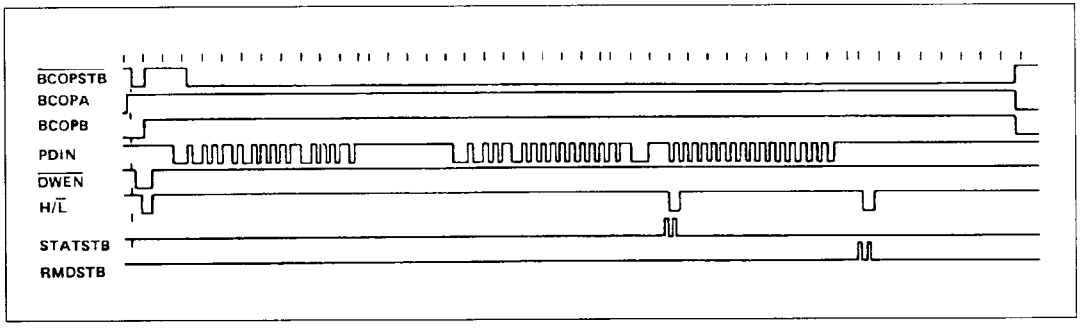
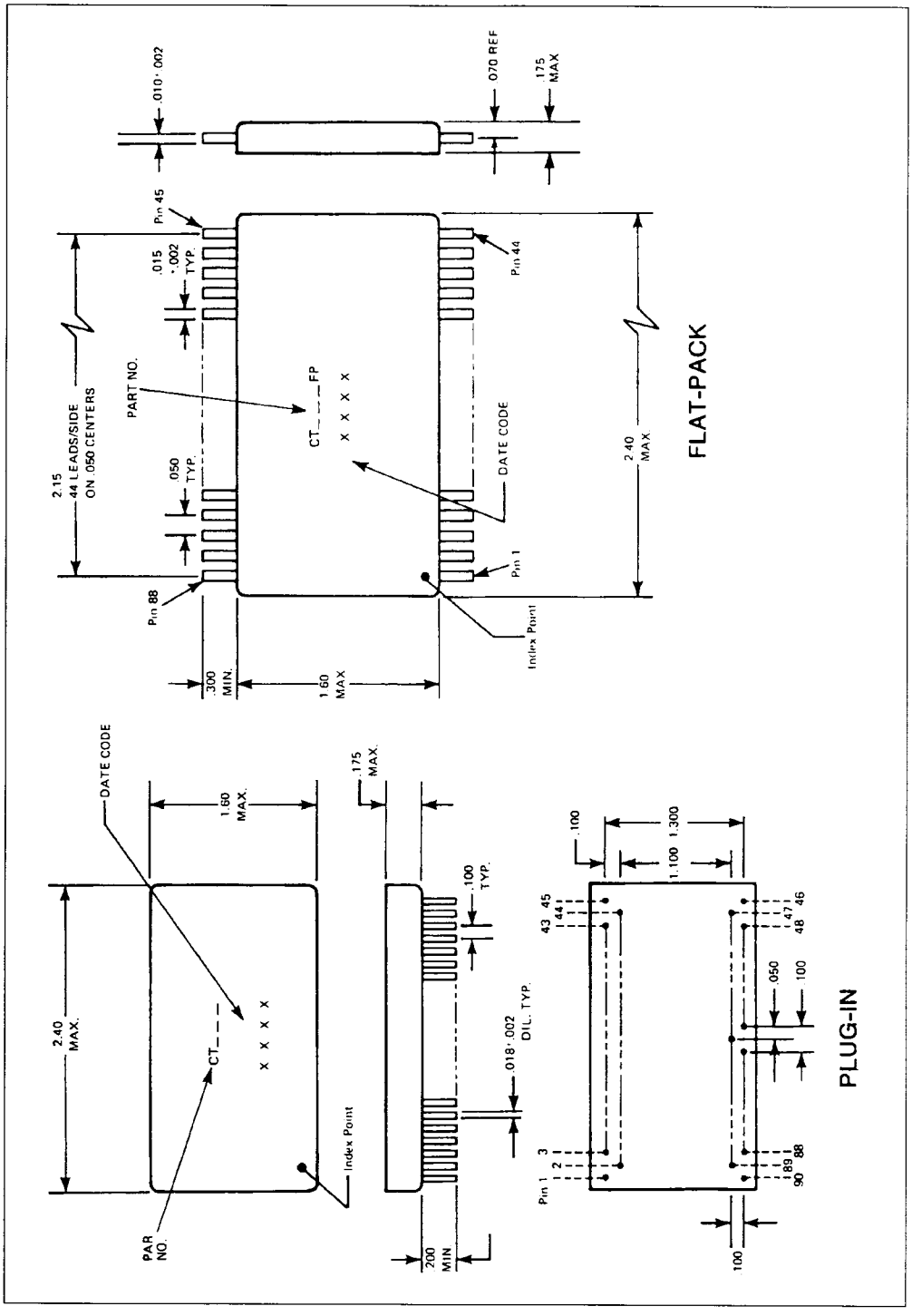


Figure 22: Bus Controller Sending Mode Command Transmit Vector Word Mode Code 10000



Package Outlines

PIN OUT

CT1610 and CT1602 Pin	CT1610FP and CT1602FP Pin	Function	CT1610 and CT1602 Pin	CT1610FP and CT1602FP Pin	Function
1	1	NC	46		NC
2	2	CWC 00 (LSB)	47	45	RTADPAR
3	3	SA 04 (MSB)	48	46	RTAD 00 (LSB)
4	4	SA 03	49	47	RTAD 01
5	5	SA 02	50	48	RTAD 02
6	6	CWC 04 (MSB)	51	49	RTAD 03
7	7	CWC 03	52	50	RTAD 04 (MSB)
8	8	CWC 02	53	51	CMSYNC*
9	9	CWC 01	54	52	DWSYNC*
10	10	GBR*	55	53	BCSTEN 00
11	11	H/L*	56	54	RX DATA 0
12	12	STATEN*/STATSTB	57	55	RX DATA* 0
13	13	EOT*	58	56	BCSTEN 01
14	14	SA 01	59	57	RTO*
15	15	SA 00 (LSB)	60	58	6 MCK
16	16	INCMD*	61	59	ERROR*
17	17	TX/RX*	62	60	LTFAIL*
18	18	DTRQ*	63	61	MANER*
19	19	VECTEN*/DWEN*	64	62	PARER*
20	20	NBGT*	65	63	VALD*
21	21	SYNC*	66	64	RTADER*
22	22	INCLK	67	65	RX DATA 01
23	23	IUSTB	68	66	RX DATA* 01
24 (2)	24 (2)	BUF INH*	69	67	+5 VIN
25	25	DTAK*	70	68	TX INHIBIT 01
26	26	BCOPA	71	69	TX INHIBIT 00
27	27	BCOPSTB*	72	70	TX DATA
28	28	BCOPB	73	71	TX DATA*
29	29	PASMON*	74	72	SERVREQ*
30	30	NDRQ*	75	73	TXTO*
31	31	REQBUSB	76	74	DBCACC*
32	32	REQBUSA	77	75	RESET*
33	33	COMMON & CASE	78	76	RT/BC*
34 (2)	34 (2)	IH DIR	79	77	DBCREQ*
35	35	NC	80	78	HSFAIL*
36 (2)	36 (2)	IH ENA*	81	79	LSTCMD*/CWEN*
37	37	IH 00/08 (LSB)	82	80	BITEN*/RMDSTB
38	38	IH 01/09	83	81	BUSY*
39	39	IH 02/10	84	82	WC 04 (MSB)
40	40	IH 03/11	85	83	WC 03
41	41	IH 04/12	86	84	WC 00 (LSB)
42	42	IH 05/13	87	85	SSERR*
43	43	IH 06/14	88	86	WC 02
44	44	IH 07/15 (MSB)	89	87	WC 01
45		NC	90	88	NC

KEY: * = True Low Signal
(2) = NO CONNECTION ON CT1610